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Development of Precision Time-Of-Flight Electronics for LHCb TORCH

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The TORCH detector is proposed for the low-momentum particle identification upgrade of the LHCb experiment. It combines Time-Of-Flight and Cherenkov techniques to achieve positive π/K/p separation up to 10GeV/c. This requires a timing resolution of 70ps for single photons. This paper will report on the electronics developed for such measurements, using commercial Micro Channel Plate devices and custom ASICs (NINO and HPTDC). The intrinsic timing resolution of the electronics measured with electrical test pulses is 40ps. With the photon detector and Cherenkov light, a resolution of 130ps has been recorded in a test beam.

Summary

The TORCH detector is proposed for the low-momentum particle identification upgrade of the LHCb experiment. In this detector, Time-Of-Flight and Cherenkov techniques are combined to achieve positive π/K/p separation up to 10GeV/c. This requires a timing resolution of 70ps for single photons.
Currently, we use an 8x8-channel Planacon Micro Channel Plate (MCP) photon detector. The outputs of the MCP are measured by custom electronics that consists of four Front End boards and a Giga-bit Ethernet-based readout/ slow control system. Each Front End board is equipped with two 8-channel fast amplifiers/discriminators ASICs (NINO), two time to digital convertor ASICs (HPTDC) and a Spartan 3AN FPGA. The NINO chips amplify the output signals from the MCP and discriminate at a threshold defined through a detector control system. In order to suit the input requirement of the HPTDCs, the outputs are converted to LVDS signals through external discrete components. The configurations of the HPTDCs are uploaded by a stand-alone JTAG programmer. The HPTDCs are intended to run in Very High Resolution Mode to offer a 25ps resolution, therefore, only 8 of 32 channels are used on each chip. The HPTDCs are read out and throttled by the on-board FPGA. The outputs are buffered on the FPGA and then transferred to a computer via the readout system. The HPTDCs require low jitter clocks to provide an accurate timing measurement. Users can select between an on-board 40MHz clock and an external clock; the selected clock is then fanned out by a low jitter device (SY89832), into the HPTDCs and the FPGA. The external trigger signal is also fanned out in the same way. The Giga-bit Ethernet-based readout/ detector control system has been developed. Three versions of firmware have been written for production tests, laboratory tests and beam tests. Labview-based DAQ software has also been developed to provide basic data transfer, online monitoring and control functions.
The intrinsic timing resolution of the electronics has been measured by injecting two separate pulses into a test channel with an Agilent 81110A generator. The difference of the two leading edges is measured and a Gaussian fit shows a timing resolution of 40ps. A beam test has been carried out at CERN using an MCP as described earlier in a low-intensity muon beam. Two 8mmx8mm borosilicate bars were coupled to the MCP to produce Cherenkov photons from the incident particles. Time differences were measured against a reference signal provided by a borosilicate bar coupled to a single-channel MCP read out with commercial electronics. The measured timing resolution is of order 130ps.
Possible improvements have been identified. This includes designing a 64-channel system based on 32-channel NINO chips to offer a higher channel density for future MCPs. Implementing Integral Nonlinearity (INL) corrections on the HPTDC chips to provide better timing resolution is also underway.

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