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Single-event upset tests on the readout electronics for the pixel detectors of the PANDA experiment.

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The Silicon Pixel Detector (SPD) of the PANDA experiment is the closest one to the interaction point and therefore the sensor and its electronics are the most exposed to radiation. The Total Ionizing Dose (TID) issue has been addressed by the use of a deep-submicron technology (CMOS 0.13 um) for the readout ASICs. While these technology are very effective in reducing radiation induced oxide damage, they are also more sensitive to Single Event Upset (SEU) effects due to their extremely reduced dimensions. This problem has to be addressed at the circuit level and generally leads to an area penalty. Several techniques have been proposed in literature with different trade-off between level of protection and cell size.
A subset of these techniques has been implemented in the PANDA SPD ToPiX readout ASIC, ranging from DICE cells to triple redundancy. The two prototypes have been tested with several ions at the INFN-LNL facility in order to measure the SEU cross section.
Comparative results of the SEU test will be shown, together with an analysis of the SEU tolerance of the various protection schemes and future plans for the SEU protection strategy which will be implemented in the next ToPiX prototype.

Summary

The PANDA experiment is one of the key projects at the future Facility for Antiproton and Ion Research (FAIR), which is currently under construction at GSI, Darmstadt. The PANDA experiment will perform precise studies of antiproton-proton annihilations and reactions of antiprotons with nucleons of heavier nuclear targets.
The silicon pixel system is the innermost detector and therefore the sensor and its electronics are the most exposed to radiation.
For what concerns the electronics, the Total Ionizing Dose (TID) issue has been addressed by the use of a deep-submicron technology (CMOS 0.13 um) for the readout ASICs. These technologies offer a better resistance to radiation as well as more dense integration with respect to previous technology nodes. However, they are also more sensitive to Single Event Upset (SEU) effects due to their extremely reduced dimensions. This problem has to be addressed at the circuit level which generally lead to an area penalty. Several techniques have been proposed in literature with different trade-off between level of protection and area penalty.
A subset of these techniques have been implemented and tested on the two prototypes of the pixel readout ASIC for PANDA (ToPiX).
In ToPiX v2, latches based on the Dual Interlocked storage CEll (DICE) architecture were implemented for the pixel cell registers in order to save area, while standard DFF have been used for the end of column logic. The chip was tested with several ions ranging from Oxygen to Bromine with energies in the range of 100-200 MeV (depending on the ion) and at both 0 and 30 degrees at the SIRAD Facility

of the Laboratori Nazionali di Legnaro (LNL) of INFN. A saturation cross section of 2e-8 cm2/bit with an energy threshold of about 0.5 MeV has been measured for the DICE latches of the pixels, while for the standard DFF the saturation cross section was 2.6e-8 cm2/bit with a threshold close to 0. In the PANDA environment, at the average value of 2x10ˆ7 interactions/s in the case of hydrogen target, these values corresponds to ˜3 SEU/hour per chip in the configuration register and between 130 and 200 in the end of column logic. These SEU rates are not easily manageable by an on-line correction system.
In order to improve the SEU immunity, the ToPiX v3 was designed with Triple Modular Redundant (TMR) latches for the pixel registers and Hamming encoding for the end of column logic. The chip has been tested at LNL with a similar set of ions and the results are under analysis. In the same test, a second chip designed in the same technology but with a full logic triplication was also tested for comparison.
Comparative results of the SEU test will be shown, together with an analysis of the SEU tolerance of the various protection schemes and future plans for the SEU protection strategy which will be implemented in the next ToPiX prototype.

Primary author: MAZZA, Giovanni (INFN sez. di Torino)

Co-authors: FILIPPI, Alessandra (INFN sez. di Torino); CANDELORI, Andrea (INFN sez. di Padova); CALVO, Daniela (INFN sez. di Torino); DE MORI, Francesca (Dipartimento di Fisica, Università di Torino); ZOTTI, Laura (Dipartimento di Fisica, Università di Torino e sezione INFN); SILVESTRINI, Luca (Università di Padova e sezione INFN); MIGNONE, Marco (INFN sez. di Torino); DE REMIGIS, Paolo (INFN sez. di Torino); WHEADON, Richard (INFN sez. di Torino); MATTIAZZO, Serena (Università di Padova); MARCELLO, Simonetta (Dipartimento di Fisica, Università di Torino)

Presenter: MAZZA, Giovanni (INFN sez. di Torino)

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