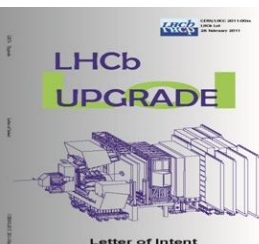


Front-End architecture

- ◆ Upgrade architecture
 - What is unchanged ?
- ◆ ECAL HCAL Front-end Crate
- ◆ FEB and CROC architecture
- ◆ Link between Front-end, readout and TFC crate
- ◆ Data format
- ◆ New development for Tests Board
- ◆ Summary



Calorimeter upgrade architecture

◆ What is (un)changed ?

■ On the detector side

- Most of the module are kept (some modules in the inner region replaced)
- PMT : a reduce gain is applied on the gain to keep them alive
- Cockcroft-Walton bases (and PS), signal cables, etc ... are kept
- Remove the SPD, PRS and lead absorber

■ On the balcony

- Keep the crates, backplanes, power supplies, ...
- Replace the Front-end electronics (GBT 40 MHz readout)
 - Make it compliant with the crates, power supplies, ...
- Migrate L0 Calo electronics to LLT

■ Counting room

- TELL1 \Rightarrow TELL40
- Slow control : SPECS \Rightarrow GBT

Calorimeter upgrade architecture

◆ What is changed ?

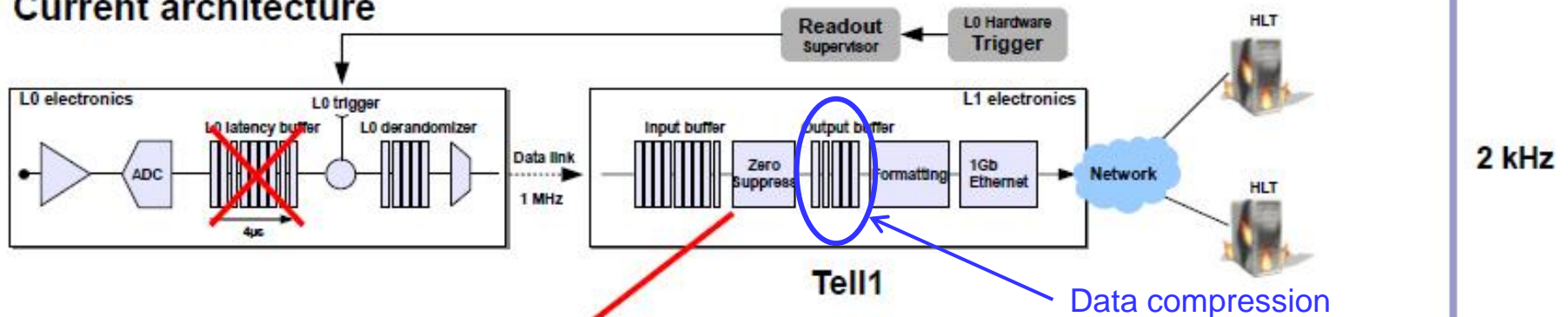
■ Current architecture

- Data compression in the TELL1 board
- L0 latency buffer

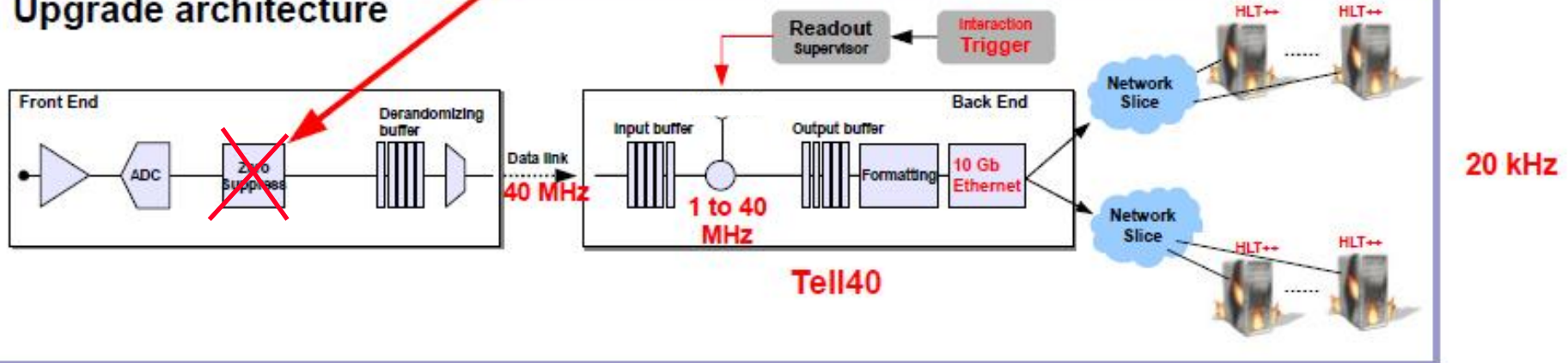
■ Upgrade architecture

- No zero suppression
- Used 112 bit width of the GBT

Current architecture



Upgrade architecture



ECAL-HCAL Front-end crate

◆ Front-end crate

■ Same backplane

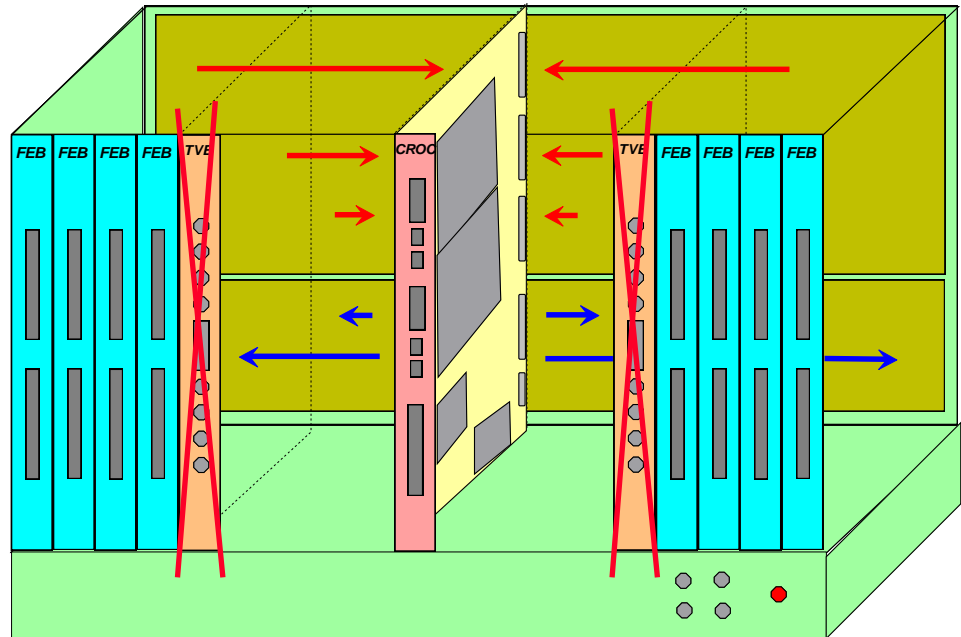
- 3U \Rightarrow power supply, clock distribution, ...
- 6U \Rightarrow links between boards inside the same crate

■ New Front-end Board

■ New CROC board

■ Remove TVB

Add an extra LLT fiber on the FEB



◆ FEB and GBT

■ On the new Calorimeter FEB

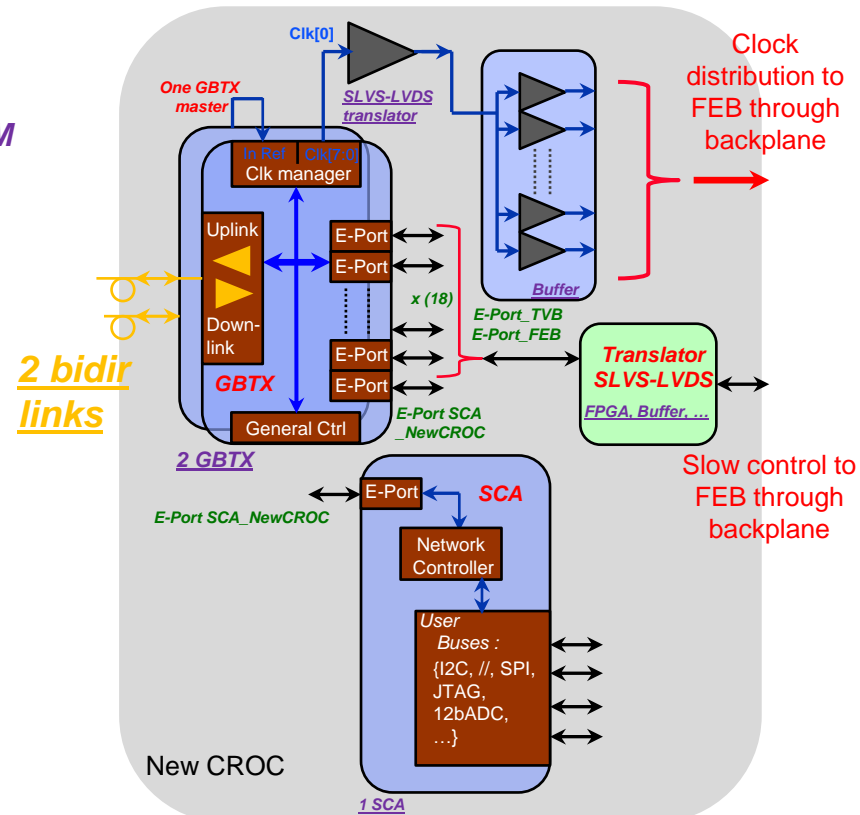
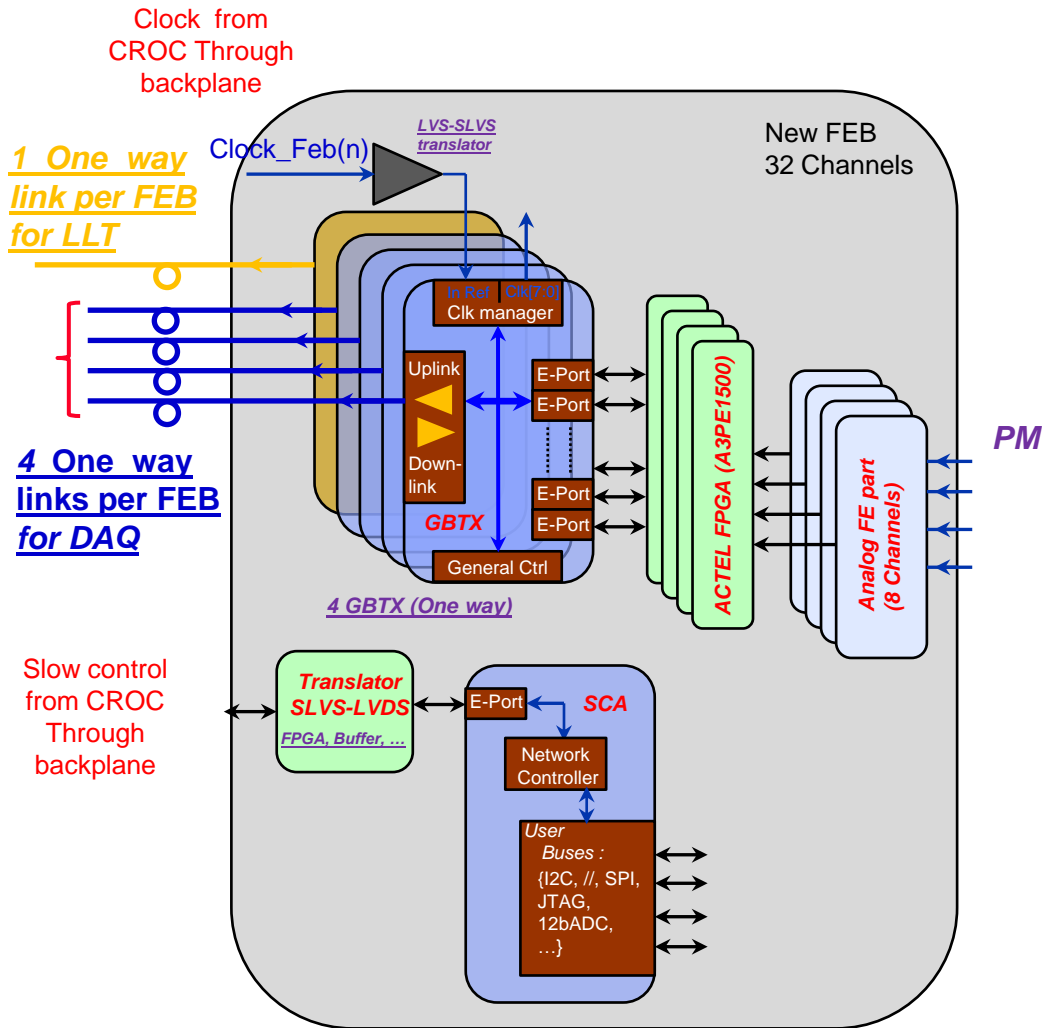
- 4 GBTX chip (one way) for Data
- 1 GBTX chip (one way) for LLT
- 1 SCA chip (FEB Ctrl/Cmd)

◆ CROC and GBT

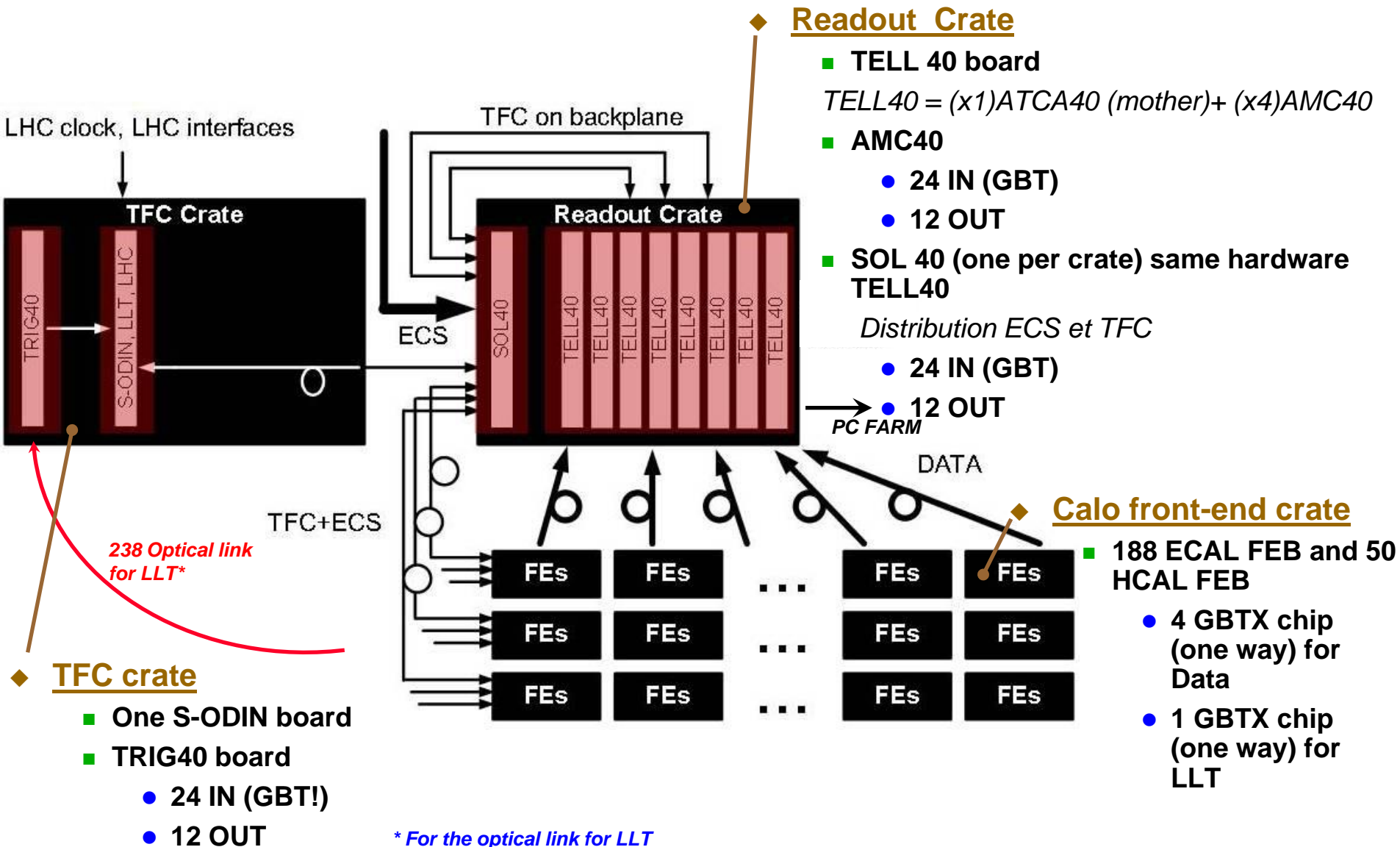
■ On new CROC board

- 2 GBTX (one master) chip with bidirectional optical fiber (right side and left side of FE crate)
- 1 SCA chip (CROC Ctrl/Cmd)

Front-end Board and CROC Board architecture



Links Calo front-end crate ATCA40



* For the optical link for LLT
see Cyril's Talk February 1st, 2013

Data format

◆ Trigger data format proposal : (1 link - 80 bits)

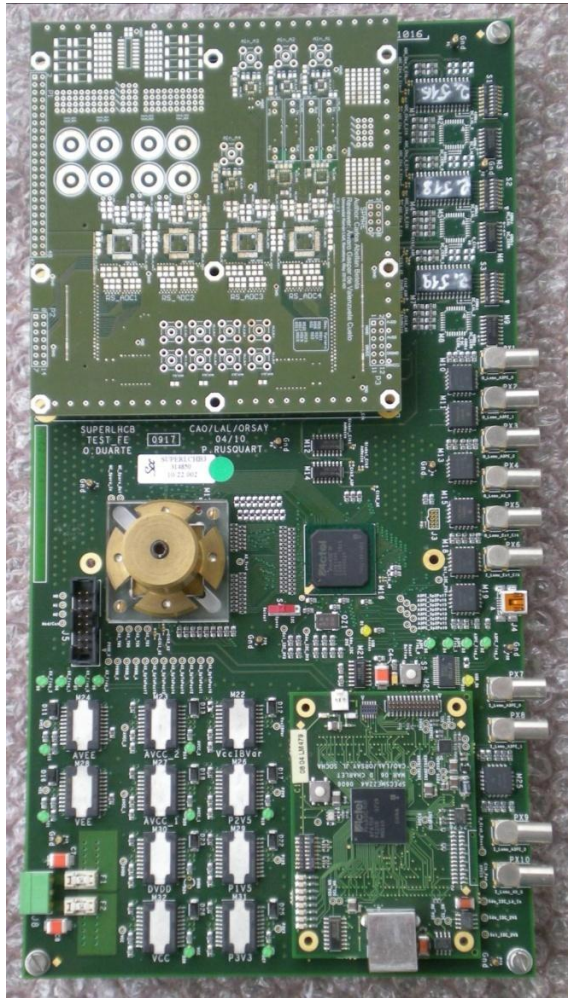
- 5b ⇒ local address
- 16b ⇒ data for trigger(8b Max ET, 8b Sum ET)
- 12b ⇒ BXID
- 6b ⇒ Calo Hit (number of channel under threshold)
- 5b ⇒ Crate Id, under discussion (see Patrick's talk)
- 4b ⇒ FEB Id, under discussion (see Patrick's talk)
- 1b ⇒ Status
- 49 / 80 bits used

◆ Data format proposal (4 links - 112 bits)

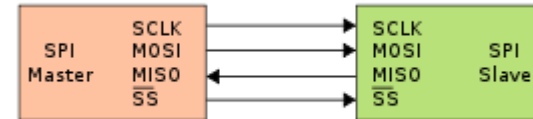
- (8x12=96b) ⇒ data
- 5b ⇒ Crate Id
- 4b ⇒ FEB Id
- 7b ⇒ Lsb of BXID

*One 112 bit word for
each bunch crossing,
No compression,
continuous data flow*

New and last development for test board ?



◆ SPI



- We need 4 spare wire between A3PE FPGAs and analog mezzanine
 - Spare_A3P_To_Analog_Mezza[3:0] used to clock 20 MHz
 - Used parallel bus implementation wire to SPI
(Add_ParBus[7:0], N_Rd_ParBus, N_Wr_ParBus, N_OE_ParBus)
- Re-used block developed at LAL (Christophe, Jihane)

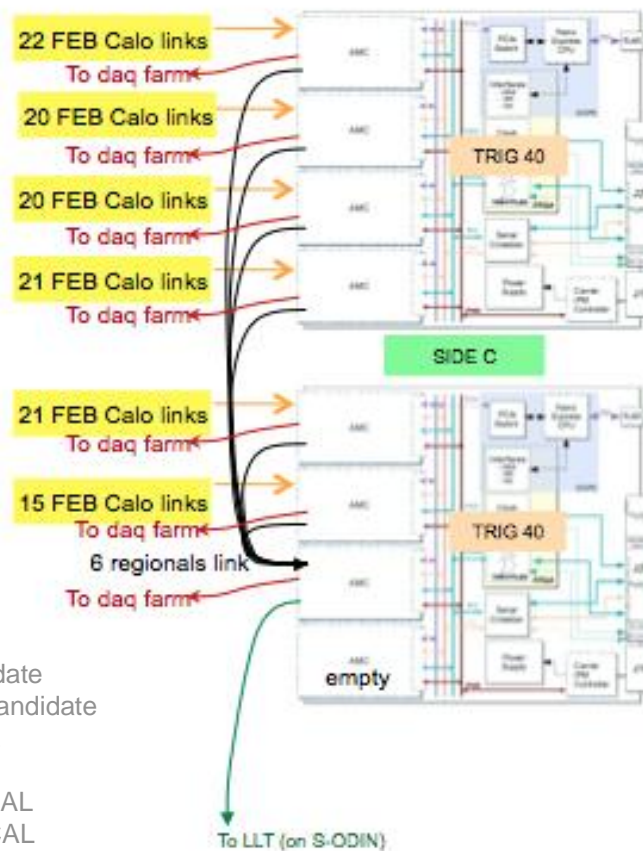
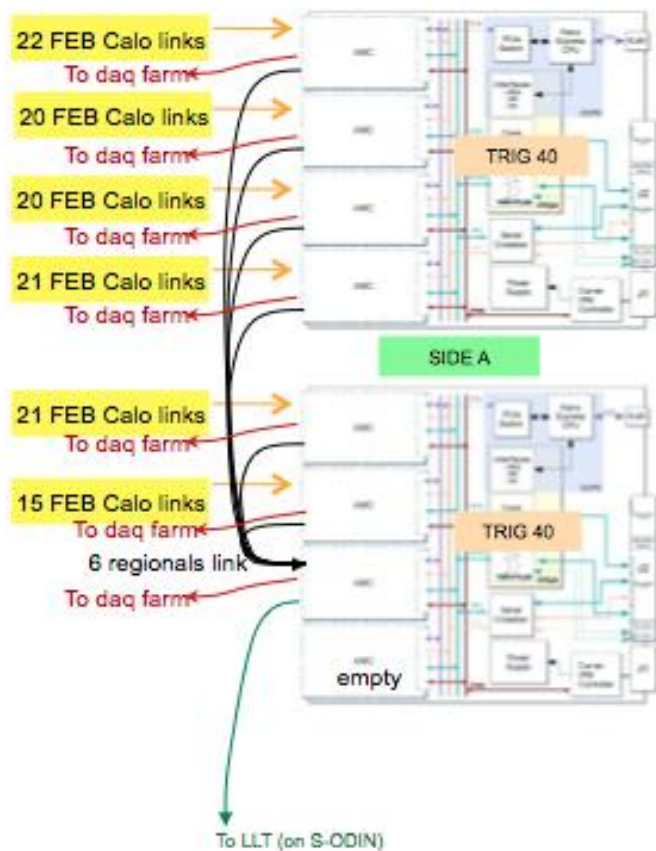
Summary

- ◆ Upgrade architecture with New FEB, New CROC board and without TVB.
- ◆ Re-used old Front-end crate and old 6U and 3U backplane.
- ◆ On each FEB, 4 GBTX chip (one way) for data, 1 GBTX chip (one way) for LLT.
- ◆ Used Actel FPGA family reprogrammable (A3PE family) for new and new CROC board.
- ◆ Prototype new feb and new Croc current 2014 (GBT available ?)

Spare

LLT Calo

◆ Implementation on the TRIG40 side



Output (per side):

- Hadron candidate
- « Electron » candidate
- SumET HCAL
- SumET ECAL
- Multiplicity ECAL
- Multiplicity HCAL

Cyril Drancourt Slide