Pole Zero Shaping: plateau and spill-over

Upgrade of the front end electronics of the LHCb calorimeter

E. Picatoste

Universitat de Barcelona

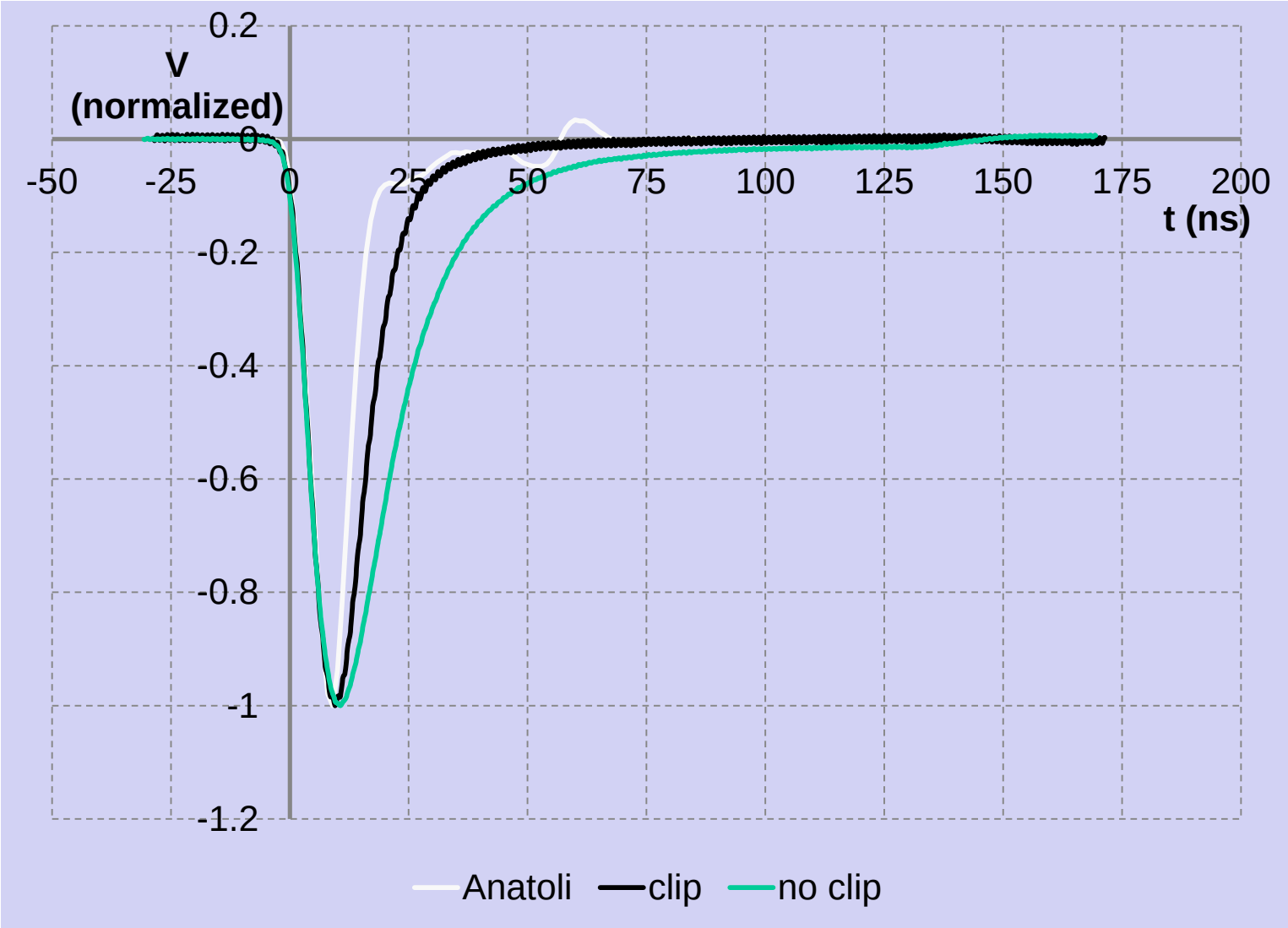
Institut de Ciències del Cosmos ICC-UB

Calorimeter Upgrade Meeting – April 12th 2013

Outline

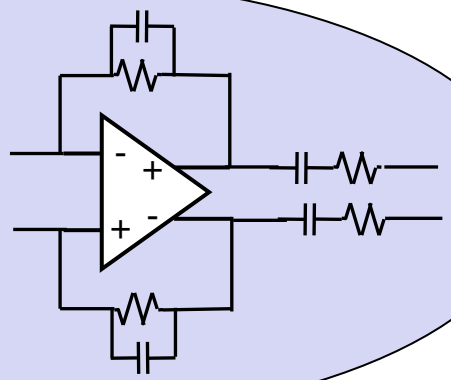
I. Signal Shapes
II. Proposed PZ filters
III. Transient simulations
IV. Plateau
V. Spill Over
VI. Noise

Signal Shapes



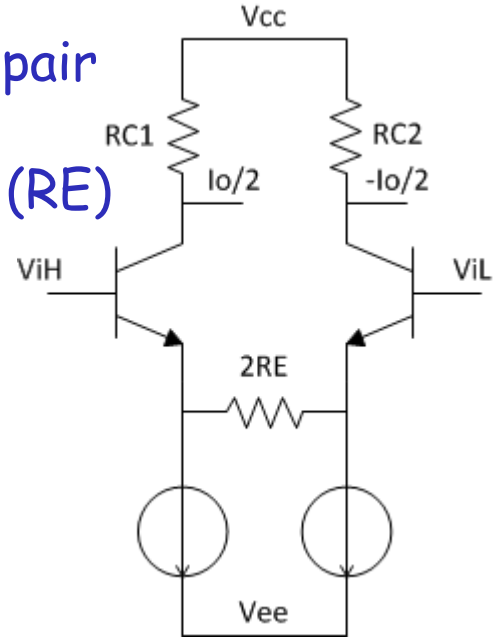
Proposed solution

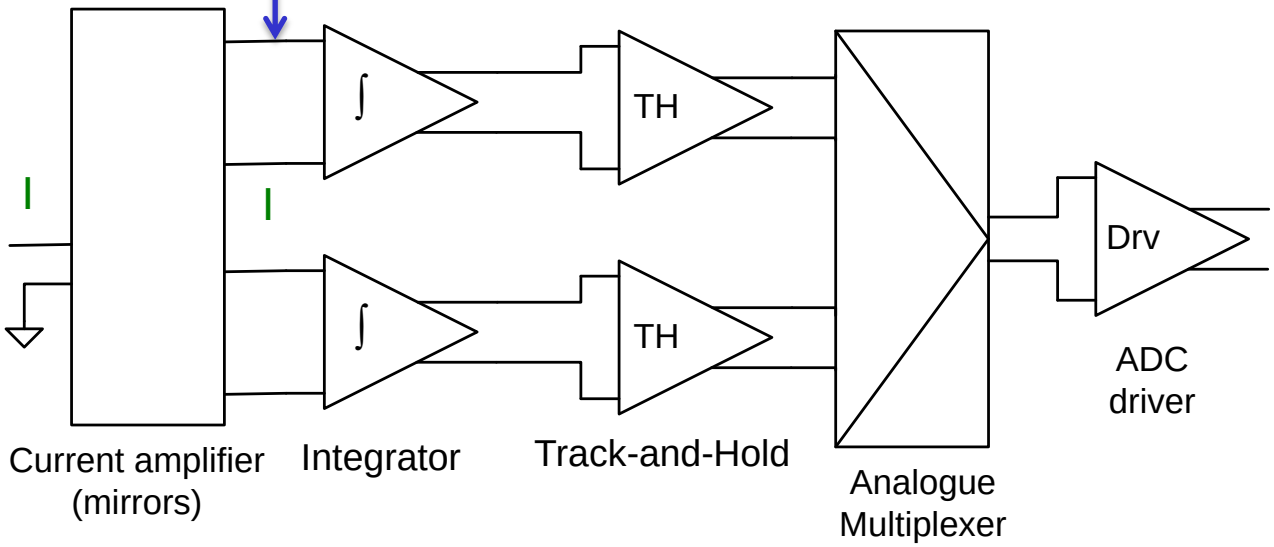
Insert:
Fast pole-zero filter



If needed:

add a bipolar pair with emitter degeneration (RE)

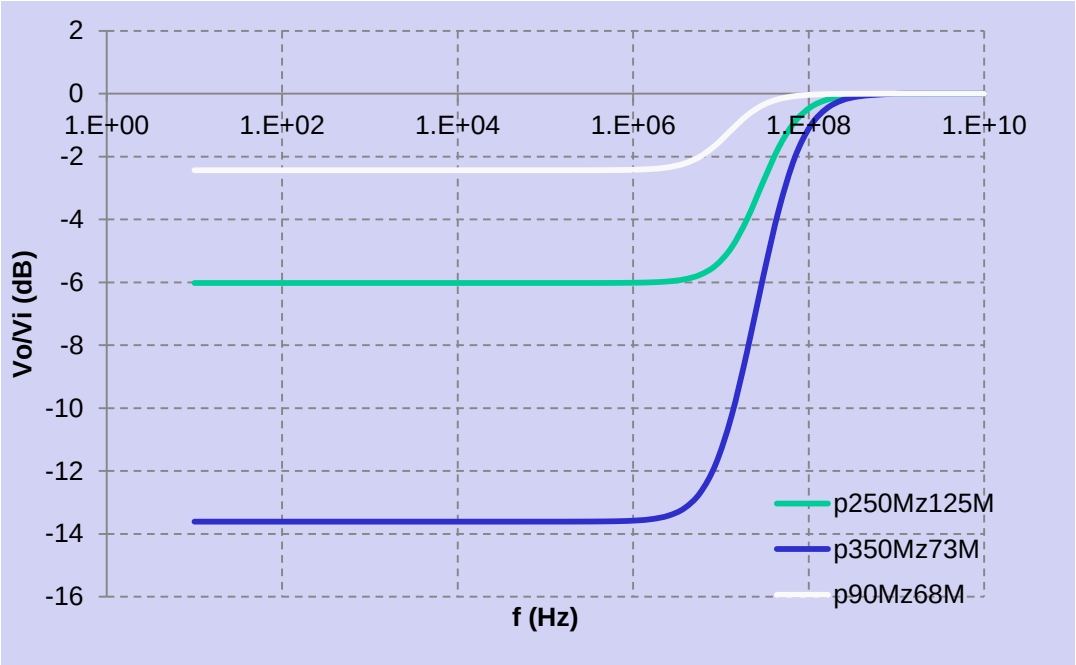




PZ filter Bode diagrams

Signal	Pole	Zero
TB2012 clipped	250 MHz	125 MHz
TB2012 not clipped	350 MHz	73 MHz
Anatoli	90 MHz	68 MHz

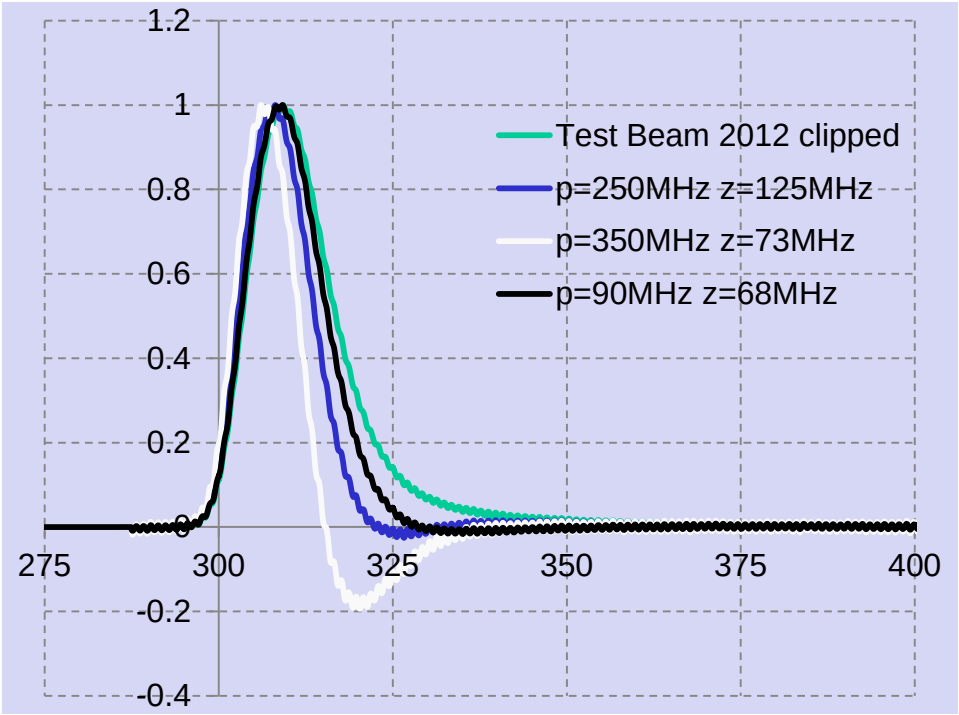
- PZ filter Bode diagrams for the different signals



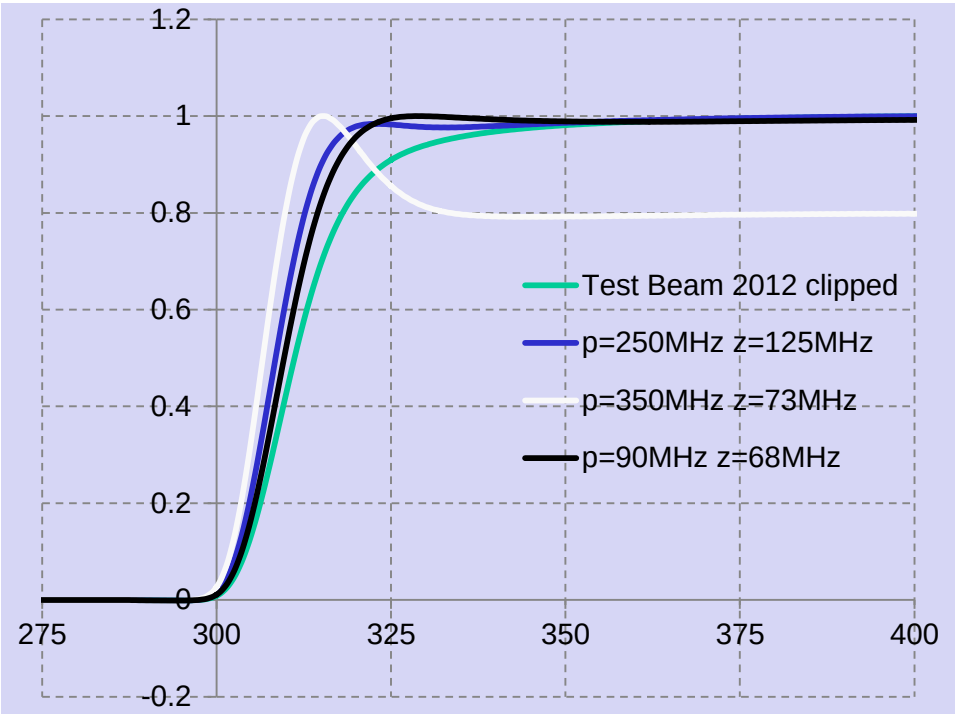
(Note: Functional simulation with VerilogA)

PZ filtered TB2012 clipped signal

TB2012 signal and filter output



Integrated TB2012 clipped signal with filter

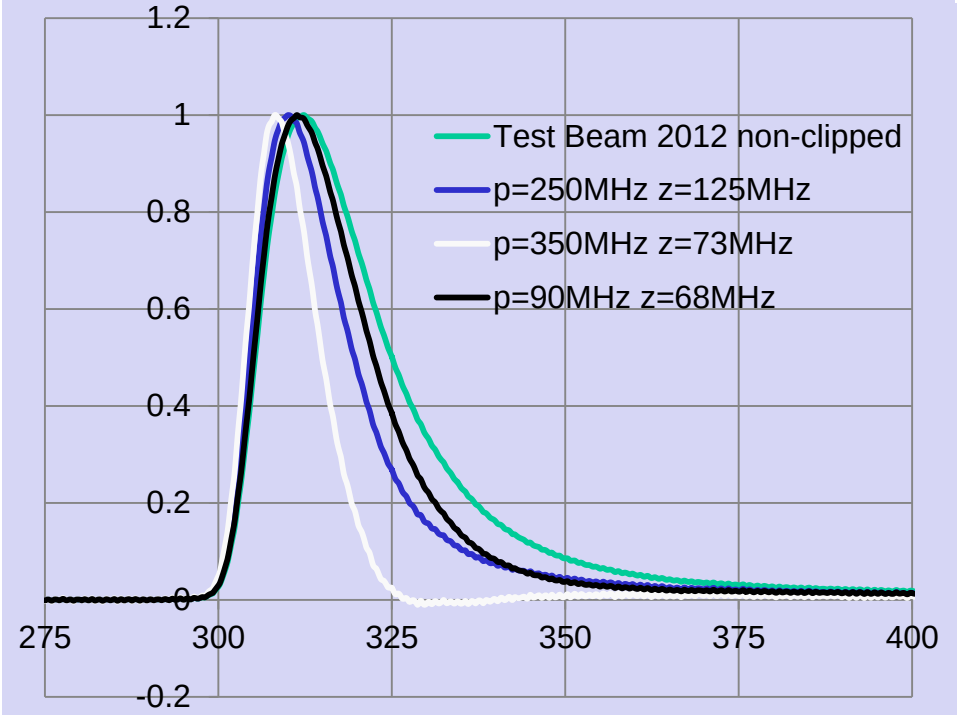


- Test Beam 2012 clipped signal
- Optimum filter pole and zero:
  - Pole at 250MHz
  - Zero at 125MHz

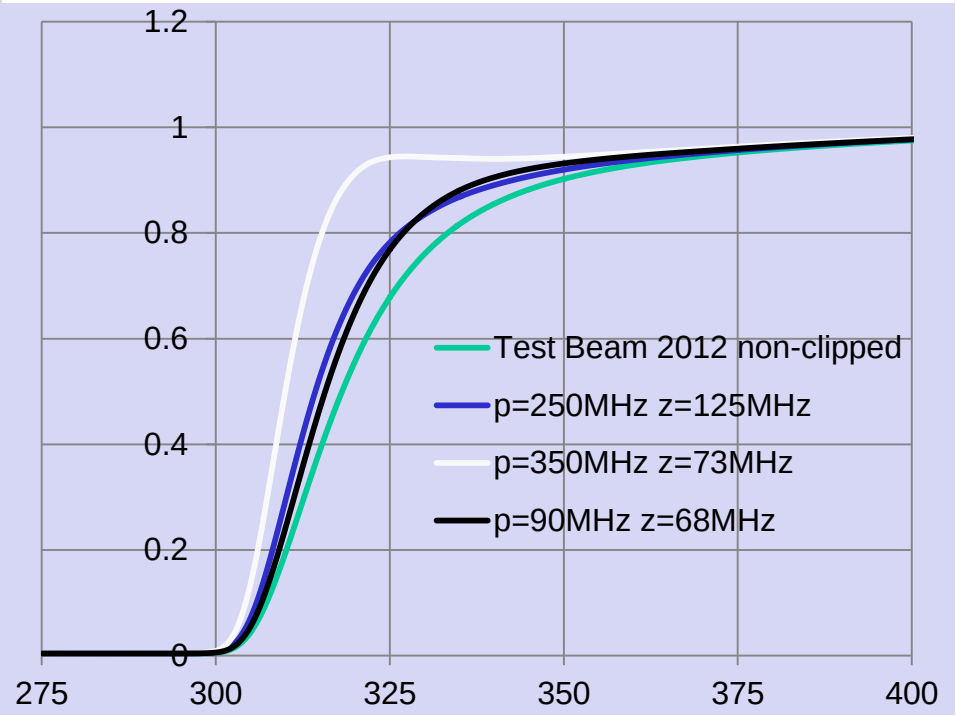
(Note: Functional simulation with VerilogA)

PZ filtered TB2012 non-clipped signal

TB2012 non-clipped signal and filter output



Integrated TB2012 clipped signal with filter

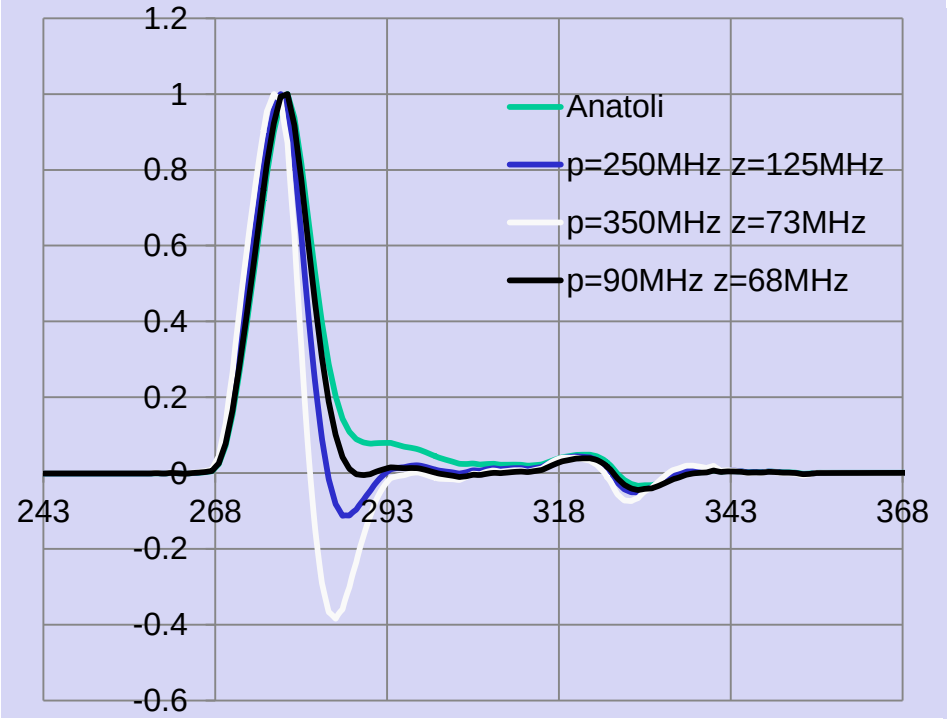


- Test Beam 2012 non-clipped signal
- Optimum filter pole and zero:
  - Pole at 350MHz
  - Zero at 73MHz

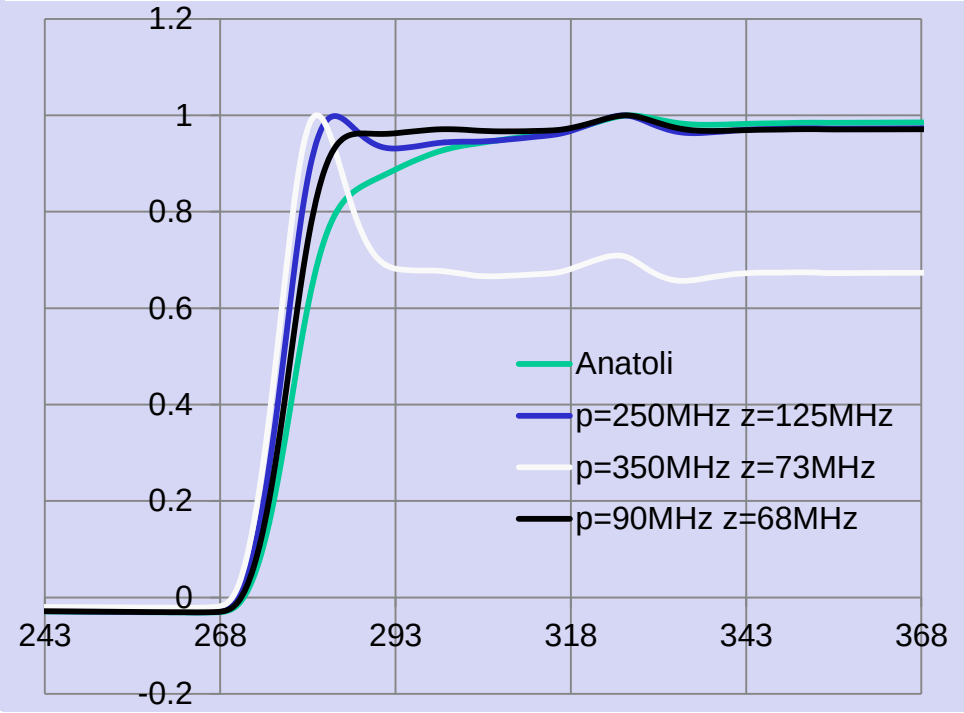
(Note: Functional simulation with VerilogA)

PZ filtered Anatoli's signal

Anatoli's signal and filter output



Anatoli's signal with filter

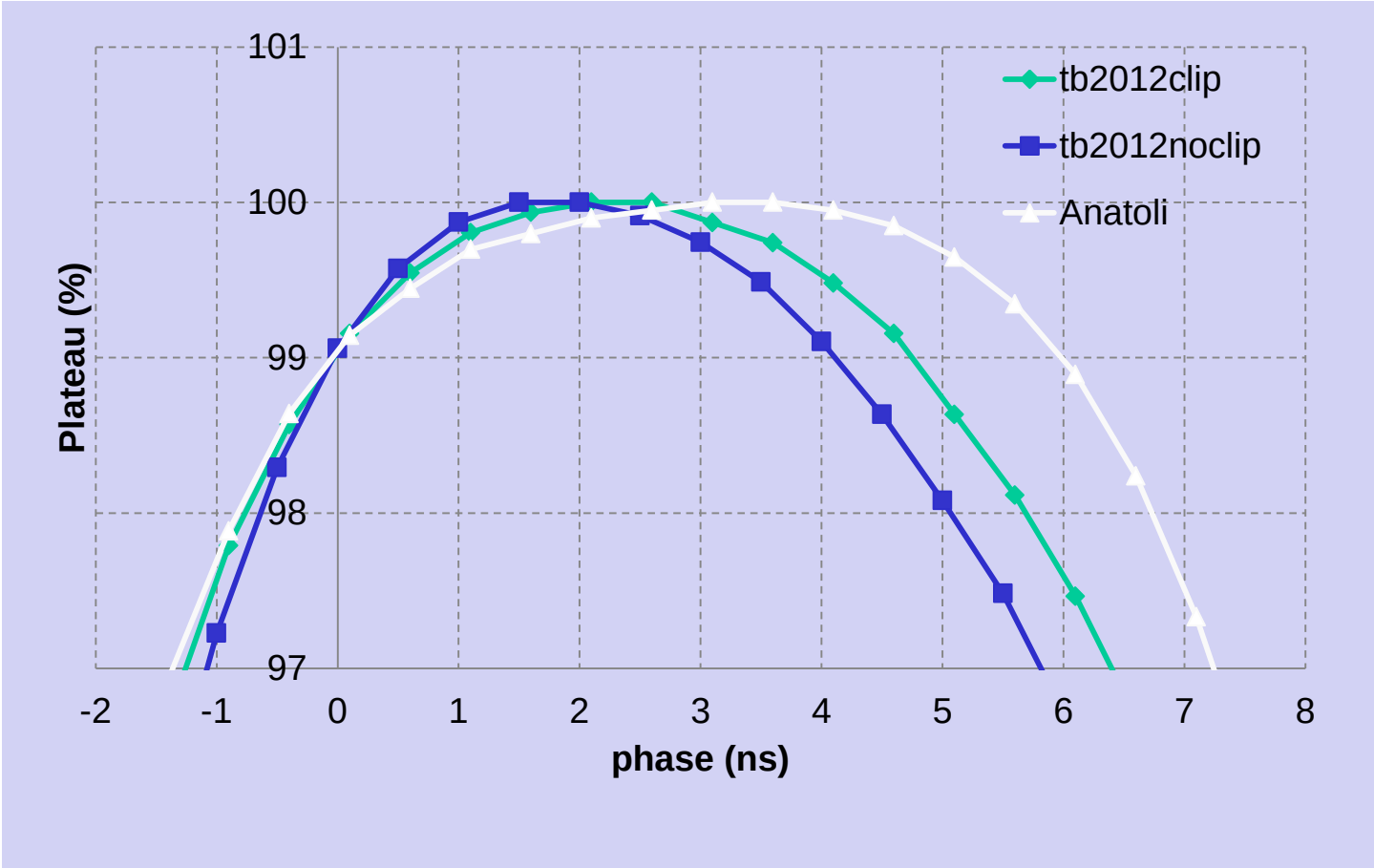


- Anatoli's signal
- Optimum filter pole and zero:
  - Pole at 90MHz
  - Zero at 68MHz

(Note: Functional simulation with VerilogA)

Plateau

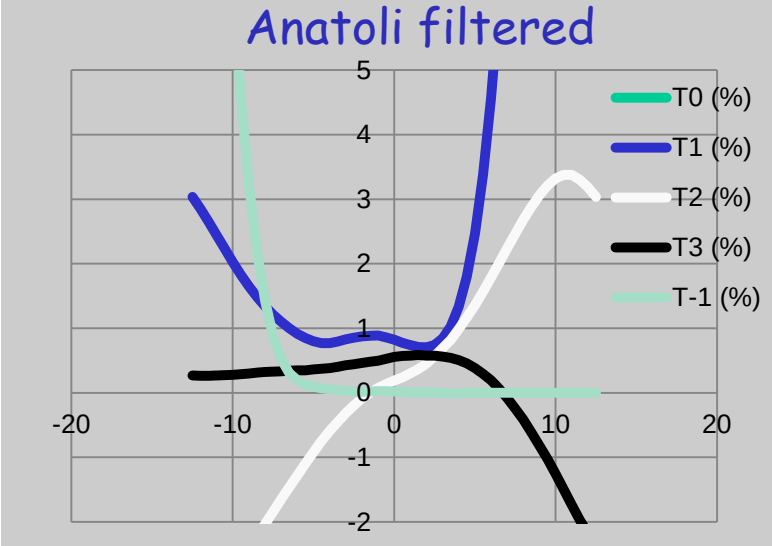
Plateau for each signal and corresponding optimal filter

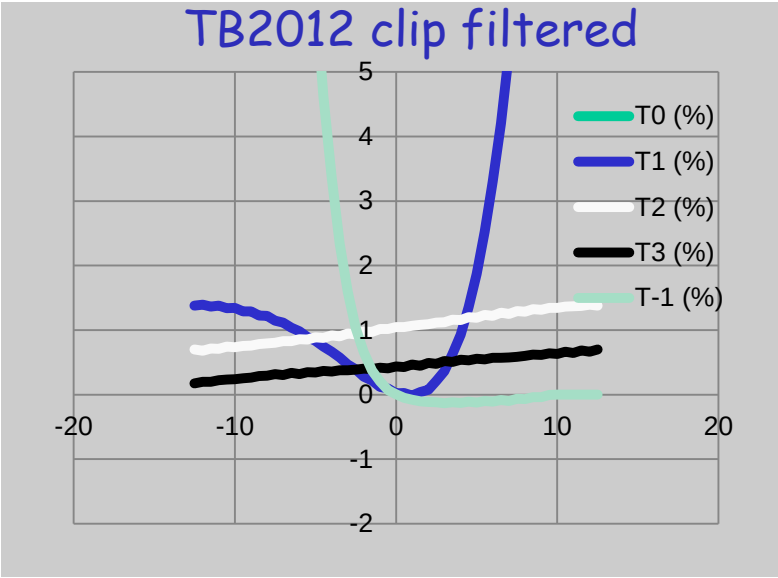


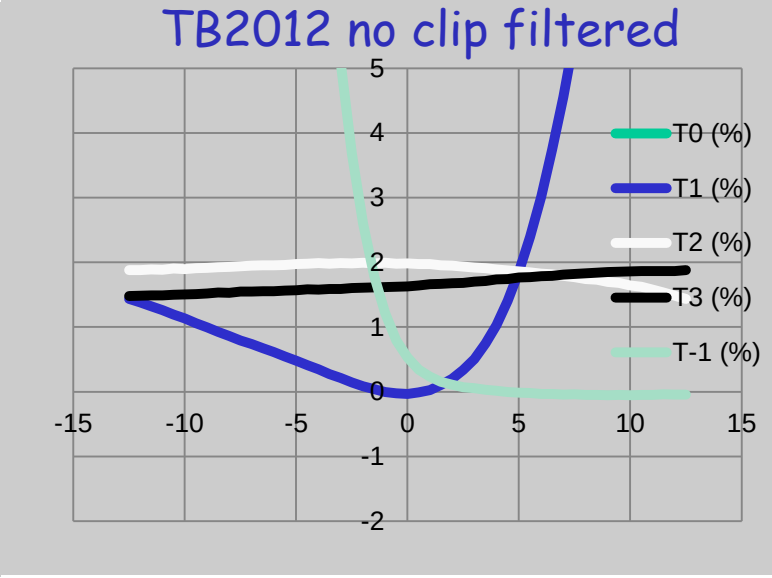
(Note: Functional simulation with VerilogA)

Spill Over

- Integration output over different clock cycles:
  - T-1, T0, T1, T2, and T3
- Main signal in T0
- Other values must be <1%





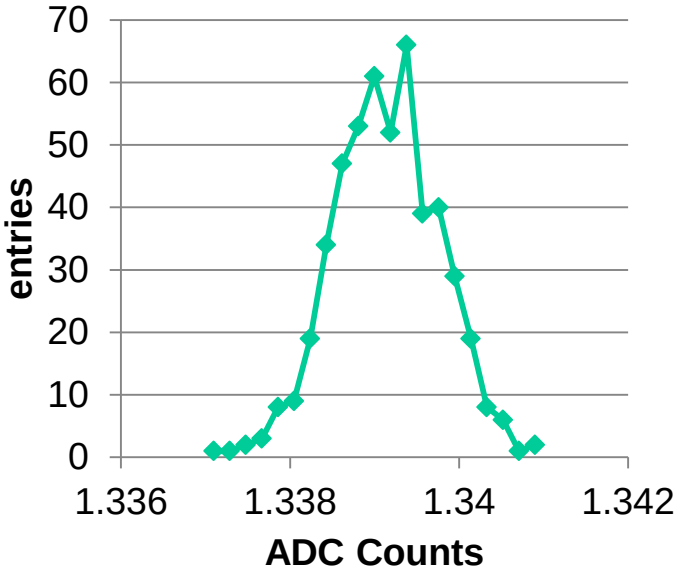


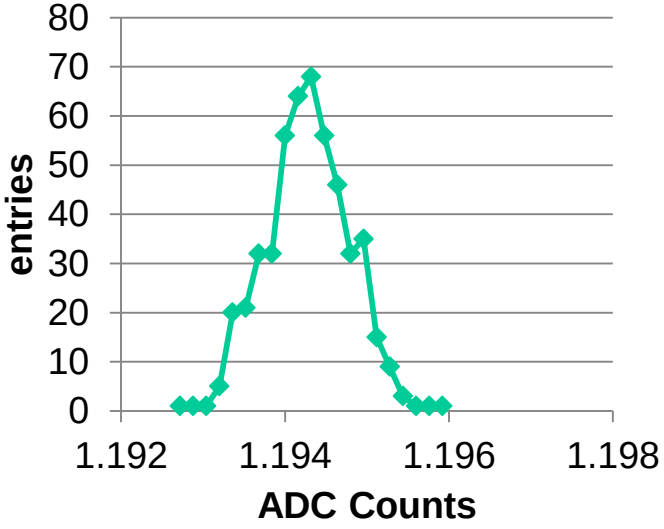
(Note: Functional simulation with VerilogA)

Noise variation

- Transient noise analysis
  - 500 iterations
  - Calibration taken into account
- Results:

Noise no filter (ADC Counts)	Noise with filter (ADC Counts)	Noise increase
1,03	1,13	10 %



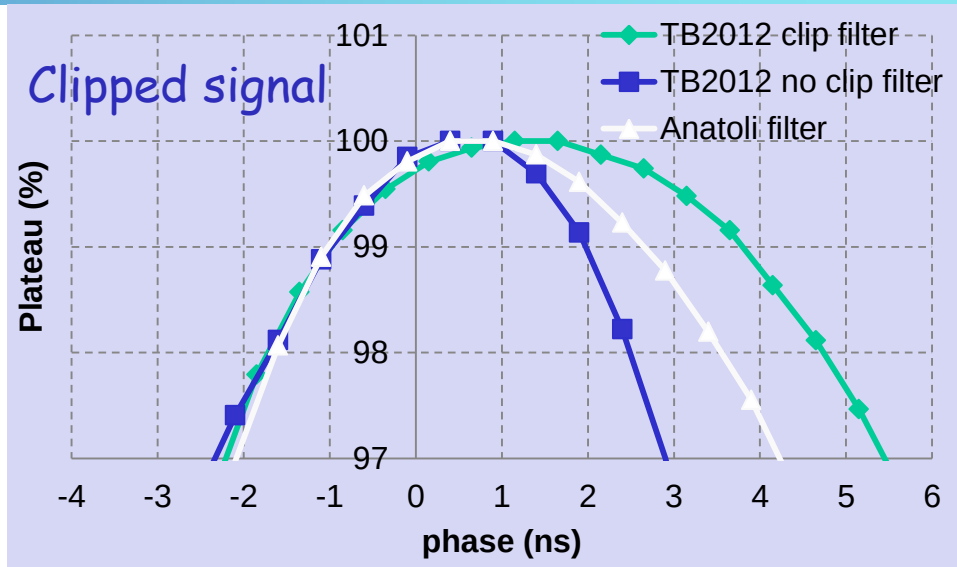


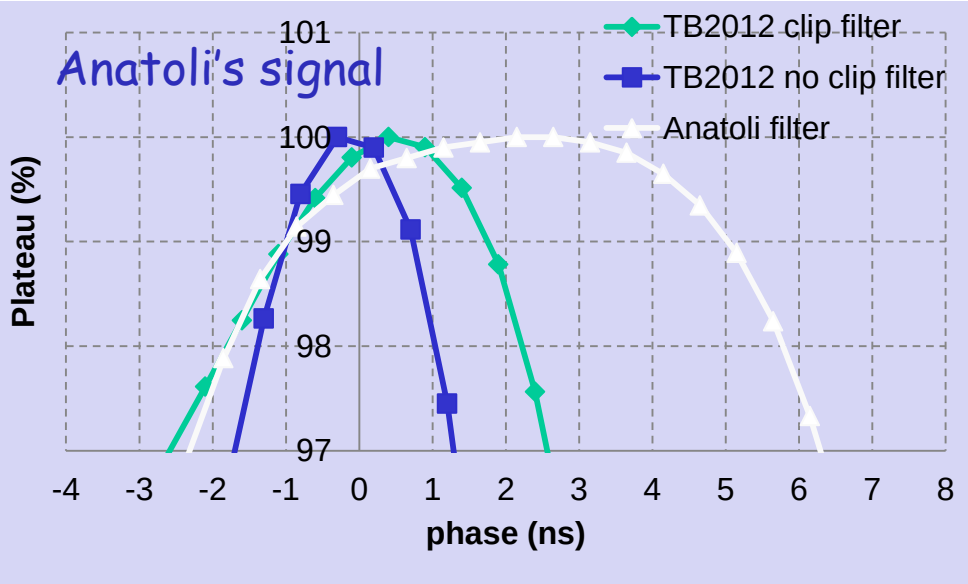
(Note: Functional simulation with VerilogA)

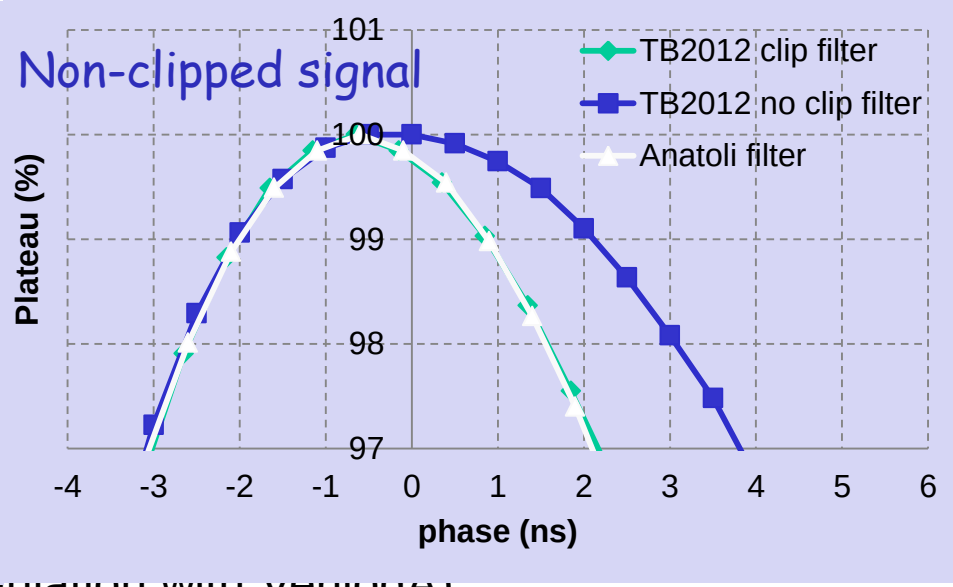
Backup

Plateau

- Effect of the different filters on each signal plateau:



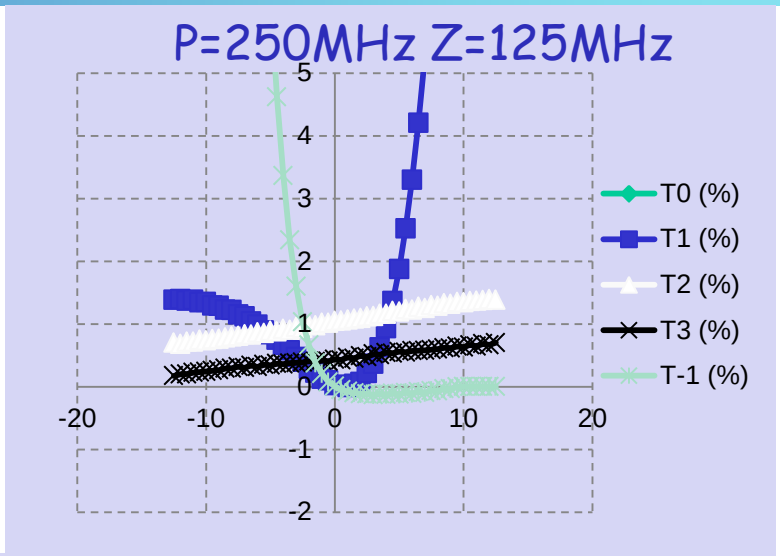


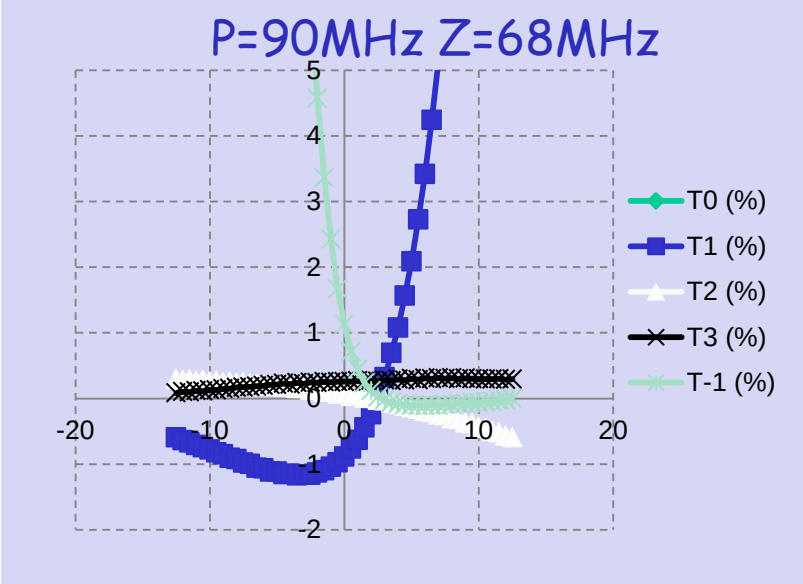


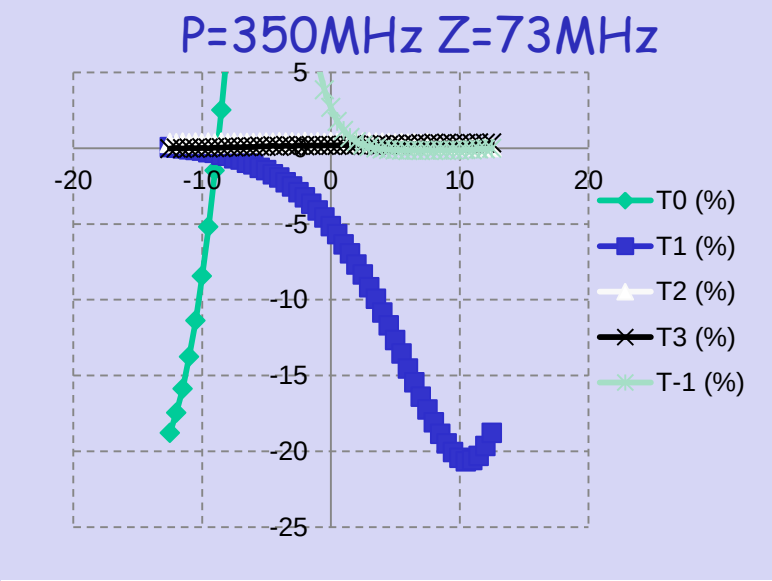
(Note: Functional simulation with VerilogA)

Spill Over: Clipped Signal

- Integration output over different clock cycles:
  - T-1, T0, T1, T2, and T3
- Main signal in T0
- Other values must be <1%



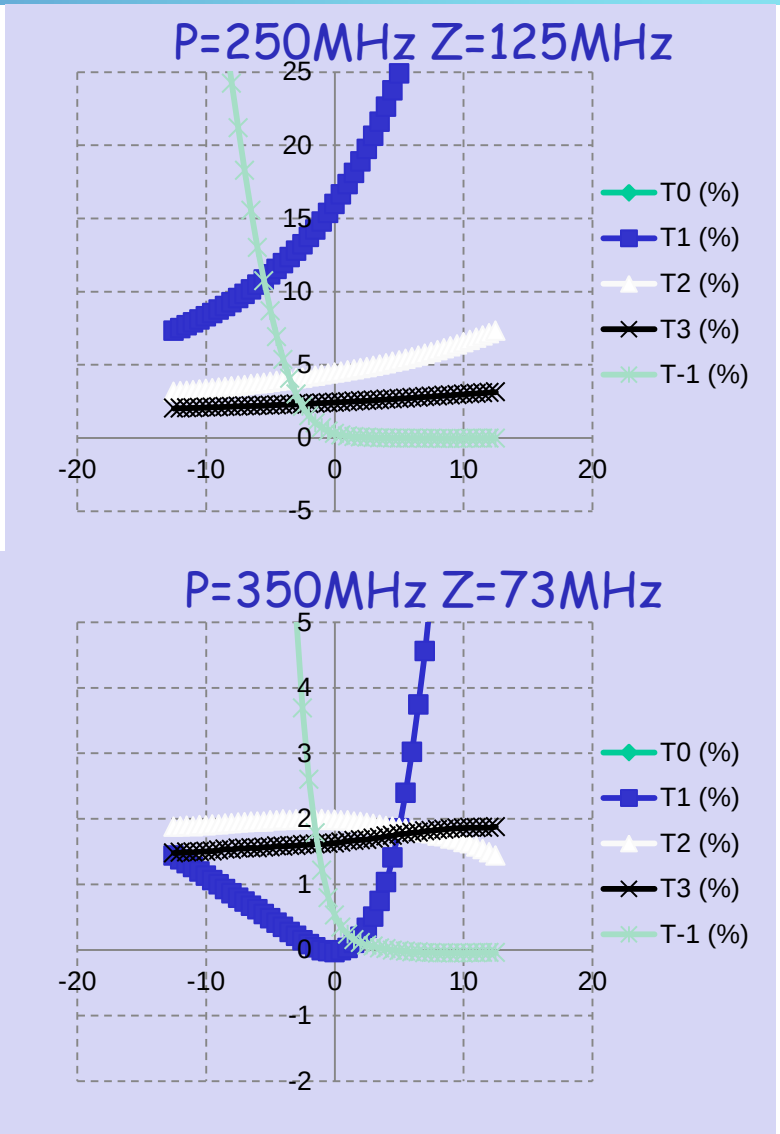


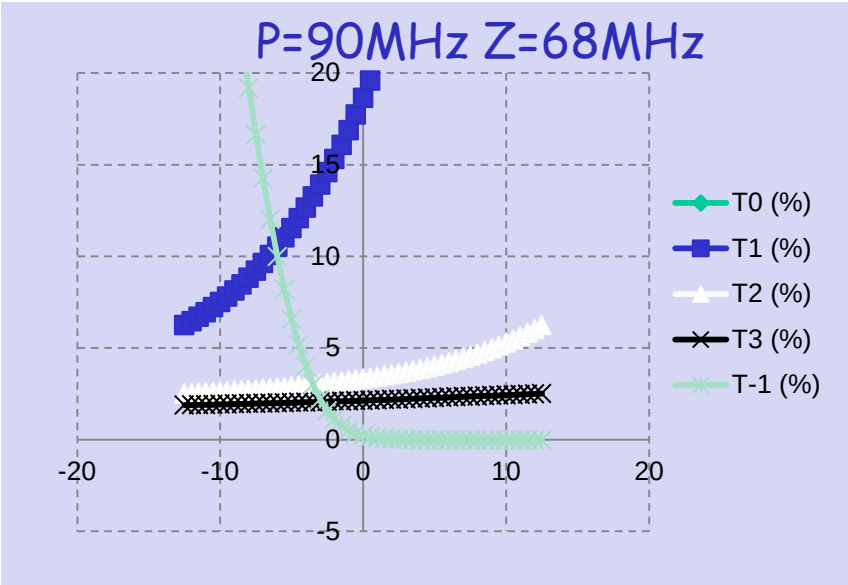


(Note: Functional simulation with VerilogA)

Spill Over: Non-Clipped Signal

- Integration output over different clock cycles:
  - T-1, T0, T1, T2, and T3
- Main signal in T0
- Other values must be <1%

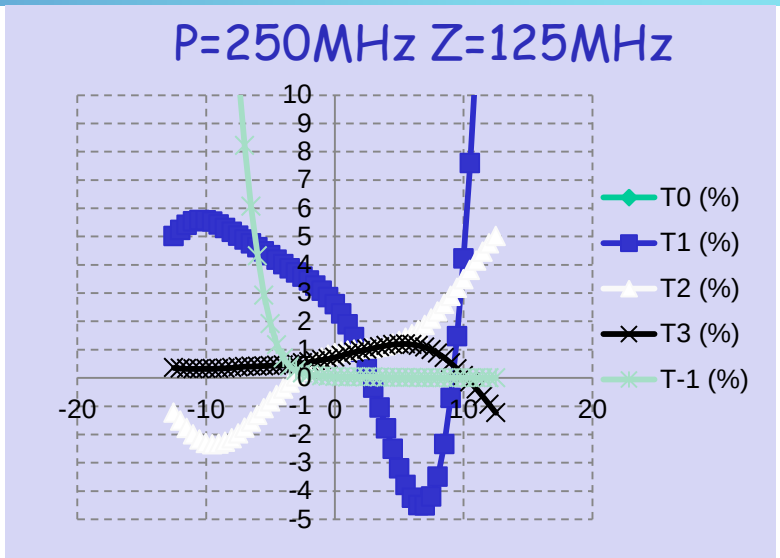


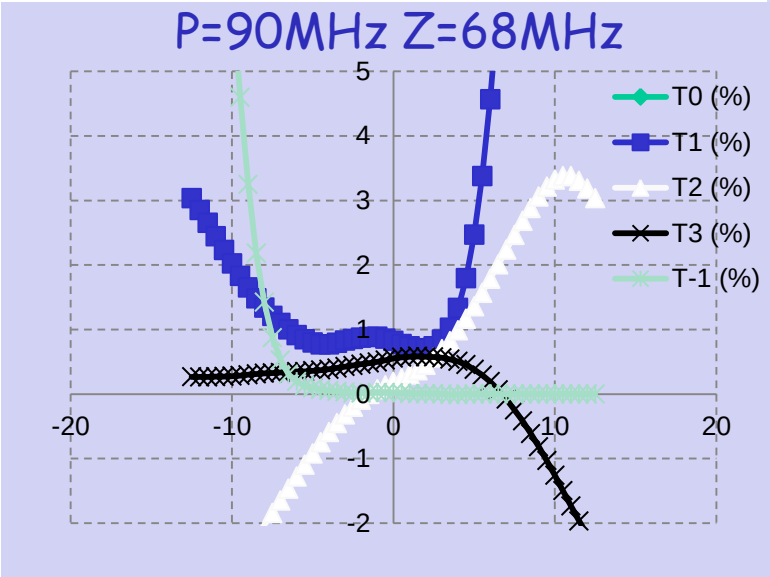


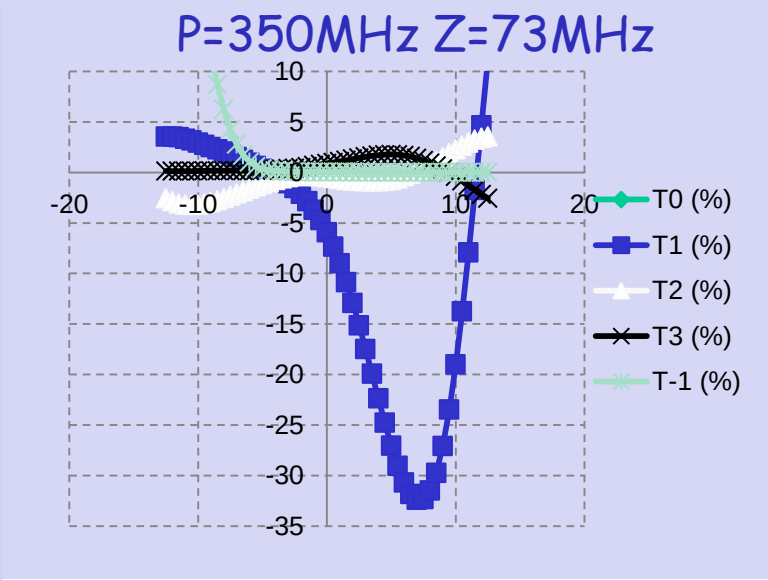
(Note: Functional simulation with VerilogA)

Spill Over: Anatoli's Signal

- Integration output over different clock cycles:
  - T-1, T0, T1, T2, and T3
- Main signal in T0
- Other values must be <1%







(Note: Functional simulation with VerilogA)