Title: Radiation hard programmable delay line for LHCb Calorimeter Upgrade.

Abstract (max 100 words):

This paper describes the implementation of a SPI-programmable clock delay chip based in a Delay Locked Loop (DLL) to delay the LHC clock (25 ns) in steps of 1ns, with 4 ps jitter and 18 ps of DNL. The delay lines will be integrated into the Front-End ICECAL ASIC in a near future. The stringent noise requirements of the ASIC imply minimizing the noise contribution of digital components. This is accomplished by implementing the DLL in differential mode. To achieve the required radiation tolerance several techniques are applied: double guard rings between PMOS and NMOS transistors as well as glitch suppressors and TMR Registers. This 5.7 mm2 chip has been implemented in CMOS 0.35um technology.

Summary (max 500 words):

Delay lines are commonly used in high energy physics experiments since synchronization is critical for such kind of applications. The operating principle of digital delay lines is very simple: the user can set an arbitrary delay and thus compensate the latency introduced by cables and fibers.

This paper describes the implementation of a SPI-programmable 4 triple channel (12 clock outputs) delay line based in a Delay Locked Loop (DLL) and developed for the LHCb Electromagnetic Calorimeter (ECAL) Upgrade. The user can configure up to 25 different clock phases to cover the 25 ns LHC clock in 1-ns steps. The DLL is adjusted by means of two control voltages: the former is automatically generated by the phase comparator and charge pump circuit, while the later is externally adjusted by the user. This dual adjust provides an operating range of 17.45 to 39.88 ns, wider enough to ensure that systematic process variations or environmental variations will not prevent working properly with the LHC clock. The differential design as well as the use of Weak Inverters to ensure 180º phase and the implementation in 0.35um technology favors the minimization Differential Non Linearity (DNL), which is equal to 18 ps for each 1-ns delay element.

Despite this delay line chip can operate in standalone mode, it will be integrated into the next Front-End ICECAL ASIC implementation in a near future, and consequently, the stringent noise requirements of the ASIC analog components must be met by the digital components that delay line integrates. Therefore, the fully differential design of the DLL aims to reduce the switching noise produced by delay lines. The use of double guard rings also decreases the noise propagation through the substrate. The clock jitter produced by transient noise is lower than 4 ps.

Design methodology of this chip prototype is also determined by the radiation environment where DLLs will operate. ICECAL chips will be assembled into ECAL Front-End Boards (FEBs), placed inside the LHCb cavern. What is more, the energy increase of the LHC machine (from 7 to 14 TeV) will increase the potentially dangerous ionizing radiations and thus, the probability of suffering from single events. Consequently, design must tolerate SEUs, SETs and SELs. The probability of suffering SELs is reduced by increasing the distance between PMOS and NMOS transistors and inserting double guard rings between them, so that PMOS and NMOS transistors are confined inside islands of the same transistor type. SEUs are avoided by implementing Triple Modular Redundancy Registers to store the DLL configuration and fault tolerant Finite State Machine in the SPI Slave. Finally, reset signals are protected from SETs by means of glitch suppressors.