CNPEM
Brazilian Center for Research
in Energy and Materials

Brazilian Synchrotron
Light Laboratory

A MicroTCA system for Sirius BPM

6th meeting of the xTCA interest group

Daniel de Oliveira Tavares

On behalf of the LNLS Beam Diagnostics Team

April 9, 2013

Outline

- Overview of Sirius light source
- Sirius BPM and orbit stability specifications
- Hardware design approach
- Proposed BPM and orbit feedback hardware
- Project status and schedule
- Open-hardware collaborative work
- Summary

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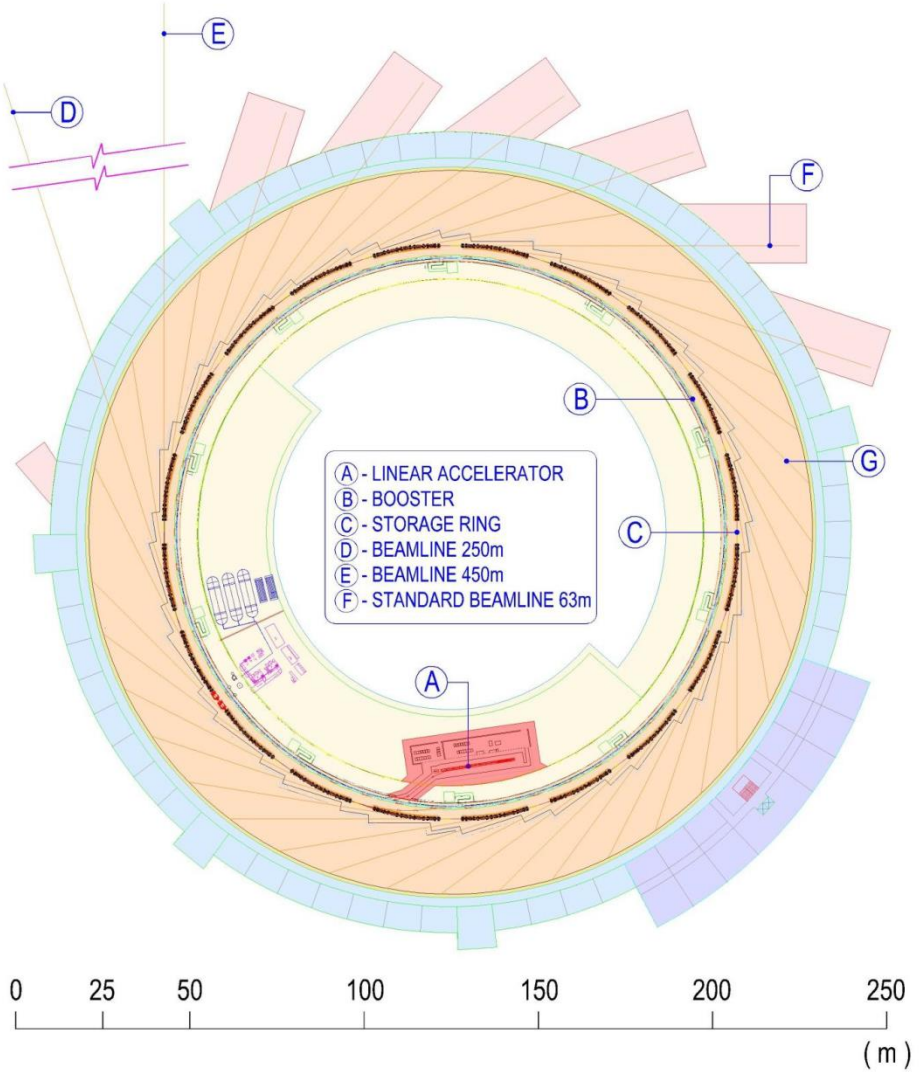
Overview of Sirius light source

- 3rd generation light source providing diffraction-limited beams
- Vertical emmitance @ 1% coupling: 2.8 pm.rad
- RF frequency: 500 MHz
- Natural bunch length: 9 ps
- Circumference: 520 m
- **First beam due to mid-2016**



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Roles of the Sirius BPM system

1. Electron and photon **beam position monitoring** from accelerator's control system
2. Sensor element on storage ring **orbit feedback control**: stabilizes beam orbit at sub-micron level
3. **Orbit interlock**: prevents machine from damage due to mis-steered high power photon beams
4. Machine studies: **turn-by-turn readouts** provide valuable information of machine behavior
5. Failure diagnostics: beam loss analysis (**post-mortem**)
6. General **diagnostics**

Sirius BPM and orbit stability specifications

- Orbit stability at source points*: 10% beam size
- BPM resolution*: 0.14 µm

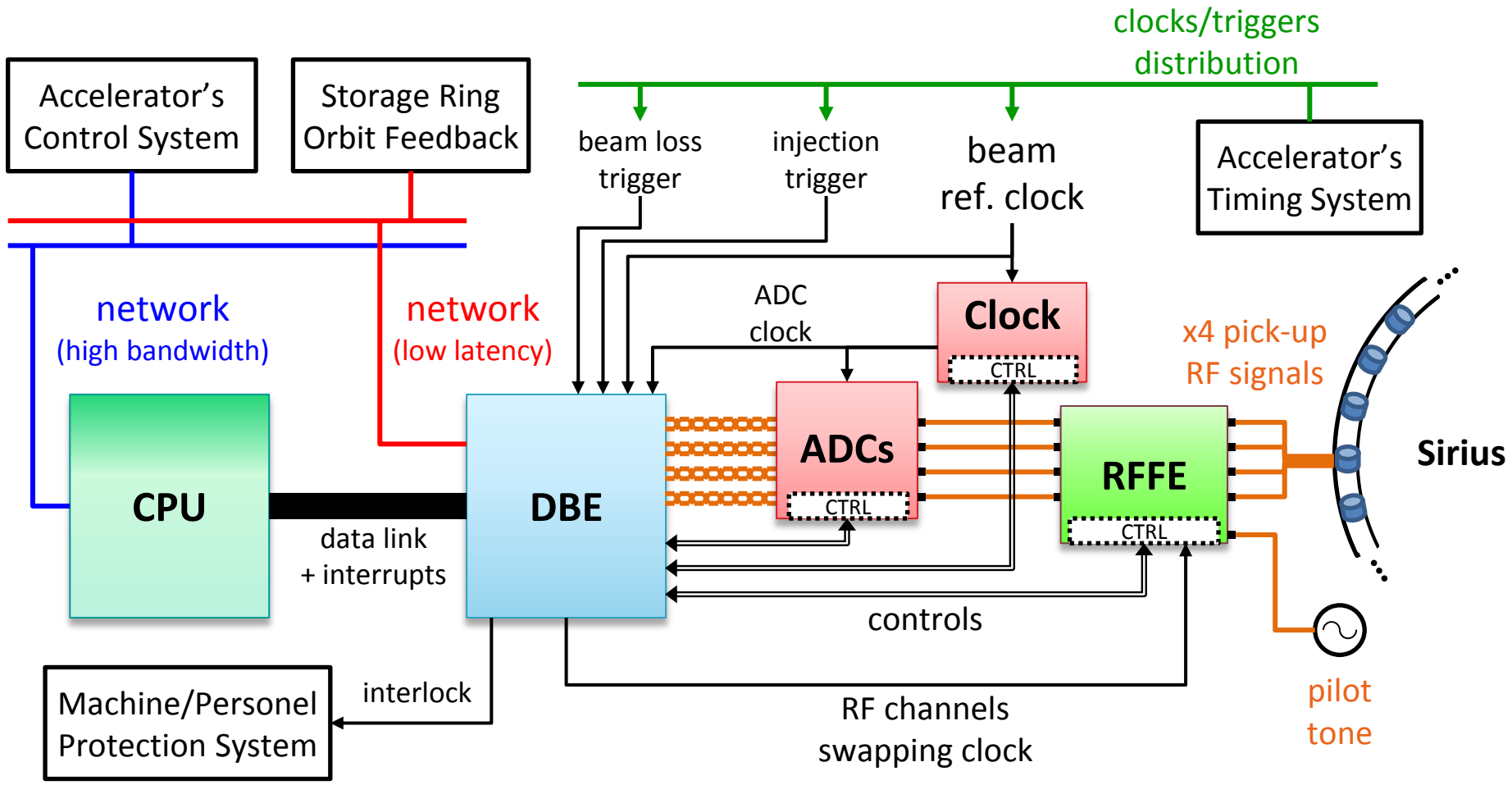
1 µm ≈ 1 mdB
RF signal disbalance

- Beam current dependence/accuracy (with top-up injection): 0.14 µm
- Long-term stability (1 week): +/- 5 µm peak
- Orbit feedback operation availability: 99.8 %

*Integrated RMS over 0.1 Hz to 1 kHz bandwidth

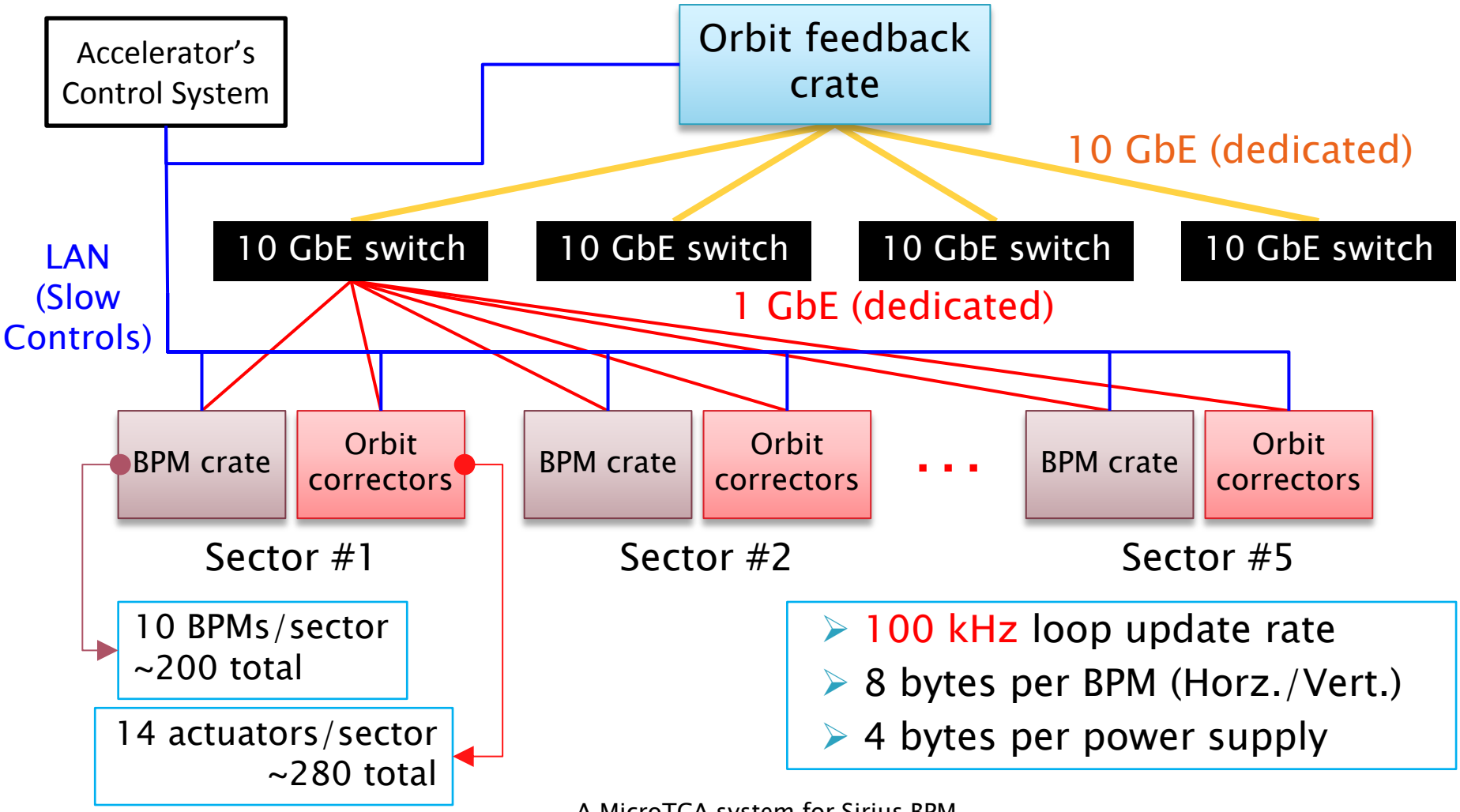
BPM and orbit feedback system

- BPM electronics – interfaces



BPM and orbit feedback system

- Storage Ring orbit feedback – interfaces (planning)



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Hardware design approach

- LNLS approach to fulfill Sirius BPM and orbit feedback hardware requirements with a small engineering team:
  - **RF-BPM analog front-end:** in-house specification and design → accelerator-specific, main performance limiter
  - **BPM ADC boards:** technical specification and design in conjunction with an external company → make bridge between BPM specifications and hardware performance
  - **FPGA board:** only functional specification, 100% outsourced design → generic board with standard interfaces, usable in BPM, orbit feedback and many other applications
  - **System integration:** standard COTS equipment with guaranteed reliability + large user base open-source software → **MicroTCA platform + Ethernet switches + EPICS**

Why MicroTCA?

1. High availability platform

2. Backplane with appropriate connectivity (PCIe x4, GbE)

3. Hardware standard with large user base and diverse available products

4. MicroTCA for physics: clock + trigger distribution

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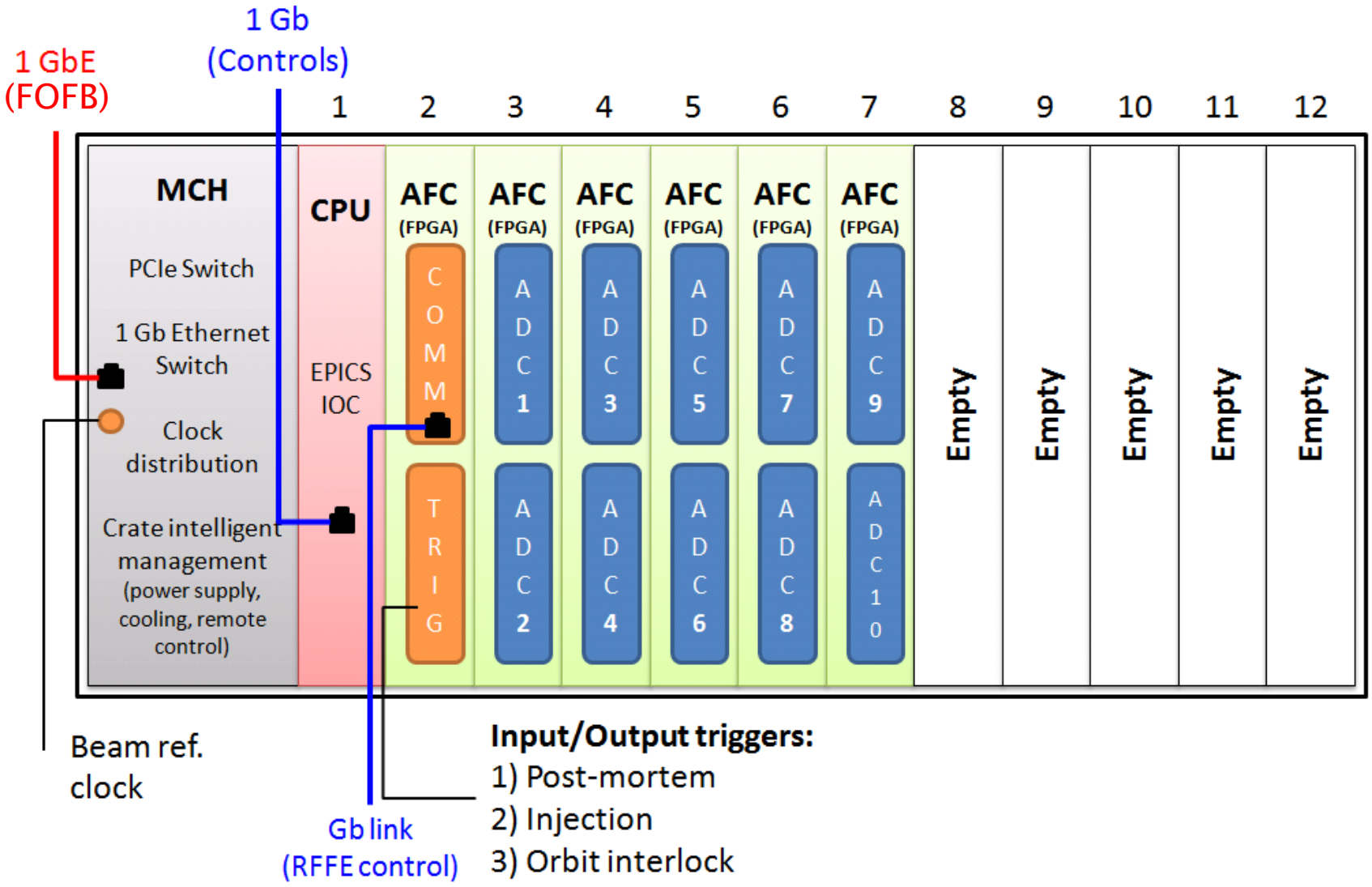
MicroTCA crate for BPM



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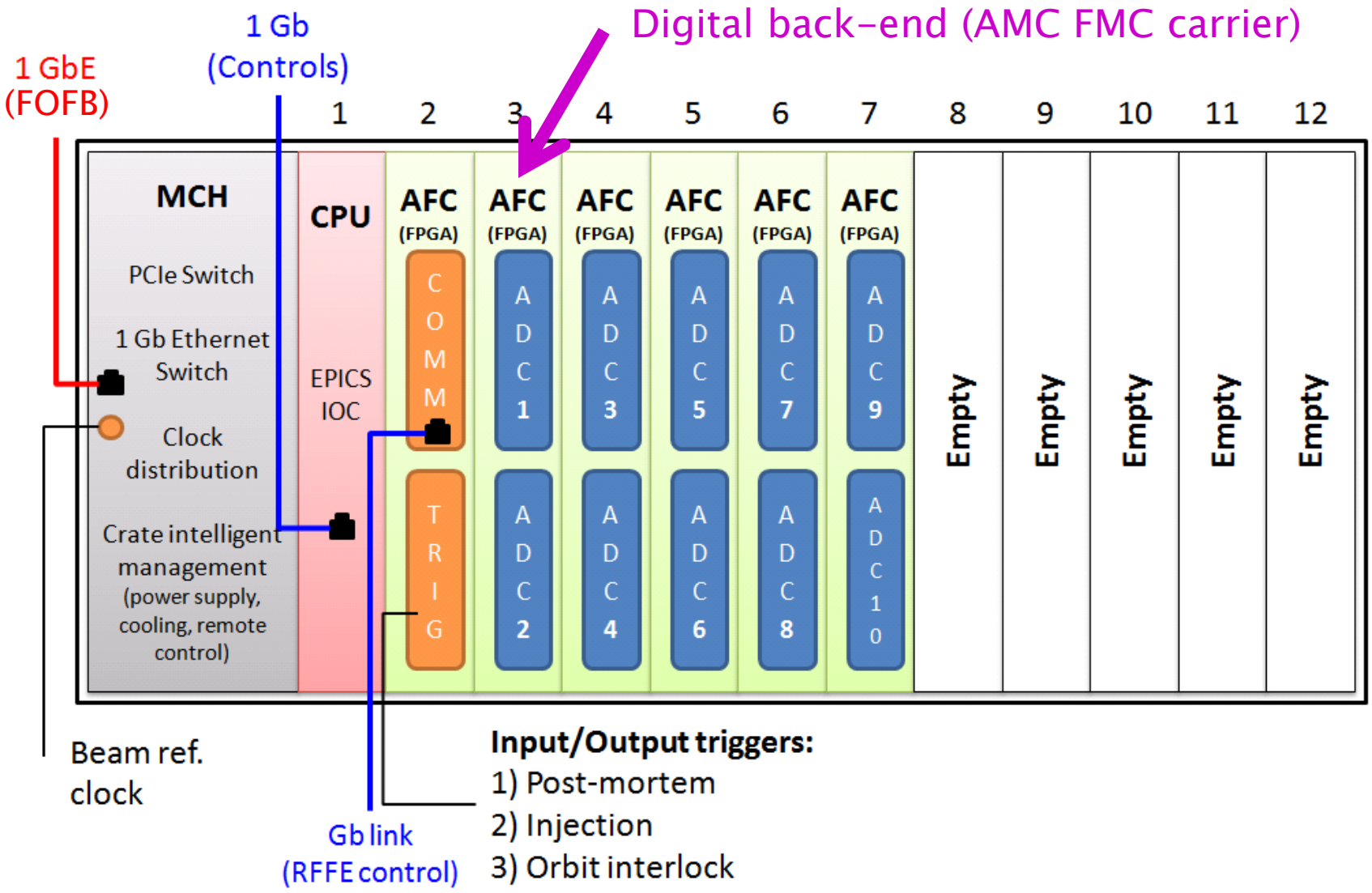


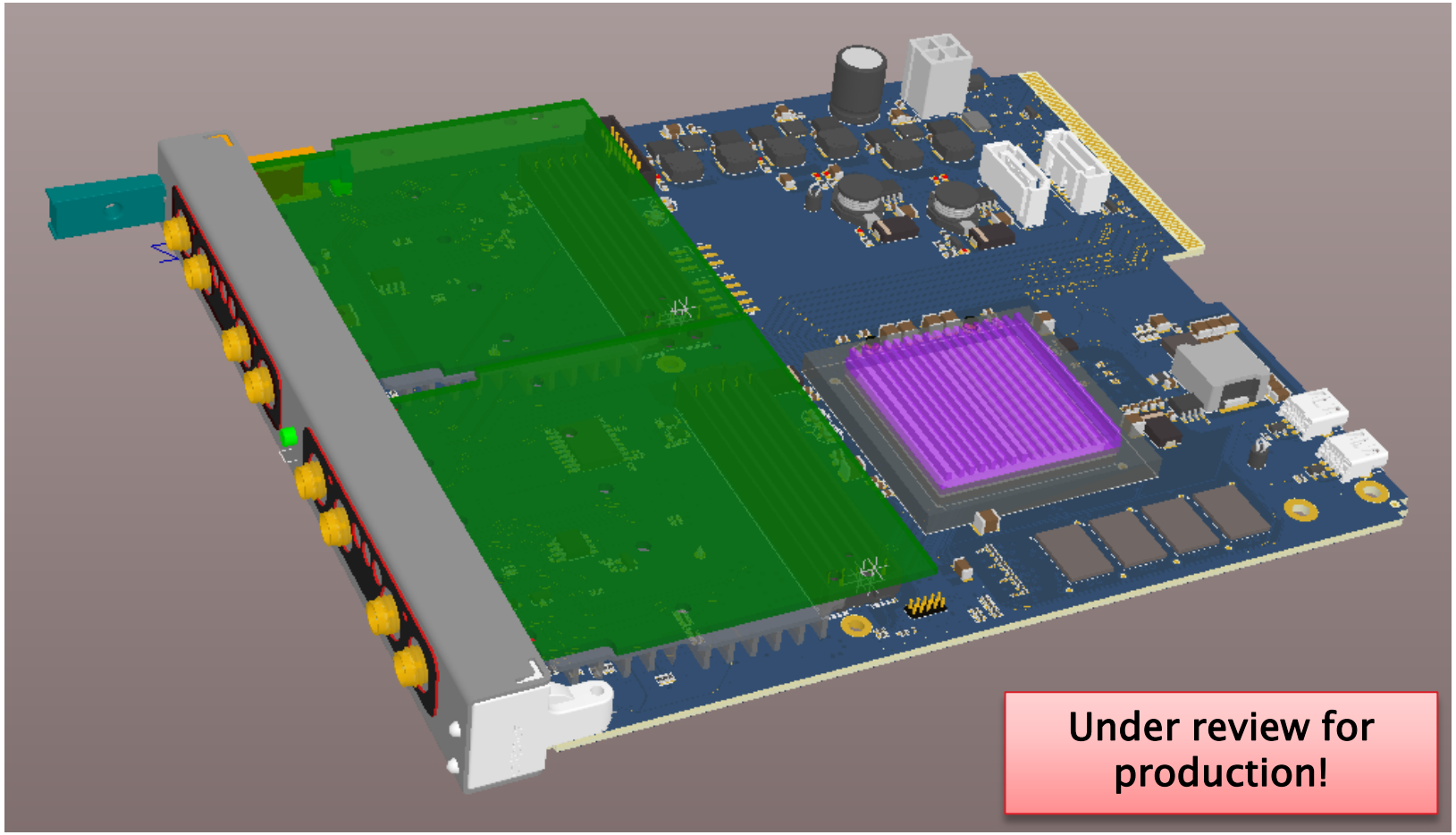
BPM and orbit feedback hardware

- **AMC FMC Carrier (AFC) – Digital Back-End (DBE)**
  - PICMG® AMC compliant
  - Xilinx Artix-7 200T FPGA
  - 2 high-pin count FMC slots, 4 MGT per slot
  - Clocking:
    - FMC clocks CLK[2..3]_BIDIR of any FMC slot can be source or sink of any AMC telecom clock
    - White Rabbit ready
  - 32-bit interface 2 GB DDR3 SDRAM
  - Non-volatile storage:
    - 32 MB NOR Flash
    - 2 Kb EEPROM with unique MAC address identifier
  - GbE ports [0..1] + fat pipe ports [4..11] fully assigned to FPGA MGTs
  - MicroTCA.4 M-LVDS triggers
  - Board health monitoring (temperature, voltages, currents)

Designed by Creotech and Warsaw University of Technology (WUT) for LNLS

BPM and orbit feedback hardware

- AMC FMC Carrier (AFC)



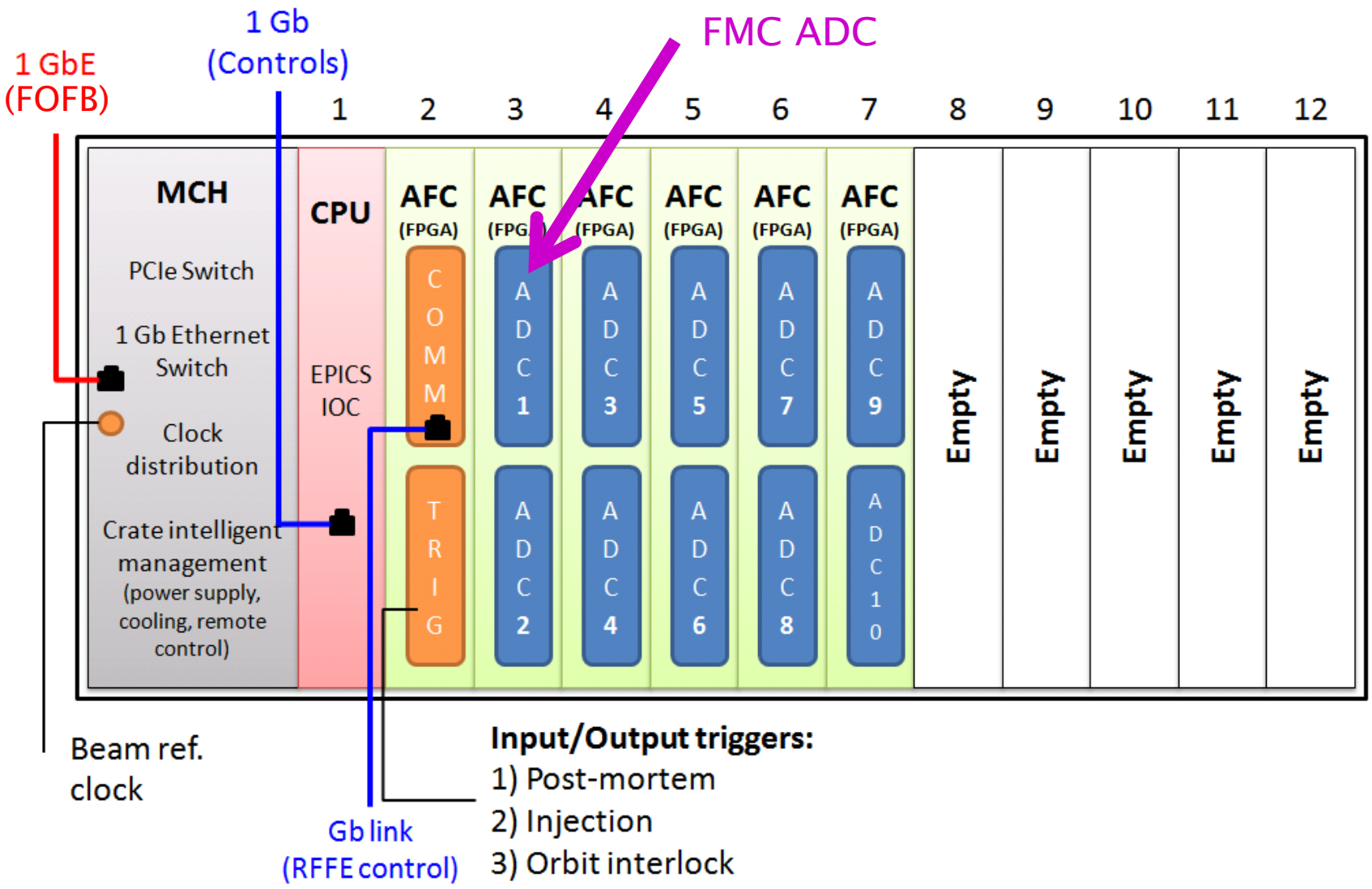
BPM and orbit feedback hardware

- **AFC as BPM digital back-end:**
  - FMC slots: 4-channel FMC ADC boards (2 boards per DBE, then 2 BPMs per DBE)
  - Input triggers (beam loss, injection) from backplane M-LVDS lines
  - Output trigger (interlock) to backplane M-LVDS lines
  - Slow controls and data acquisition readout via PCIe x4 fat pipe
  - Dedicated orbit feedback low latency communication via 1 GbE backplane port

BPM and orbit feedback hardware

- **AFC as orbit feedback controller (planning):**
  - FMC slots: COTS FMC 10 GbE board (SFP+, XAUI interface)
  - Slow controls and data acquisition readout via PCIe x4
  - Fast data storage via SAS/SATA (e.g.: daily buffer of fast orbit data)

MicroTCA crate for BPM



BPM and orbit feedback hardware

- **FMC ADC modules**
  - ANSI/VITA 57.1 compliant
  - 4-channel 16-bit ADC
  - 2 board versions
    - 130 MS/s – LTC2208
    - 250 MS/s – ISLA216P25
  - Input/output trigger
  - ADC clock: from external input or from PLL locked to external reference
  - External clock/reference from front panel or FMC connector
  - PLL frequency fine tuning (+/- 10 kHz range, 50 Hz granularity)
  - 700 MHz bandwidth, optimized for 500 MHz input signal
  - ENOB @ 500 MHz > 10 bits

Jointly designed by LNLS, Creotech and Warsaw University of Technology (WUT)

BPM and orbit feedback hardware

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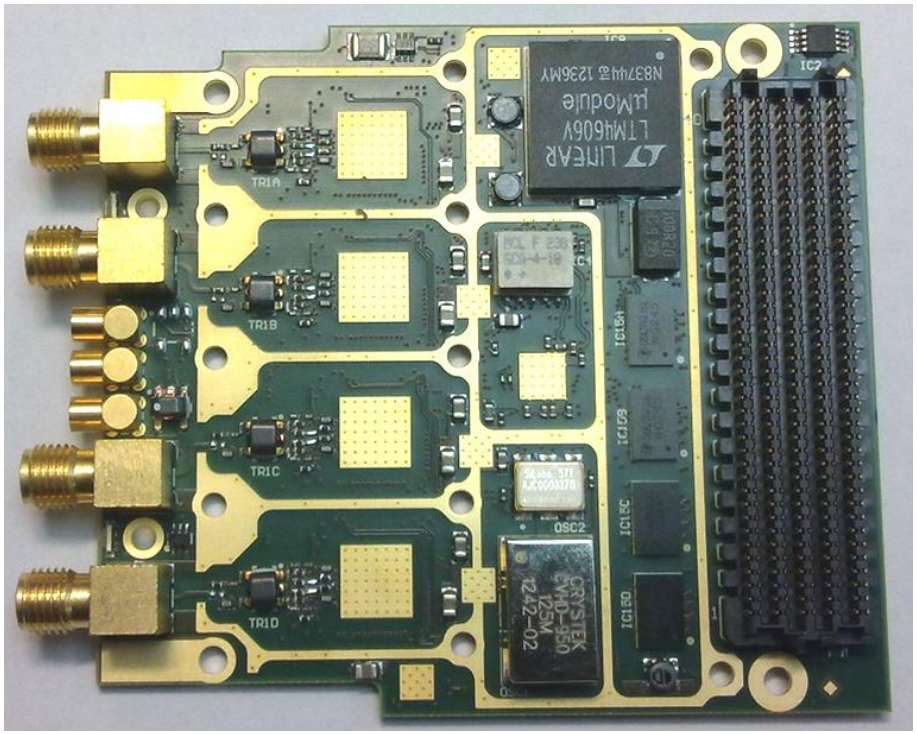

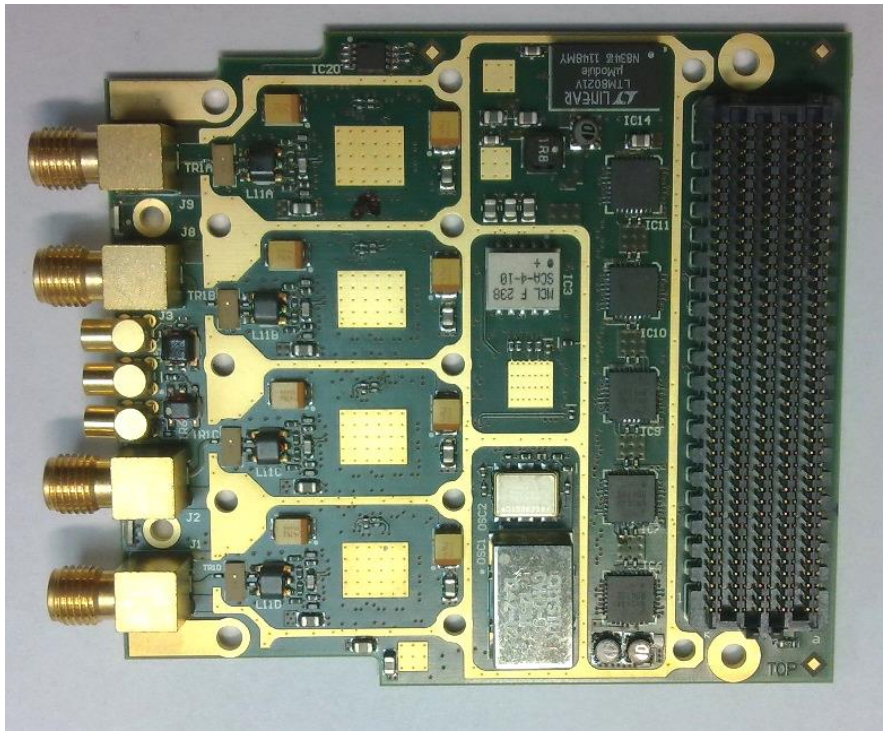

BPM and orbit feedback hardware

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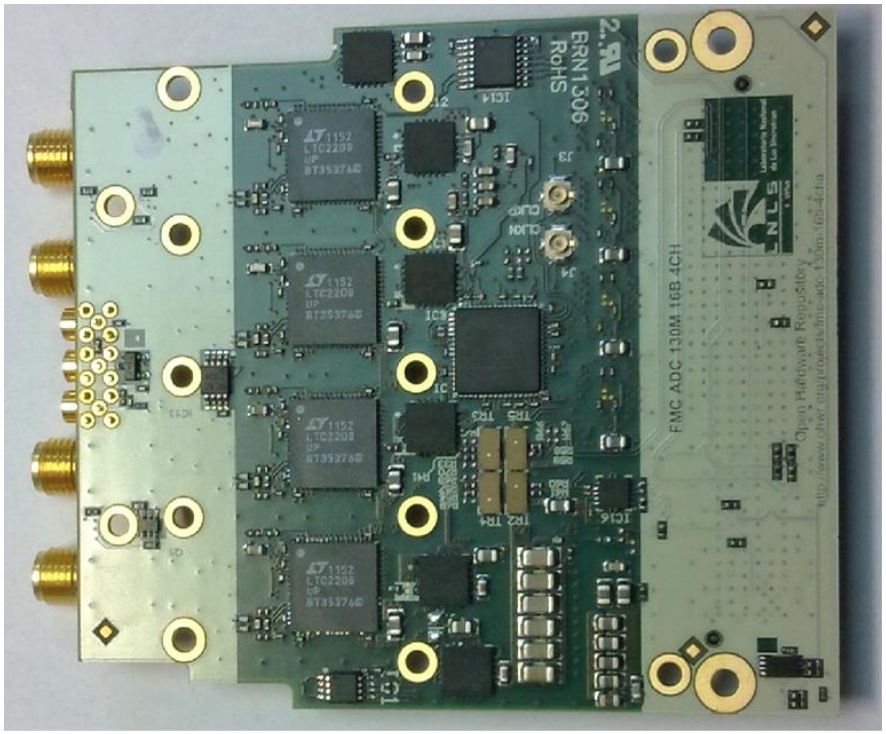

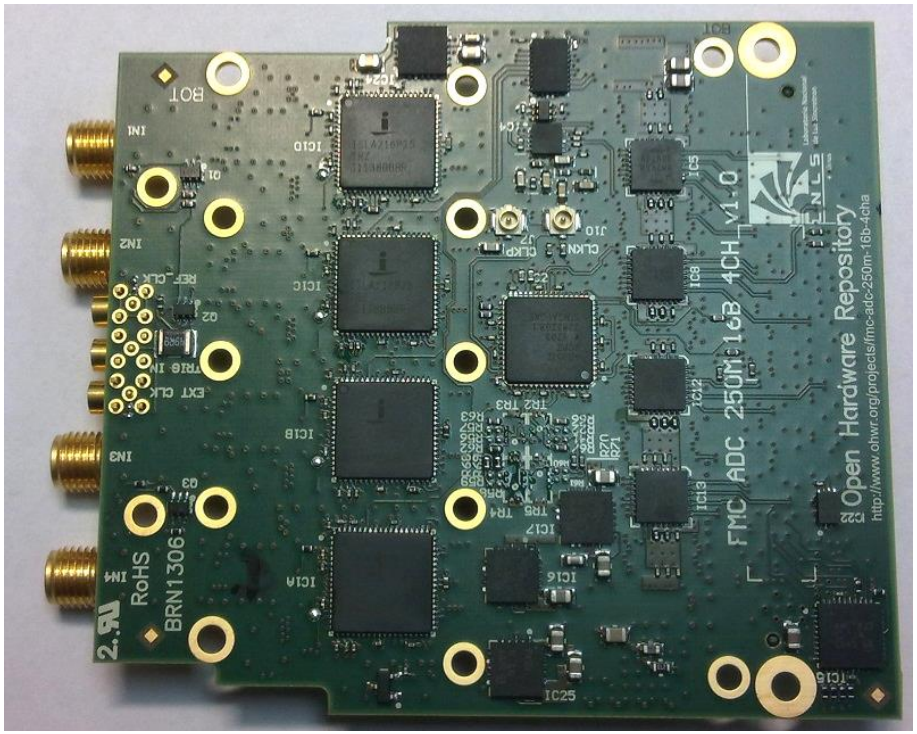

BPM and orbit feedback hardware

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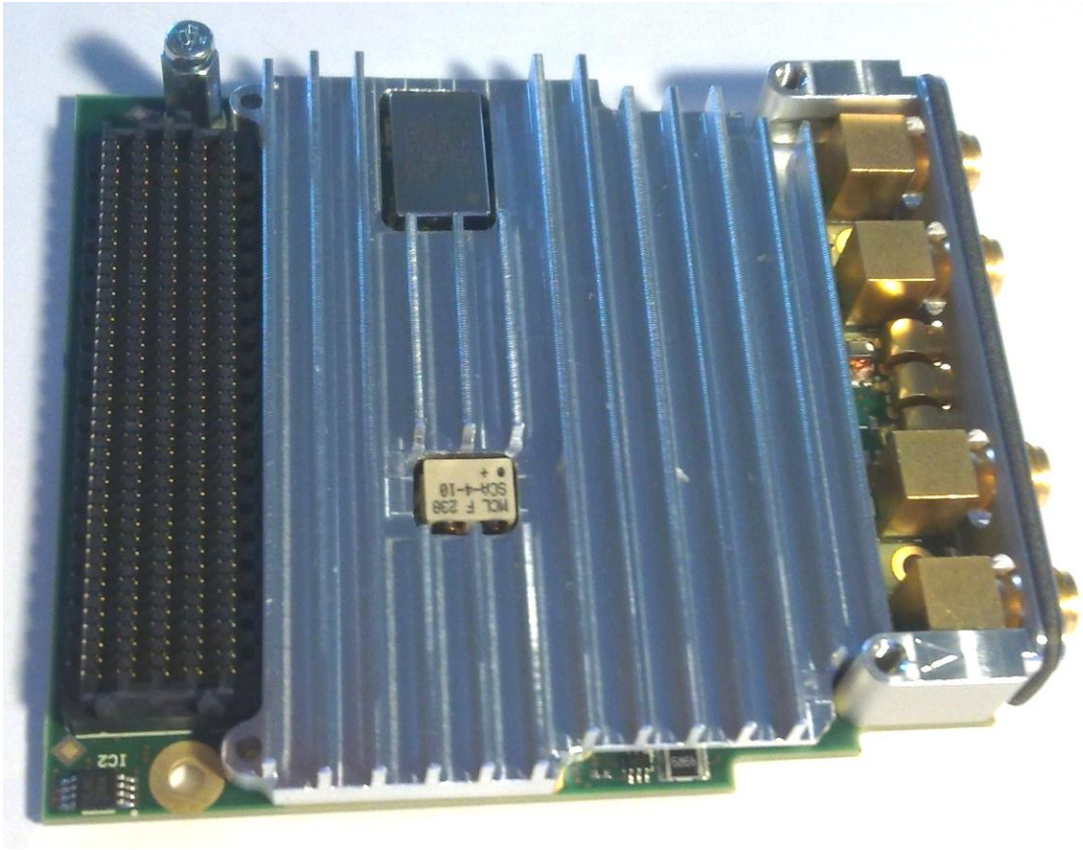
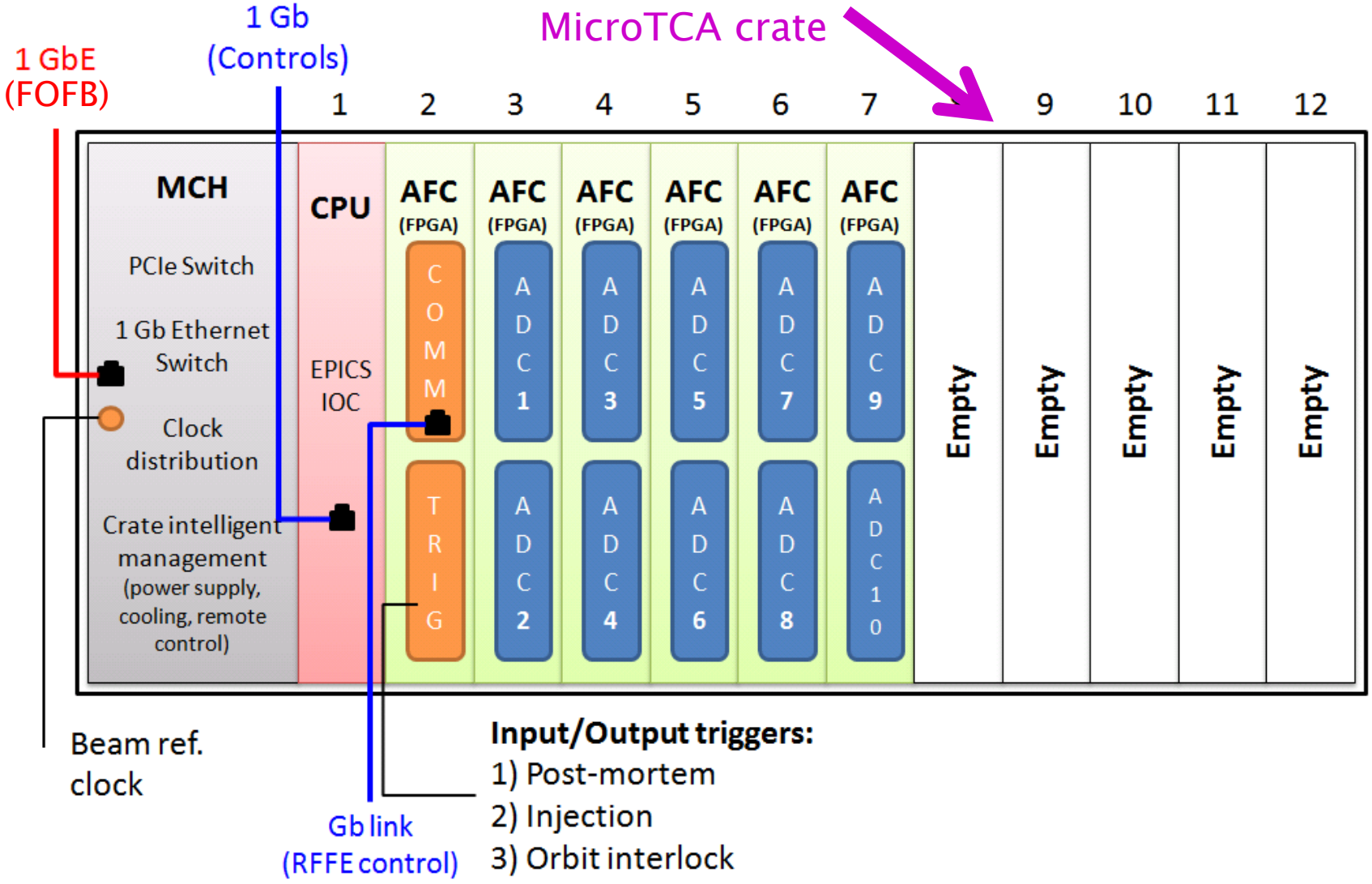


Common shielding/heatsink, front pannel and connectors

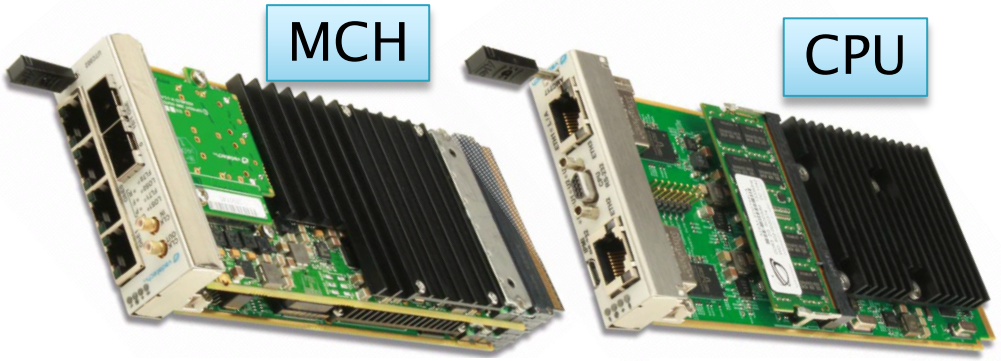
MicroTCA crate for BPM



BPM and orbit feedback hardware

- COTS parts (Vadatech™):
  - MicroTCA.4 crate (VT811)
    - Redundant supply + cooling
    - Full JTAG solution
    - Passive backplane
  - MCH (UTC002)
    - MCMC and Shelf Manager
    - PCIe x4 switch
    - GbE L2 switch
    - Clock distribution
  - CPU AMC (AMC717)
    - 1.2 GHz dual core P2020 PowerPC CPU
    - 4 GB DDR3 SDRAM
    - PCIe x4

MicroTCA for physics crate



Why NOT Rear Transition Modules?

1. Isolate analog front-end from digital electronics
   - EMC (avoid mixing analog and digital)
   - Temperature drifts
   - Analog cables with SMA connectors are reliable
2. ADC and FPGA boards would need to be redesigned and/or change form factor
3. Increase price per slot

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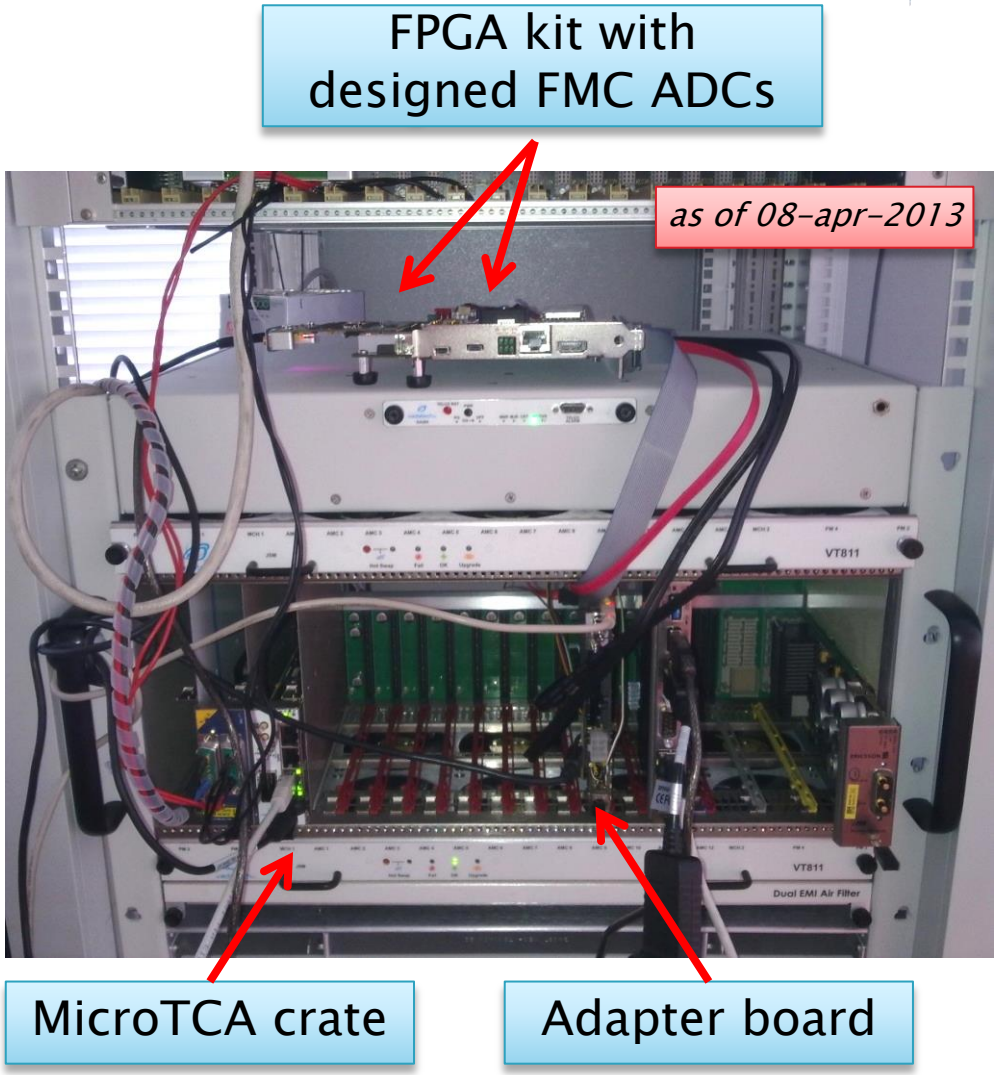
Project status and schedule

- **Jan-Feb'13**: RFFEv1 tests
- **Mar-Apr'13**: FMC ADCs and AFC debugging at WUT/Creotech
- **May'13**: MicroTCA crate with AFCs and FMCs at LNLS
- **May-Jun'13**: benchmark of designed FMC ADCs with COTS board (FMC-516 by Curtiss-Wright™)
- **Dec'13**: Basic HDL ready
- **Dec'13**: EPICS IOC ready
- **2nd sem 2013**: RFFEv2 design (minor modifications)
- **2nd sem 2014**: Production
- **1st sem 2015** : Reliability tests

Project status and schedule

Tests at Creotech/WUT

- MicroTCA crate:
  - Vadatech AC power supplies and CPU were not shipped yet
  - Minor problem when booting – CPU needs to be detached and attached to get power (likely to be cross-vendor incompatibility)
  - Besides that, crate works stable
- FMC ADC boards
  - FPGA firmware development ongoing



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Open-hardware collaborative work

- General requirement for designs: CERN Open Hardware Licence (OHL)
- Open discussions on project's mailing list led to improvements on hardware specifications and design
- Joint hardware/firmware/software design LNLS/WUT/ Creotech
  - Public repositories
  - Professional exchanges
- GSI Cryring will use AMC FMC carrier and FMC ADC 250 MS/s board for BPM system. GSI CBM experiment evaluates this possibility as well.

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Summary

- Sirius BPM and orbit feedback have very stringent requirements
- Use of MicroTCA.4 for clock/trigger distributiom but not for RTM
- AFC (AMC carrier board) is under final review for production
- FMC ADC boards are produced, tests are ongoing
- MicroTCA.4 crate has minor incompatibility issues that should be solved when final parts arrive
- Open Hardware has been key factor for the entire devolepment since the specification phase

Sirius BPM electronics team

- **Sérgio Rodrigo Marques** – Beam Diagnostics Group Head
- **Fernando Henrique Cardoso** – ADC/timing
- **Daniel de Oliveira Tavares** – DBE/orbit feedback
- **Rafael Antonio Baron** – RFFE design
- **Lucas Maziero Russo** – DBE firmware/software

- Students:
  - **José Alvim Berkenbrock** – DBE FPGA firmware
  - **João Leandro de Brito Neto** – RFFE temp. control + tests
  - **Igor Henrique Soares Nunes** – software, EPICS

Sirius BPM on the web

- Public documents and file repositories at CERN Open Hardware Repository (OHWR):
  - BPM project (general):
    - http://www.ohwr.org/projects/bpm
  - BPM RF Front-End:
    - http://www.ohwr.org/projects/bpm-rffe
  - BPM Firmware and Software:
    - http://www.ohwr.org/projects/bpm-sw
  - FMC ADC modules:
    - http://www.ohwr.org/projects/fmc-adc-130m-16b-4cha
    - http://www.ohwr.org/projects/fmc-adc-250m-16b-4cha
  - AMC FMC carrier (digital back-end):
    - http://www.ohwr.org/projects/bpm-dbe

Acknowledgments

- Special thanks to those who helped on discussing the digital hardware topology for Sirius BPM:
  - Creotech/WUT: Grzegorz Kasprowicz
  - PSI: Boris Keil, Goran Marinkovic, Waldemar Koprek
  - CERN: Javier Serrano, Erik van der Bij
  - LNLS technical groups