Prototyping xTCA for BPM controls

Bartosz Bielawski

bartosz.bielawski@cern.ch

April 9, 2013

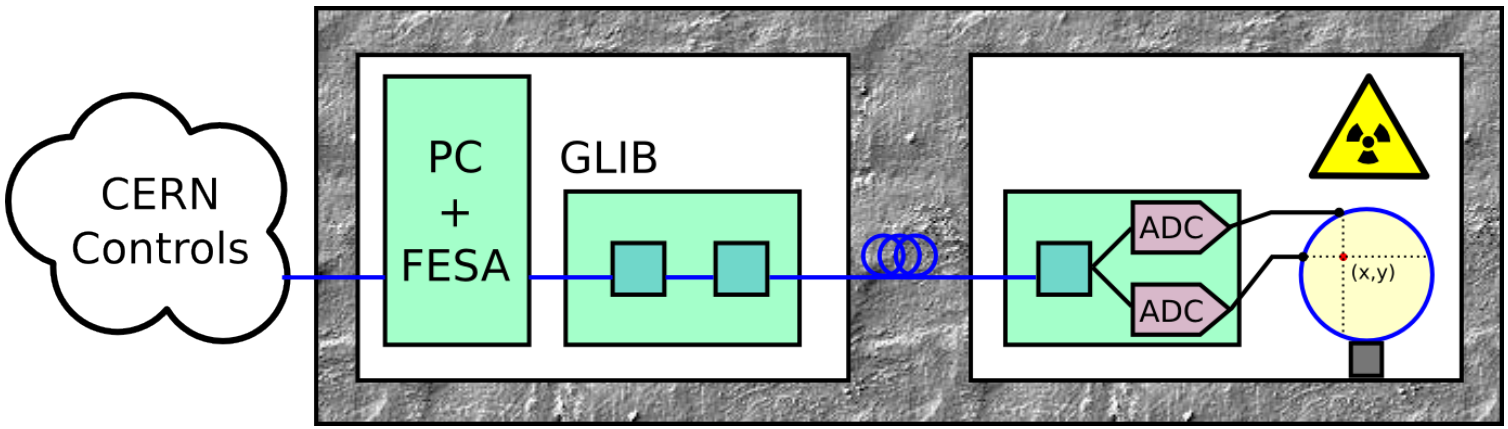
Table of contents

BPM TDAQ System

CLIC BPM

A new stripline BPM for CLIC Test Facility is being designed in collaboration with LAPP.

To integrate BPMs into CERN's infrastructure the GLIB will be used as a master and will provide commands and clock and will retrieve sampled data.



The team

The following people are involved in the project:

- CERN (BE-CO-FE):

  Stefano Magnoni GLIB-based BPM master side (VHDL),
  Bartosz Bielawski GLIB-based BPM master side (VHDL, slides),
  Sylvestre Catin μTCA system expert,
  Frank Locci project leader.

Original design:

- LAPP:

  Jean-Marc Nappa BPM front-end electonics design (HW & FW),
  Sebastien Vilalte BPM front-end electonics design (HW & FW),

Why we chose to try μTCA?

Definition

FEC — Front End Computer

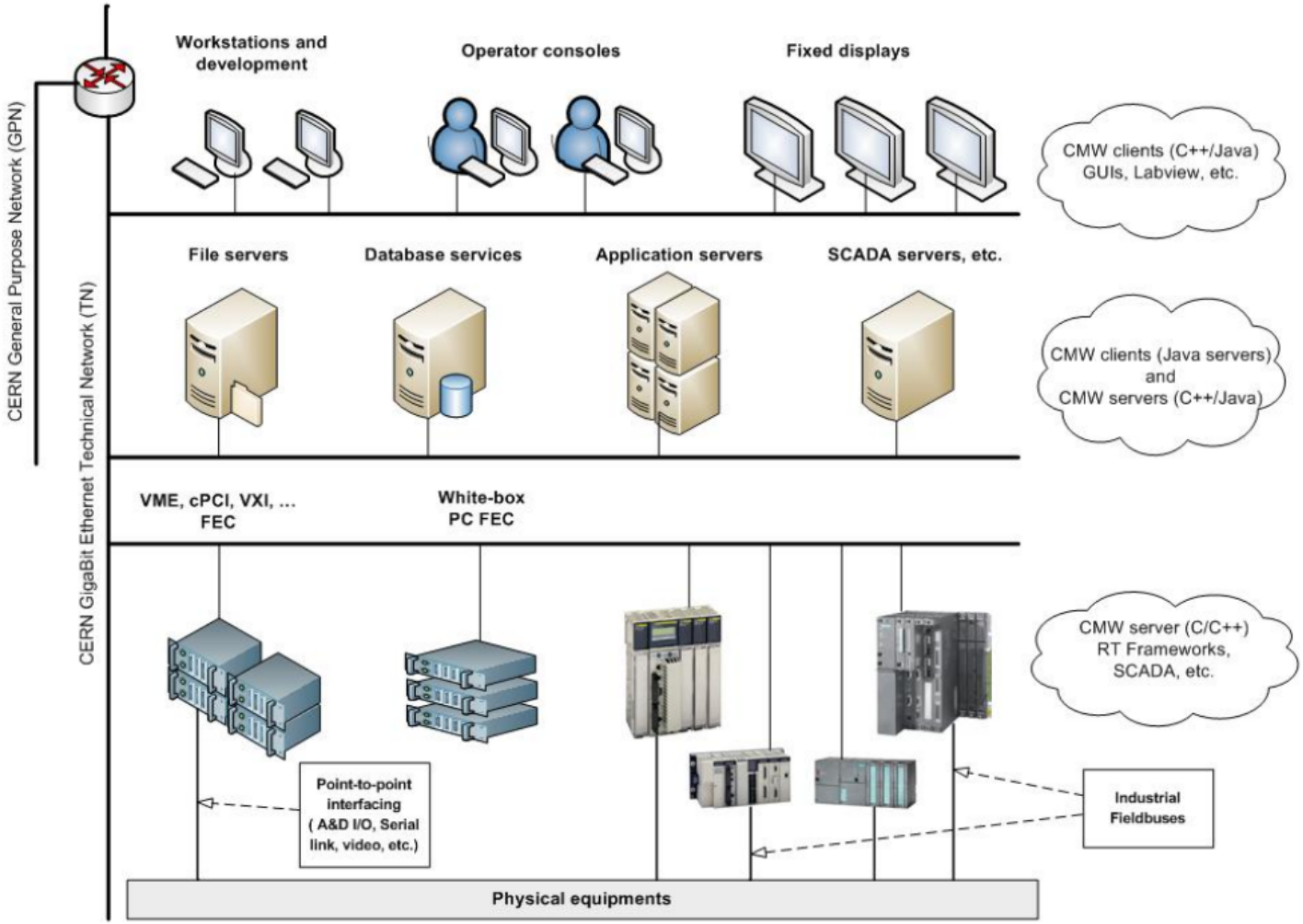
- evaluation of μTCA as a future platform for FECs is one of BE-CO projects,
- prototype BPMs need to be integrated into BE-CO infrastructure and we already have GLIB board,
- due to requirements (speed, radiation) BPMs is a good candidate as BE-CO pilot system for μTCA evaluation,
- μTCA is already evaluated at CERN,

Current state of FEC

- Over 1000 FECs for control of all accelerators,
- There are many different systems currently used at CERN:
  - VME64x*, VXI*, VXS,
  - cPCI*, PXI,
  - uTCA, ATCA,
  - Industrial PCs*
- VME standard slowly becomes obsolete,
- Migration from PPC to Intel CPUs,
- CLIC project needs a FEC for the master side (alcove).

*Used as FEC

Current CO infrastructure



RAS requirements

Definition

RAS — Reliability, Availability, Serviceability

- remote management over Ethernet:
  - monitor: voltage/current, temp., power and fan status, bandwidth usage,
  - control: fan speed, CPU reset, power on/off.
- highly modular design (reduced repair time),
- redundant power supply,
- support for RTM (Rear Transition Module),
- clock lines and trigger lines (White Rabbit?),
- service units (power, fanout, LED panels) and sockets (power, ethernet, serial terminal) accessibility.

Additional features

These are not actual requirements but we would like to have:

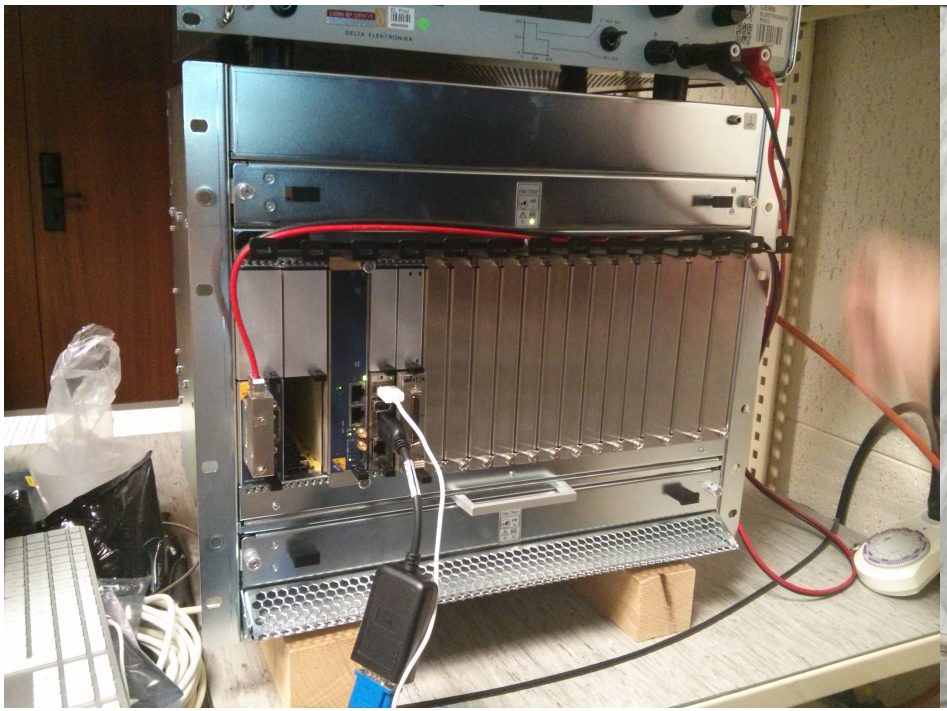
- multiple fast serial links (to hub and/or adjacent slots) supporting Gigabit Ethernet and/or PCI Express and/or other differential buses,
- hot-swap for power supply and cooling units,
- common management interface for different devices,
- supported by multiple companies,
- based on commonly used standards,
- modules available off the shelf:
  - digital and analogue I/Os,
  - fast digitizers/oscilloscopes,
  - waveform generators,
  - serial interfaces (RS232, RS485, CAN, ...),
- standardized connectors/backplane layout,
- cost effective.

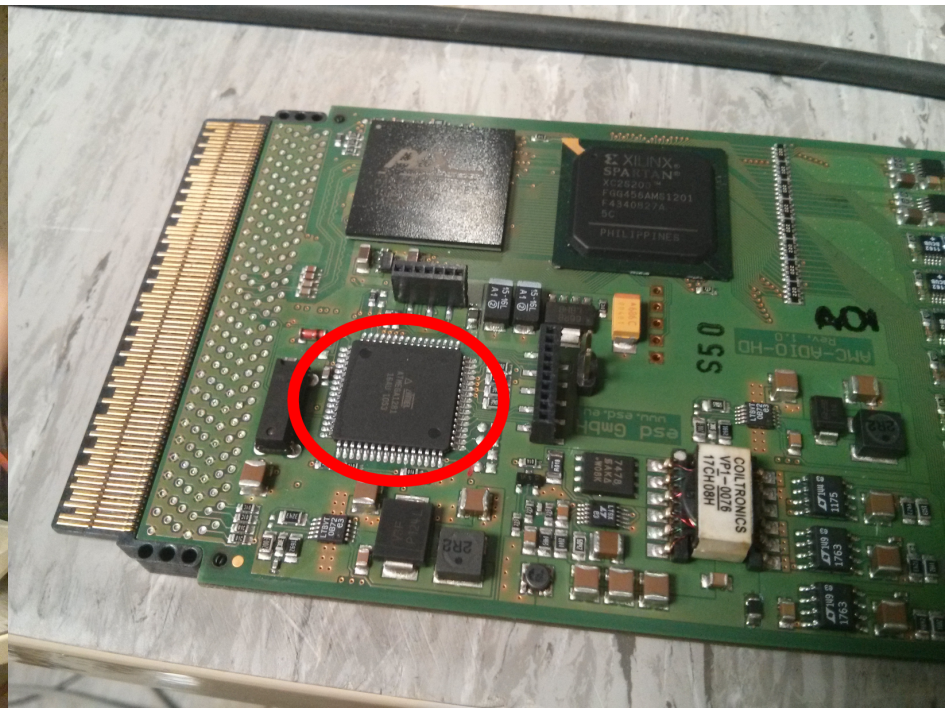
Test system

For evaluation purposes we have bought:

- Schroff 19" Rack:
  - 2x MCH slot, 4x PM slot,
  - 12x ACM slots double height, mid size,
  - double star backplane conforming to μTCA.4.
- 1x NAT MCH with Clock Module,
- 2x NAT μTCA AC Power Module (600W),
- 1x CT CPU module with Intel Core-i7, 4 GB RAM,
- 1x ESD ADC/DAC ACM (24x DIO, 8x ADC (16b@200kHz), 2x DAC (16b@200kHz), 4x RS485,
- GLIB (from PH-ESE).

Test system — photos





The first impressions

Our first impressions are not very positive...

- We placed the order* 2/11/2012, ETA: 2/03/2013 (4m),
- ... the crate arrived after 5 months (27/03/2013),
- ... with wrong power supplies †,
- Some of the boards we got seem to were fixed by hand,
- Extracting boards can be tricky, the handles are small and the boards fit tight.

*NAT (Provider: INA Swiss)
†48 VDC in place of 230 VAC

GLIB

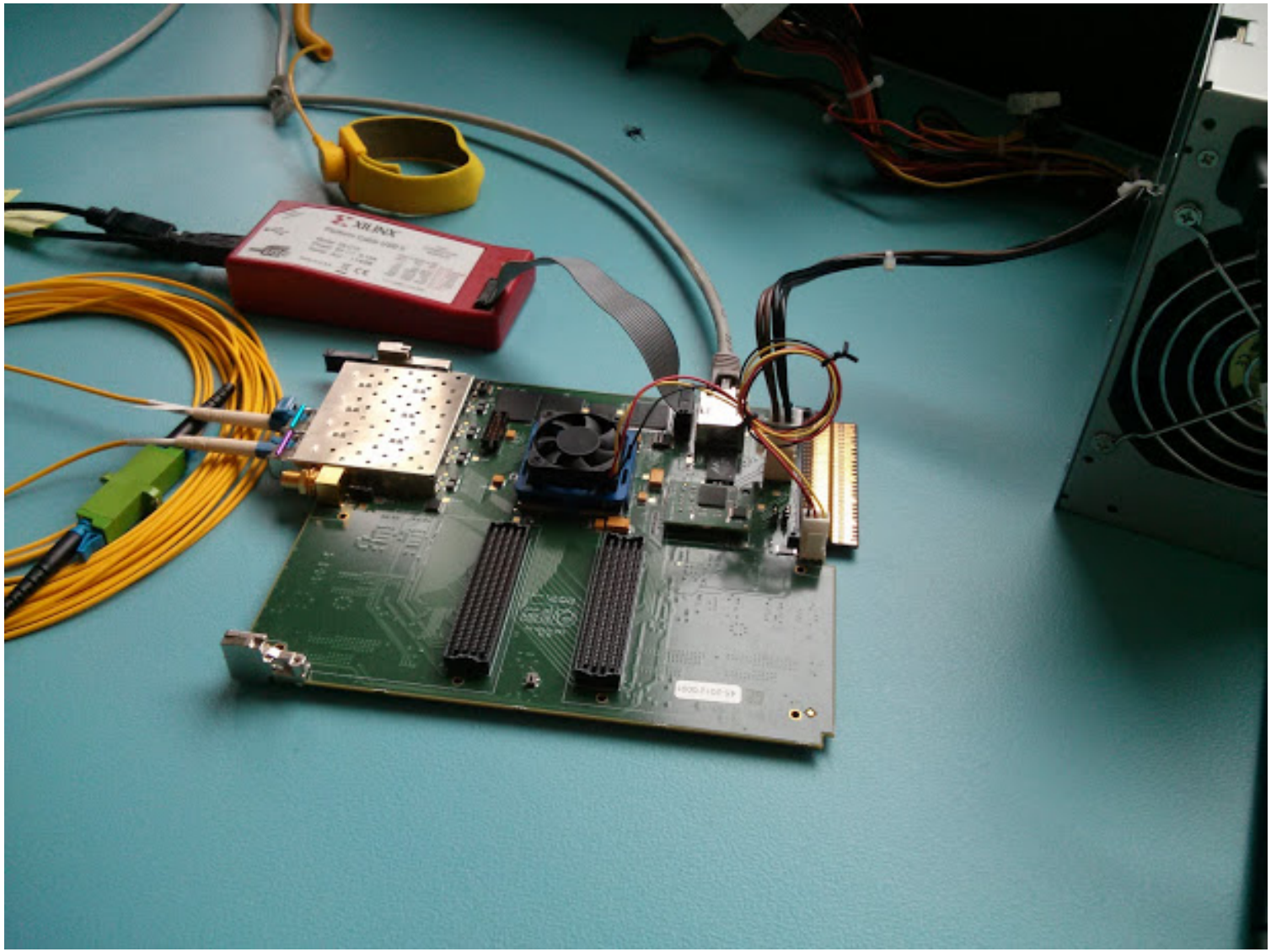
On the other hand GLIB seems to be a nice piece of hardware!

- 4 cages for SFP+ on-board,
- 2 FMC sockets,
- flexible clock distribution system,
- can work in stand-alone mode (without crate)

The software/firmware:

- system part provided already written,
- internally uses IPBus and Wishbone,
- Ethernet connectivity out of the box,
- Python scripts can be used to test/manage the board.

GLIB: Test setup



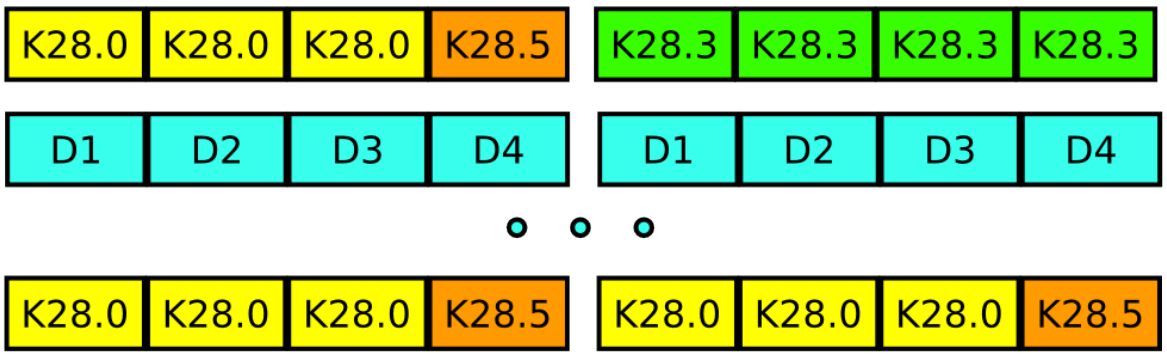
Prototype BPM Read-out system [1]

The system consists of two boards:

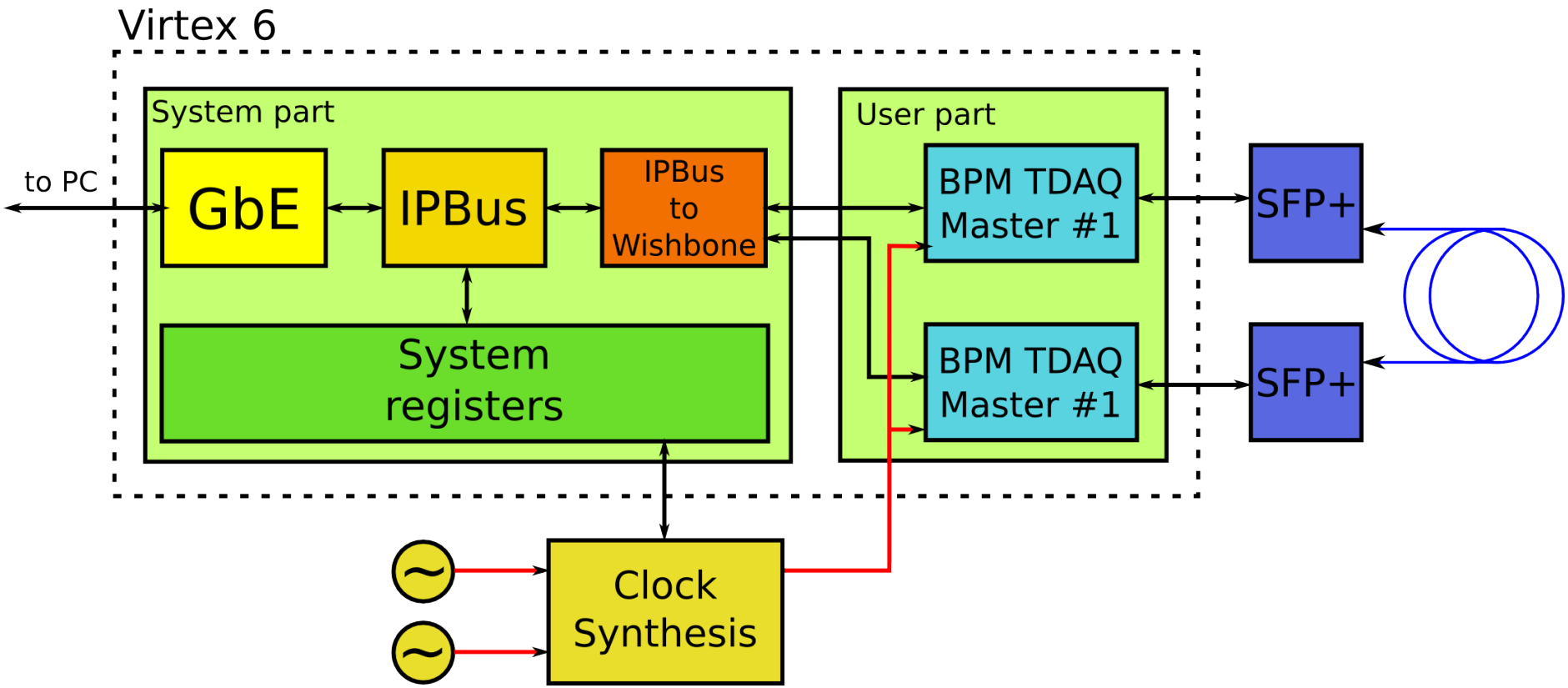
- the slave board (analogue frontend),
- the master board (GLIB in μTCA)

Protocol:

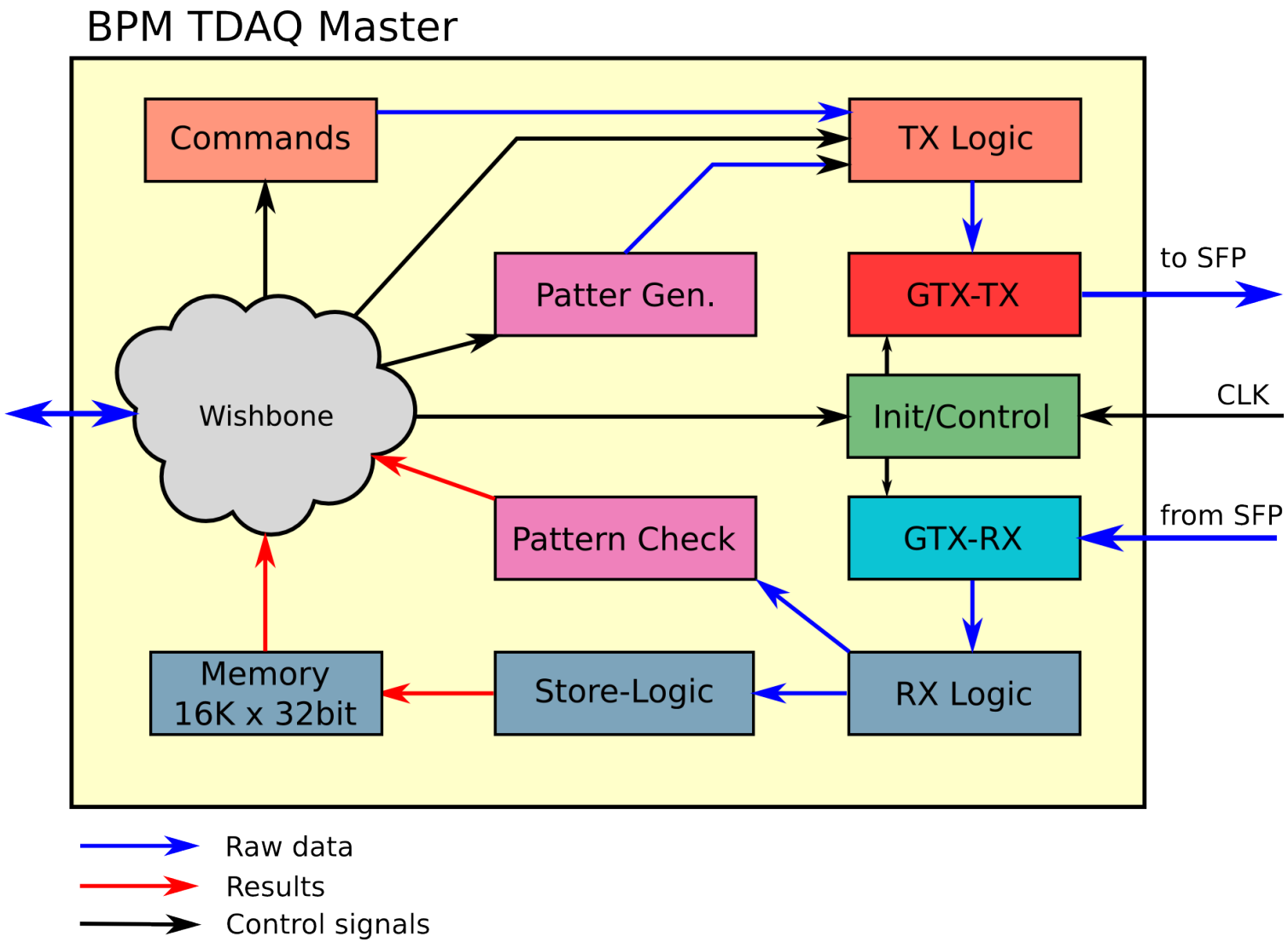
- Line rate: 3.84 GHz,
- 8b/10b encoding, 32b words, K28.5 comma, SOF K28.3,
- Record size: 64b x 8192.



Prototype BPM Read-out system [2]



Prototype BPM Read-out system [3]



Progress and Plans for the future

We have already:

- set up the GLIB and environment for the stand-alone mode,
- wrote BPM TDAQ core, simulated and integrated with GLIB project,

Work in progress:

- test the design with real BPM readout card,
- make it work with GLIB used in the μTCA crate and with SLC6,
- write a FESA class to support the BPM,

Possible future improvements:

- add PCIe support,
- add more (than 4) slaves using FMC with SFPs.

Summary

- The μTCA devices are not so OTS as they are advertised,
  - that is why we did not yet test our crate,
  - but CO is working on making SLC6 run on it.
- GLIB is a nice project:
  - stand-alone mode is great!,
  - IPBus with PyChips makes work much easier,
  - we used wbgen2[‡] to generate interfaces for our core,
  - the White Rabbit[§] capabilities could be added,
  - the quality of supplied scripts could be improved,
  - and some more comments in the VHDL code could be handy...
- We will start playing with our crate as soon as the PSUs arrive,
- Those tiny ATmega16 IPMI modules are used even in commercial equipment.

[‡] http://www.ohwr.org/projects/wishbone-gen
[§] http://www.ohwr.org/projects/white-rabbit

Questions and Answers

That's all we prepared for today.

Do you have any questions?