Status of the Beam Phase and Intensity Monitor for LHCb

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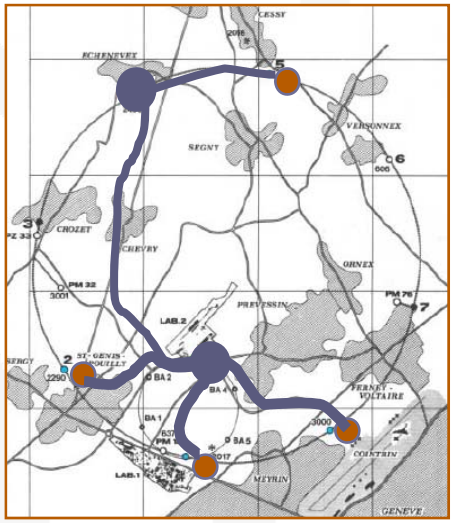
Why BPIM?

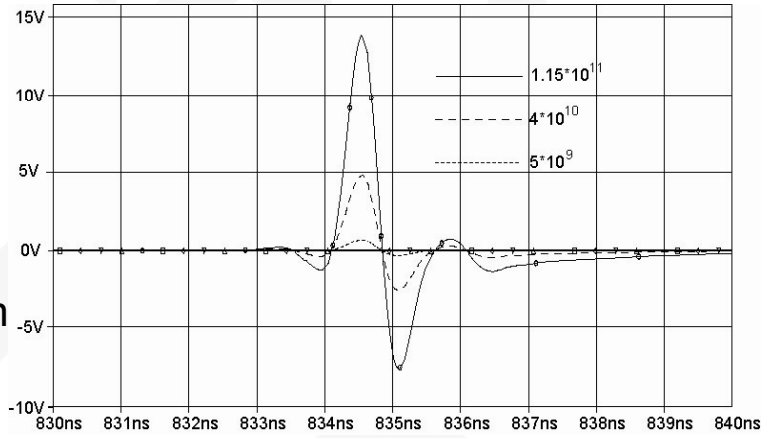


General clock issues:

- Clock locked with the beam transmitted over 14 km of optical fibres at a depth of ~1 m
- Estimated diurnal (200 ps) and seasonal drift (7 ns) due to temperature variations (AB/RF ref.)

Aid in the coarse and fine time alignment of the experiment

- Monitor individual bunch position (ghost bunches)
- Measure bunch intensity bunch-by-bunch for trigger conditions
- Measure bunch phase bunch-by-bunch for long-term stability in clock distribution

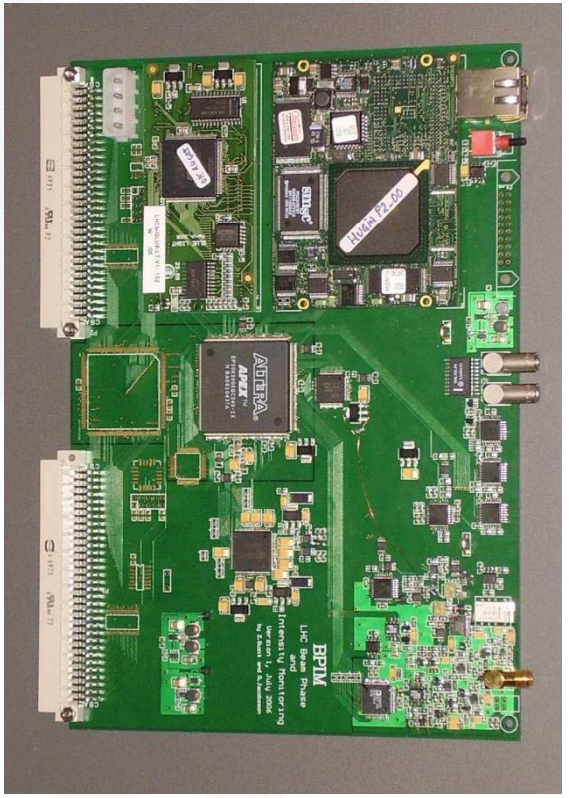


Able to

- See single bunch crossing: signal coming from BPTXs for LHCb, very fast and high bipolar pulse.
- Check trigger/detector timing alignment real-time and tag events with bunch information through the TFC system (Interfaced with ODIN)

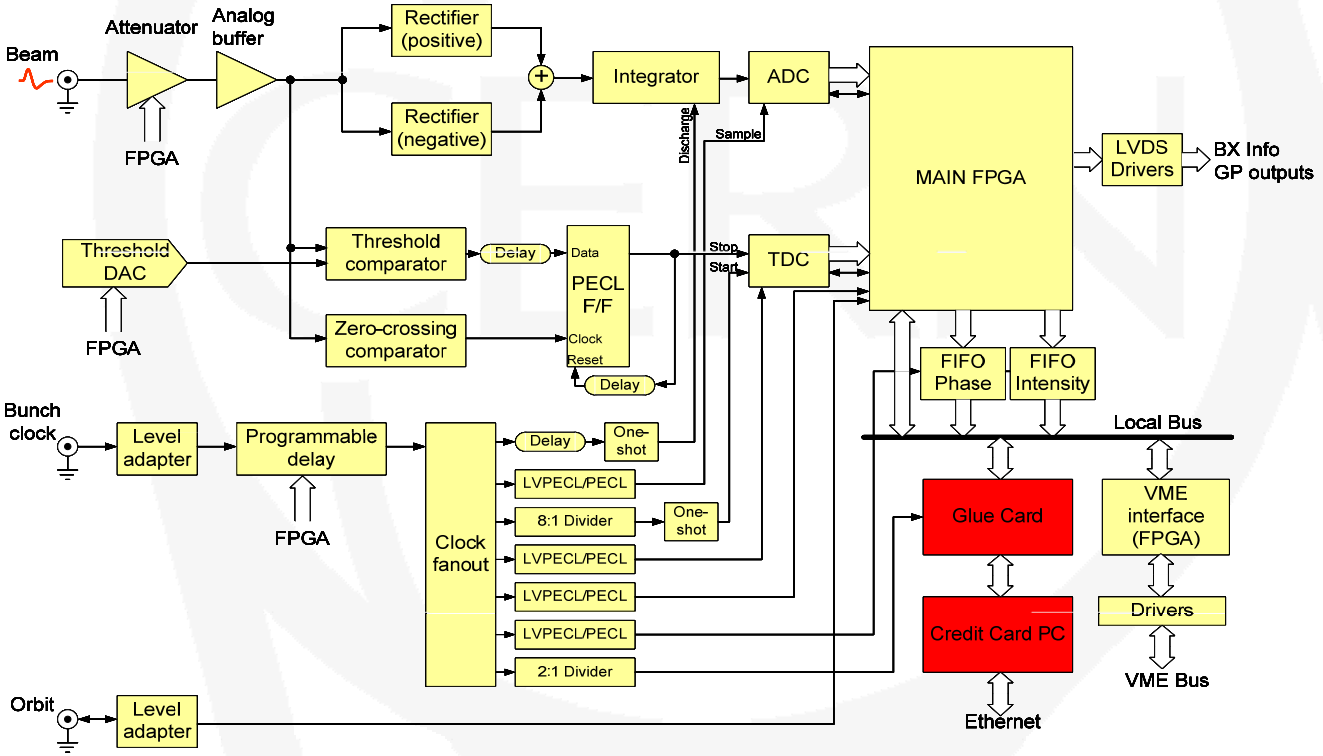
What do we aim to?

- Developing custom made acquisition board:
  - 6U VME, one per beam
  - Online analysis of a bipolar pulse: FWHM 1 ns at 40 MHz, ±5Vmax processing amplitude (onboard attenuator for higher pulses)
  - Measure time between bunch arrivals and LHC bunch clock locally
    - Bunch-by-bunch for a full LHC turn filled in FIFO
    - Triggered via controls interface
    - <100 ps precision and averaging phase as a function of bunch crossing
  - Measure continuously bunch intensities bunch-by-bunch
    - 12-bit resolution by integrating pulse per bunch
    - Output intensity on front-panel at 40 MHz (8/4-bit resolution)
    - Triggered via controls interface, fill in FIFO with intensities for full turn
    - Intensity per bunch as a function of bunch crossing
  - Readout and control via Experiment Control System, CCPC based interface and VME alternatively
  - Interfaced directly to LHCb Timing and Fast Control system
  - Data processing on FPGA



Picture of the 1st prototype

Overview of the board



6 logical blocks:
- Intensity measurement chain
- Phase measurement chain
- Clock distribution
- Digital processing and data accumulation
- I/O interfaces
- Board control via ECS

a lot of debugging

Every block has been tested and adjusted, and all blocks are working!

Debugging

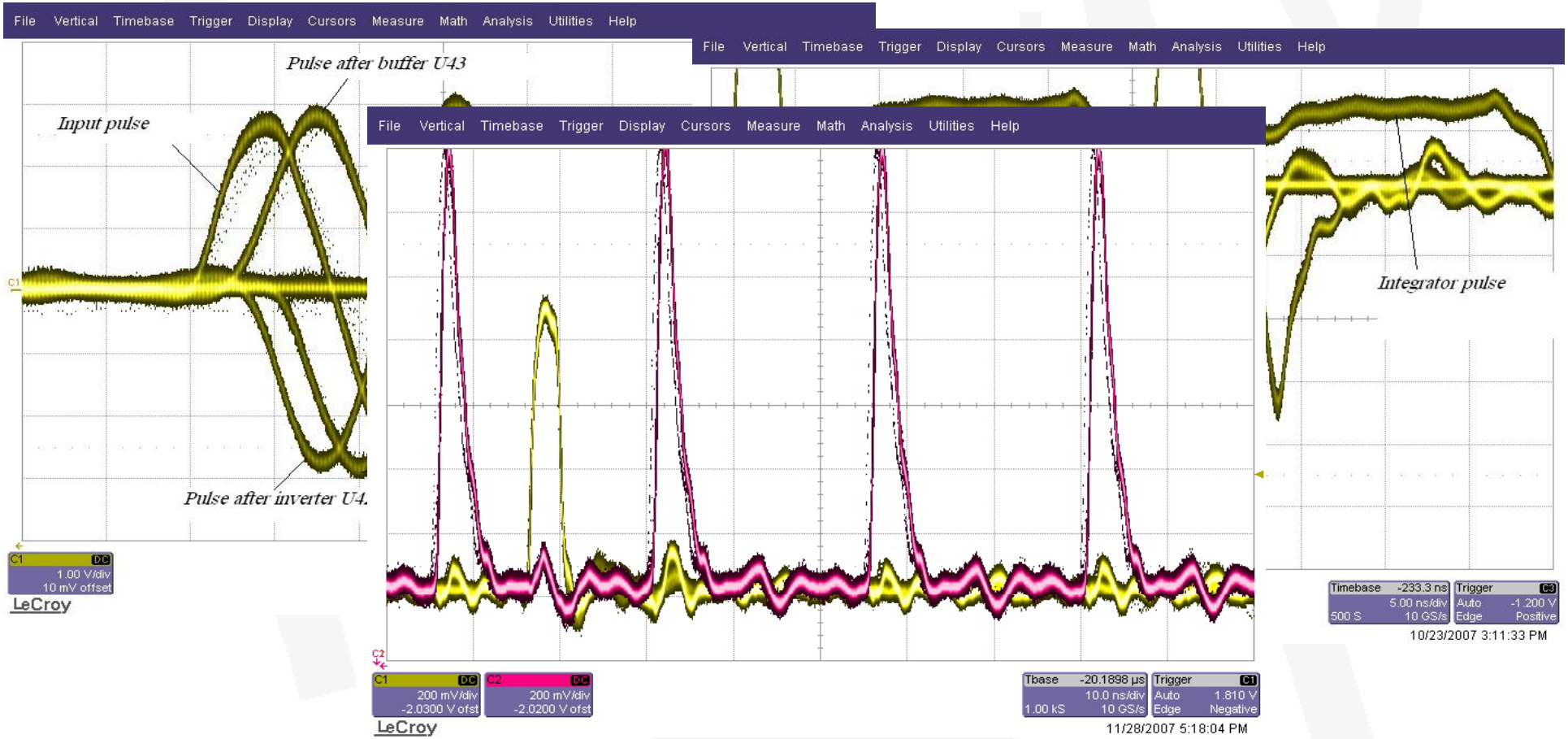
The first prototype has been mounted and debugged in stages: a lot of modifications (thanks to the Mounting Workshop!) and understanding of the problems.

- The analog chain is designed with current-feedback amplifiers: impressive slew rate and high gain-bandwith.
- The stabilization of the rectifier chains has been a difficult task: the current feedback amplifiers are very unstable, but the best configuration has been found
- New designs of the integrator have been implemented: improve stability, undershoot and baseline
- Programmable attenuator fixed and constant-level-crossing method with programmable level (DAC)
- Fixed Start and Stop signals for the TDC, still a problem with one mode of operation to be investigated with the manufactury (ACAM)
- A lot of PECL – LVPECL and LVPECL – TTL translators implemented for improvements
- Firmware written and implemented to control FIFOs for Intensity and Phase measurement
- FIFOs are autonomous: each FIFO has its own RCLK, WCLK, OE, RENB, WENB

The board has very satisfactory performance!

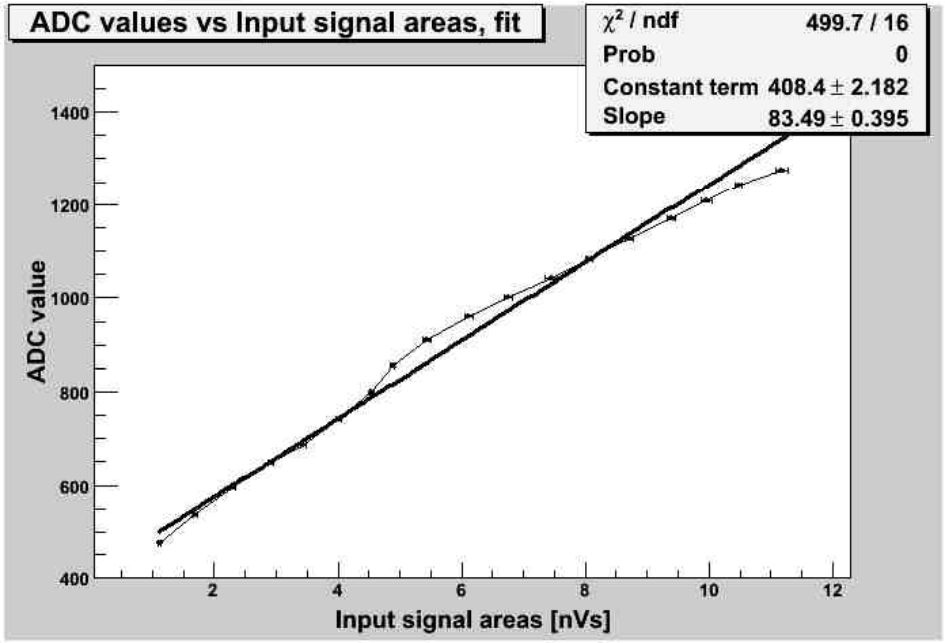
Analog processing

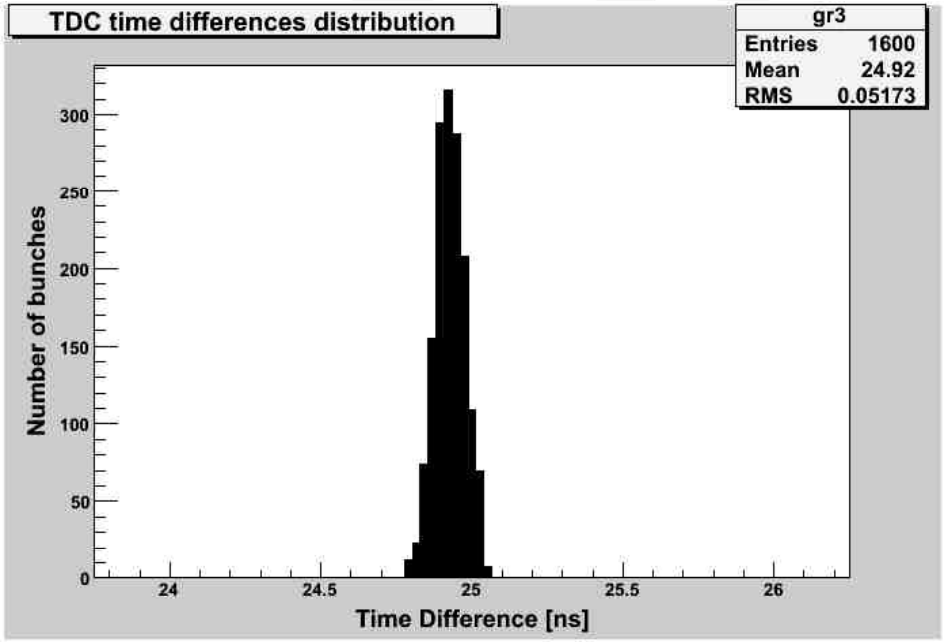
The analog chain for the intensity measurement is working as simulated



Performance in the lab

The board has extensively been tested in laboratory …

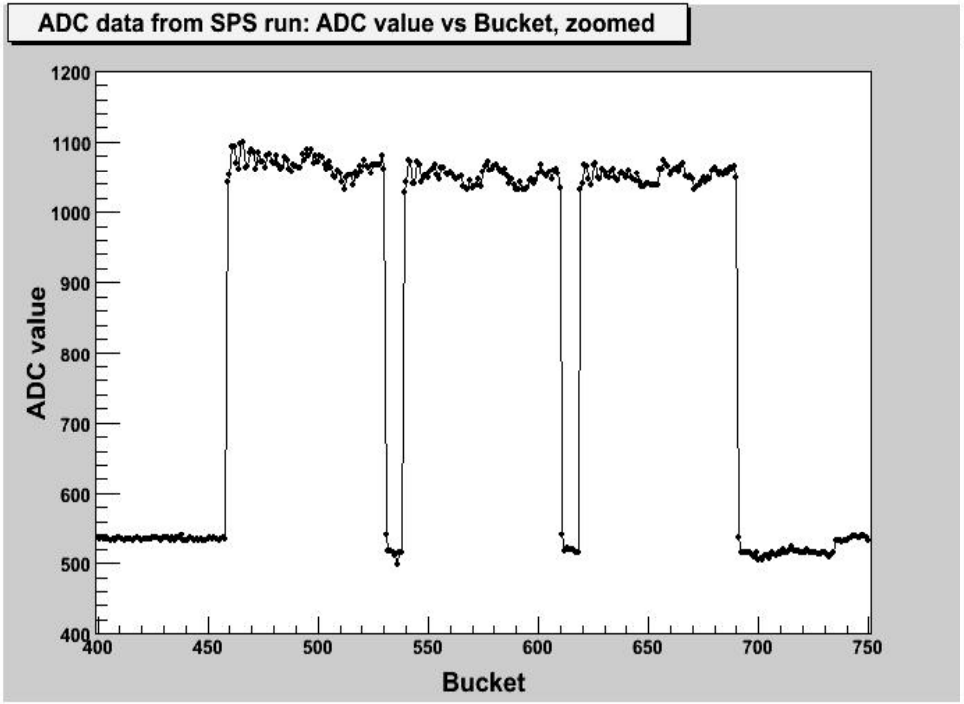


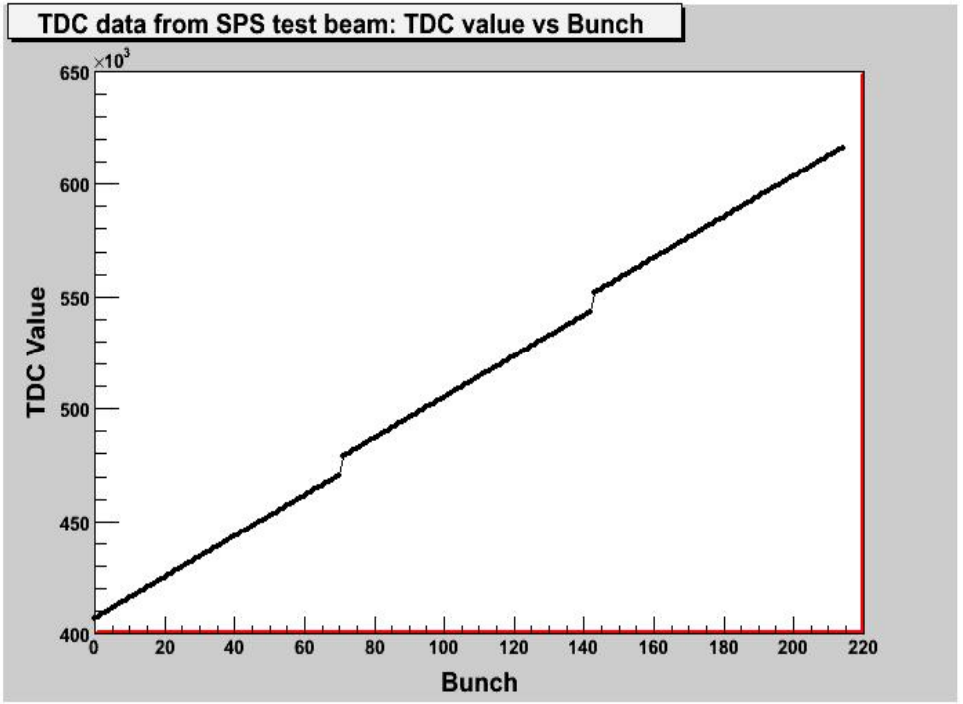


- Linearization to be performed in the FPGA during the data processing
- Understanding of the TDC problem in order to improve the confidence on the distribution

Performance in the SPS

… and in the SPS with a LHC-like structure 72 bunches (in 3 groups) spaced by 25 ns.





- Undershoot of the baseline after the sampling of the bunches to be understood

Conclusions

- A second prototype has been designed with the mentioned changes. The production of 2 boards will be launched in the next weeks.
- We are confident that the second prototype will work as designed.
- The boards will be tested in the lab during January/February.
- Unless major problems come up, the test process should be short and the production will be extended to a few more boards depending on the interest of other experiments.

Thank you for your attention.