

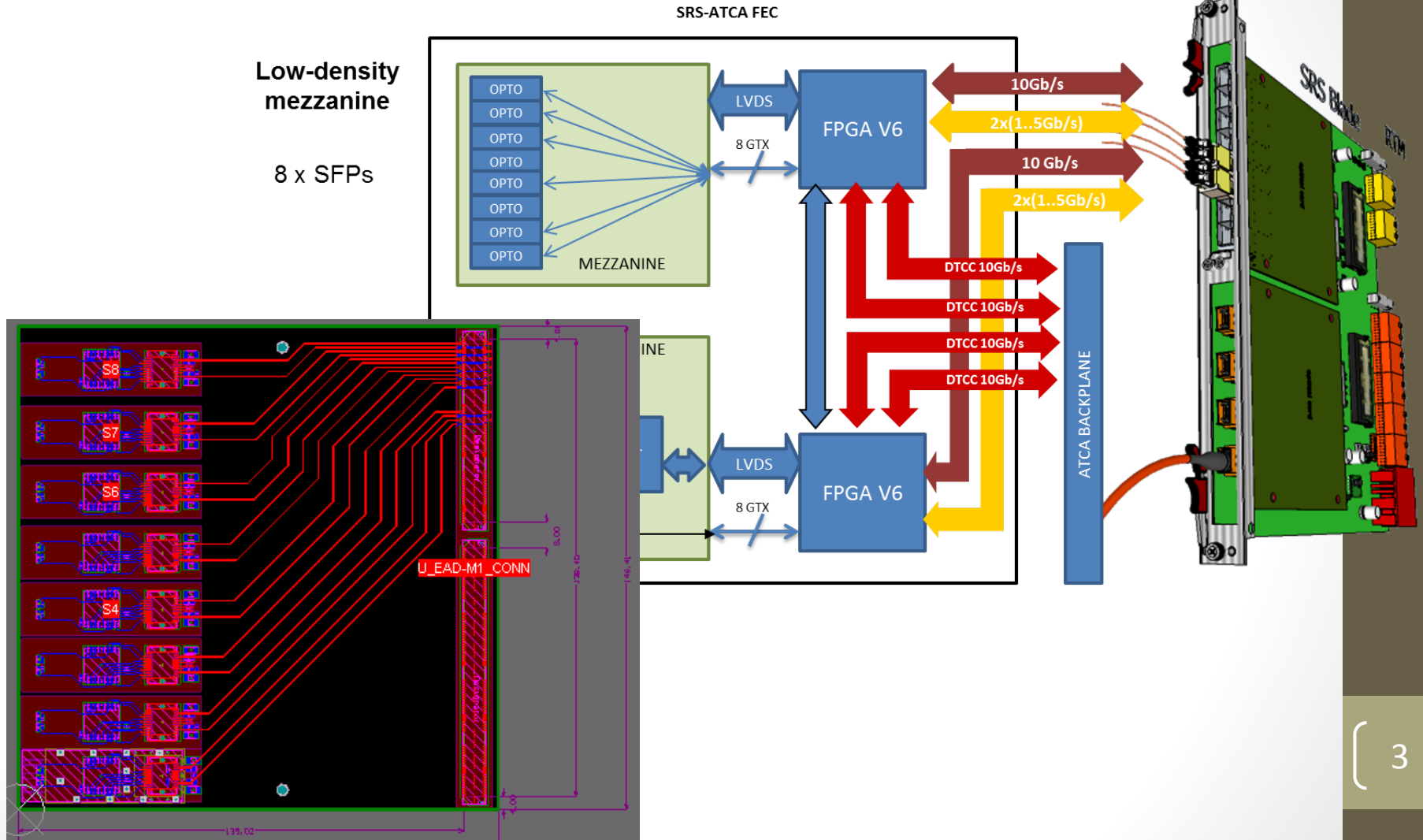
SRS Developments at IFIN-HH

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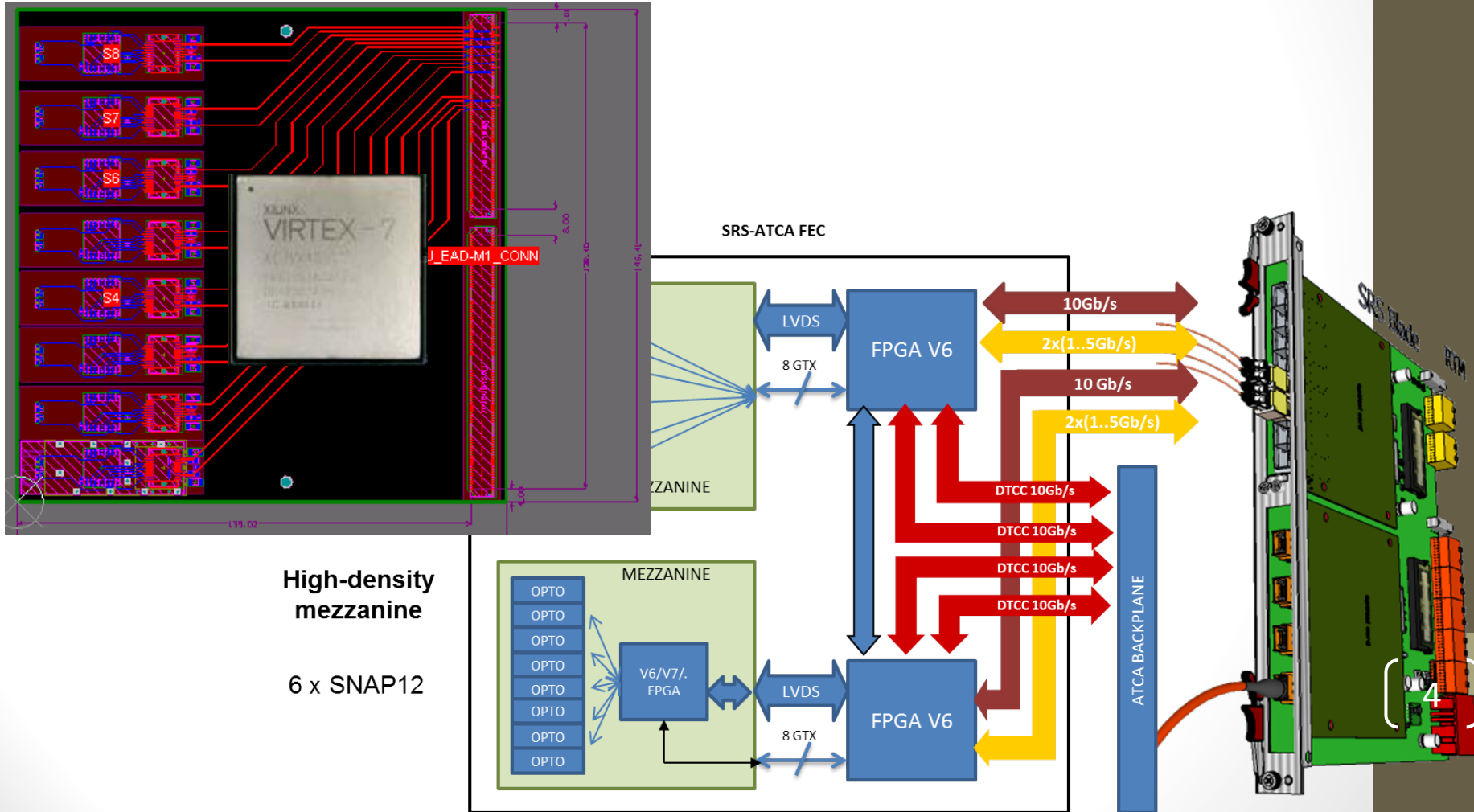
Outline

- On-going activities
 - Digital HDMI C-Card
 - ATCA-SRS
 - optical mezzanine design
 - VFAT2 adapter for existing hybrid
- Future plans
 - VMM2/3 integration into (ATCA-)SRS
 - “All-SRS” Laboratory

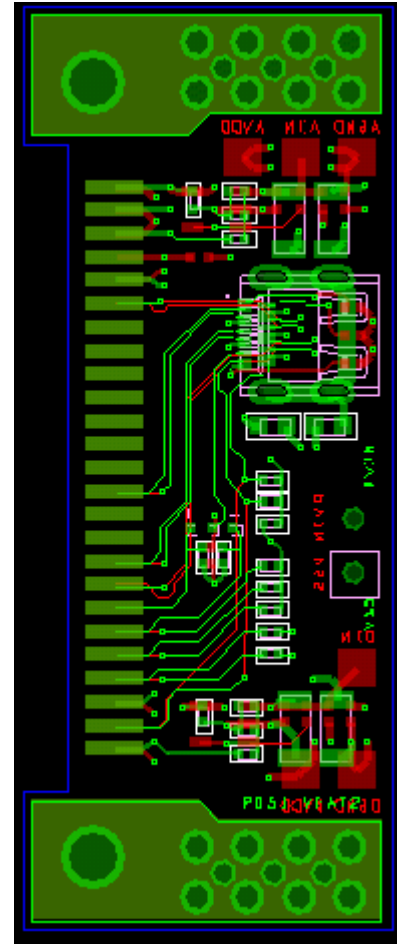
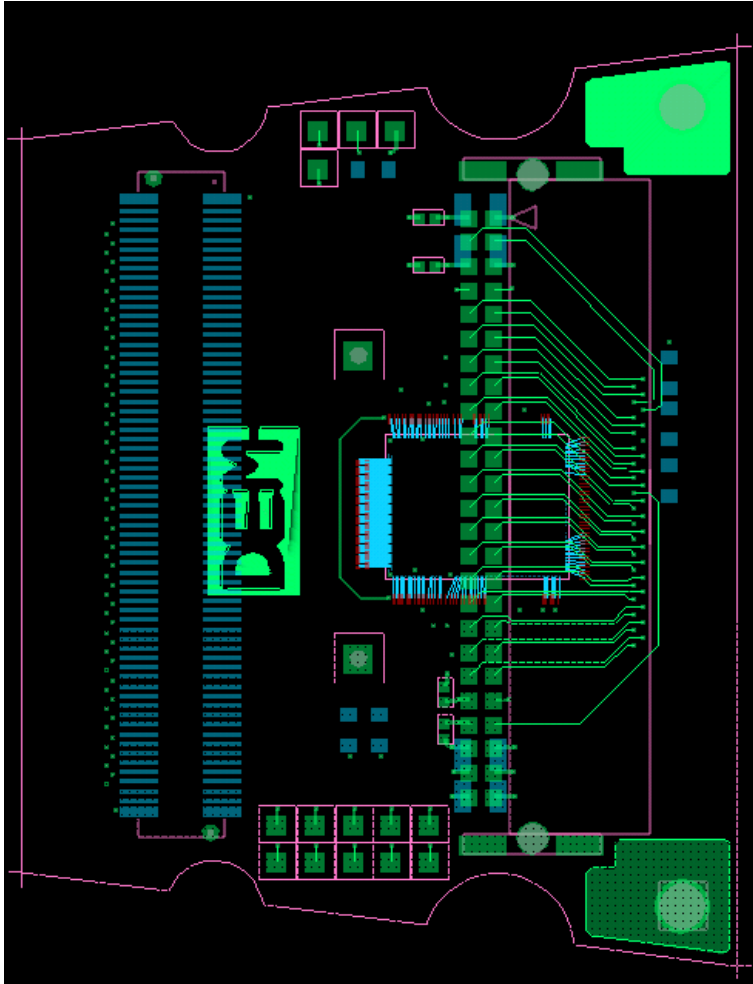
ATCA-SRS Contribution



ATCA-SRS Contribution



VFAT2 RD51 Adapter

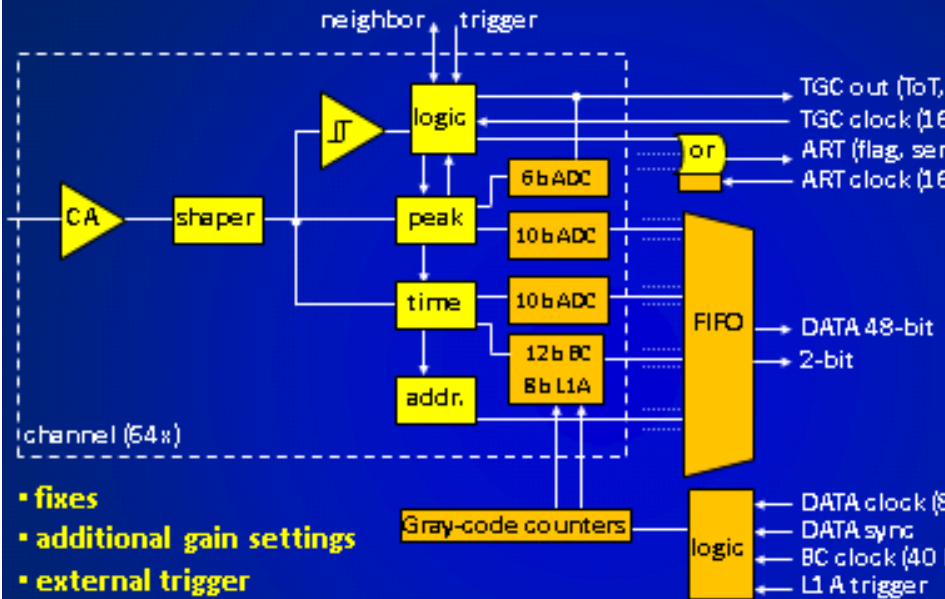


SRS adaptation of an existing VFAT2 hybrid from TOTEM/CMS

- HDMI (D)
- LDOs
- Separate A/D power planes
- Multiple options for the power connections

VMM1/VMM2

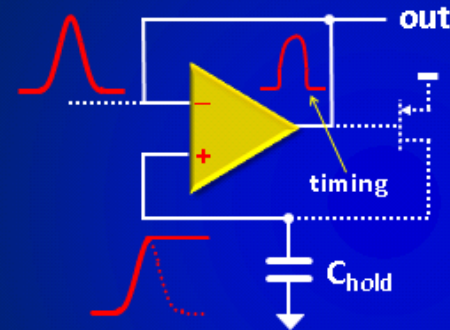
Architecture of VMM2



- fixes
- additional gain settings
- external trigger
- TGC: 64 outputs, PTT, 6-bit ADC 25ns serial with dedicated clock
- ART: flag and address serialized with dedicated clock
- 10-bit ADCs 200ns for amplitude and timing, digital memories
- Gray-code counters for BC-ID (12-bit) and L1A-ID (8-bit)
- 2-bit DATA output with dedicated sync and 80 MHz clock

Note: VMM2 will maintain all the functionalities of VMM1.

Multi-Phase Peak Detector

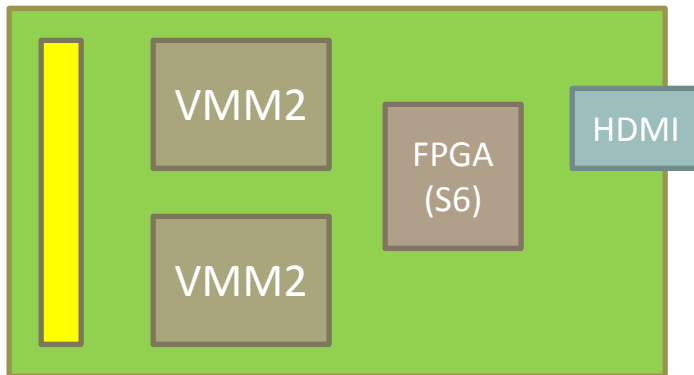
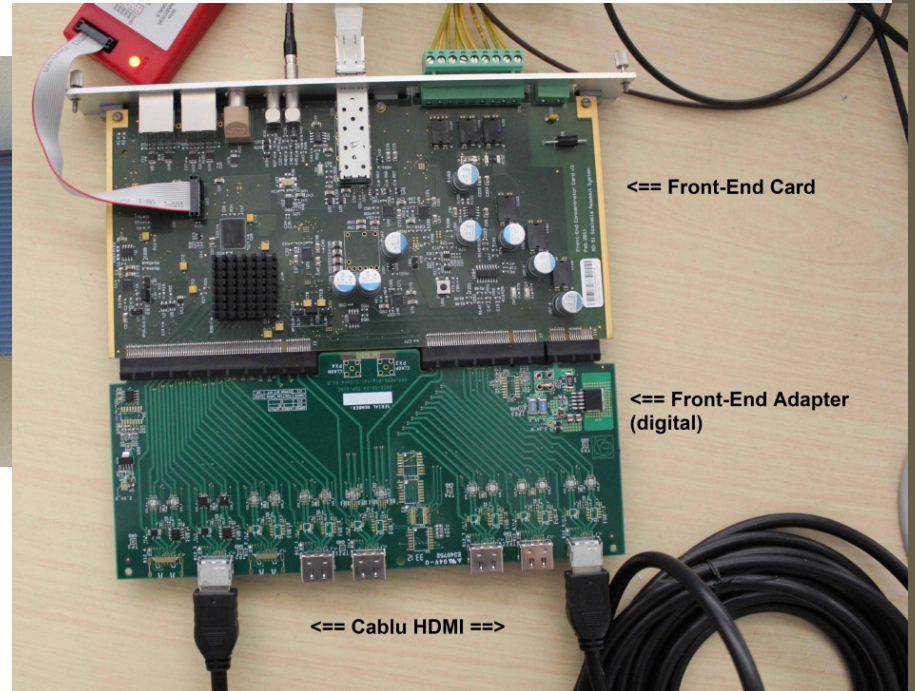
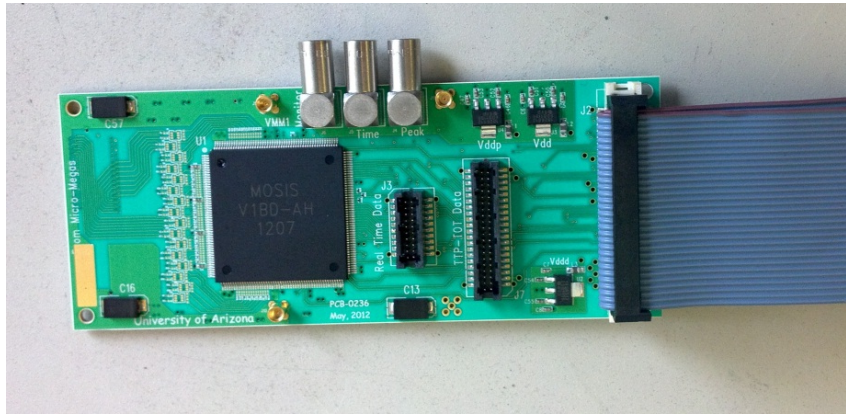


- peak
- timing at peak
- analog memory
- offsets cancel
- high drive

thr	1-bit
addr	6-bit
ampl	10-bit
time	10-bit
BC	12-bit
L1A	8-bit

- Designed for ATLAS NSW
- Data driven (self-trigger)
- Variable gain/shaping
 - dual polarity,
 - adj. gain (0.5-9 mV/fC),
 - adj. peaktime (25-200 ns),
 - DDF shaper
- Peak and time readout
- Trigger-out interface
- Integrated ADC/TDC (10b/1ns)

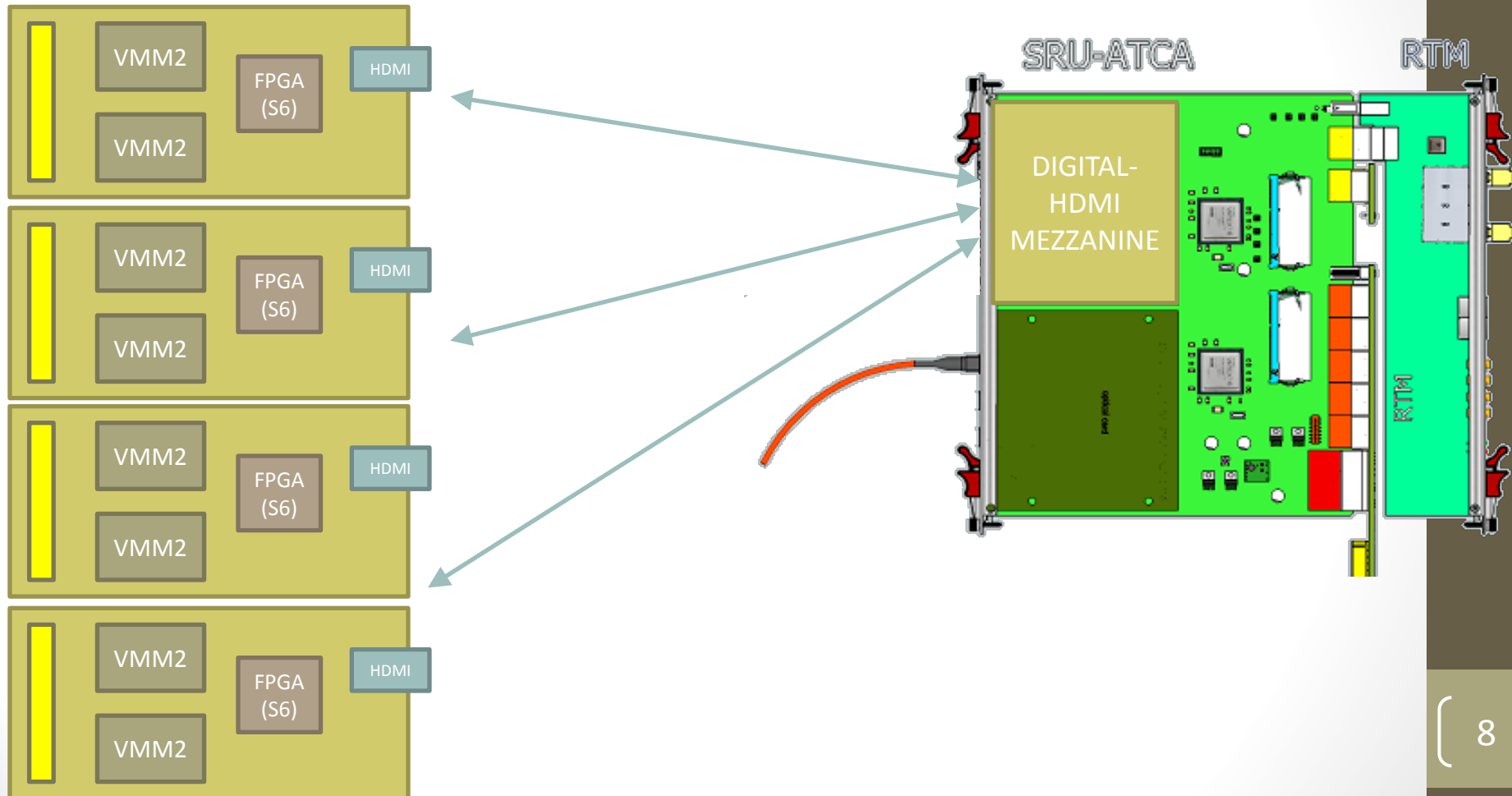
Integration of VMM2 into SRS



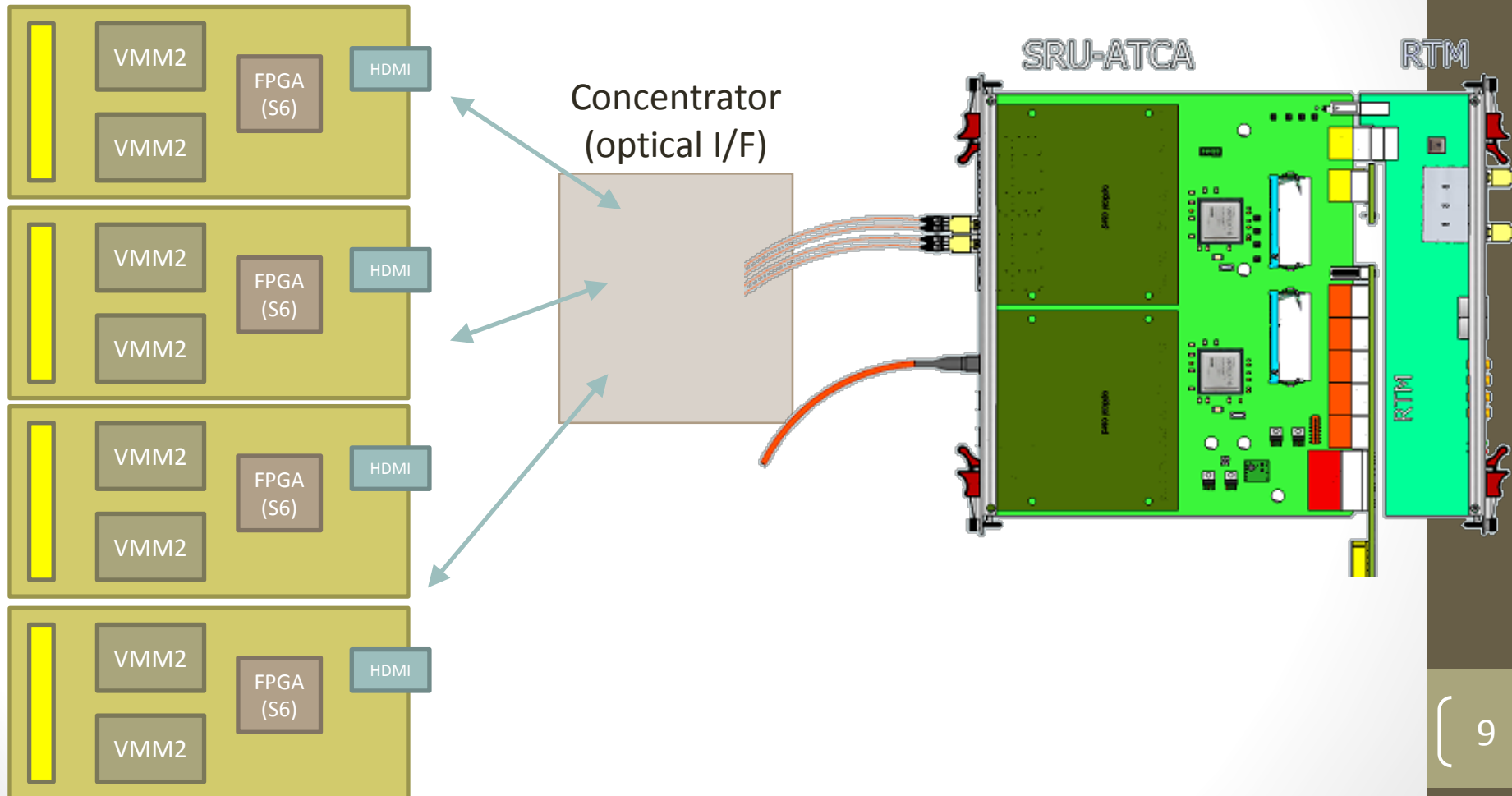
- 2 x VMM2 = 128 ch.
- Small FPGA(eg. Spartan6)/ASIC* (I/F and control)
- Readout via Digital C-Card

* An ASIC is planned in the ATLAS NSW framework

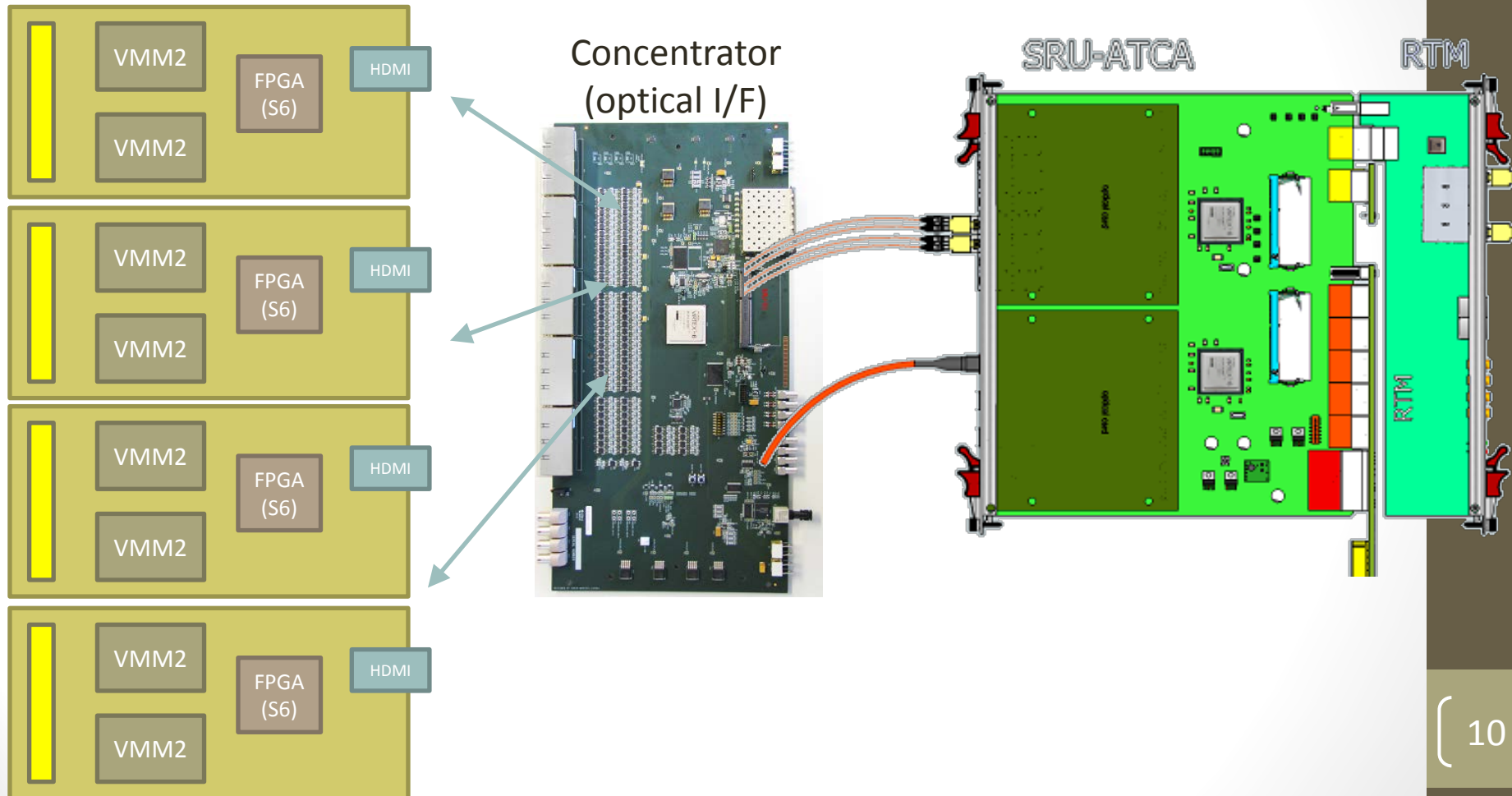
Integration of VMM into SRS (ATCA)



Integration of VMM into SRS (ATCA)

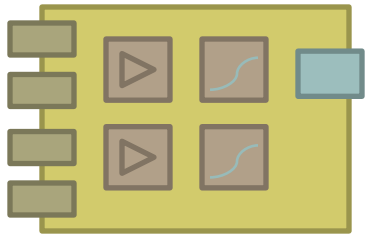


Integration of VMM into SRS (ATCA)



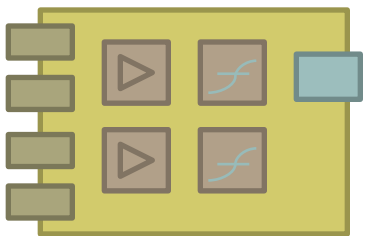
All-SRS Laboratory

Preamplifier/Shaper Hybrid



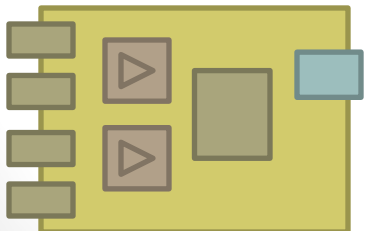
- Variable gain, shaping
- Mesh/GEM pick-up

Discriminator Hybrid



- Variable gain, shaping, threshold
- Mesh/GEM trigger
- Fast timing

Digitizer Hybrid



- SCA sampling
- Up to 2-3 GSPS
- DRS4(5), ... (see following presentation)



- Parameter control (I2C)
- Digitizer
- Shape Processing
 - digital-CFD
 - Peak finder, baseline restorer
 - ...
- Digital processing (coincidence ...)
- Fast FPGA-based TDC (10-20ps)

Thank you!