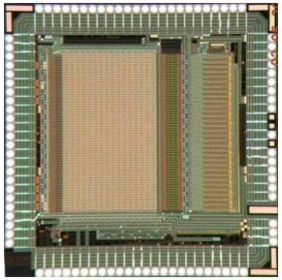
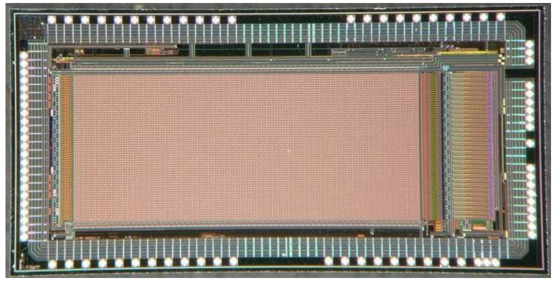
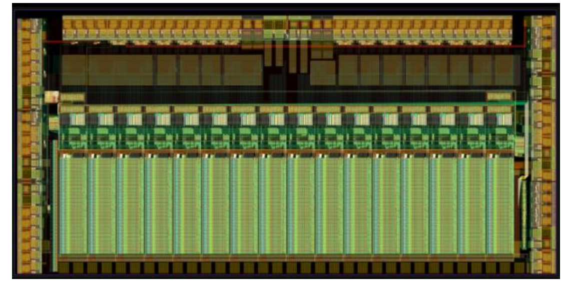
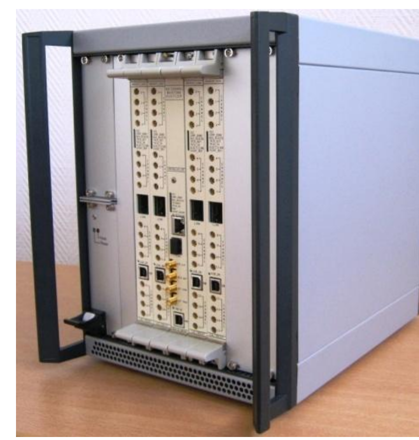
  

Analog-Memory-based Waveform Digitizers for HEP Instrumentation

D.Breton, J.Maalmi, P.Rusquart (LAL Orsay), E.Delagnes, H.Grabas (CEA/IRFU)

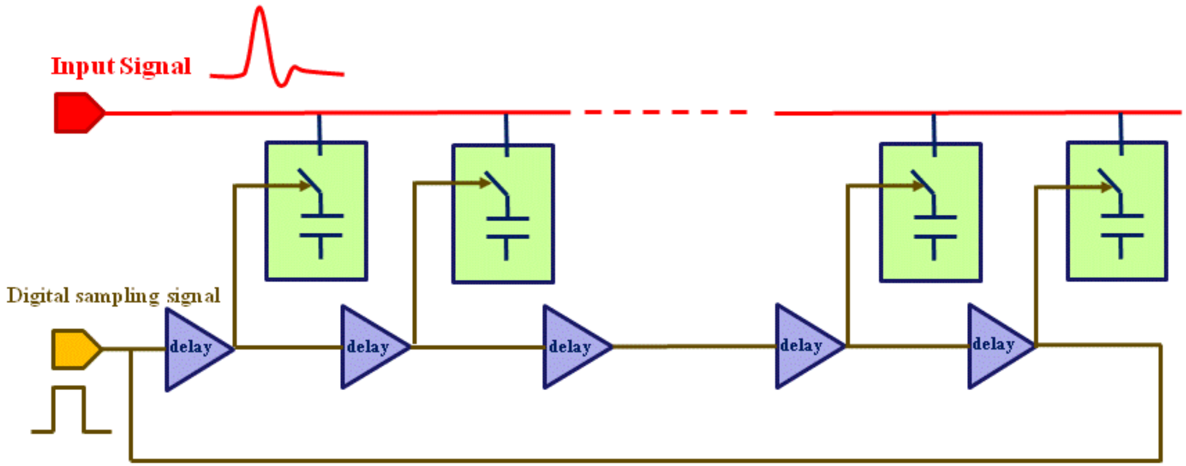


Introduction

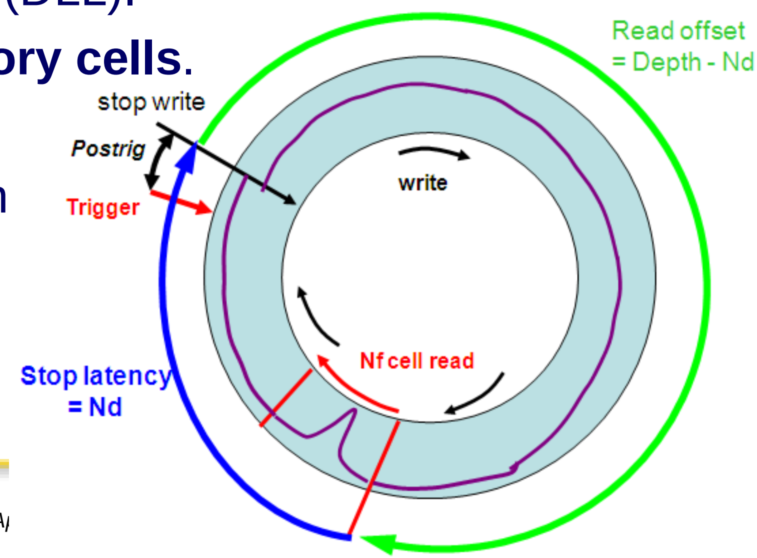
- **Many types of detectors** are implied in HEP instrumentation. Associated electronics is used either for their **characterization** (test benches) or for their **readout** (experiments).
- For **test benches**:
  - Ultimate performance of the electronics is requested
  - If the number of channels is small (≤4), then high-end oscilloscopes can be used, but they are expensive.
  - Dedicated hardware/software can also be very useful and effective
  - If the **number of channels is higher**, and if one wants to study all of them simultaneously, cost and power increase rapidly.
- For **physics experiments:**
  - Usually, **dedicated ASICs** are used
  - They shape the signal and measure Amplitude, Charge and/or Time
- **Analog-memory-based systems** permit:
  - Building **high performance test benches** at a reasonable cost
  - **measuring A, Q and/or T with a high precision**, but also seeing the **waveforms** on demand

Circular analog memories: basic principles

An analog memory can record waveforms at very high sampling rate (>>GS/s)
After trigger, they are digitized at a much lower rate with an ADC (~20 MHz)



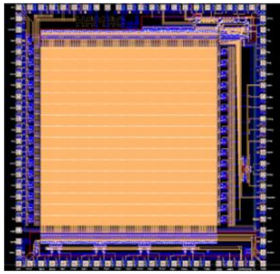
- A write pulse is running along a folded **delay line** (DLL).
- It drives the recording of signal into **analog memory cells**.
- Sampling stops upon **trigger**.
- **Readout** can target an area of interest, which can be only a **subset** of the whole channel
- **Dead time** due to readout has to remain as small as possible **(<100ns / sample)**.



Our favourite solution: a Sampling Matrix

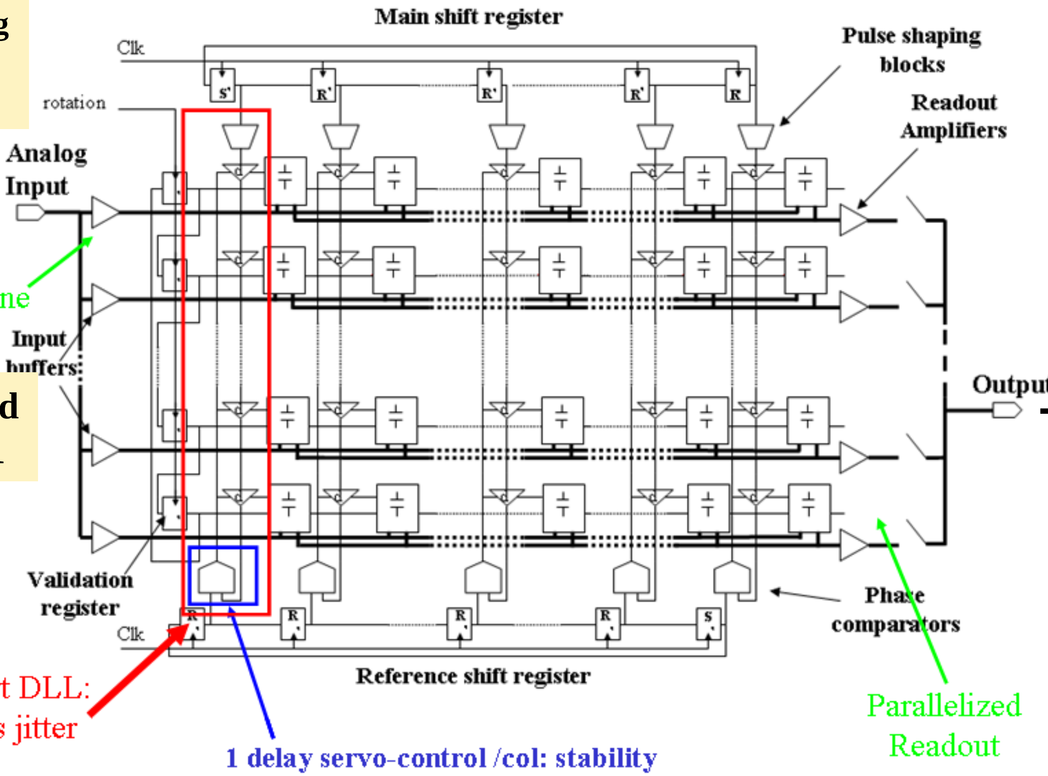
- We started designing analog memories in 1992 with the first prototype of the Switched Capacitor Array (SCA) for the ATLAS LARG calorimeter. 80,000 chips produced in 2002, now on duty on the LHC.
- Since 2002, 3 new generations of fast samplers have been designed (ARS, MATACQ, SAM): total of more than 30,000 chips in use.

HAMAC
1998-2002



Sampling at 3.2GS/s

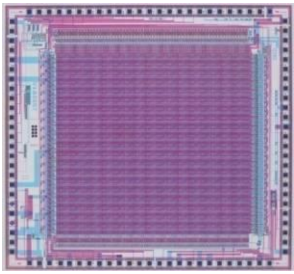
Patented in 2001



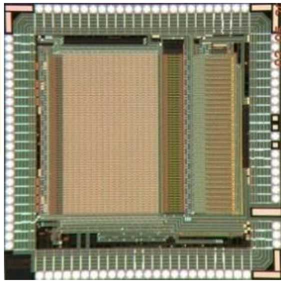
Readout 12 bits 20 MHz

ADC

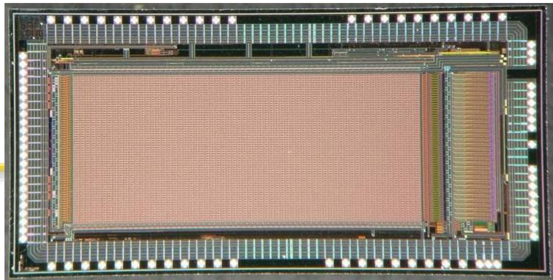
MATACQ
2000-2003



SAM
2005



SAMLONG
2010-2012



Analog memories vs ADCs

- **Analog memories** actually look like perfect candidates for **high precision measurements** at **large scale**:
  - Like ADCs they catch the signal waveform
  - TDC is built-in (position in the memory gives the time)
  - Only the useful information is digitized (vs ADCs) => **reduced dataflow and power**
  - Any type of digital processing can be used
  - Main difficulty is less sampling frequency than signal **bandwidth**
- Their drawbacks:
  - The limited recording **depth**
  - The readout **dead-time** limiting the input rate
- But:
  - Only a few samples/hit can be read => this may limit the dead time
  - **Simultaneous write/read** operation is feasible, which may further reduce the dead time

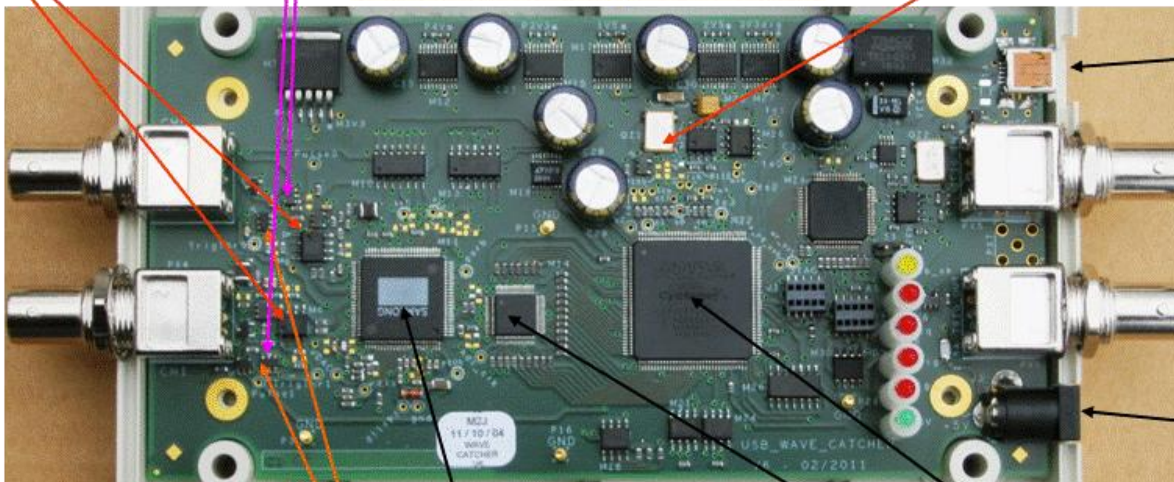
The USB_WaveCatcher board (V6)

Pulsers for reflectometry applications

1.5 GHz BW amplifier.

Board has to be powered by USB
=> power consumption ≤ 2.5W

Reference clock:
200MHz => **3.2GS/s**



µ USB

Trigger input

Trigger output

+5V Jack plug

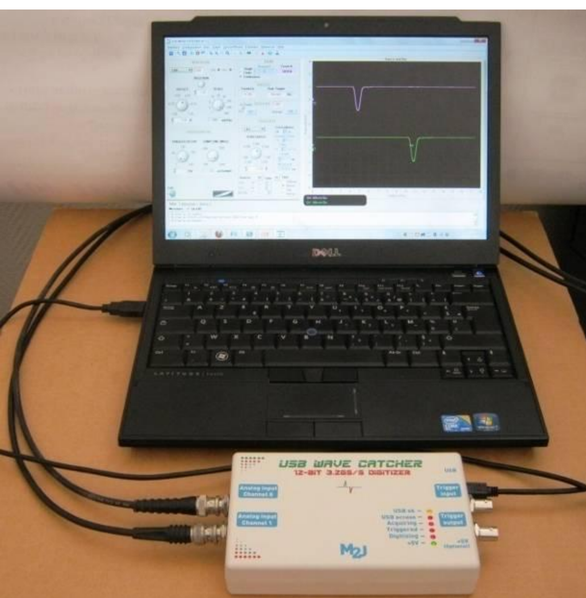
2 analog inputs. DC Coupled.

SAM Chip

Cyclone FPGA

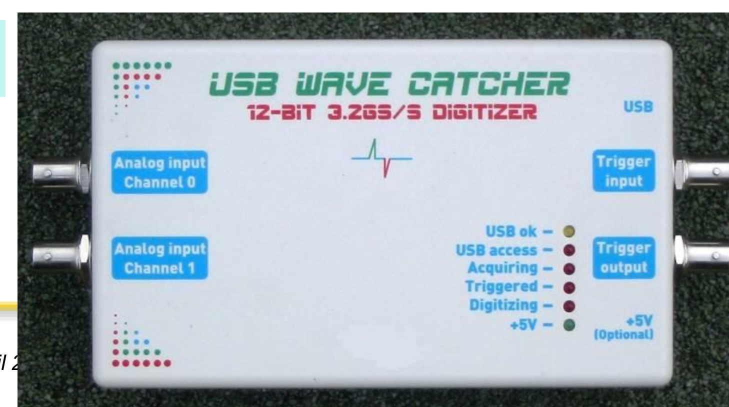
Trigger discriminators

Dual 12-bit ADC



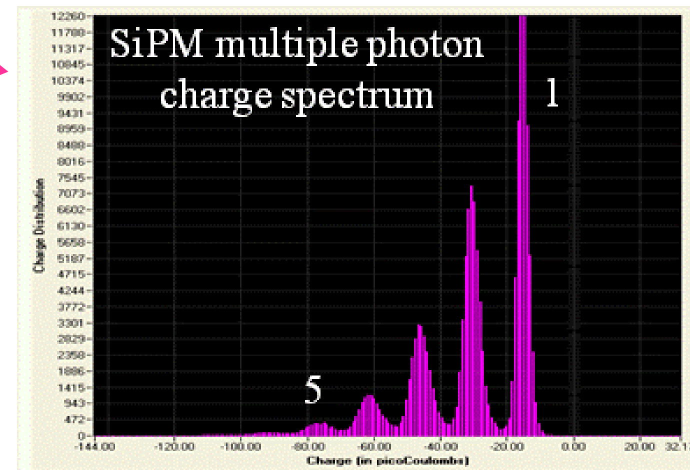
The autonomous test bench

The module

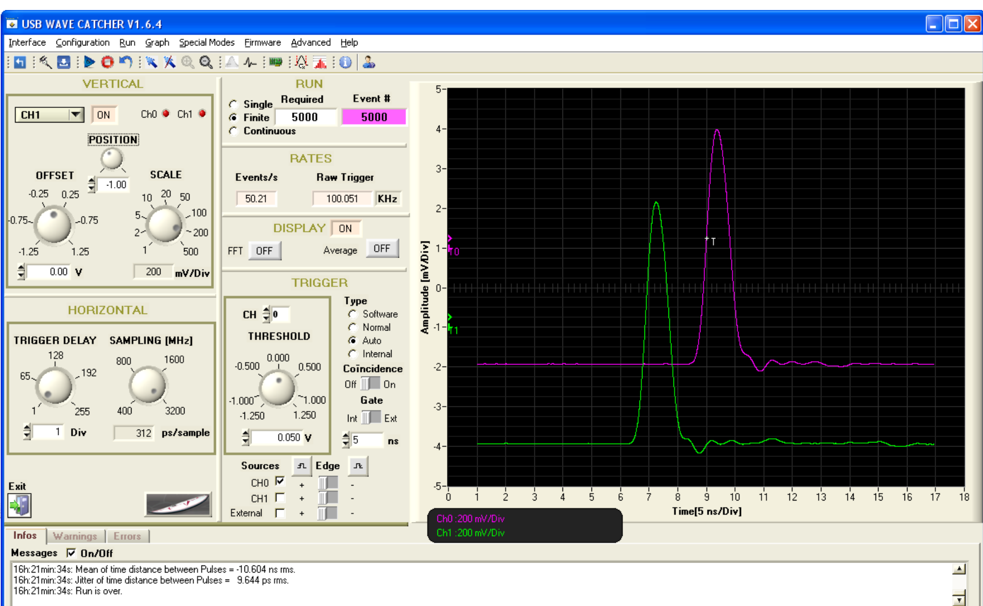


Board Specific Features

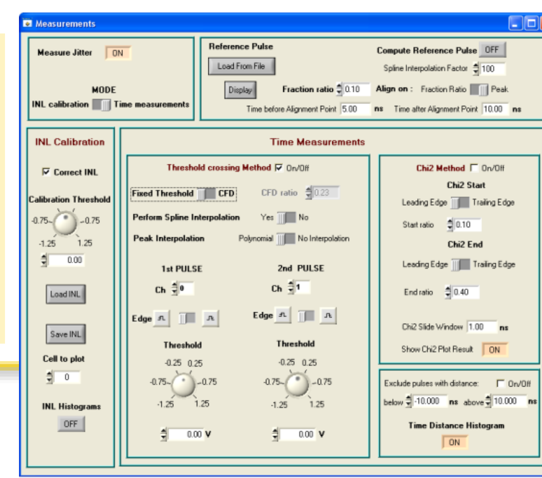
- ❖ Possibility to add **an individual DC offset** on each signal
- ❖ Individual **trigger discriminator** on each channel
- ❖ External and internal trigger + numerous modes of **triggering on coïncidence** (11 possibilities including two pulses on the same channel) => useful for afterpulse studies
- ❖ **Real time trigger counting** independent of acquisition rate
- ❖ **Embedded charge mode** (integration starts on threshold or at a fixed location) => high rates (~ 7 kEvents/s)



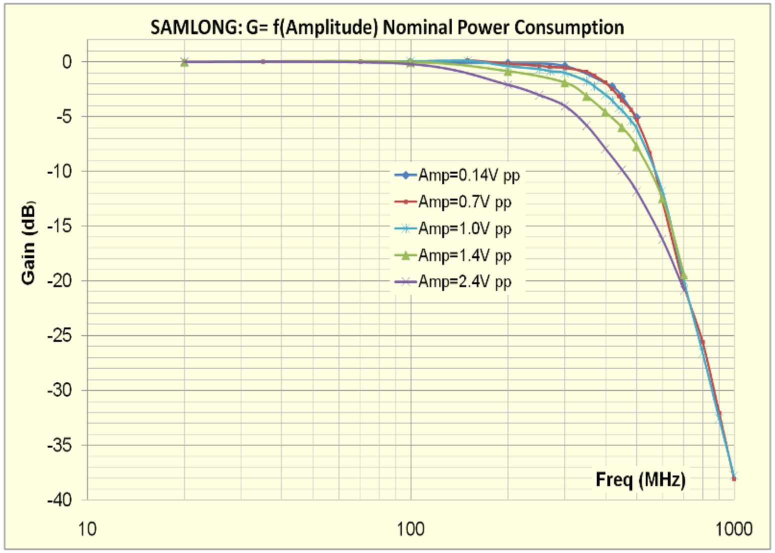
- ❖ **Embedded pulse generators** for reflectometry applications

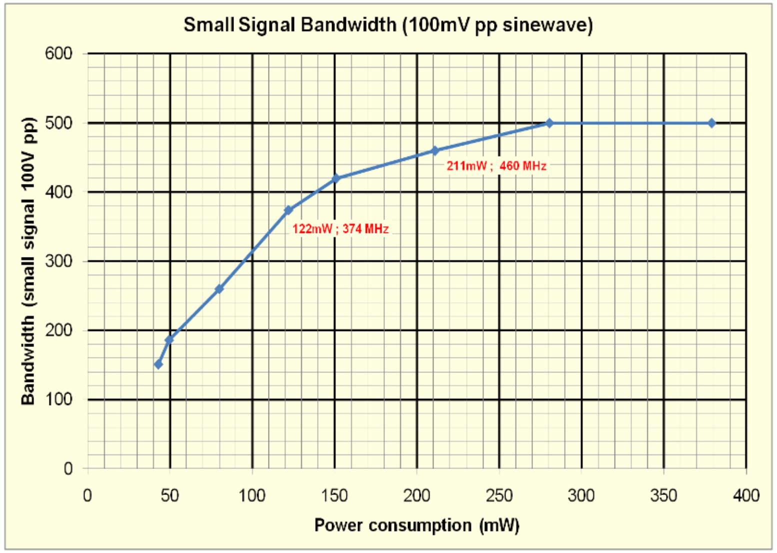


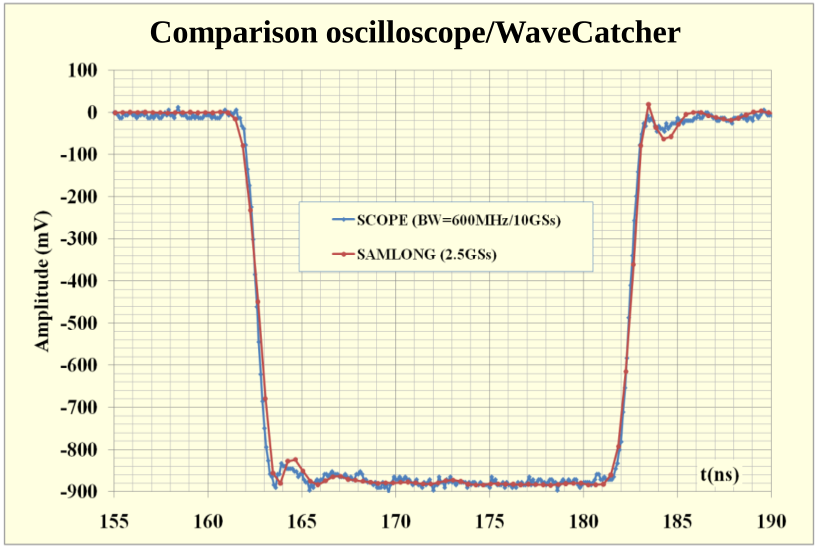
This oscilloscope-like software was developed by the team.

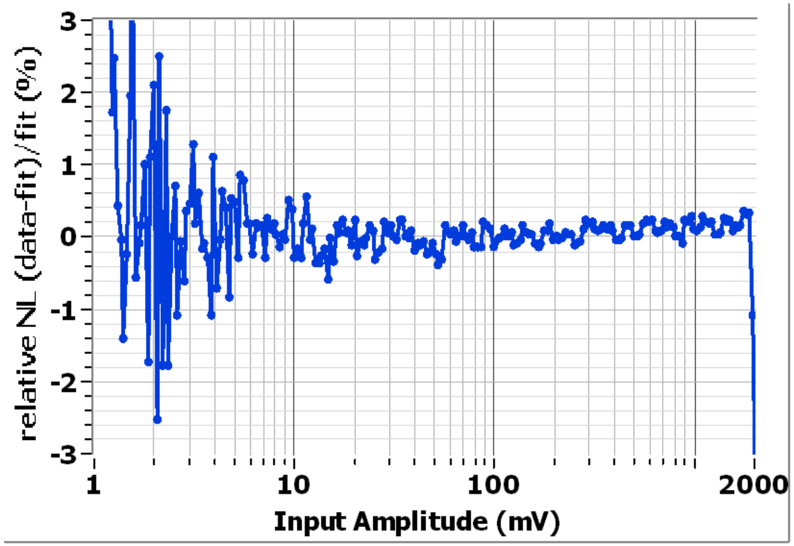


Board performances: examples





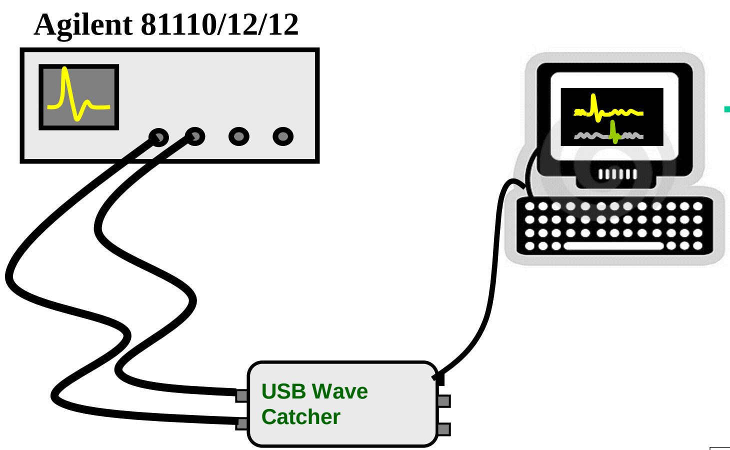


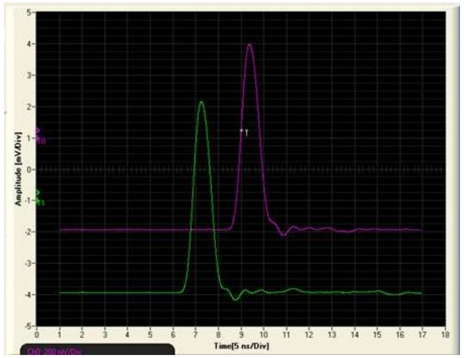


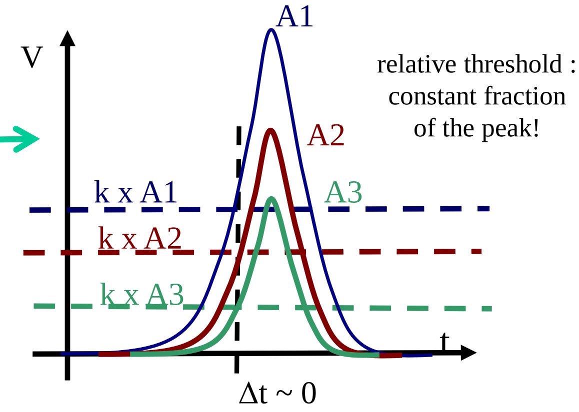
Time characterization with digital CFD method

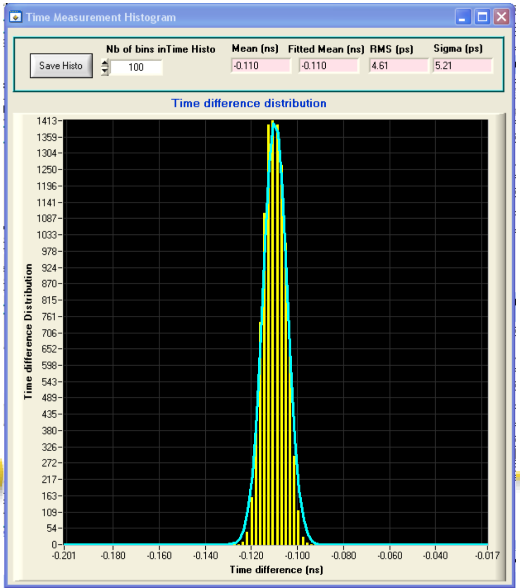
- Source: randomly distributed set of two positive pulses
- Results are the same with negative pulses or distance between arches of a sine wave

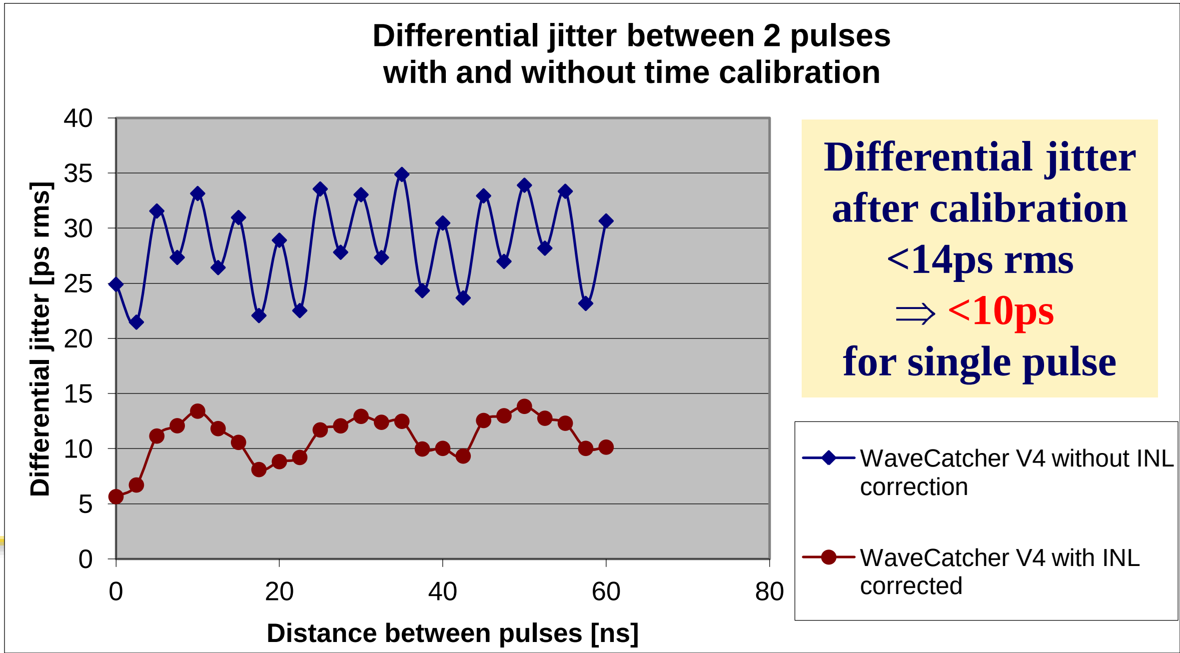
Constant Fraction Discriminator







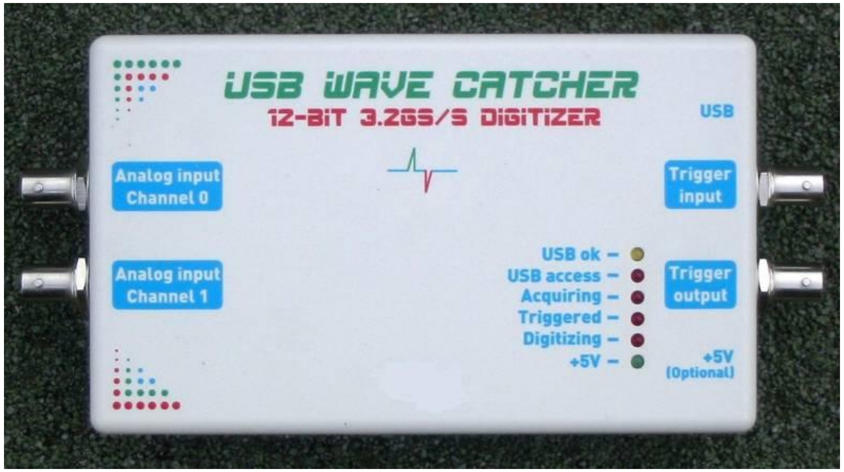




Differential jitter after calibration <14ps rms ⇒ <10ps for single pulse

Summary of the WaveCatcher performances.

- **2** DC-coupled **1024-deep channels** with 50-Ohm active input impedance
- **1.25V** dynamic Range, with full range 16-bit individual tunable offsets
- 2 individual **pulse generators** for test and reflectometry applications.
- On-board **charge integration** calculation.
- Integrated **raw trigger rate** counters
- **Bandwidth ~ 500MHz**
- **Signal/noise ratio**: **11.7 bits rms**
  (noise = **680 µV RMS**)
- **Sampling Frequency**: **400MS/s to 3.2GS/s**
- Max consumption on +5V: **0.5A**



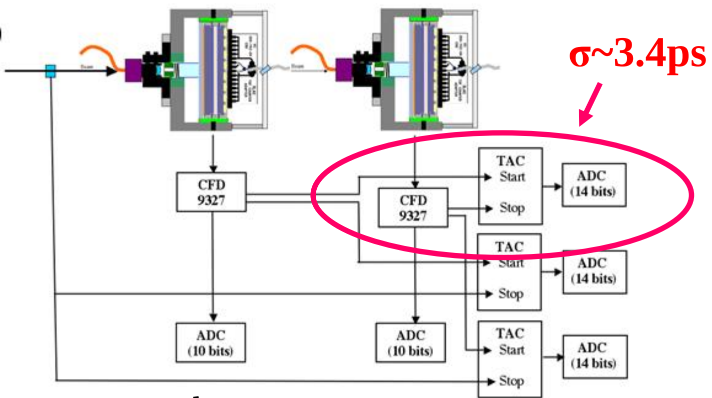
- **Absolute time precision** in a channel (typical):
  - without time calibration: ~20ps rms (@ 3.2GS/s)
  - **after time calibration** **~10ps rms** (@ 3.2GS/s)
- **Relative time precision** between channels: **<5ps rms**.
- **Trigger sources**: software, external, internal, threshold on signals,
- **11 modes of trigger** coincidence
- Acquisition rate (**full events**) Up to **~1 kHz** over 2 full channels
- Acquisition rate (**charge mode**) Up to **~7 kHz** over 2 channels

Applications to detectors: a few examples

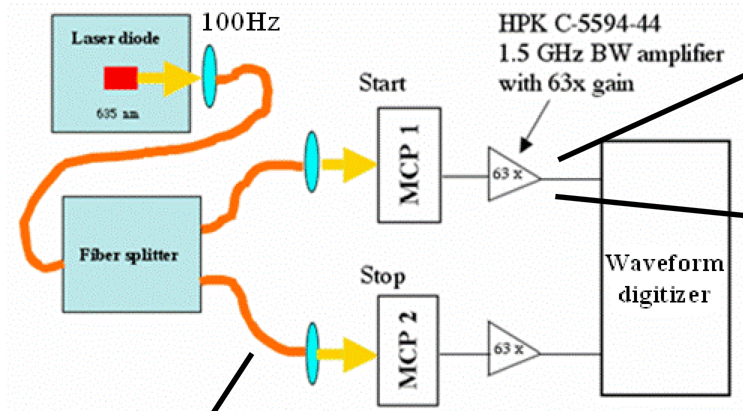
MCP-PMT characterization at SLAC (J. Va'Vra)

Goal was to compare different electronics for measuring the signal time difference between 2 MCPPMTs => NIM paper A 629 (2011) 123–132

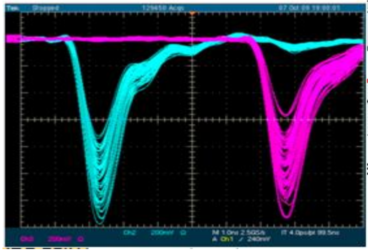
Using Ortec modules

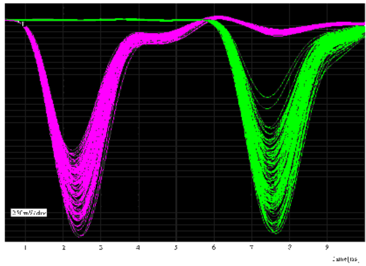


Using Waveform Digitizers

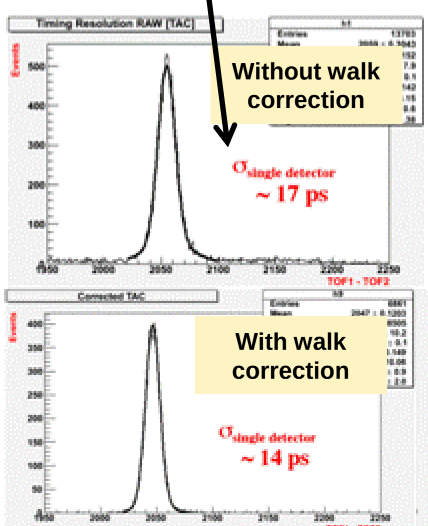


Tektronix oscilloscope

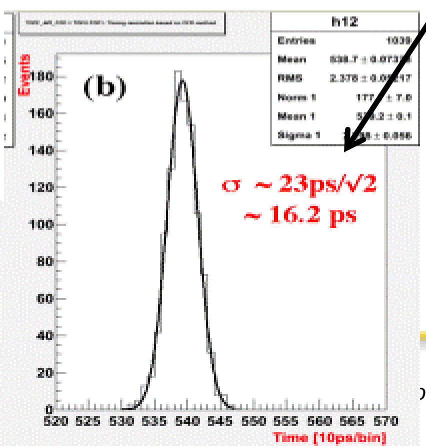




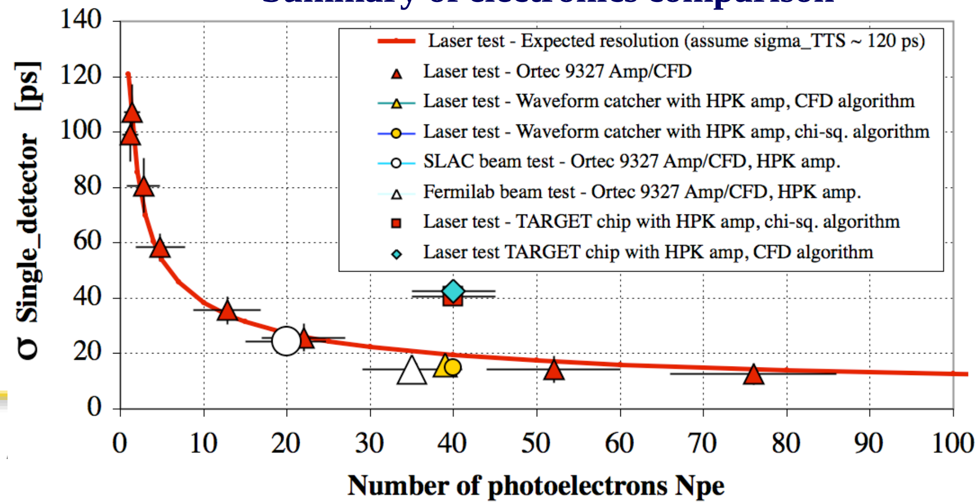
WaveCatcher board



Digital CFD method was used

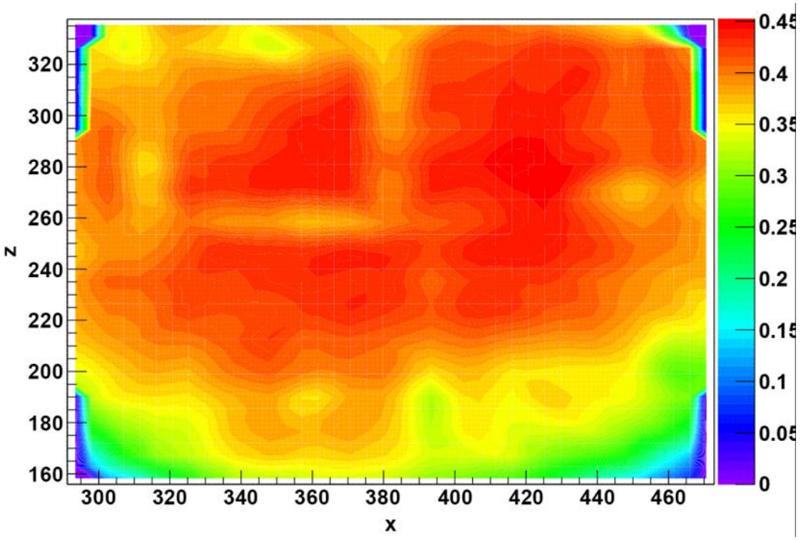


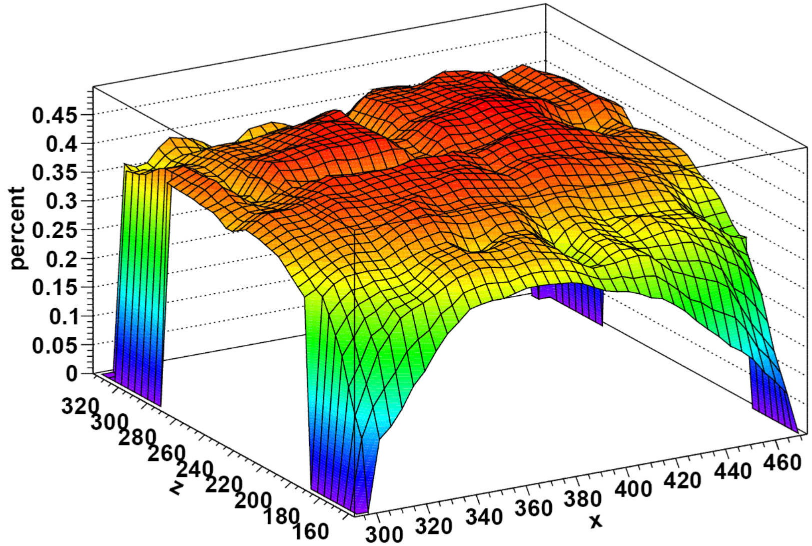
Summary of electronics comparison



PM characterization at APC

- Goal is to precisely characterize the Antares opto-modules in single photoelectron mode
- **1,000,000 triggers** per measurement step
- 0.45% of triggers give a photoelectron (=> ~1.5% of statistical error)
- There are 289 measurement steps spaced by 1cm (3 degrees of aperture on the optical module) starting from its center
- Using the **integrated charge mode**, reading out the 289,000,000 events took only 2h30 with V4.



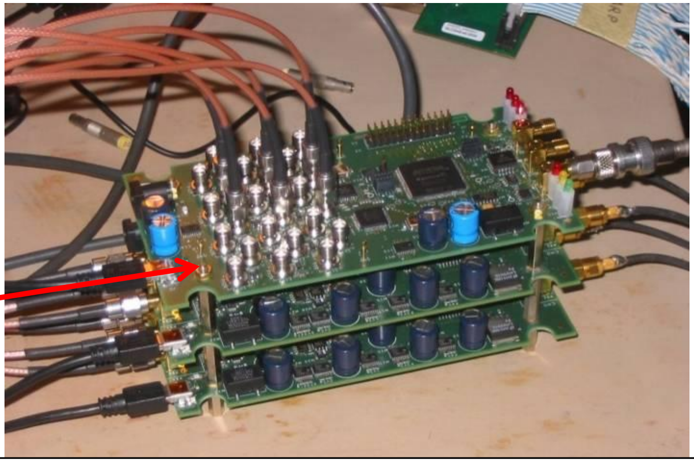


Increasing the number of channels …

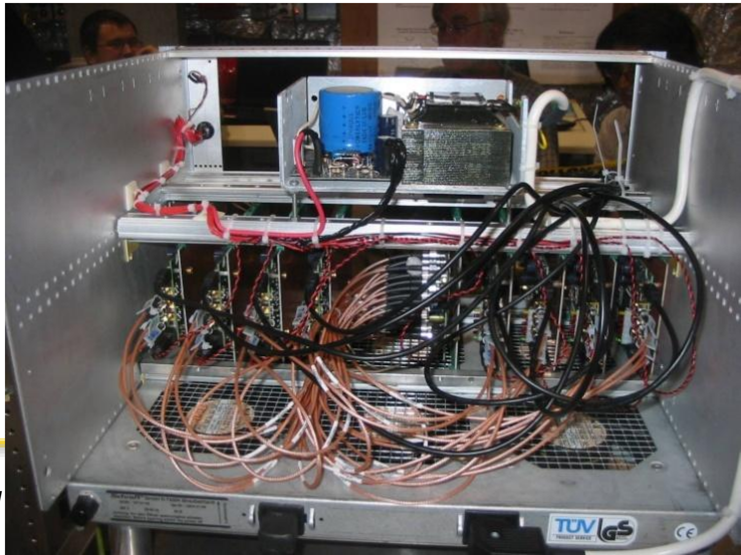
- To validate the principle, we decided to build a synchronous **16-channel** acquisition system based on **8 two-channel WaveCatcher** V5 boards
- Technical challenge: to **keep the 10ps time precision** at the crate level

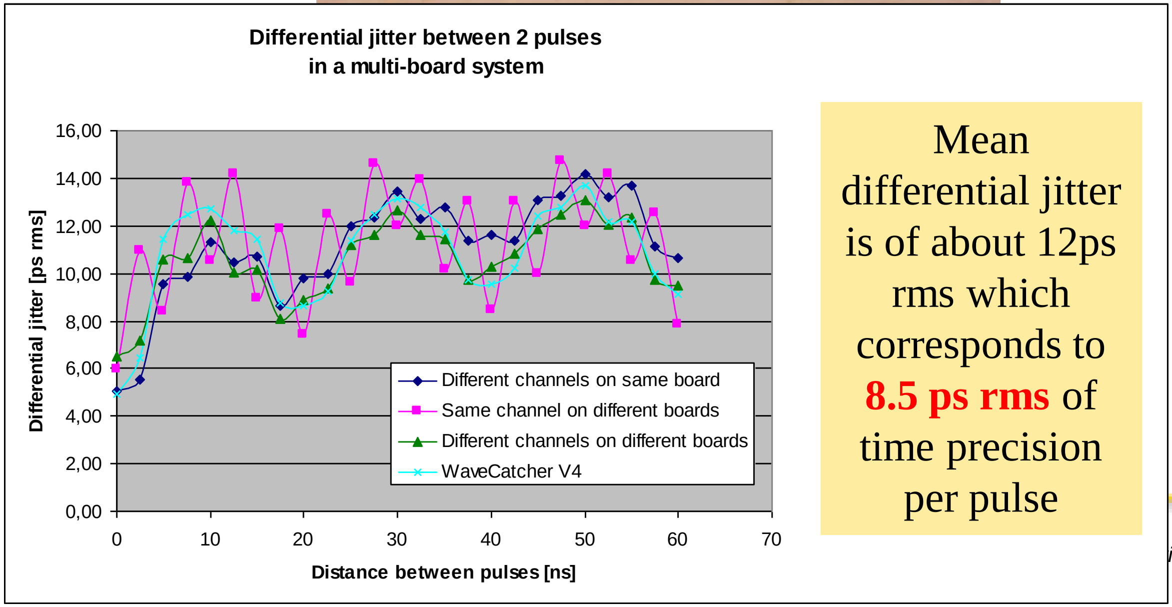
4-channel prototype

New controller board



16-channel crate

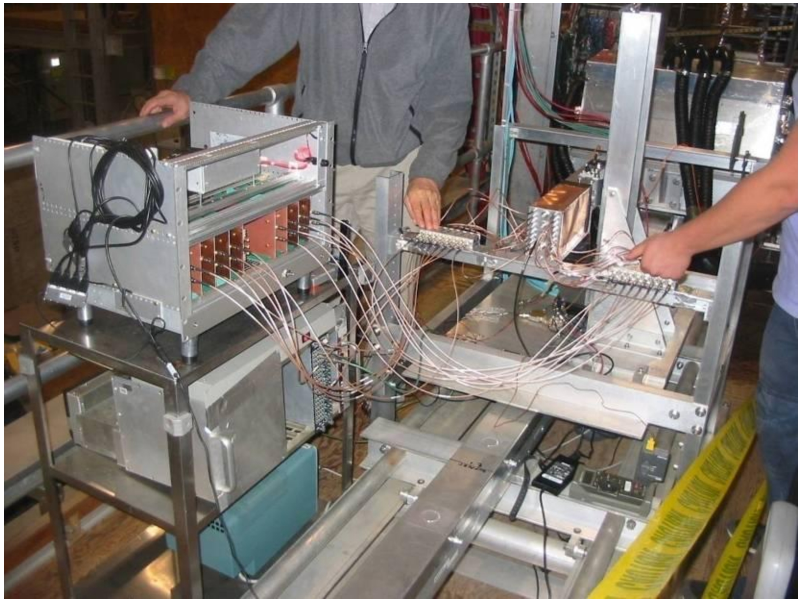


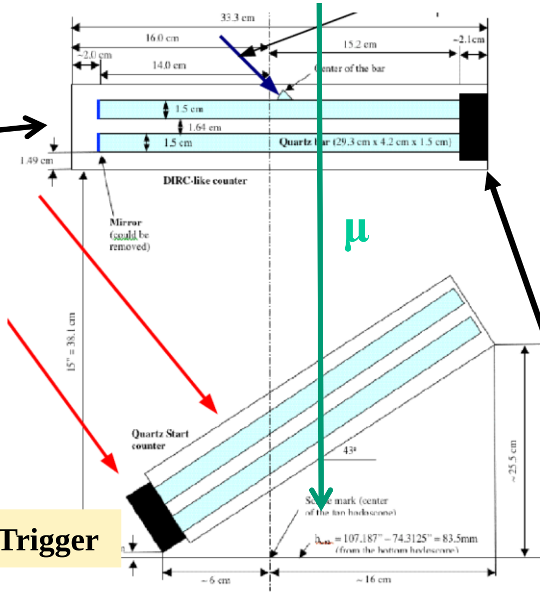


Mean differential jitter is of about 12ps rms which corresponds to **8.5 ps rms** of time precision per pulse

TOF at the SLAC cosmic ray telescope

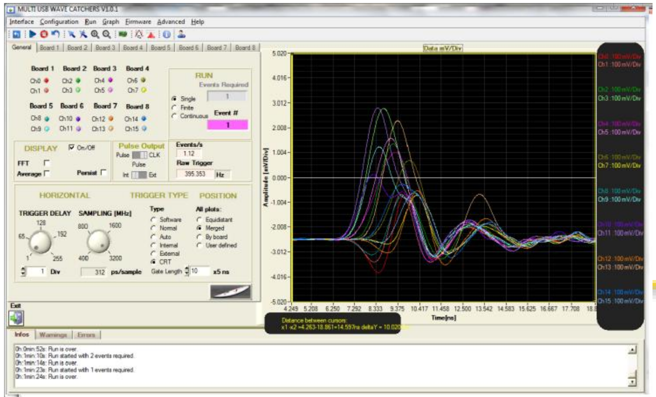
- TOF experimental setup on the CRT
- Goal was to measure the time difference in cosmic muon detection between the two quartz bars in view of SuperB FTOF prototype



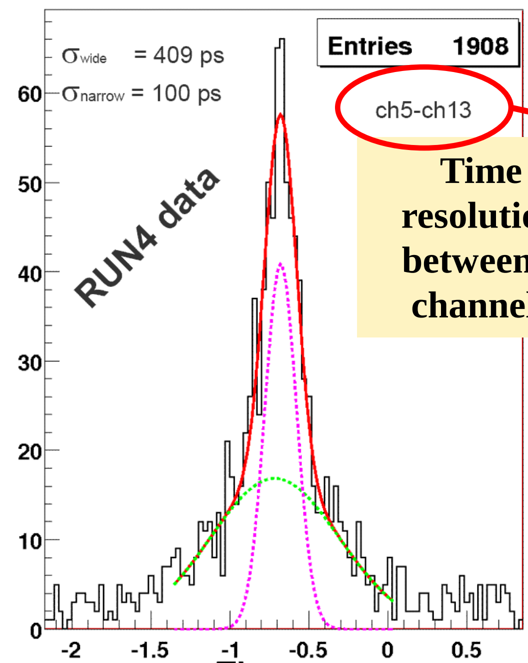


Trigger

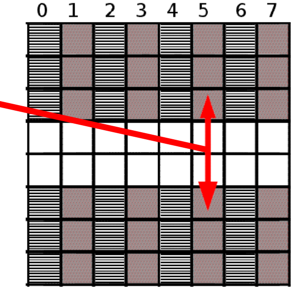
More than adequate for final physics goal of 50 ps with 5 to 10 photoelectrons



New 8-board acquisition software



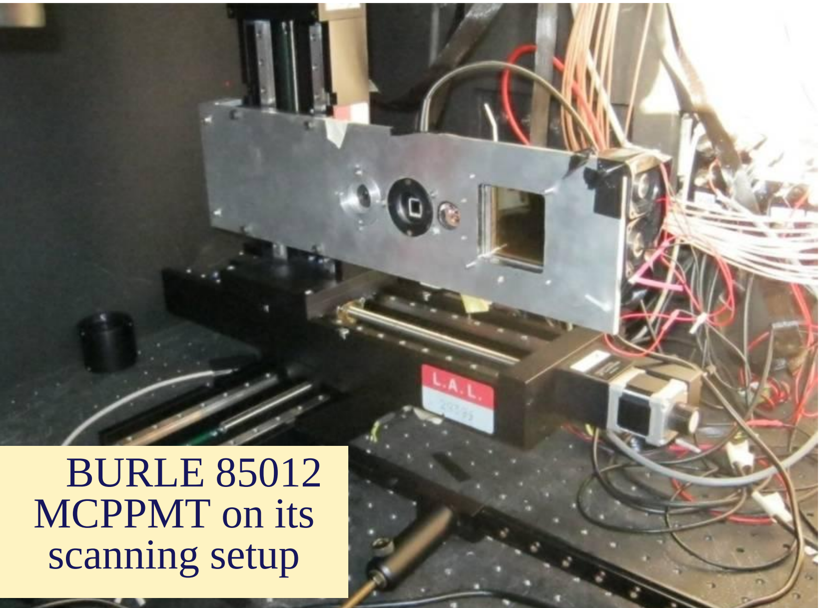
Time resolution between 2 channels



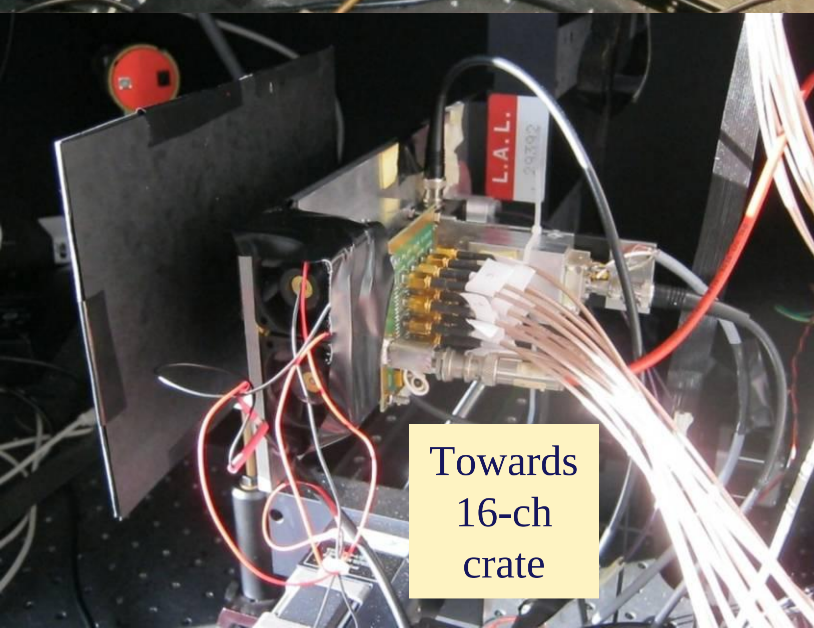
One example of time difference

$\sigma_{narrow}/\mathrm{sqrt}(2) \sim 70$ ps

MCPPMT test bench at LAL

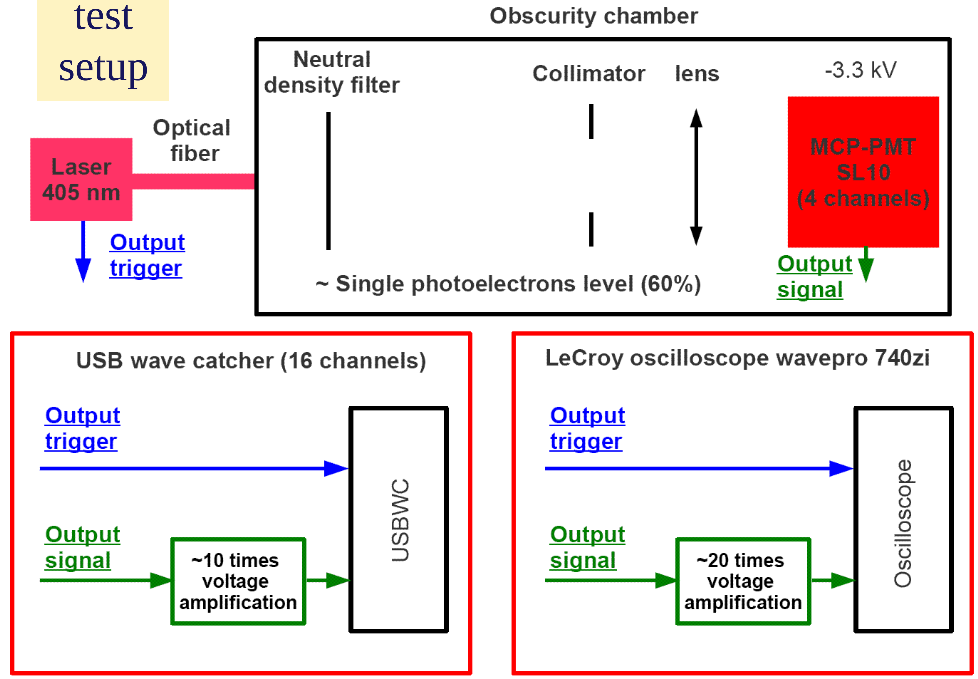


BURLE 85012 MCPPMT on its scanning setup



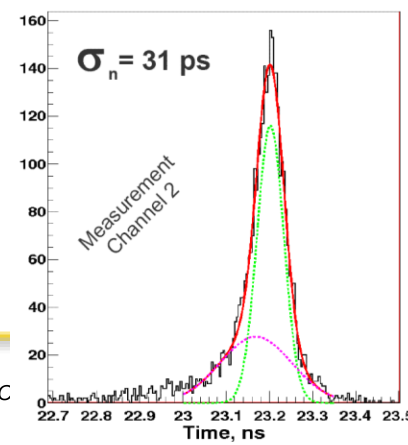
Towards 16-ch crate

SL10 test setup

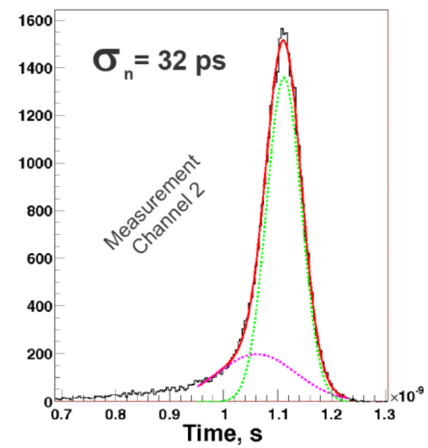


SL10 test results

USB wave catcher (16 channels)



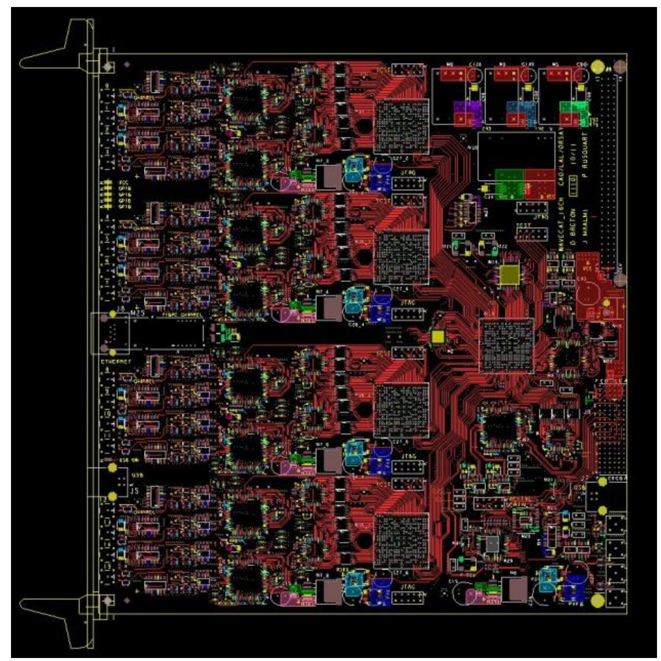
LeCroy oscilloscope wavepro 740zi



Latest developments

2010

2011



…

2012

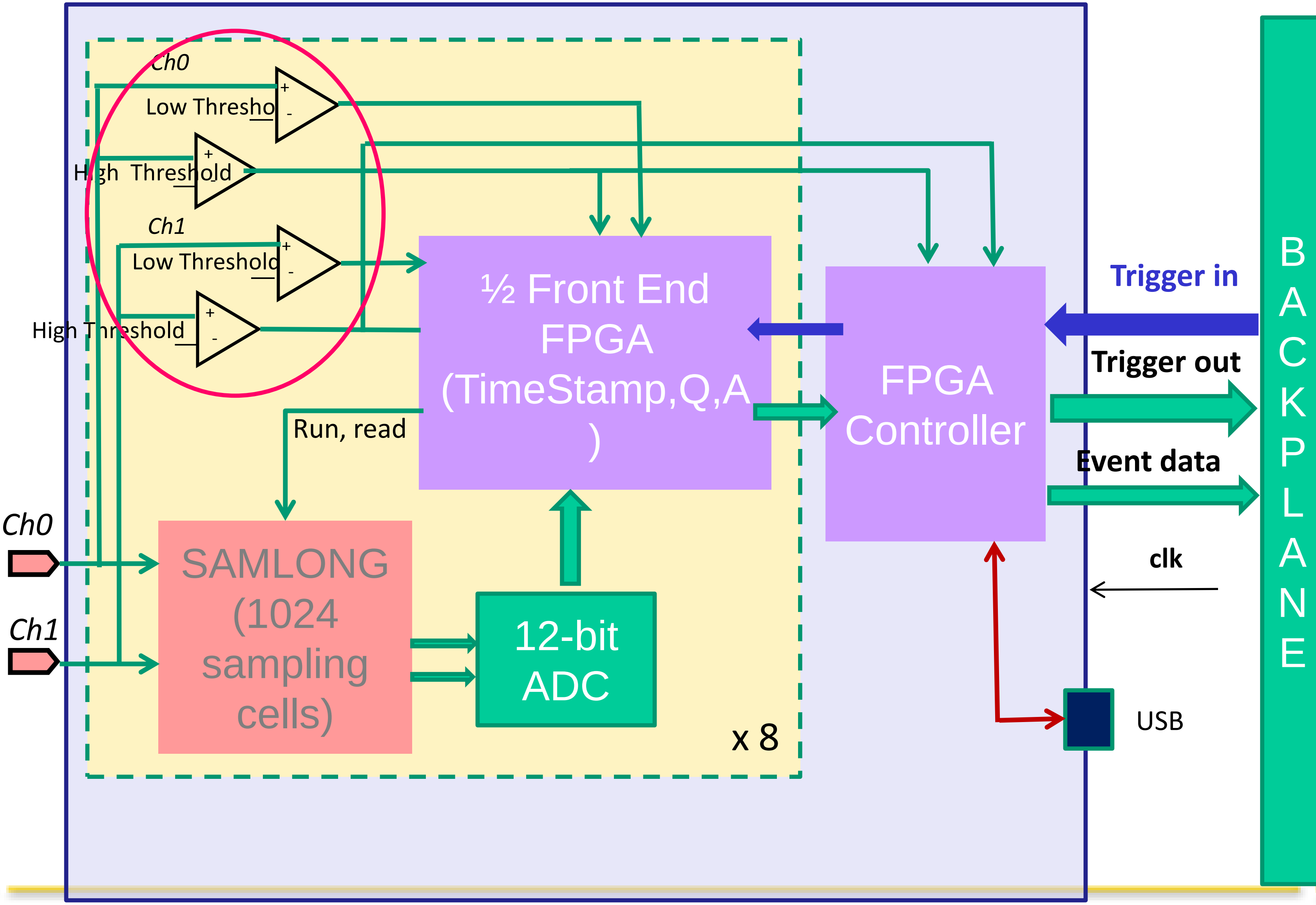
The 16/18-channel board

- 1.6mm thick
- 10 layers
- 233 x 220 mm²
- **3200 components**
- 25 power supplies (5 global, 20 local)

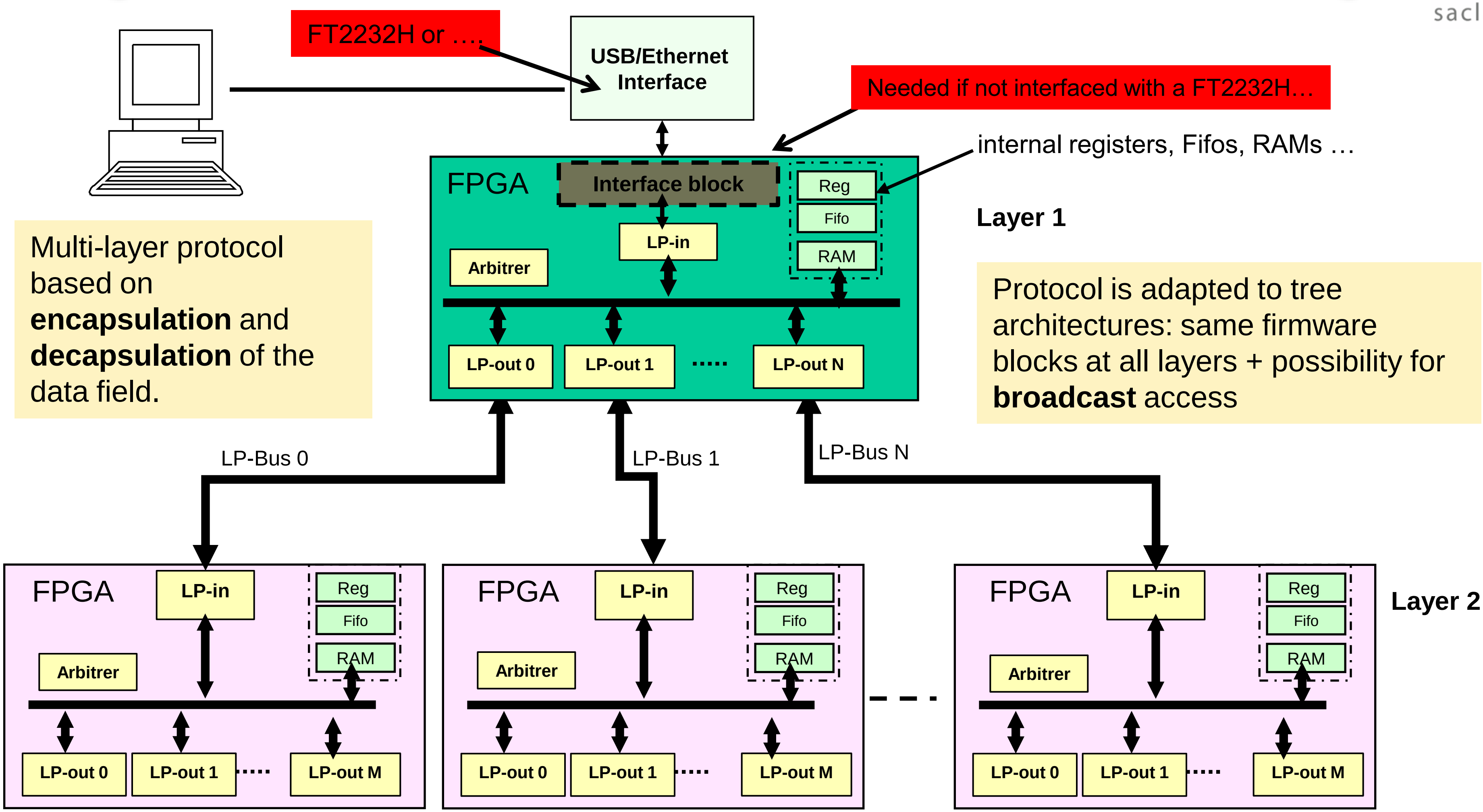
- 4 **4-channel blocks** (can be used as **mezzanines** on other boards)

- 2 channels dedicated to digital signals

2-channel front-end diagram



A flexible architecture thanks to LP-BUS



Multi-layer protocol based on **encapsulation** and **decapsulation** of the data field.

Protocol is adapted to tree architectures: same firmware blocks at all layers + possibility for **broadcast** access

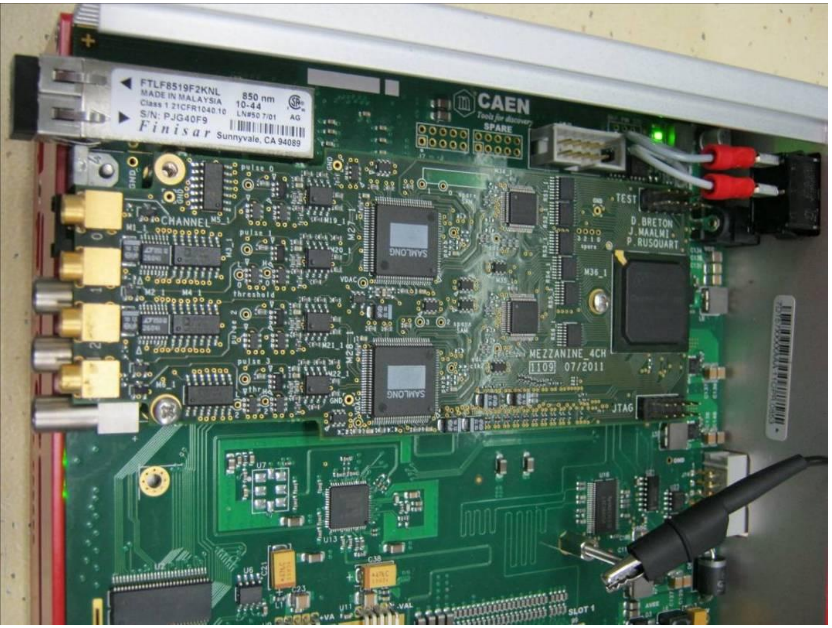
Event fragments are **pushed** towards USB => this permits a **sparsified readout**
=> can be based on the dual signal threshold

Present and future board features (not exhaustive)

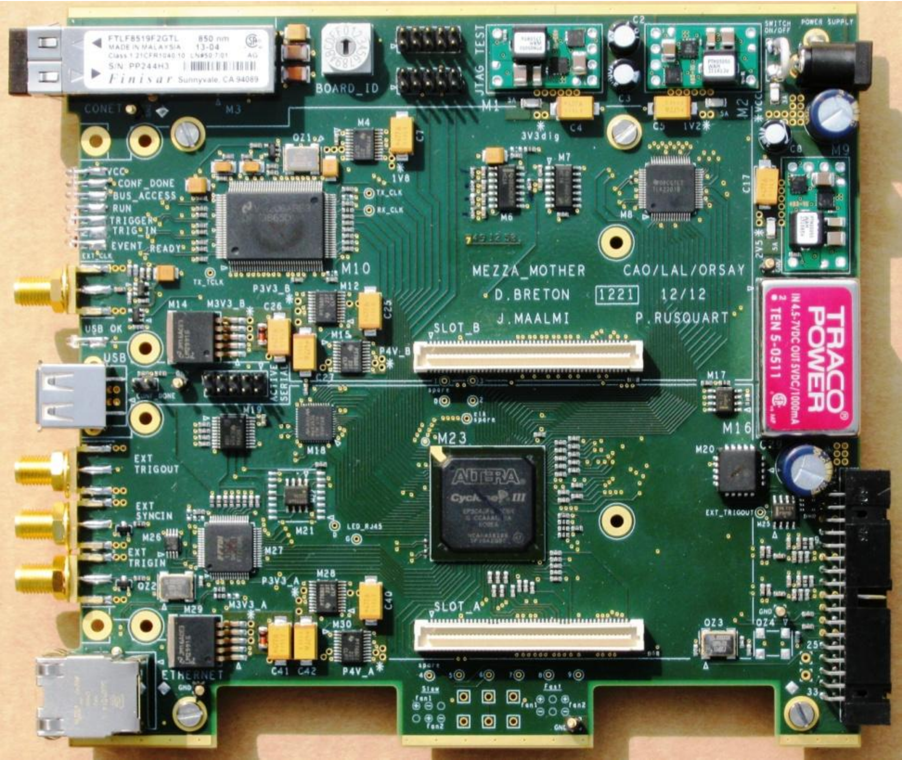
- Possibility to add an **individual DC offset** on each signal
- **Individual trigger discriminator** on each channel
- External and internal trigger + different modes for **triggering on coïncidence**
- **Embedded charge mode** (integration starts on threshold or at a fixed location) => high rates (~ 3.5 kEvents/s)
- **2 extra memory channels** for digital signals
- One **pulse generator** on each input
- **External clock** input for multi-board applications
- Embedded **USB** and Gigabit optical interfaces
- Possibility to program the FPGAs via **USB/Backplane/**Altera Blaster
- Possibility to chain channels by groups of 2
- **Embedded digital CFD** for time measurement
- **Embedded signal amplitude** extraction

Front-end block can be used as a mezzanine

- The latter has been made compatible with the **CAEN** digitizer board family
- Measurements results are equivalent to those of the WaveCatcher module: noise level : **0.72 mV**, signal bandwidth ~ **500 MHz**, time precision < **10ps rms**
- Will be available on the market **this summer (DT5743, V1743, N6743)**

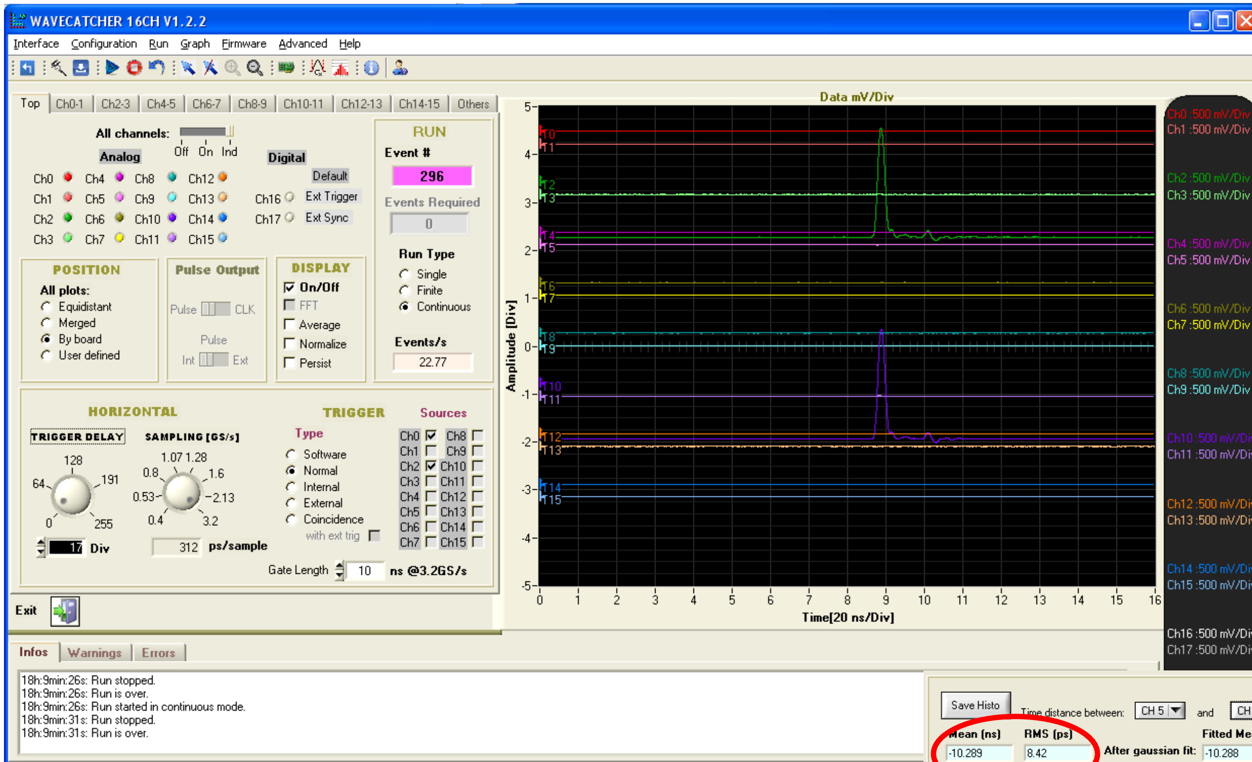


LAL motherboard
for 2 mezzanines

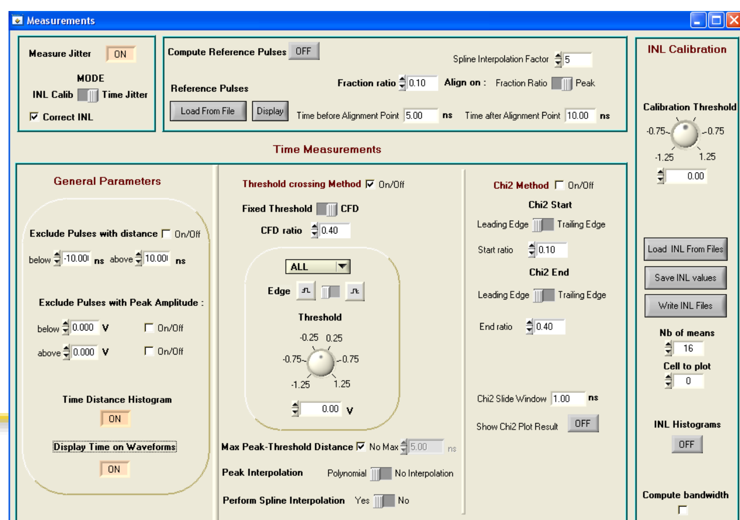


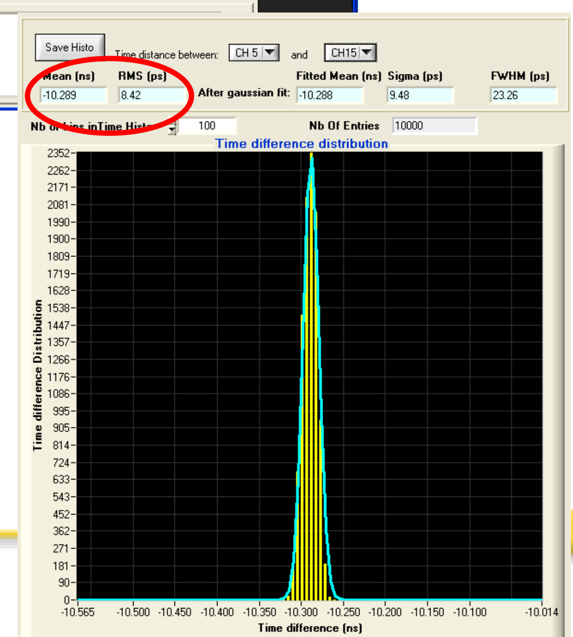
16-channel acquisition software

Main panel: oscilloscope like, but 16 channels

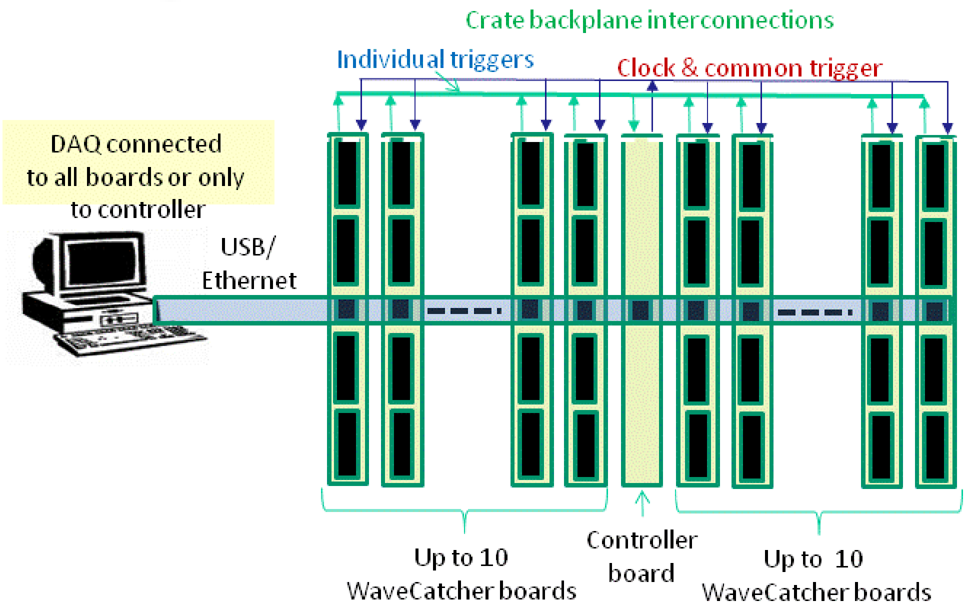


Time measurement panel

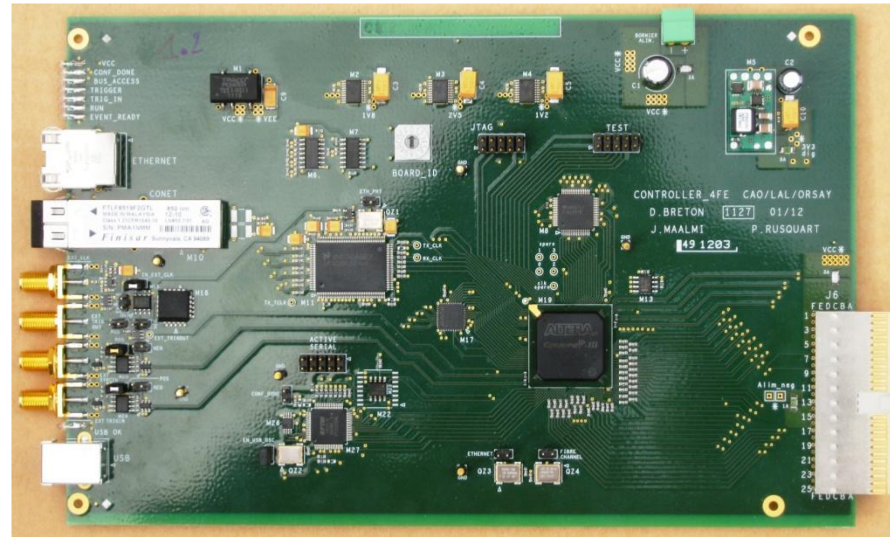




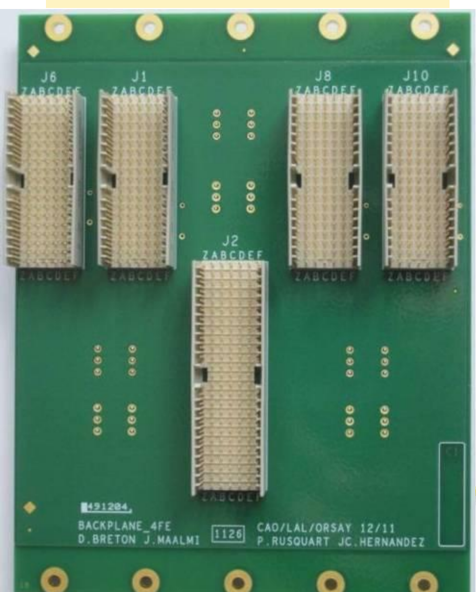
Building large scale systems



The controller board



64-channel backplane



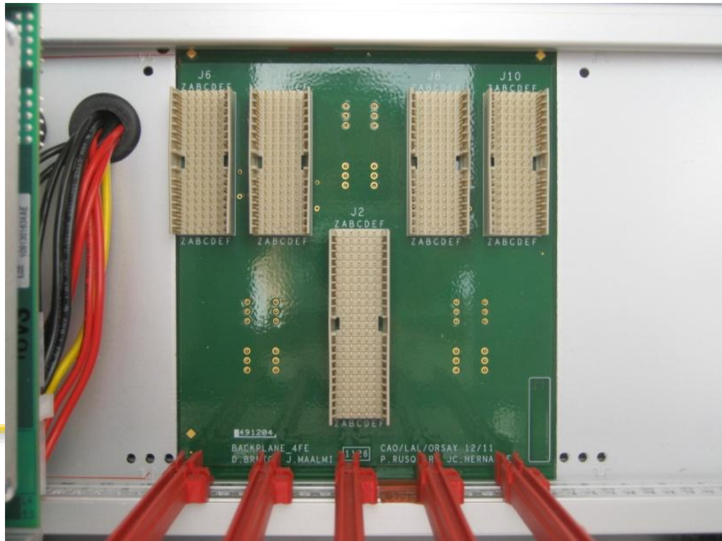
➢ To synchronise N boards a controller board is needed + a backplane for the interconnections

➢ we have built a very compact 64-channel system:

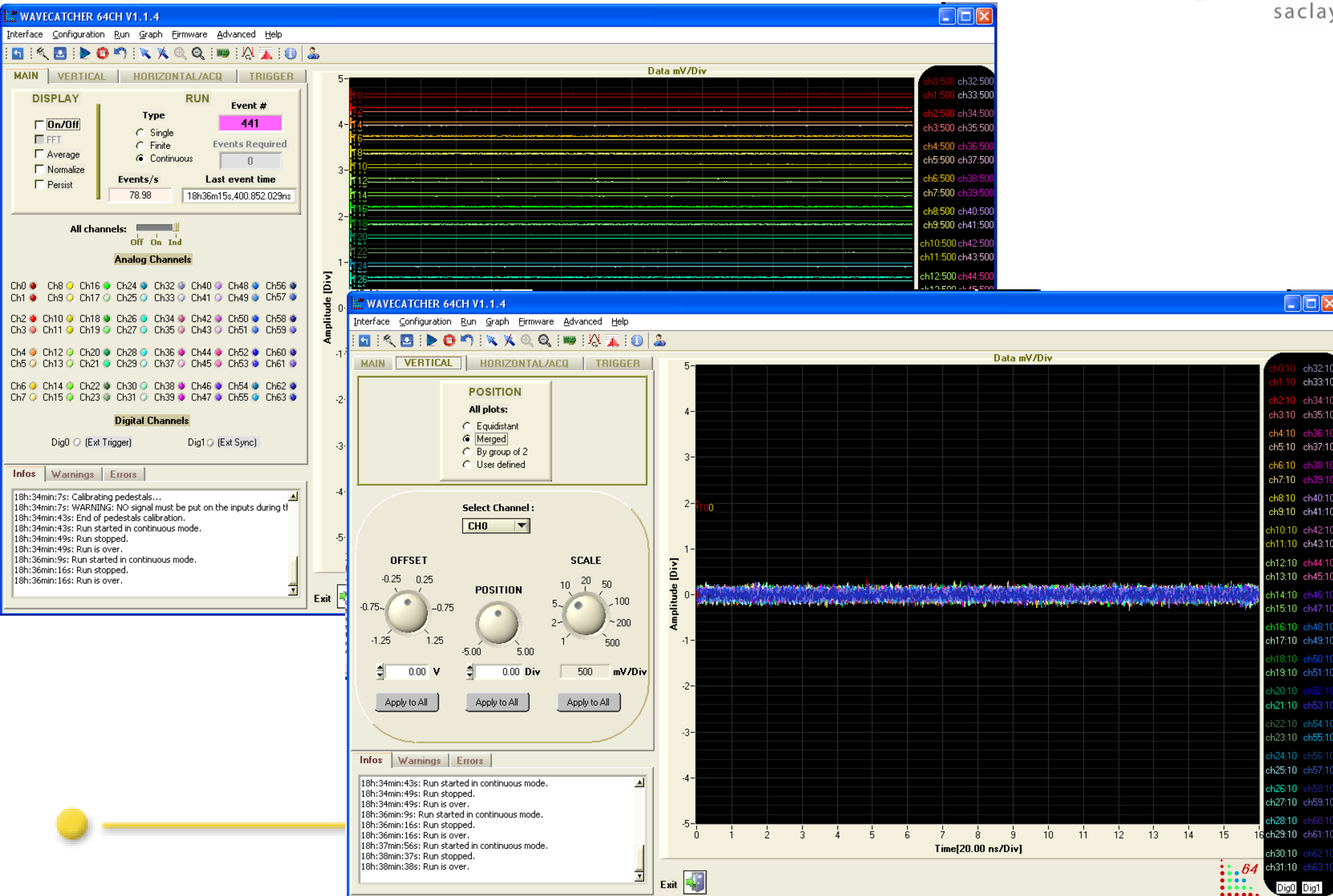
→ will soon be used for the CORTO Cosmic Ray Telescope at Orsay and for a prototype of new Gamma Spectrometer for particle detection

➢ we are also building a 960-channel system based on 3 6U-crates (one module of the future SuperNemo experiment)

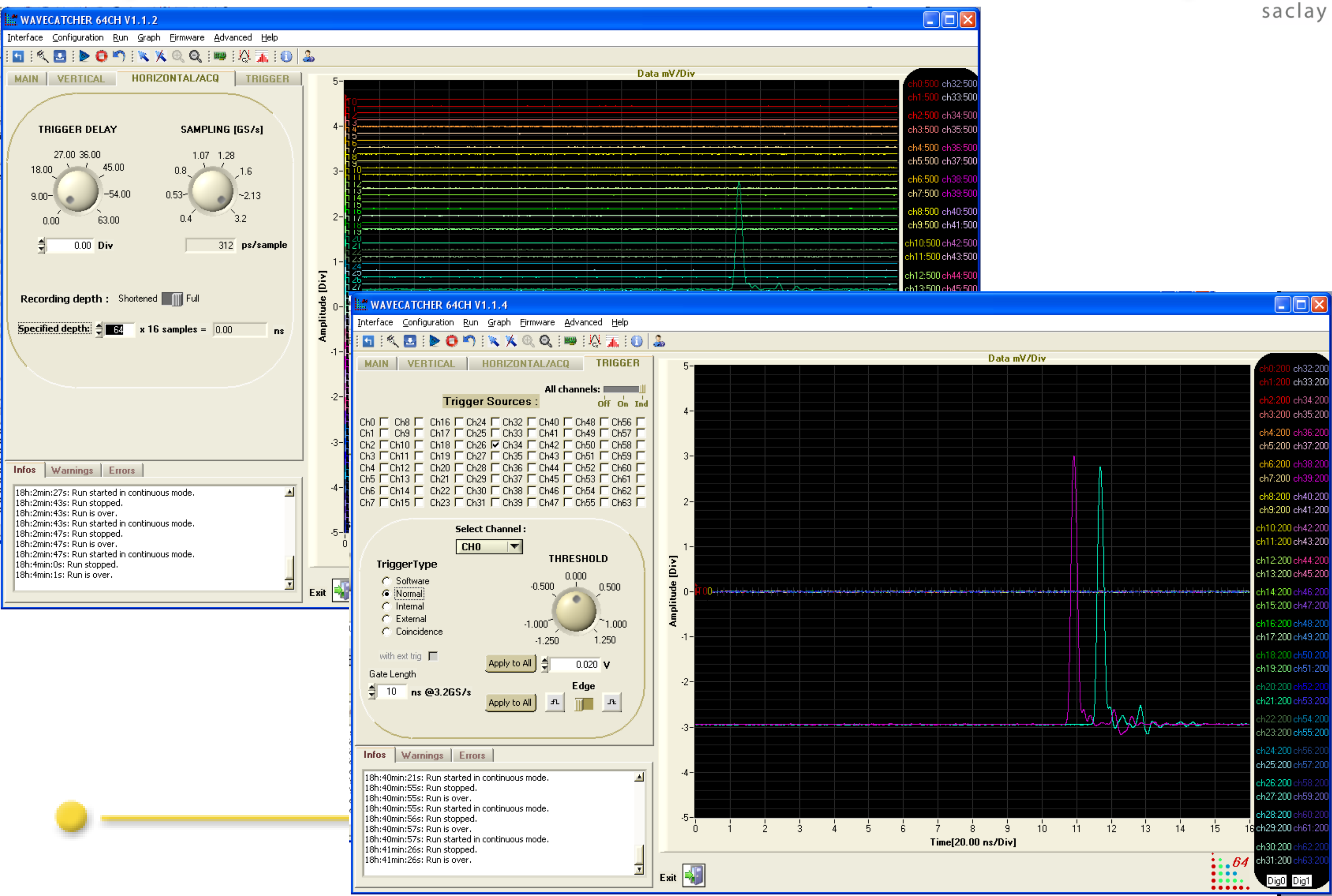
The 64-channel digitizer



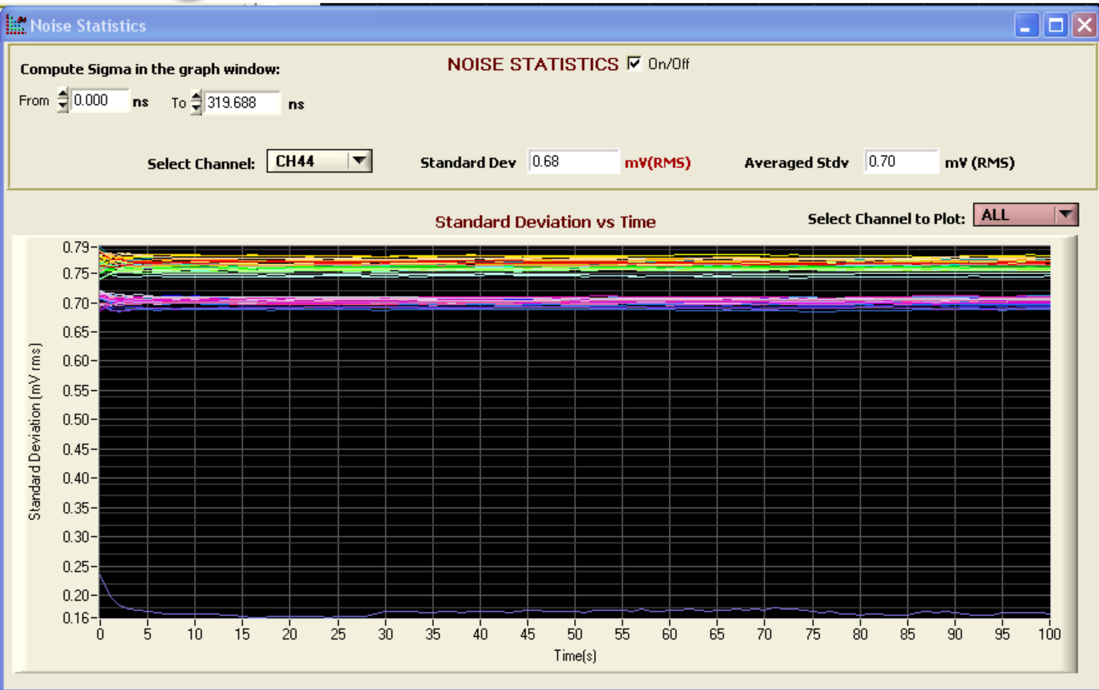
The 64-channel (prototype) software



The 64-channel software (2)



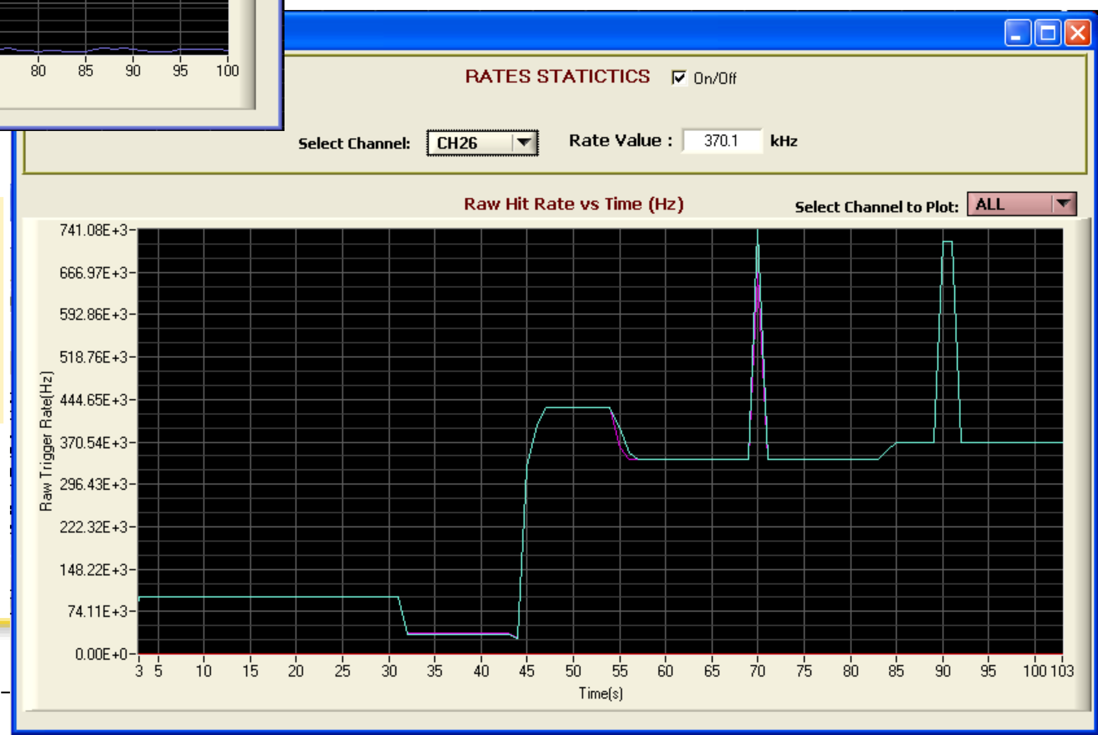
The 64-channel software (3)



Noise statistics panel

➢ Software also comprises the same powerful time measurement panel as the 16-channel version

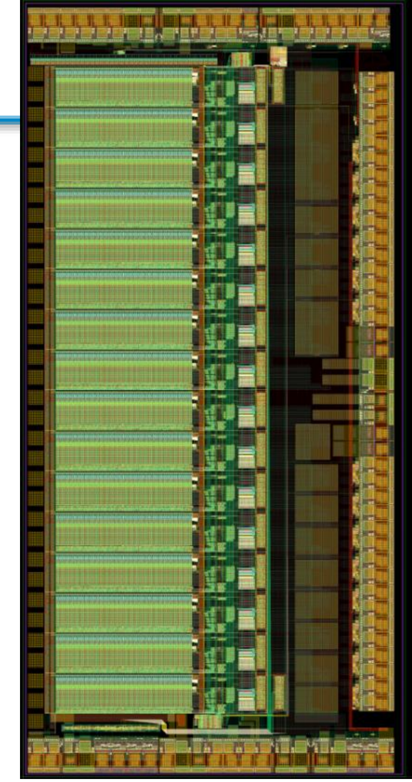
Channel hit rate statistics panel (measures up to ~400 MHz)

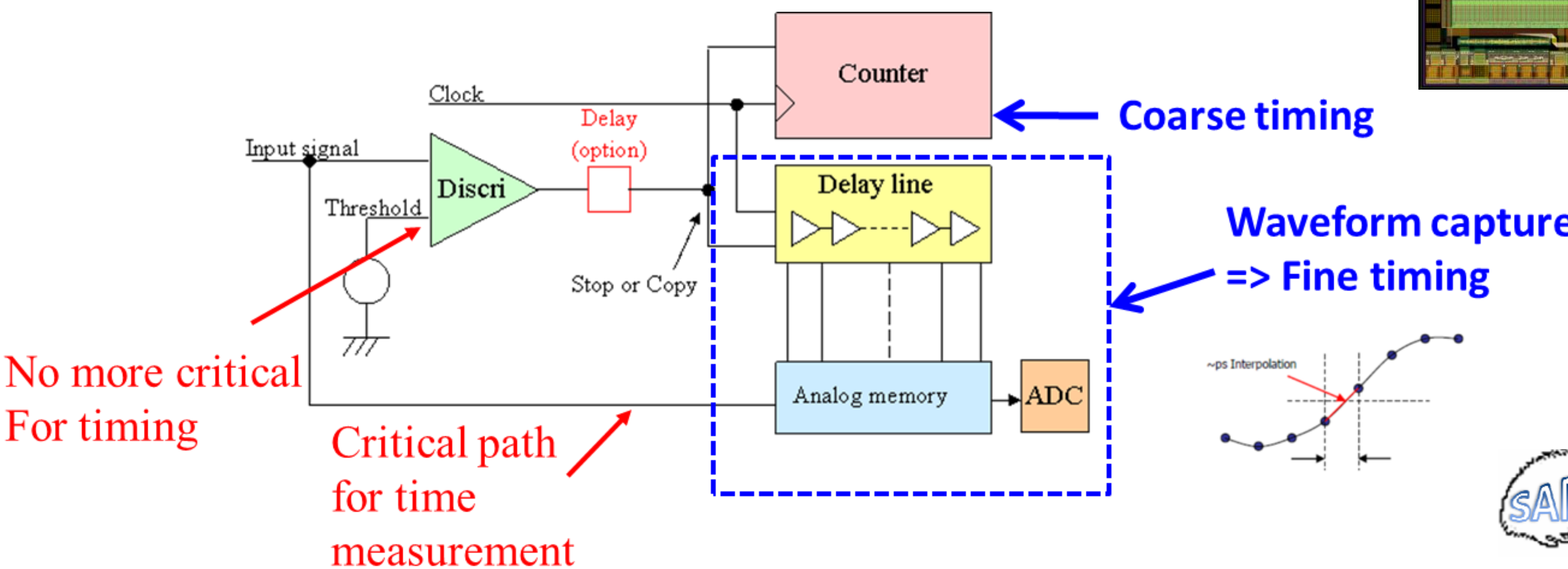


Continuing R&D: SAMPIC, the 5-ps WTDC

➢ Waveform TDC: works on **analog** signals !

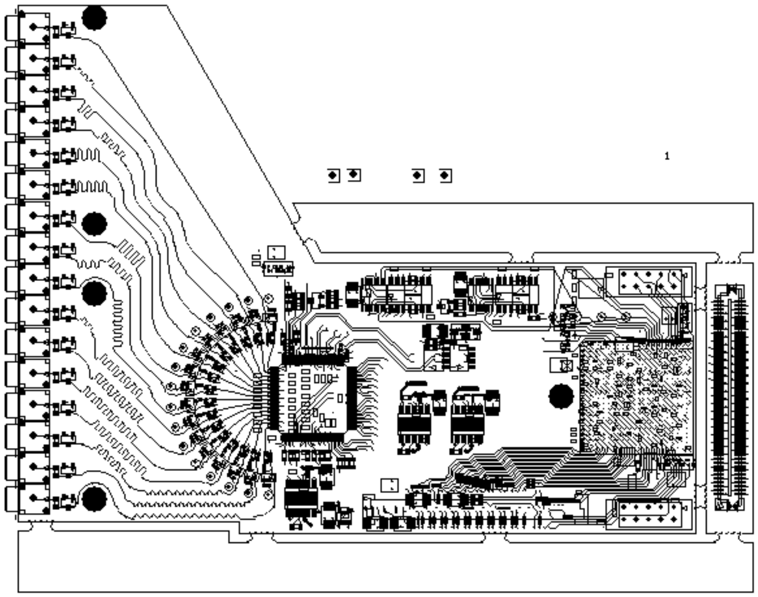
- Time :
  - Coarse = timestamp counter
  - Middle = DLL based TDC to define Zone of interest
  - Fine = few samples in the ZOI of the waveform.
- Waveform Shape, Charge, Amplitude available





More about SAMPIC

- We moved to AMS CMOS 0.18µm technology
- First version will house 16 blocks each with 64 analog memory cells
  - ⇒ Sampling is performed at **10GS/s** or less (standard main clock is **160 MHz**)
  - ⇒ Signal bandwidth is ~ **1 GHz**
- Digitization will be performed inside the chip with a parallel 8/11-bit Wilkinson ADC running at 2 GHz in each cell => conversion time < 1µs for the whole chip
  - ⇒ The 2-GHz clock is not distributed to the cells but runs a unique gray counter
  - ⇒ The cells house a fast comparator and a latch
- The chip is ready to be integrated in a system
  - ⇒ Smart trigger configuration
  - ⇒ Data Readout with channel priority management
  - ⇒ High rate serial differential outputs (14 diff lines)
- The chip was submitted last February
  - ⇒ First tests should take place in May
- Test setup is almost ready
  - ⇒ The chip will be mounted on stackable mezzanine board compatible with both LAL and CAEN motherboards
  - ⇒ It will benefit from former smart developments of firmware and software



Conclusion

- The **2-channel USB Wave Catcher** module is already used worldwide, together with the software we developed.
  - It offers our most advanced software measurement tools
- The **16-channel board** is already used on different detector test benches, and will soon equip high-scale experiments.
  - We are still developing its firmware
- The **64-channel system** will be a great tool for multi-channel detector characterization
  - We are currently working on its software (USB-based)
  - Next step is **UDP with integrated flow control**
- If things go well, the new multi-channel **SAMPIC WTDC** should soon propose both **5-ps timing** and **signal waveforms** …
  - First results this summer

- Our current main axis of effort for ASIC R&D: still increasing the **time precision** and the **hit rate capability** …