SRS-ATCA design status

Wojciech Jalmuzna
on behalf of SRS-ATCA design team

eicSys GmbH
Embedded Integrated Control Systems

Agenda

- Scalable Readout System in an ATCA shelf
- ATCA back-plane regions
- SFEC-ATCA board changes
- SFEC-ATCA board schematics, pcb and view
- First prototype system and project time-line

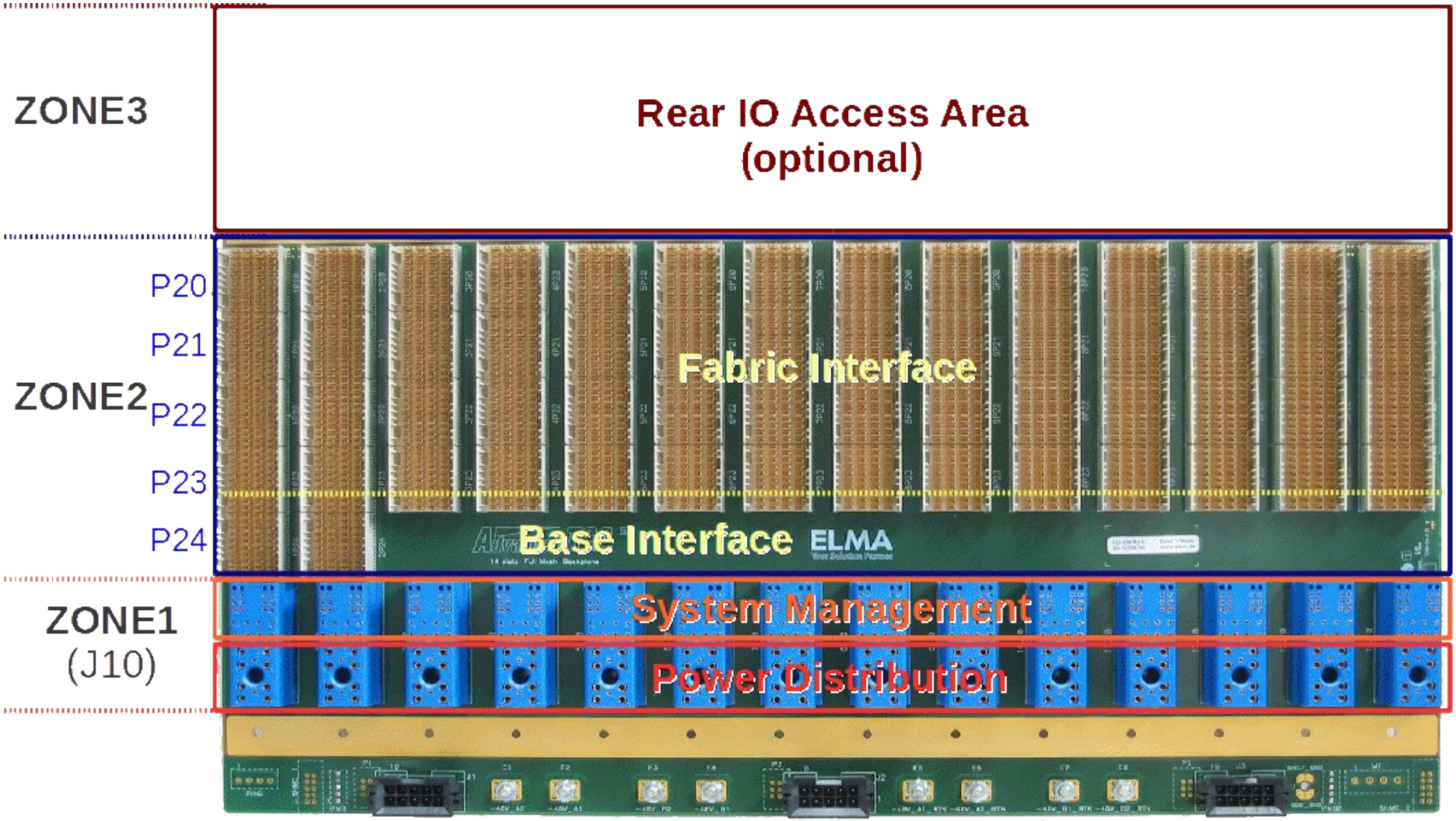
Scalable Readout System in an ATCA shelf

- ATCA offers suitable infrastructure for SRS
  - Back-plane - compact system, connection over backplane
  - Front panel - space for many connectors
  - Read IOs (RTM) – additional space for connectors
- There is an option for various system sizes
  - 14 slot ATCA (up to 86016 channels)
  - 5 slot ATCA (up to 61440 channels)
  - 2 slot ATCA (up to 12288 channels)
  - mTCA systems

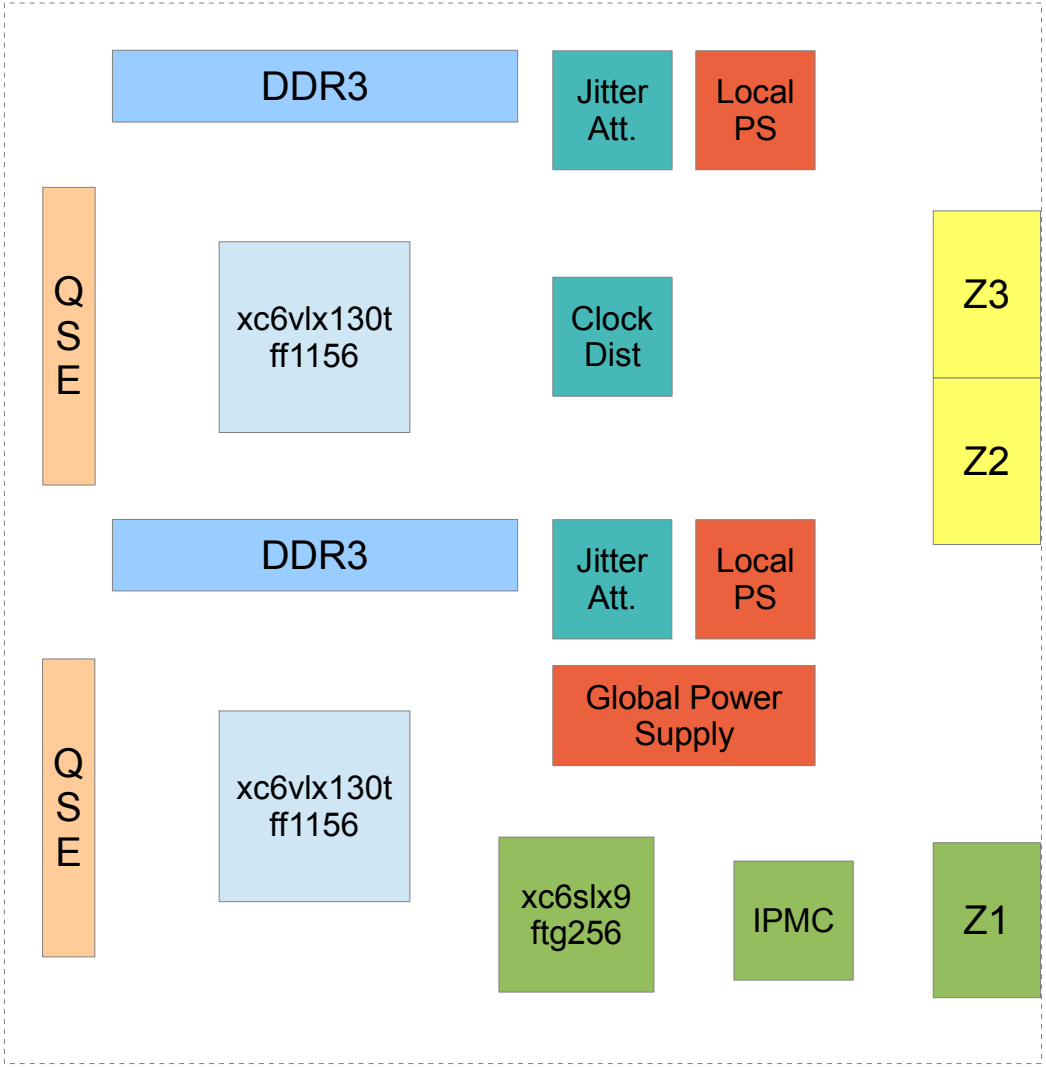
Scalable Readout System in an ATCA shelf

- Up to 11 FEC Boards in the shelf
- 1 SRU Board per shelf
- Connection over standard back-plane
  - p2p gigabit links between FEC and SRU
  - no external cables (maintenance, assembly)
- Scalable (1-board or many shelfs)
- Optical and/or Ethernet between shelfs
- High performance CPU in the crate (optional)
- In-built remote management and diagnostic (IPMC)

ATCA backplane regions

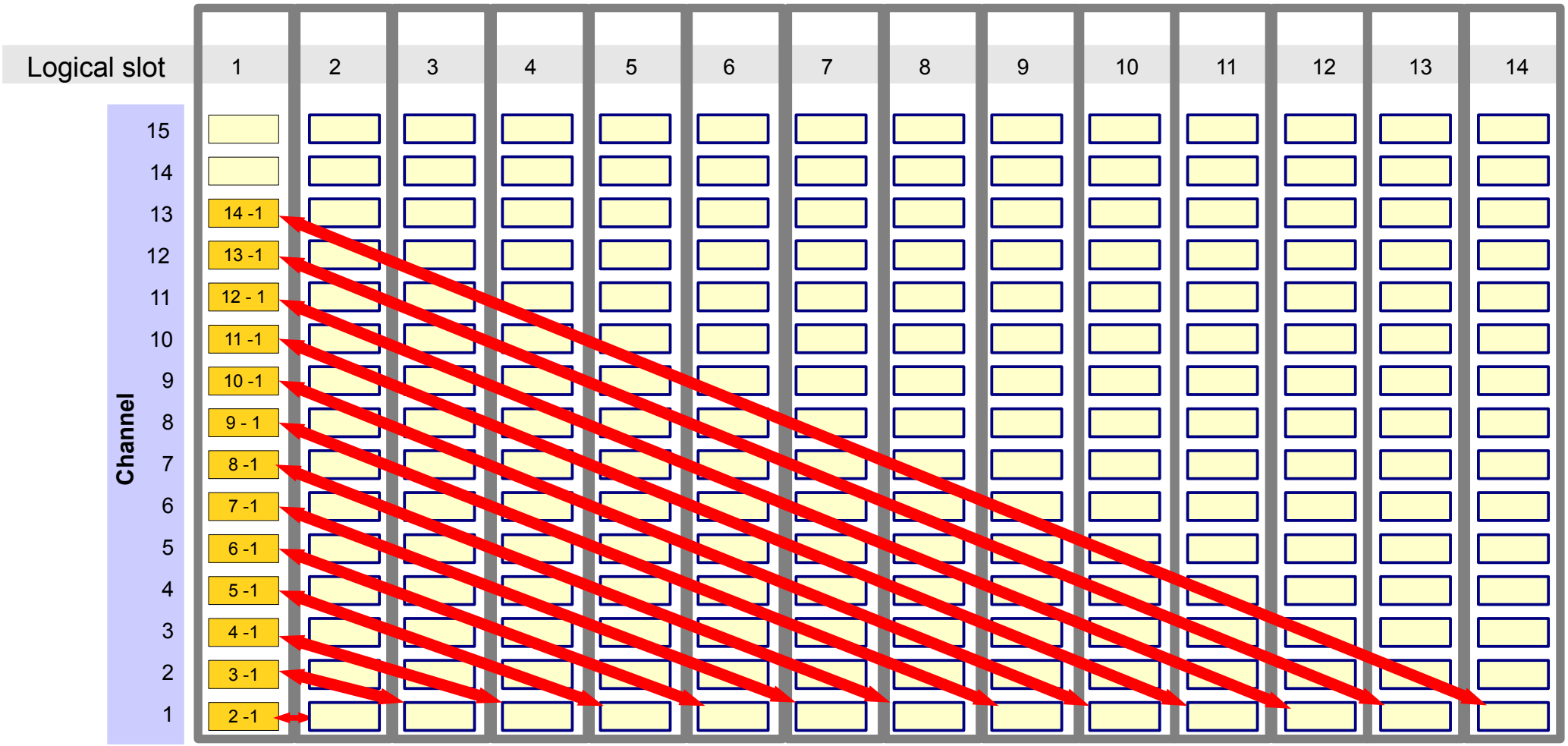


SFEC-ATCA changes summary

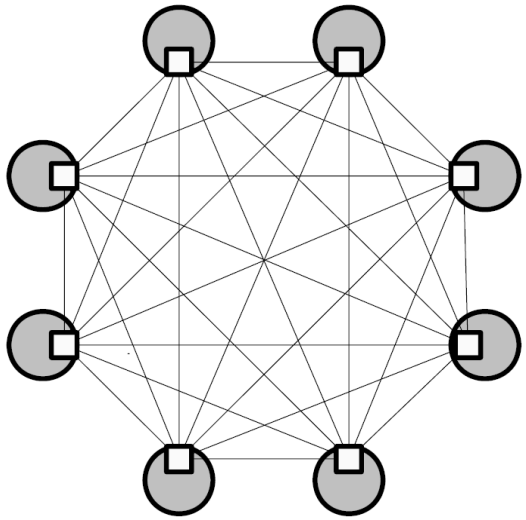


- FPGA changed to bigger one
- Gigabit link number increased – switching possible to get 10GB connectivity to SRU
- Power requirements increased → supply part divided into local and global
- Clock distribution changed
- Additional jitter attenuators added

ATCA back-plane configuration

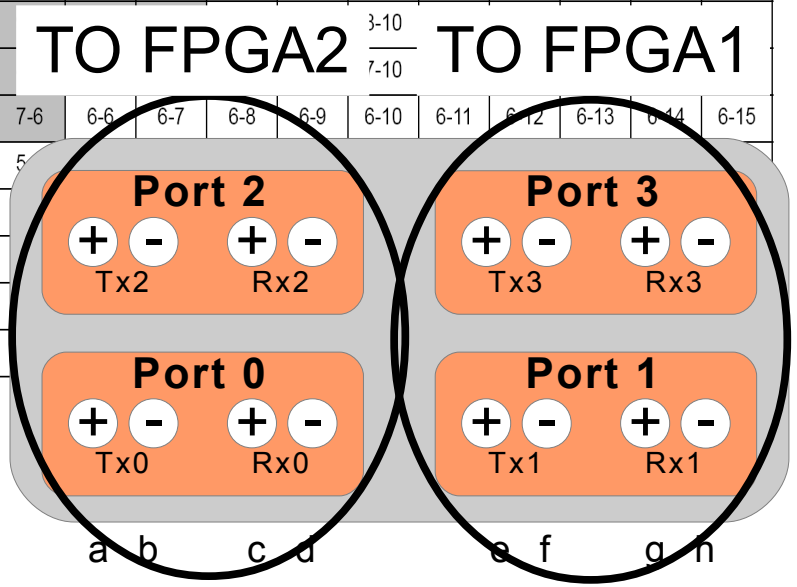


ATCA back-plane configuration

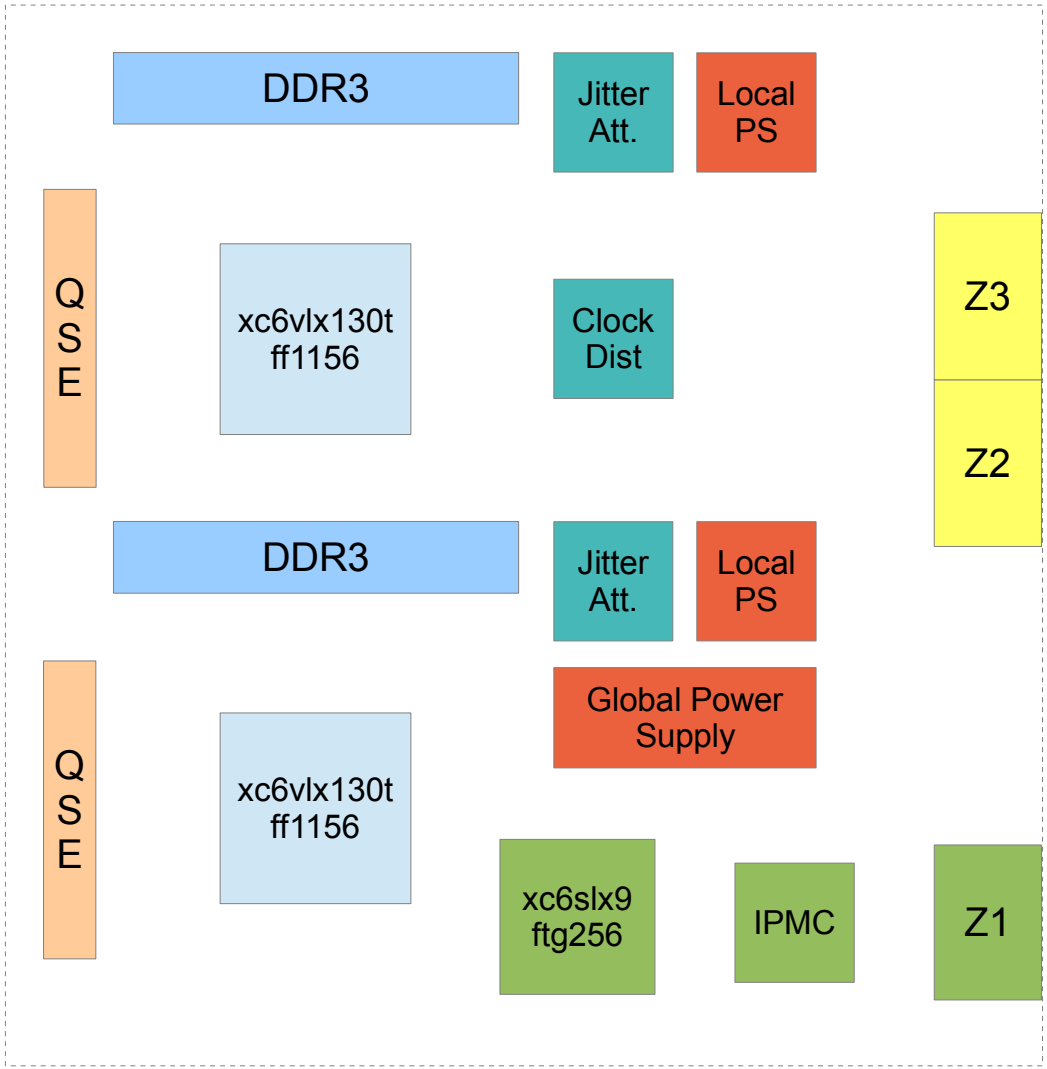


8 LVDS pairs to each slot

Connector	Logical Slot # / Channel #	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
P20	15	16-1	16-2	16-3	16-4	16-5	16-6	16-7	16-8	16-9	16-10	16-11	16-12	16-13	16-14	16-15	15-15
P20	14	15-1	15-2	15-3	15-4	15-5	15-6	15-7	15-8	15-9	15-10	15-11	15-12	15-13	15-14	14-14	14-15
P20	13	14-1	14-2	14-3	14-4	14-5	14-6	14-7	14-8	14-9	14-10	14-11	14-12	14-13	13-13	13-14	13-15
P21	12	13-1	13-2	13-3	13-4	13-5	13-6	13-7	13-8	13-9	13-10	13-11	13-12	12-12	12-13	12-14	12-15
P21	11	12-1	12-2	12-3	12-4	12-5	12-6	12-7	12-8	12-9	12-10	12-11	11-11	11-12	11-13	11-14	11-15
P21	10	11-1	11-2	11-3	11-4	11-5	11-6	11-7	11-8	11-9	11-10	10-10	10-11	10-12	10-13	10-14	10-15
P21	9	10-1	10-2	10-3	10-4	10-5	10-6	10-7	10-8	10-9	9-9	9-10	9-11	9-12	9-13	9-14	9-15
P21	8	9-1	9-2	9-3	9-4	9-5											
P22	7	8-1	8-2	8-3	8-4	8-5											
P22	6	7-1	7-2	7-3	7-4	7-5	7-6	6-6	6-7	6-8	6-9	6-10	6-11	6-12	6-13	6-14	6-15
P22	5	6-1	6-2	6-3	6-4	6-5											
P22	4	5-1	5-2	5-3	5-4	4-4											
P22	3	4-1	4-2	4-3	3-3	3-4											
P23	2	3-1	3-2	2-2	2-3	2-4											
P23	1	2-1	1-1	1-2	1-3	1-4											

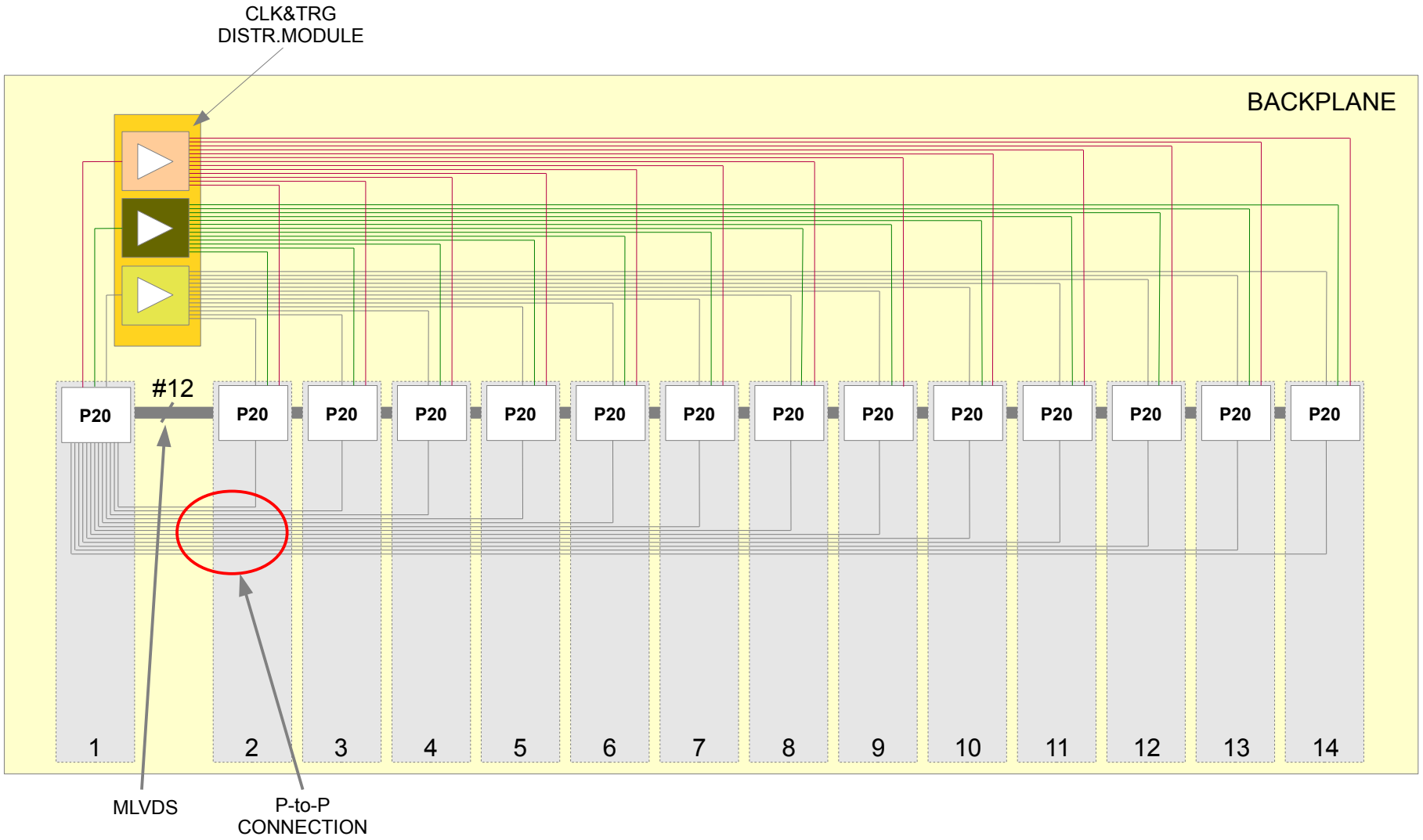


SFEC-ATCA changes summary

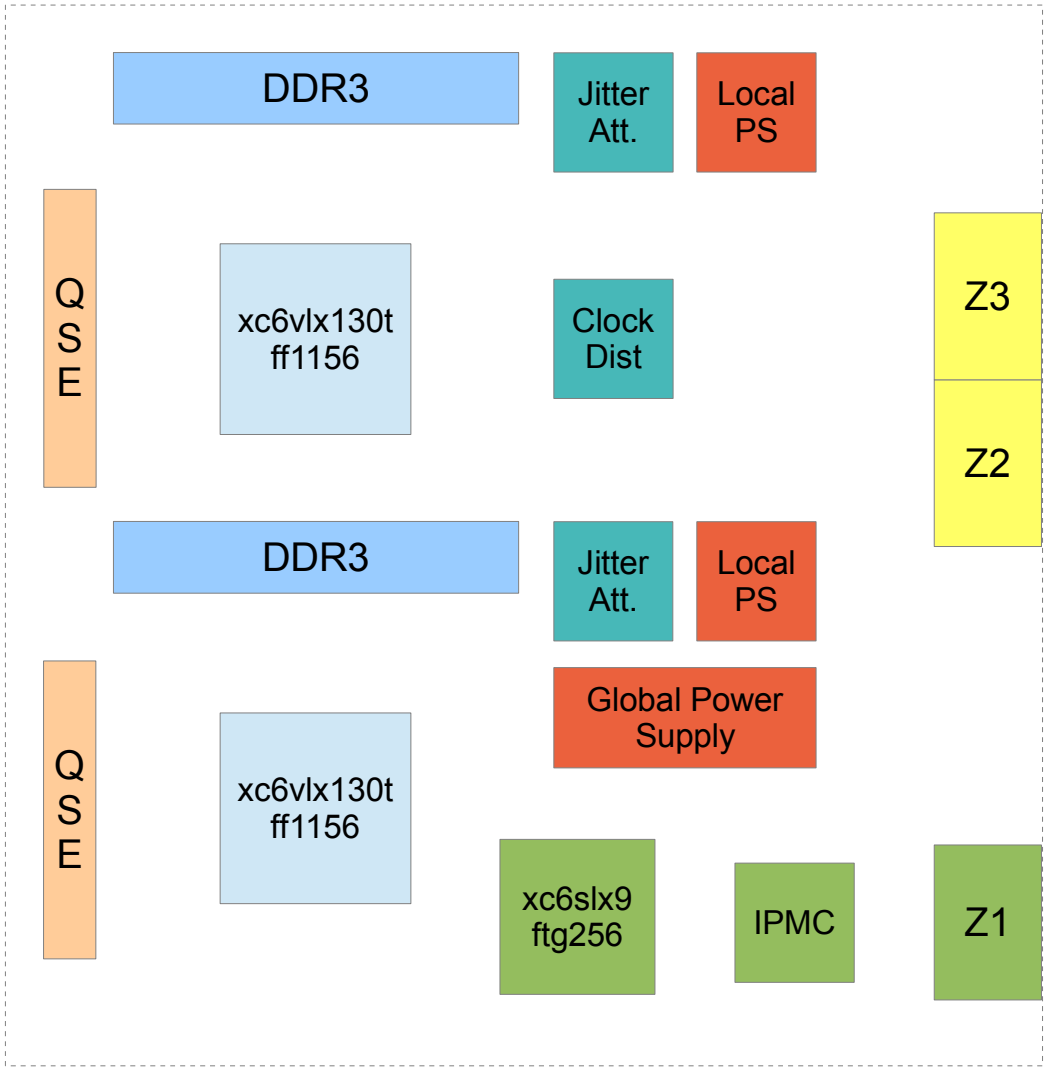


- FPGA changed to bigger one
- Gigabit link number increased – switching possible to get 10GB connectivity to SRU
- Power requirements increased → supply part divided into local and global
- Clock distribution changed
- Additional jitter attenuators added
- **Full mesh connectivity adaptation**

Timing distribution - AXIe standard

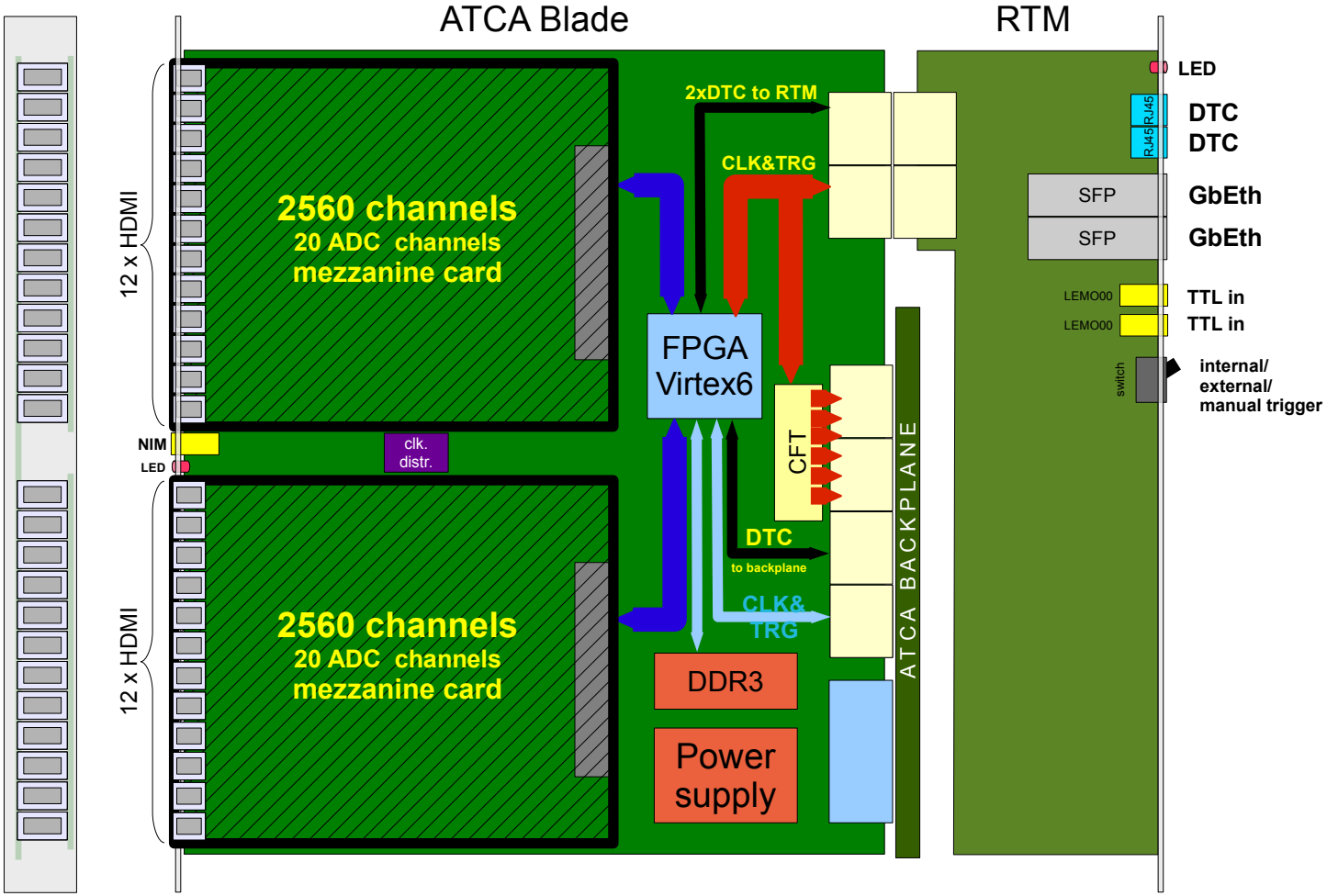


SFEC-ATCA changes summary



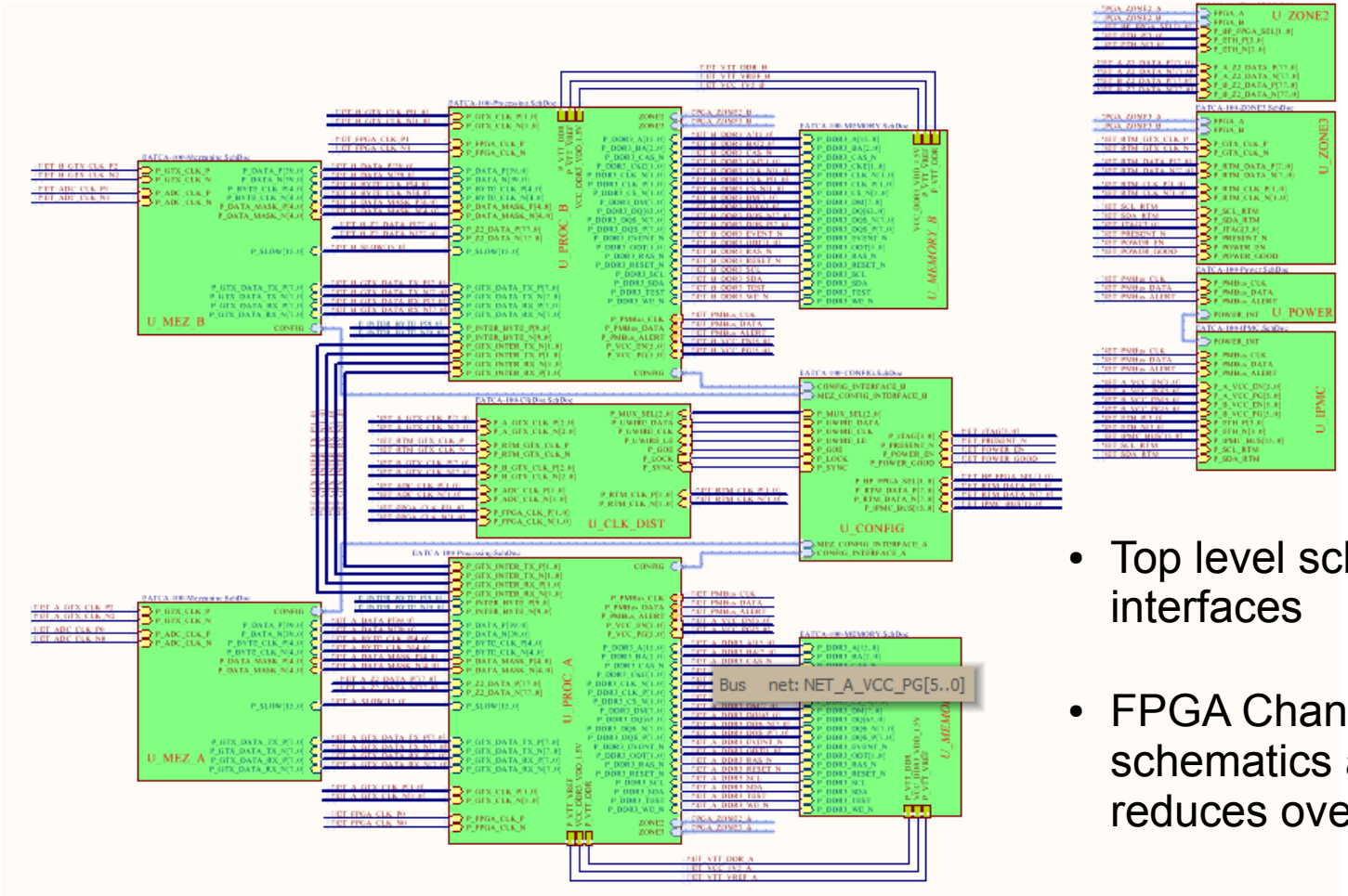
- FPGA changed to bigger one
- Gigabit link number increased – switching possible to get 10GB connectivity to SRU
- Power requirements increased → supply part divided into local and global
- Clock distribution changed
- Additional jitter attenuators added
- Full mesh connectivity adaptation !
- **Z3 custom back-plane removed - AXIe standard adapted**

SFEC-ATCA board initial plans



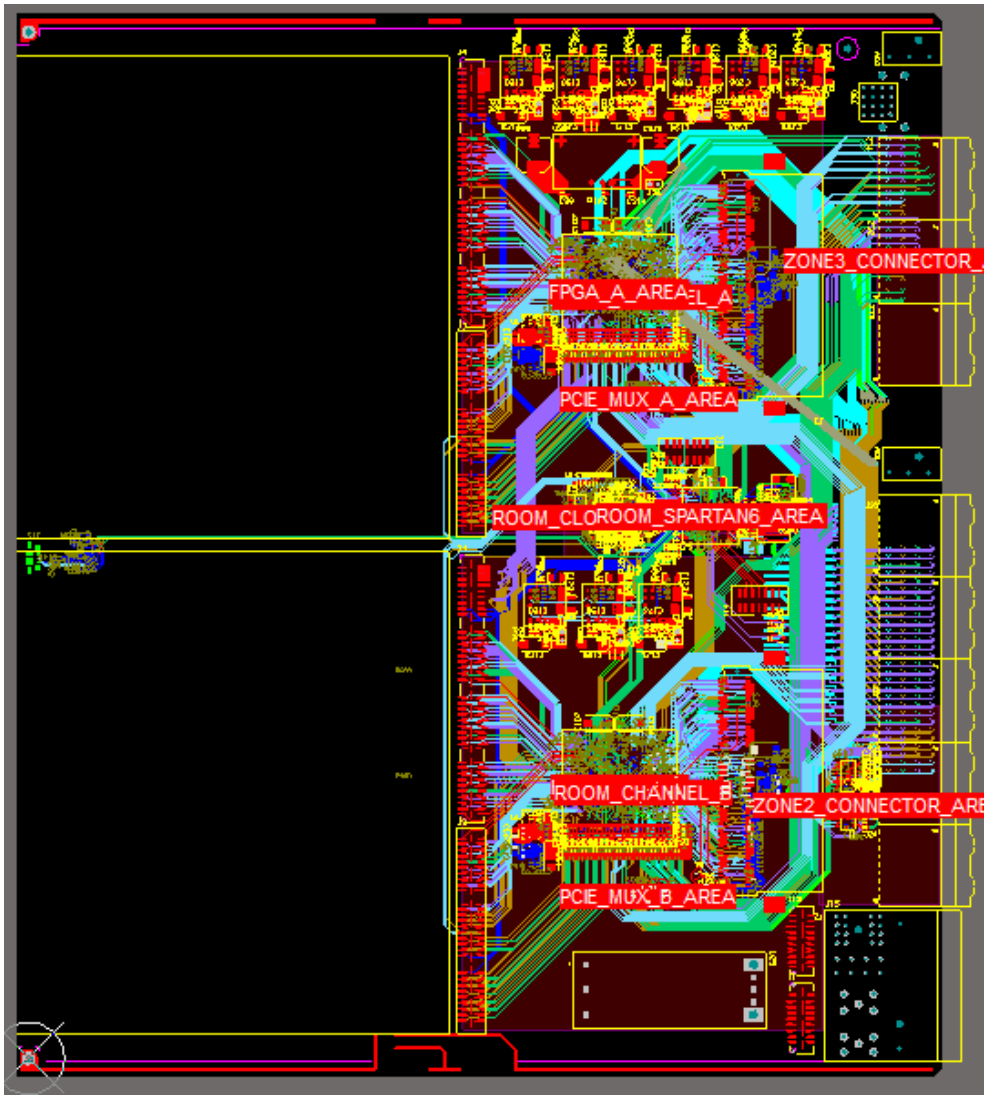
- 2 ADC mezzanine cards
- RTM to provide IO interfaces (compatible to existing SRU)
- Clk, trg and DTC links over backplane
- Single Virtex 6 based
- DDR3 memory

SFEC-ATCA board schematics



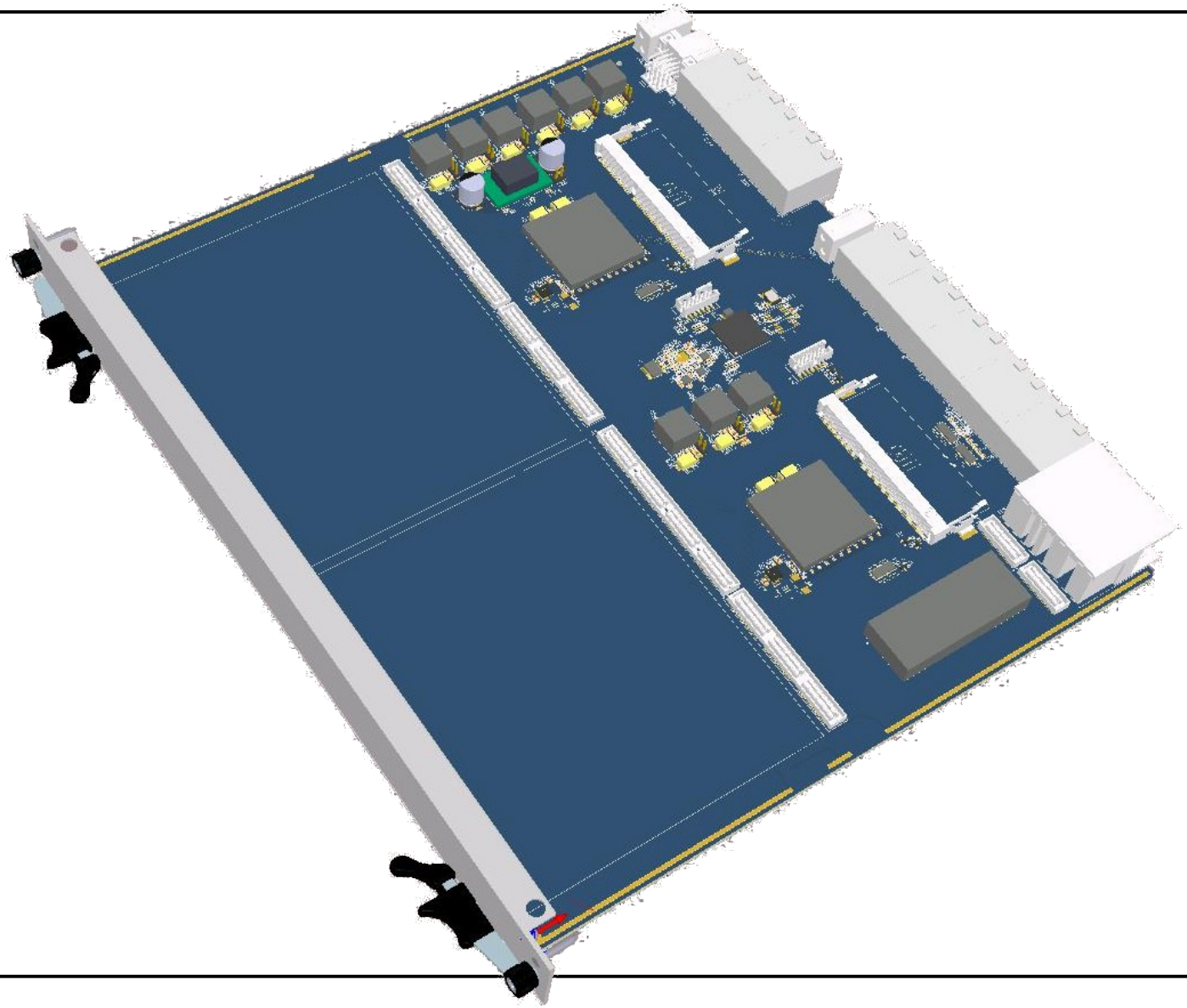
- Top level schematic view defines all interfaces
- FPGA Channels are reused – schematics and routing can be copied – reduces overall routing effort
- Review of schematics in progress

SFEC-ATCA board PCB



- 14 layers (**change from 12**)
- Final component placement
- Power plane routing finished
- Some length tuning must be done
- Routing of full-mesh connectivity in progress
- Slow management signals not routed

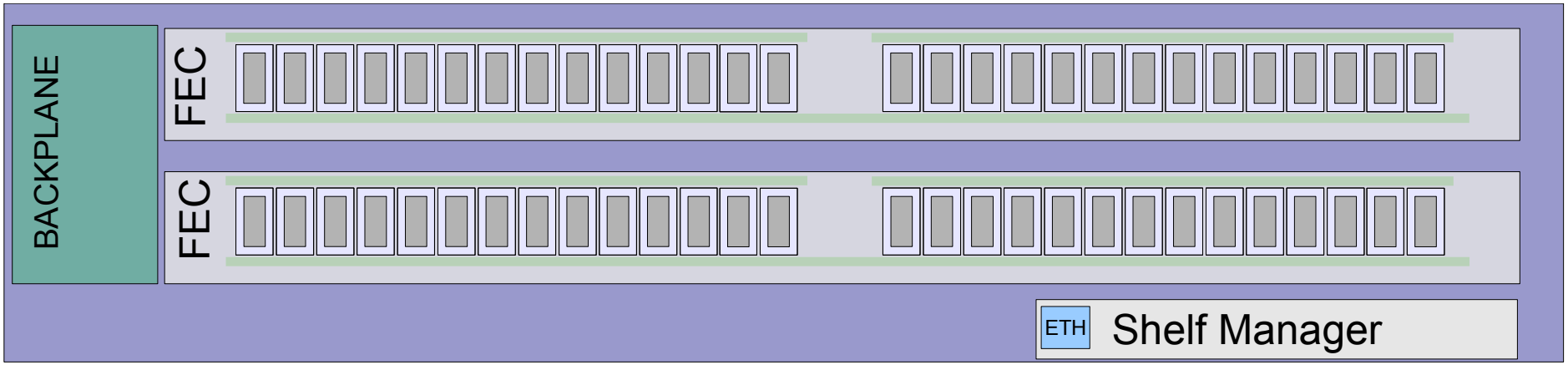
SFEC-ATCA board view



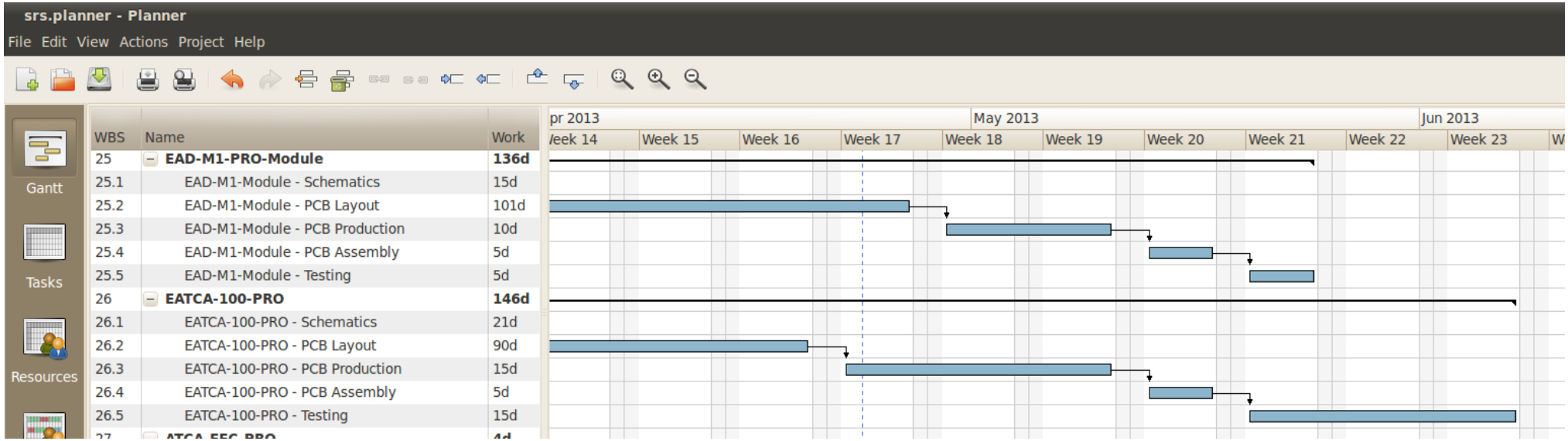
First prototype system

- **2** FEC-ATCA blades
- **2** RTM modules **(simplified)**
- **96** ADC channels in shelf
- **12288** channels per shelf

ATCA backplane used for power distribution, **inter-board connectivity** and platform management. Compatible to existing SRU modules.



Project time-line



Thank you for your attention