Progress report on the FECv6 classic routing in Bari

Layouter: Raffaele Liuzzi

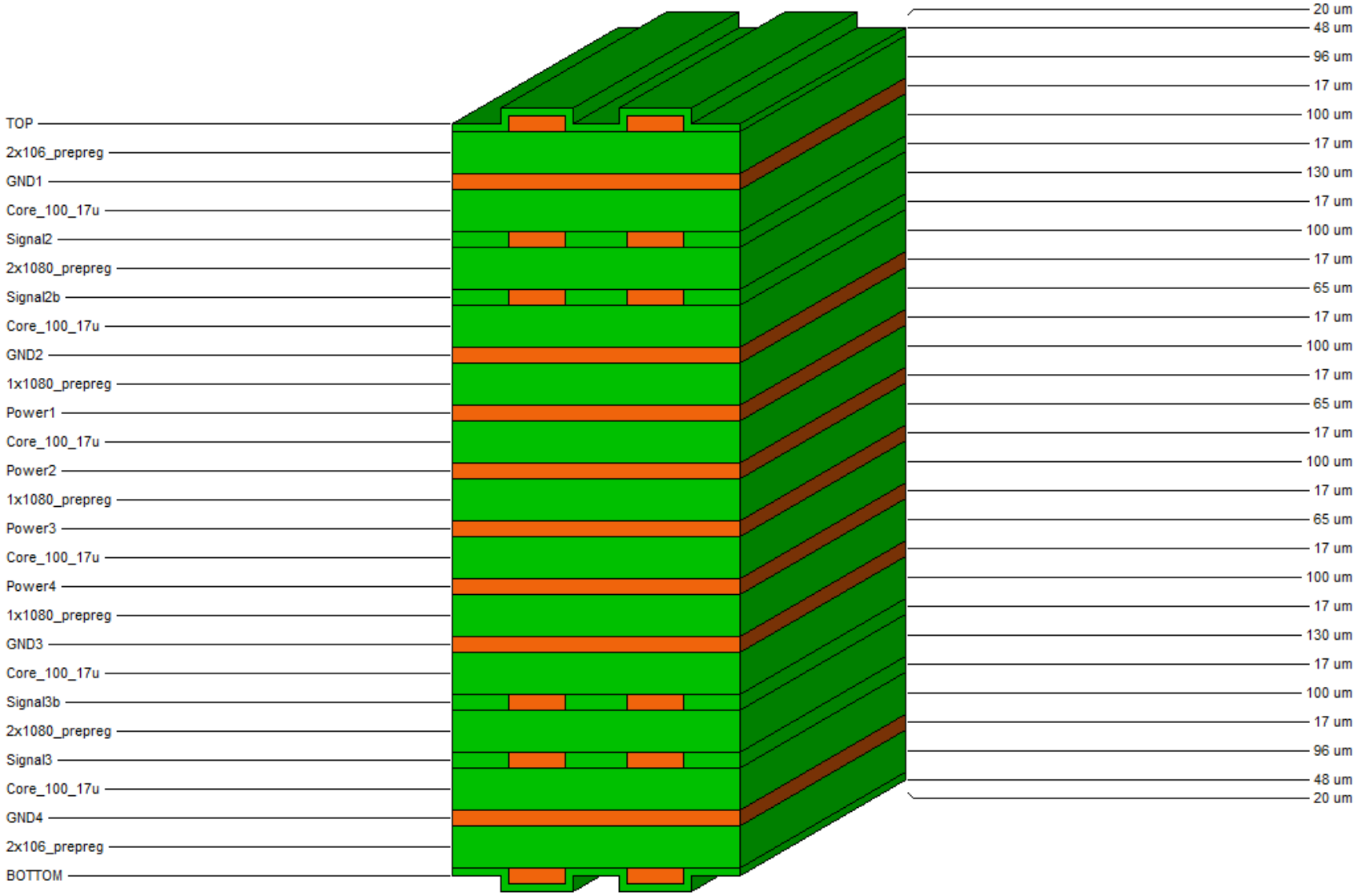
Slide #2: modified stack-up. Raffaele informed me that he needs 4 full planes for power distribution. So, I modified the stack-up to 14 layers. I've verified that the required material thicknesses are in stock at LabCircuits and that the structure can be built. I informed him on what signal widths he should use for external and internal layers, single-ended and differential routing.

Slide #3: snapshot of his board file early this morning (22nd April). He has routed so far half of the DDR3 data bus. He's swapped several data lines, according to the basic rules (you can swap data lines inside a byte boundary and you can swap address and control lines). But he also moved a couple of DQS diff pairs…I have to check if this is valid. Note that he's ruted parallel lines in adjacent layers, what may imply corsstalk (I have to simulate it). He told me he would route today the rest of the DDR3 data lines.

Slide #4: Raffaele has also worked on the power distribution planes.

Well, I think we can discuss the progress sometime tomorrow.
Best,
curro

Layer Stackup. Design: stackup14_FECv6_Nelco.ffs.
HyperLynx LineSim v8.1.1



Total thickness = 1587 um