INTEGRATION OF THE SCALABLE READOUT SYSTEM (SRS) IN THE TOTEM DAQ

TOTEM DATA ACQUISITION GROUP

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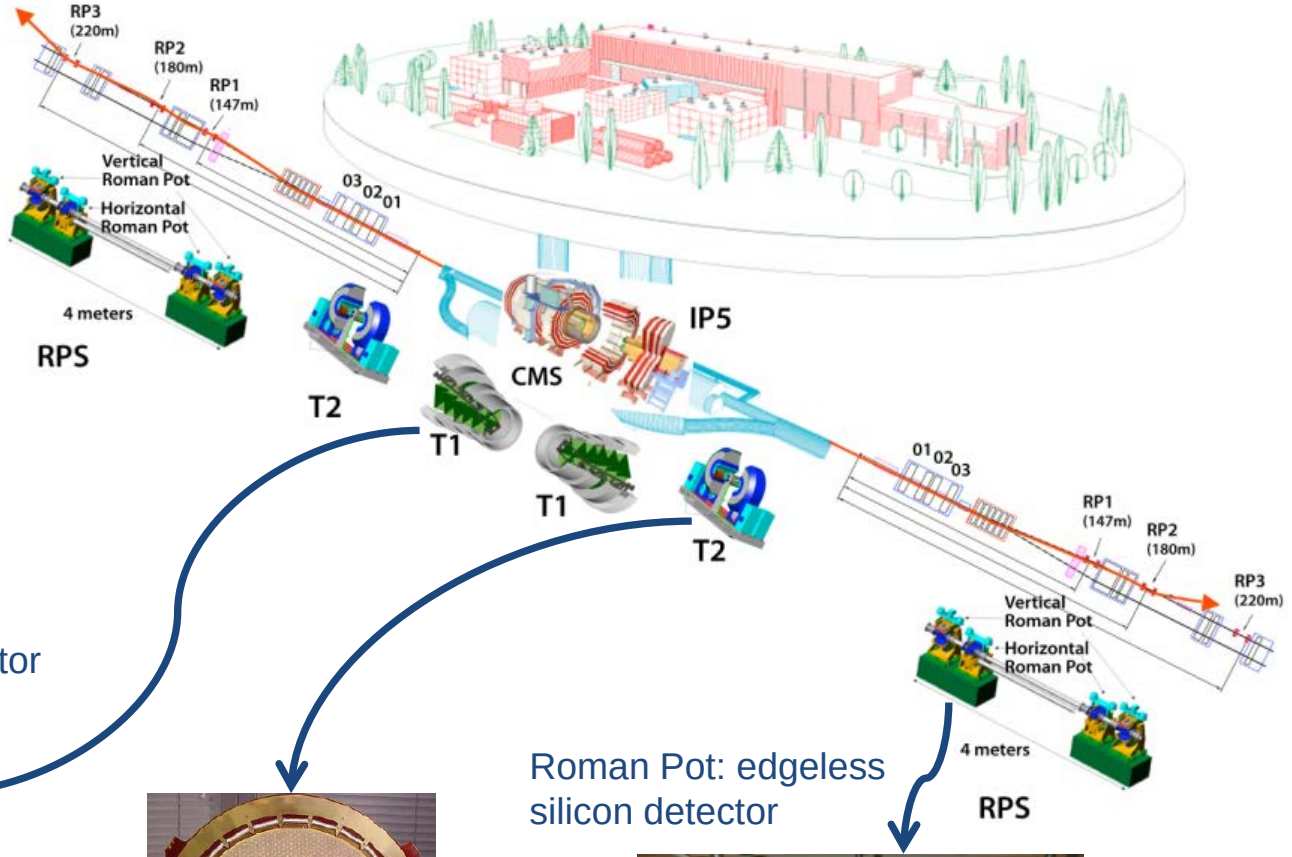
Outlines

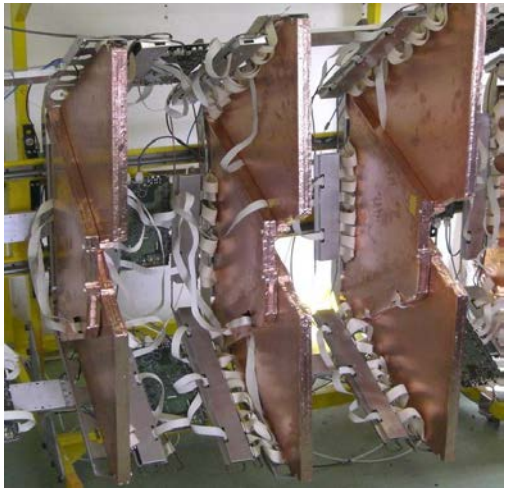
- Totem Experiment at LHC;
- The Current Totem DAQ System architecture;
- Consolidation of the TOTEM DAQ System with SRS;
- Opto-Fec (C-card) Design and Test;
- Firmware design status;
- Firmware simulation and testbenches;
- First results of detector readout at the LHC Interaction Point;
- Outlooks and future work.

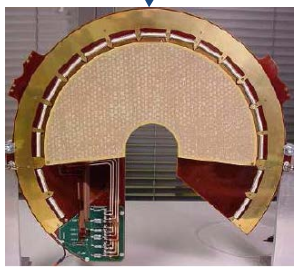
TOTEM Experiment at LHC

- TOTEM measures total p-p cross section at the LHC energies and studies diffractive processes.
- TOTEM adopts three detectors symmetrically placed at the Interaction Point 5 (T1, T2, Roman Pot).
- All TOTEM detector adopts common readout and trigger electronics. The VFAT chip provides readout and trigger capabilities.



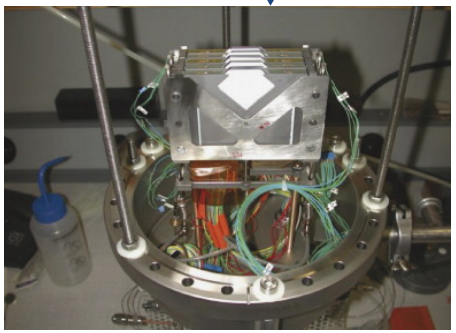
T1: Cathode Strip Chamber detector



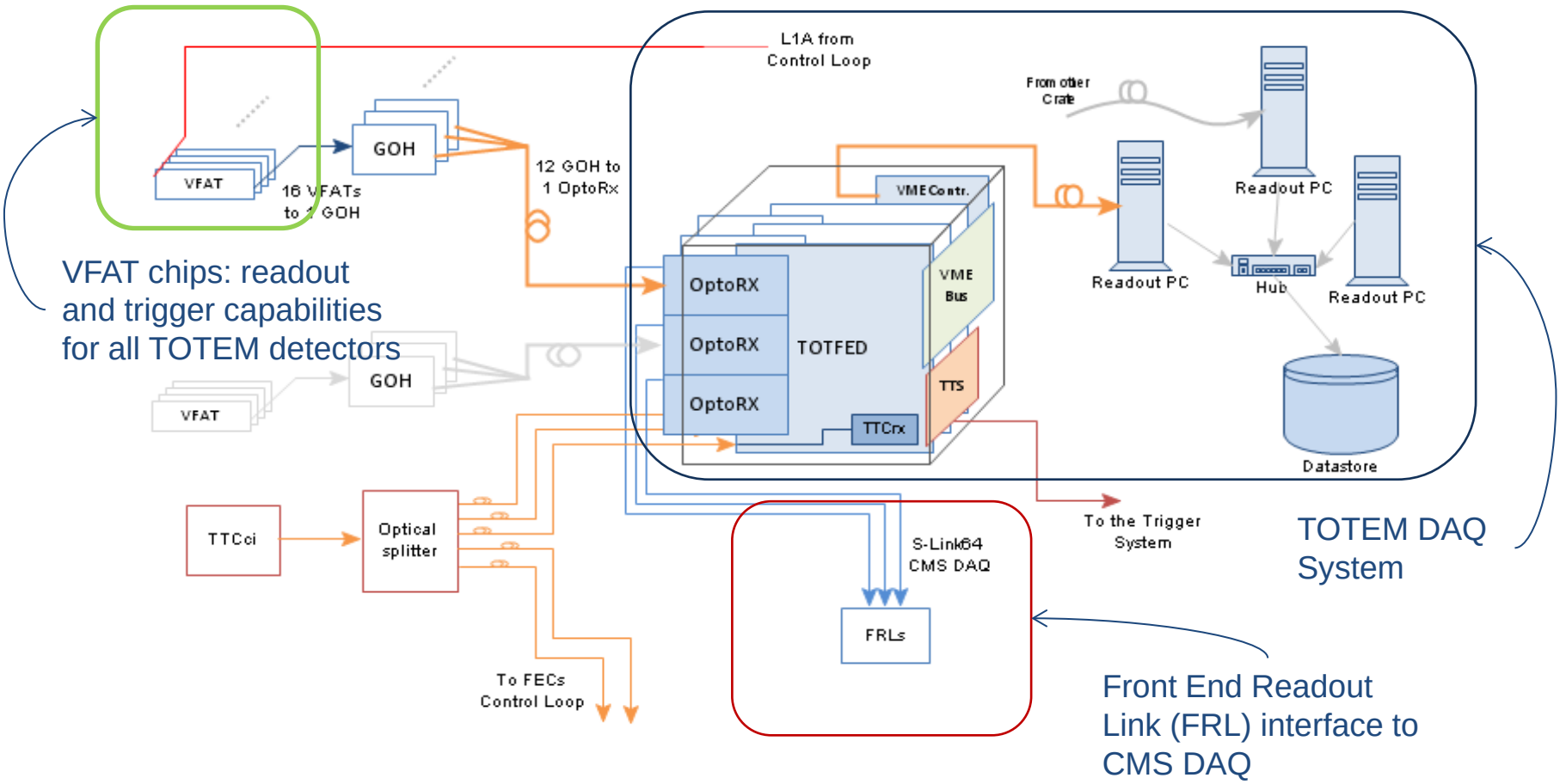


T2: triple GEM detector

Roman Pot: edgeless silicon detector



The Current TOTEM DAQ System Architecture



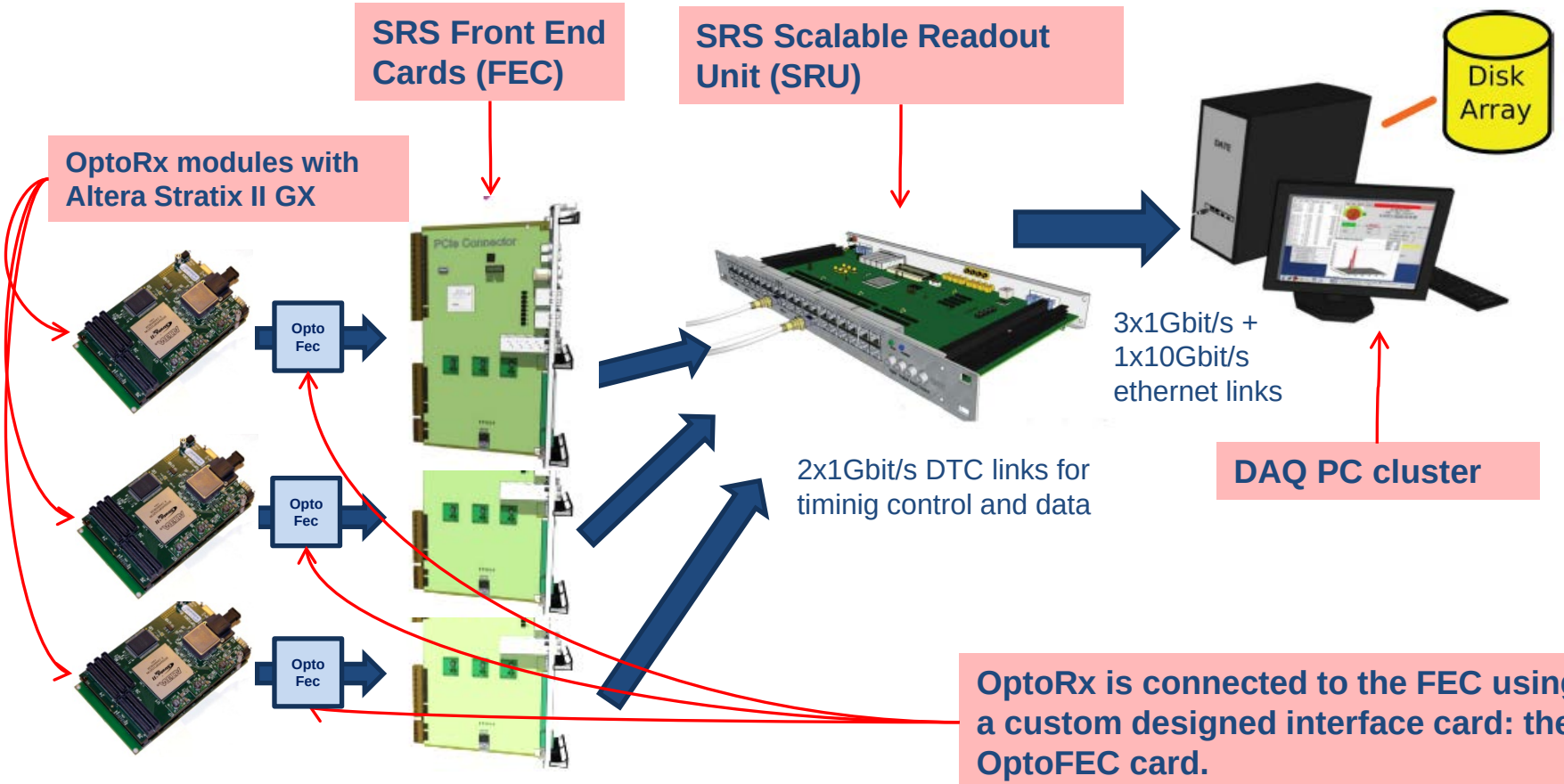
VFAT chips: readout and trigger capabilities for all TOTEM detectors

TOTEM DAQ System

Front End Readout Link (FRL) interface to CMS DAQ

- In the TOTEM standalone configuration, the VME bus bandwidth limits the trigger rate to 1kHz.

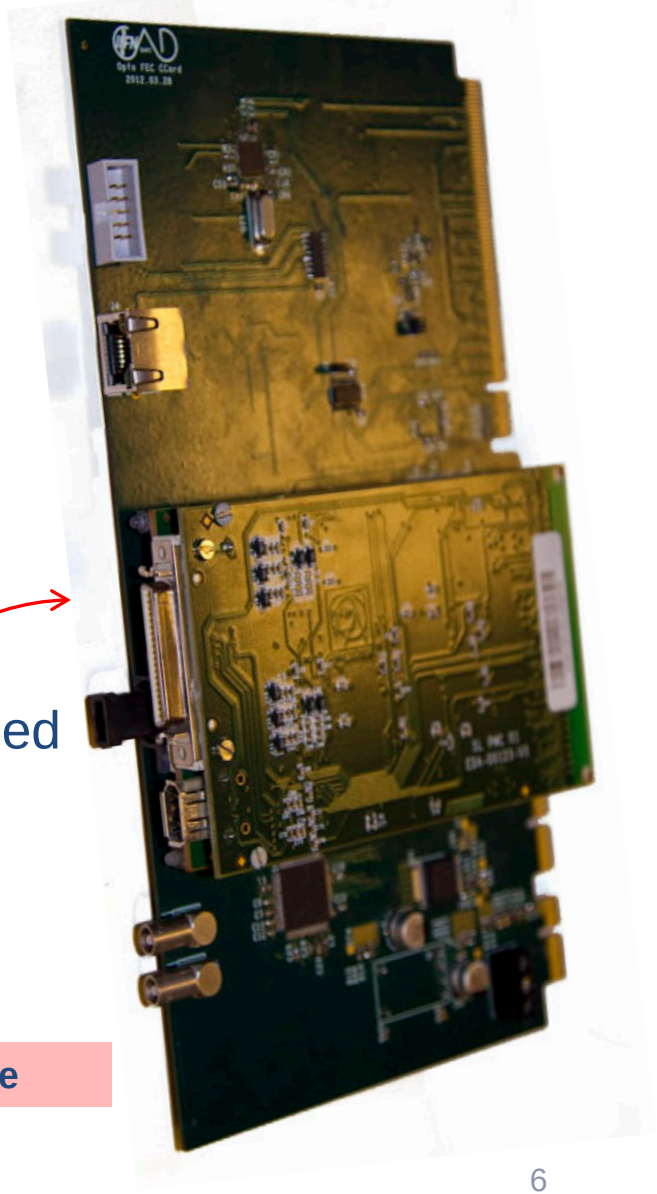
Consolidation of TOTEM DAQ with SRS System



- SRS Provides a cost effective alternative to the present VME based solution.
- SRS offers many possibilities of implementing data reduction and filtration by leveraging the SRS resources at different stages in the DAQ chain.

OptoFec Card Design and Test

- OptoFEC card was designed:
  - 8 LVDS@672MHz channels,
  - Full-Duplex 2Gbps SERDES (TLK2501),
  - Clock generator/Jitter cleaner,
  - 32-bit parallel bus,
  - Timing Trigger and Control (TTC) interface,
  - I2C bus for configuration,
  - Trigger Throttling System (TTS) support,
  - JTAG support,
  - Independent power supply mode.
- The OptoFEC card first prototype was produced and tested:
  - Electrical test was passed,
  - Parallel bus test was passed,
  - I2C bus test is on-going.



OptoFEC card and OptoRX mezzanine

Firmware Development

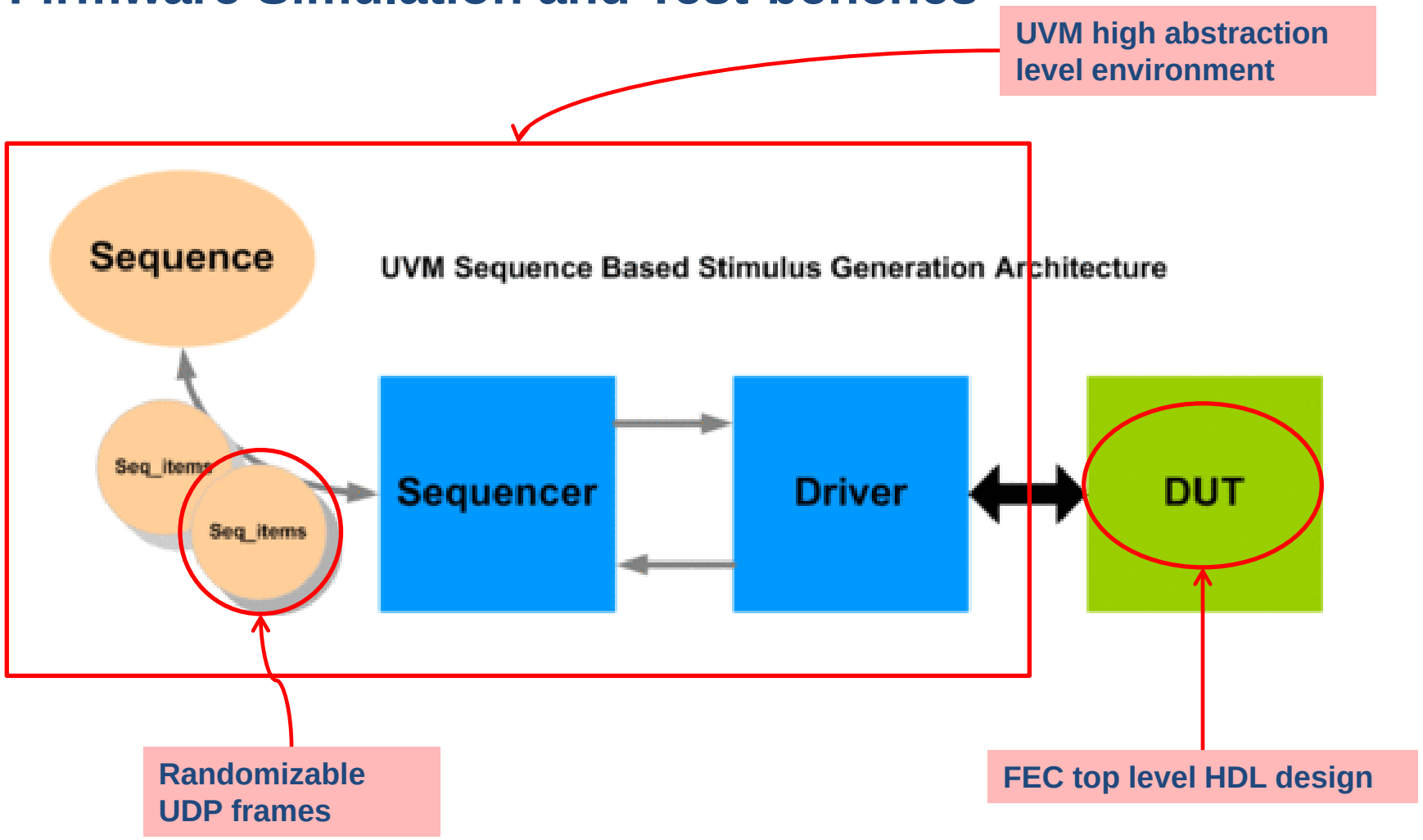
- FEC Firmware has been developed to receive OptoRX data frames over OptoFec card parallel bus.
- For the time being we send 1event for each UDP frame. Event size is ~5kByte
- SRU module has been connected to the LHC TTC system (TTCci).
- Clock and trigger distribution from SRU to FEC and OptoRx was developed and tested.
- A I2C slave controller is under test. It allows OptoRx module configuration and monitoring sending UDP control frames to the FEC. I2C slave controller is based on OpenCore blocks available at opencores.org

Firmware Simulation and Test-benches

- SRS firmware project is complex, it involves several interfaces and functional blocks.
- Development and test has to take into account interconnection and interactions between various blocks.
- Standard VHDL/Verilog test-bench complexity can easily diverge.
- Users tend to develop a test-bench for each functional block and write few test cases.

- We adopted the SystemVerilog language combined with Universal Verification Methodology (UVM) to fully test the FEC firmware design, both System part and User part, in a single simulation.
  - Complex test vectors are handled by UVM verification IP cores (Ethernet, I2C),
  - High level abstraction of SV allows easy test-bench creation,
  - SV and UVM offer constrained random verification, design can be fully tested to find corner case problems, designer does not need to write test cases by himself.

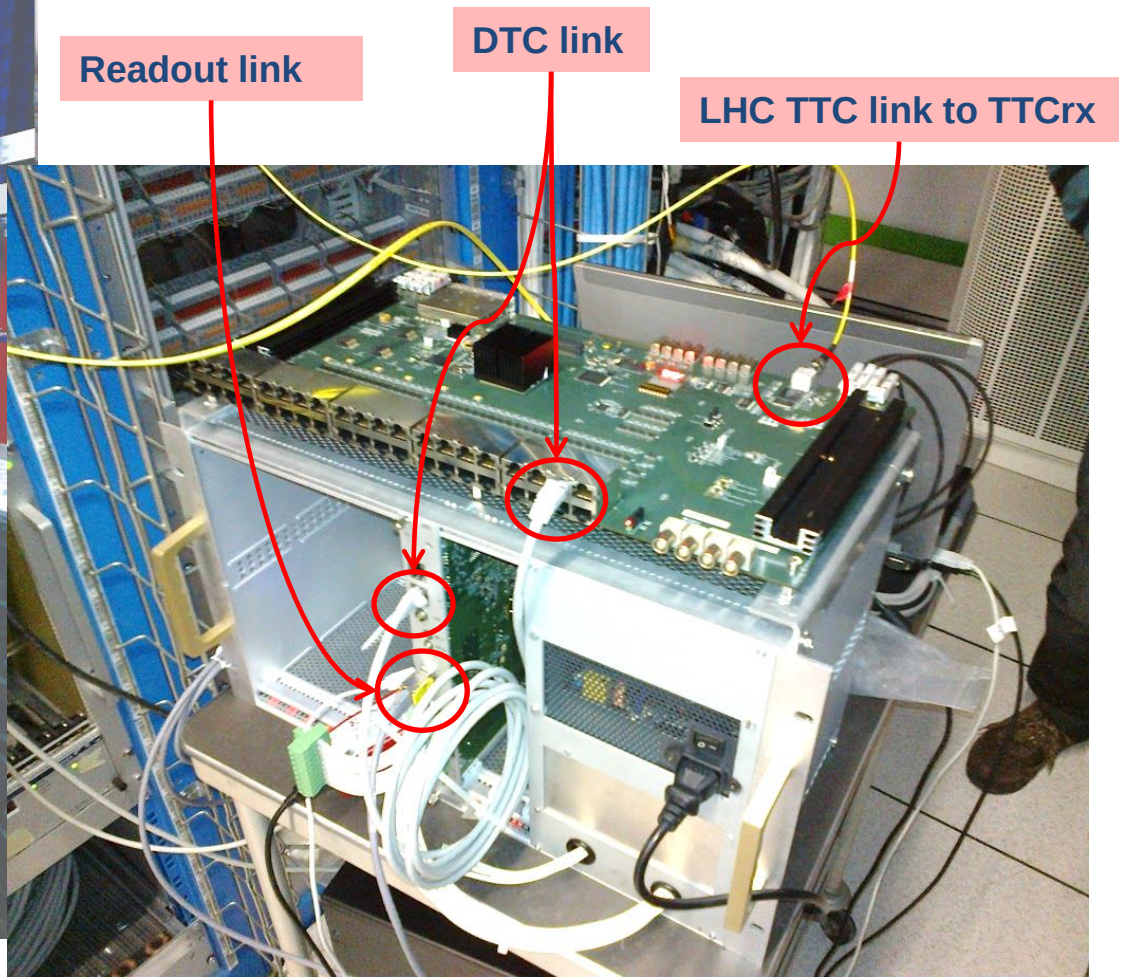
Firmware Simulation and Test-benches



First results of detector readout at the LHC Interaction Point

- During the last LHC p-Pb campaign we took data reading out one FEC card with its OptoRX (3 full Roman Pot)
  - 2 million events were readout and stored using a stand alone readout PC,
  - Performances are encouraging: 10kHz of trigger rate were reached,
  - Readout limited by SATA drive,
  - Data throughput still beyond FEC link capability (50MByte/s), but without backpressure,
  - No data transmission error were detected checking CRC codes at different level in our data frames (OptoRX frame, VFAT frame).
- First test results were fully satisfactory: an important milestone was reached!

On field test at Interaction Point 5



Outlooks and future work

- Optimize FEC firmware design, possibly introducing standard interfaces (i.e.: AMBA AXI4-Stream bus);
- Test back pressure algorithm over Ethernet links (we wait for a mature release form A.Tarazona);
- Reach maximum link speed with data storage;
- Implement full TTC signal distribution SRU -> FECs -> OptoRXs;
- Fully implement DTC links as soon as mature release will be available;
- Test OptoFEC serial interface to evaluate a future version with 2 OptoRX for each FEC.

Thank you for your attention!