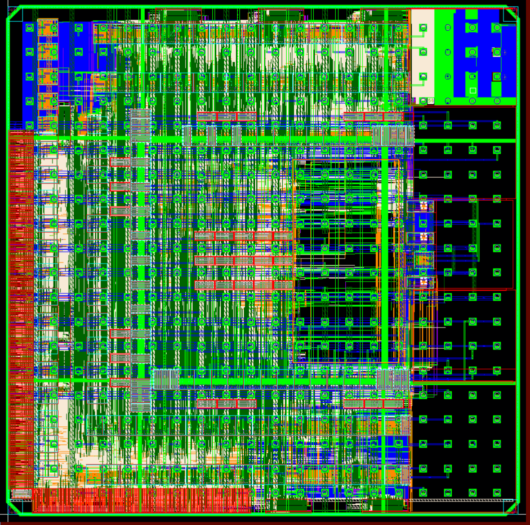

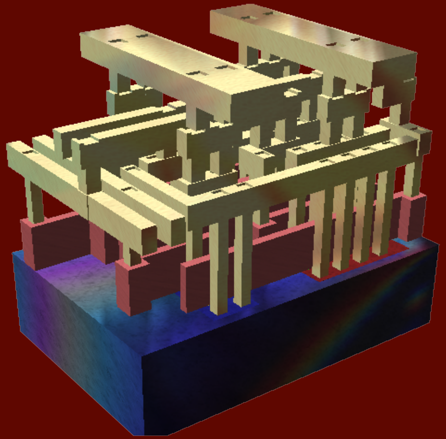

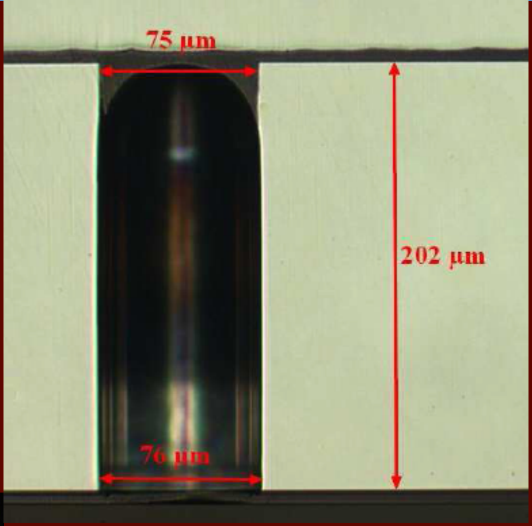

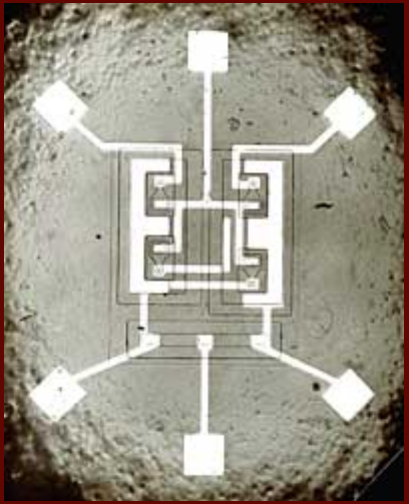

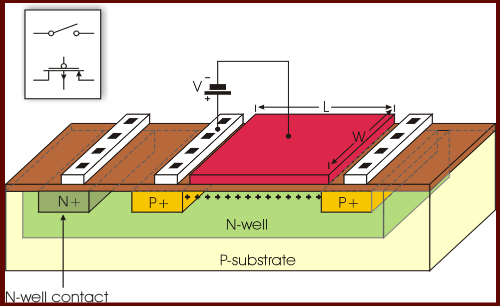

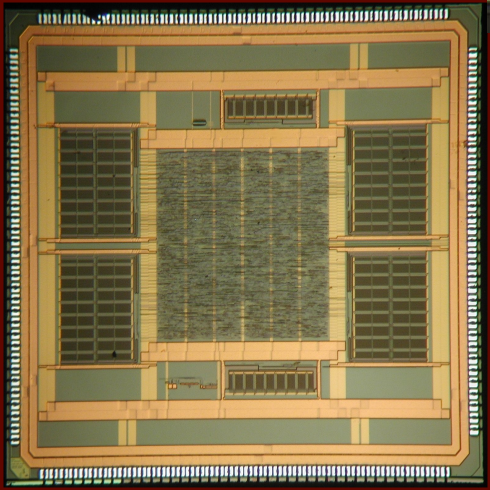

Advanced CMOS Technologies: current trends and future prospects

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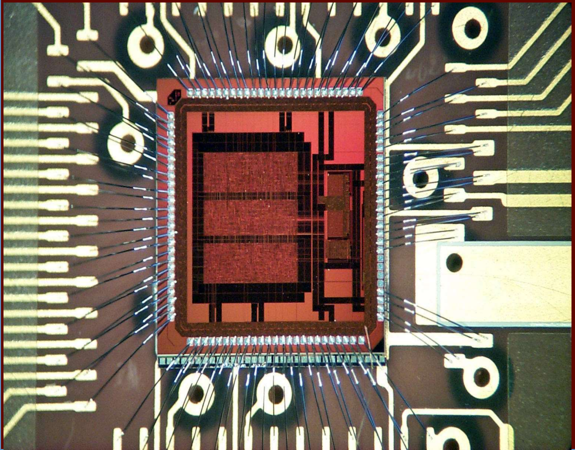
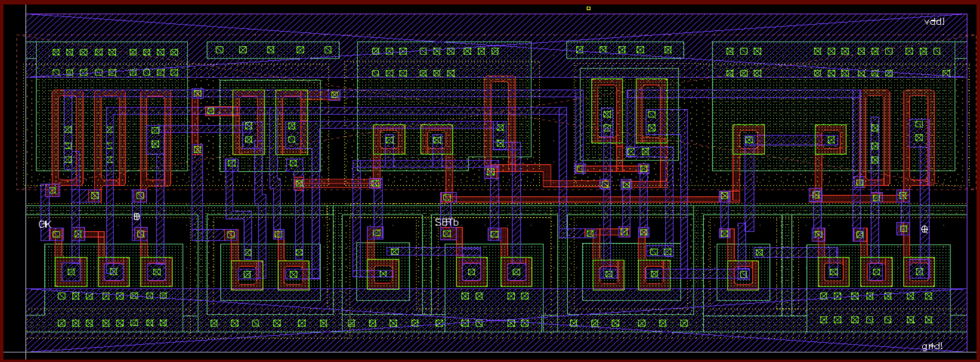




Outline

- Motivations
- Introductory Microelectronics
- Trends and Issues

Some of the many reasons why you need (more and more) chips

MOTIVATIONS

Why on Earth do I need chips?

Amplification

- Detectors (transducers) fundamentally are of two types:
  - those with enough internal gain producing a large primary signal
    - ex.: carbon microphone, human eye and ears, spark or bubble chamber, some gas chambers etc.
  - those generating a tiny signal
    - ex.: an accelerometer, most silicon detectors, most calorimeters, light emitters etc.

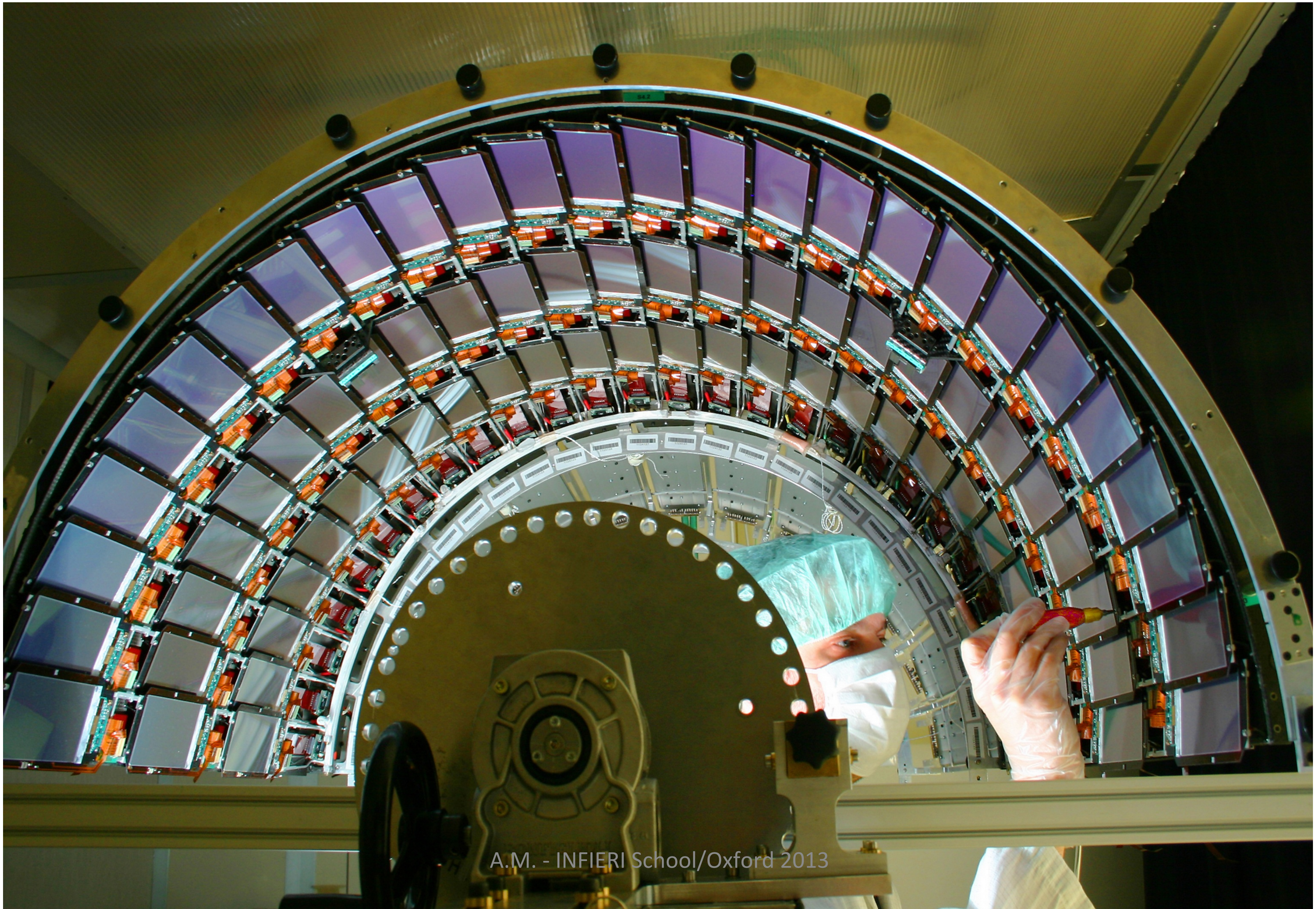
Timing + other Functionality

- Sometimes we need to extract non-amplitude information:
  - e.g.: time (need precise timing electronics) in TOF detectors, frequency in the auditive system

Intelligence

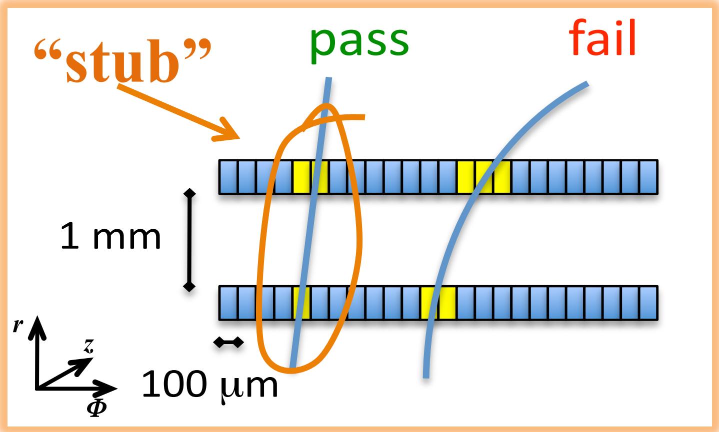
- In the future we will need to extract “features” and not just “dots”

CMS Tracker

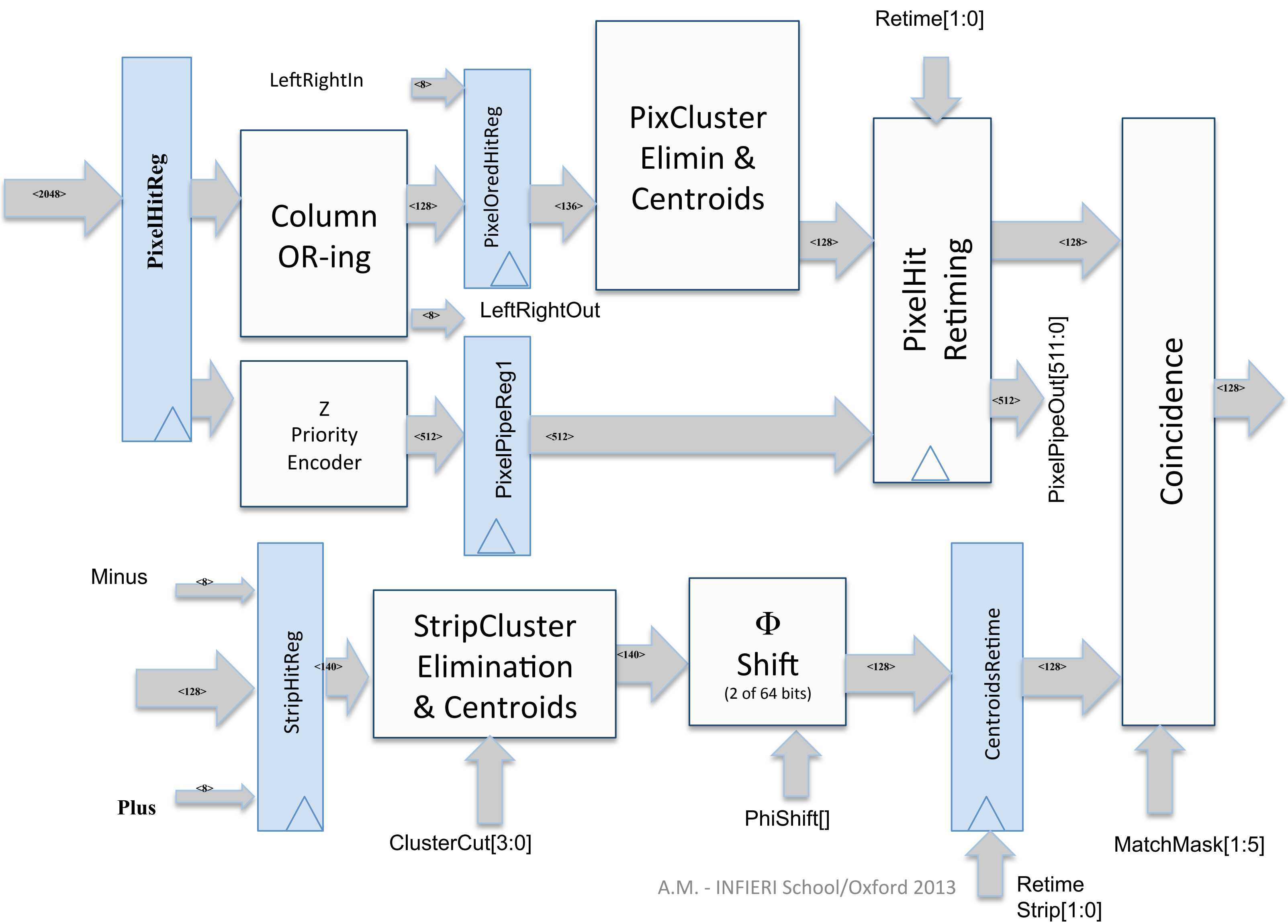


Local feature extraction for trackers

- Level-1 data require local rejection of low-p_T tracks
  - To reduce the data volume, and simplify track finding @ Level-1
    - Threshold of ~ 1÷2 GeV ⇒ data reduction of about one order of magnitude
- Design modules with p_T discrimination ("p_T modules")
  - Correlate signals in two closely-spaced sensors
    - Exploit the strong magnetic field of CMS
- Level-1 "stubs" are processed in the back-end
  - Form Level-1 tracks, $p_T > 2÷2.5$ GeV
    - To be used to improve different trigger channels



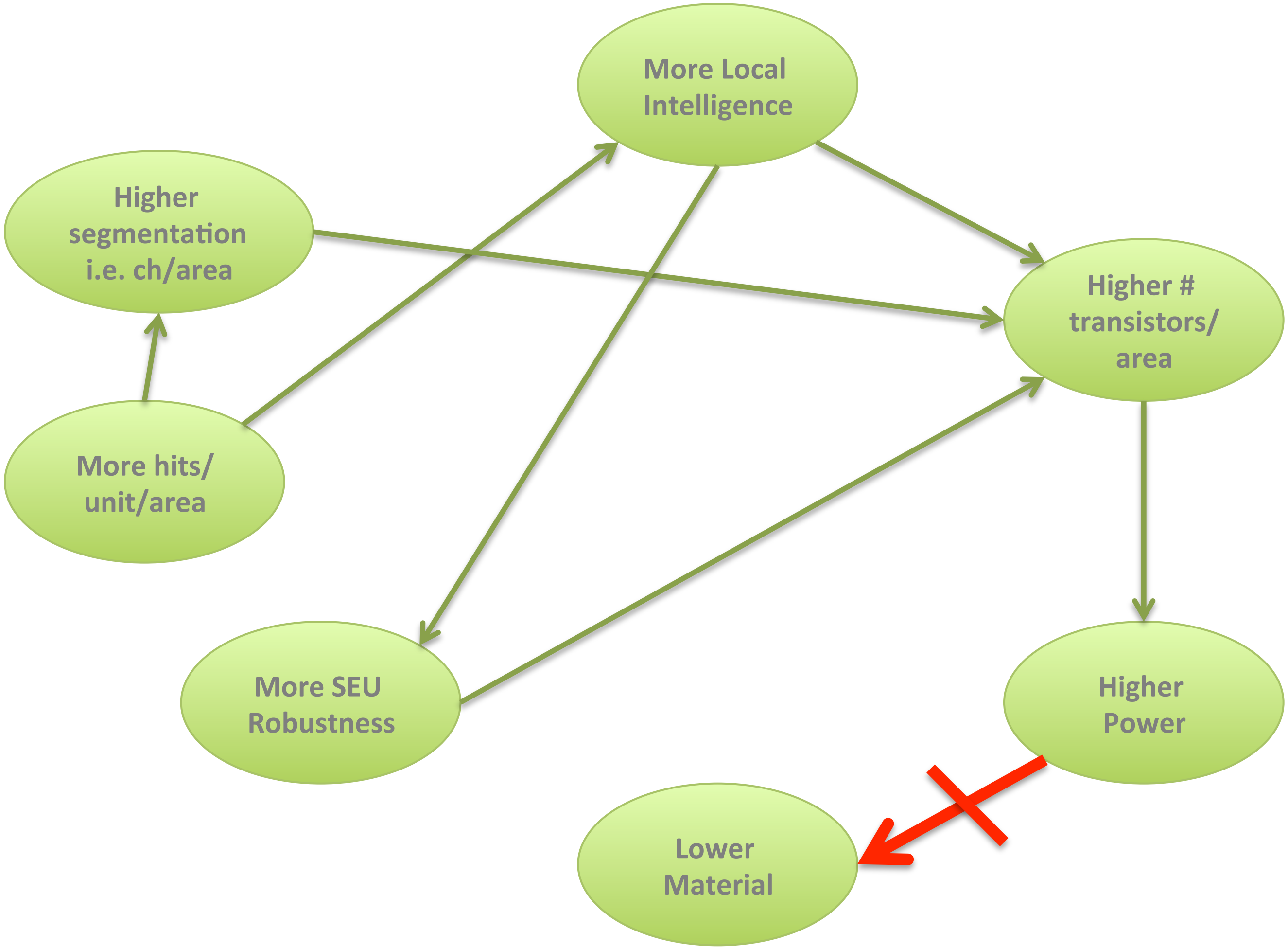
Stub finding for CMS tracker



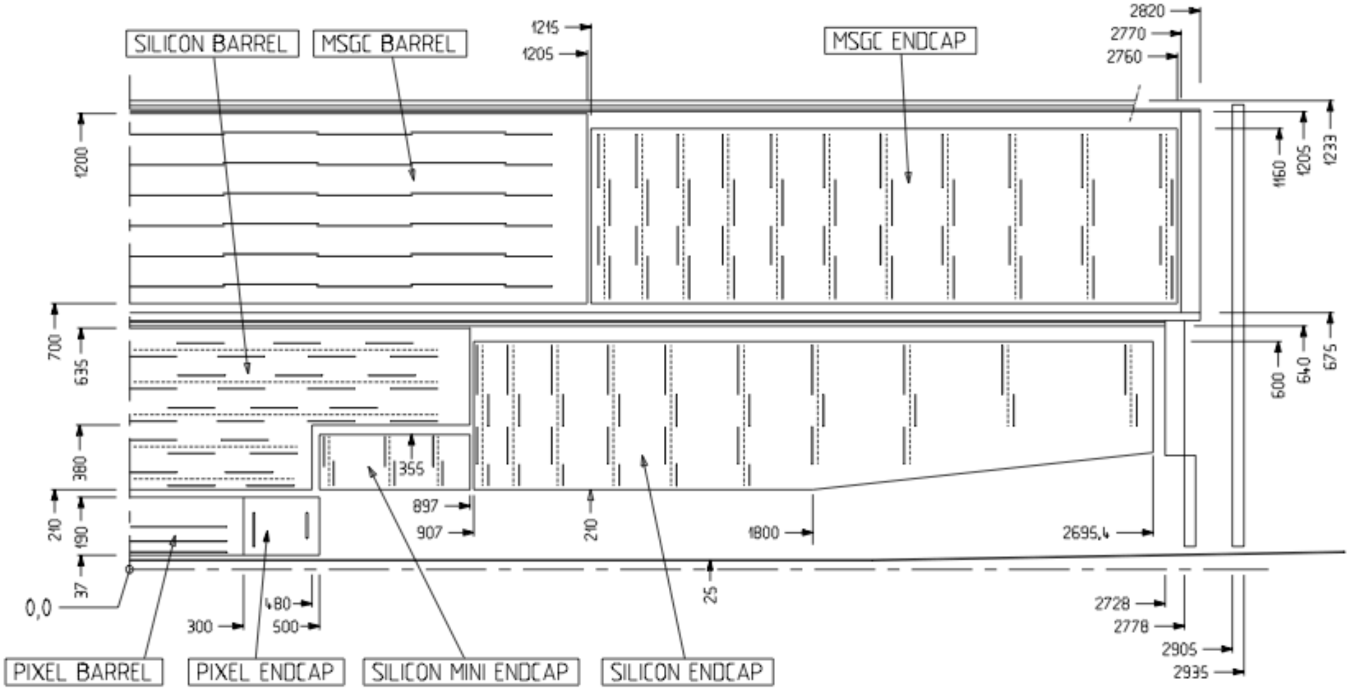
Areas for improvements

- Performance
  - Functionality (fashionably also called “intelligence”)
  - Precision (space, time)
  - Reduce interference from overall detector (passive) materials
- Key technologies
    - Microelectronics
    - Interconnect
    - Optoelectronics [not discussed here]
- Fabrication and assembly cycles [not discussed here]
- Cost (reduction) [not discussed here]

Wish List Dependencies
i.e. the Great Engineering Compromising Chart

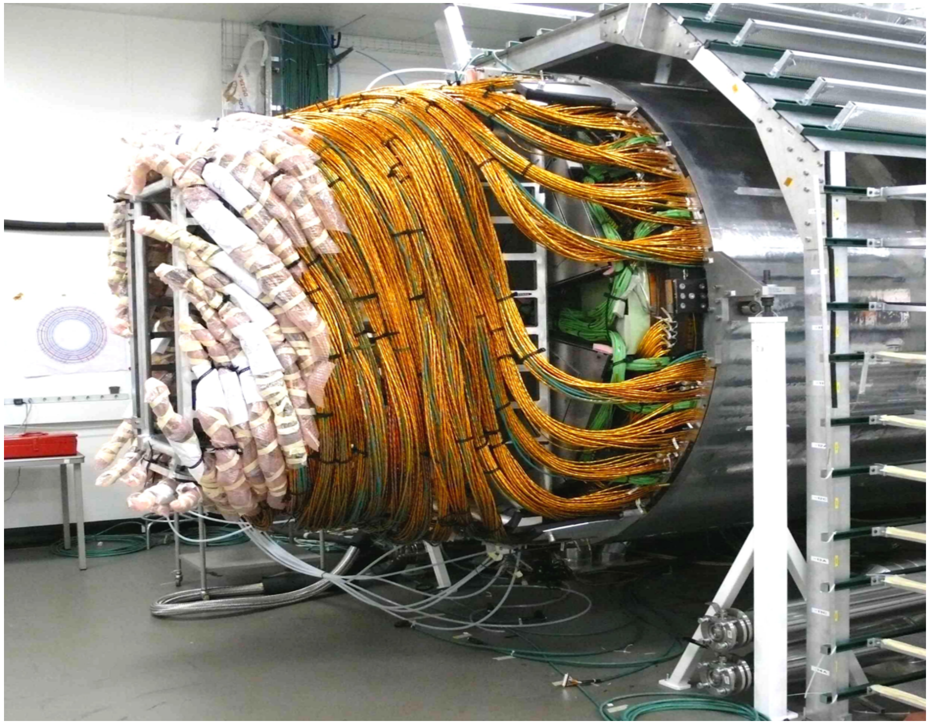


From serene and ethereal dreams…



Source: CMS Tracker TDR, 1999, changed to all Si later

… to hard reality



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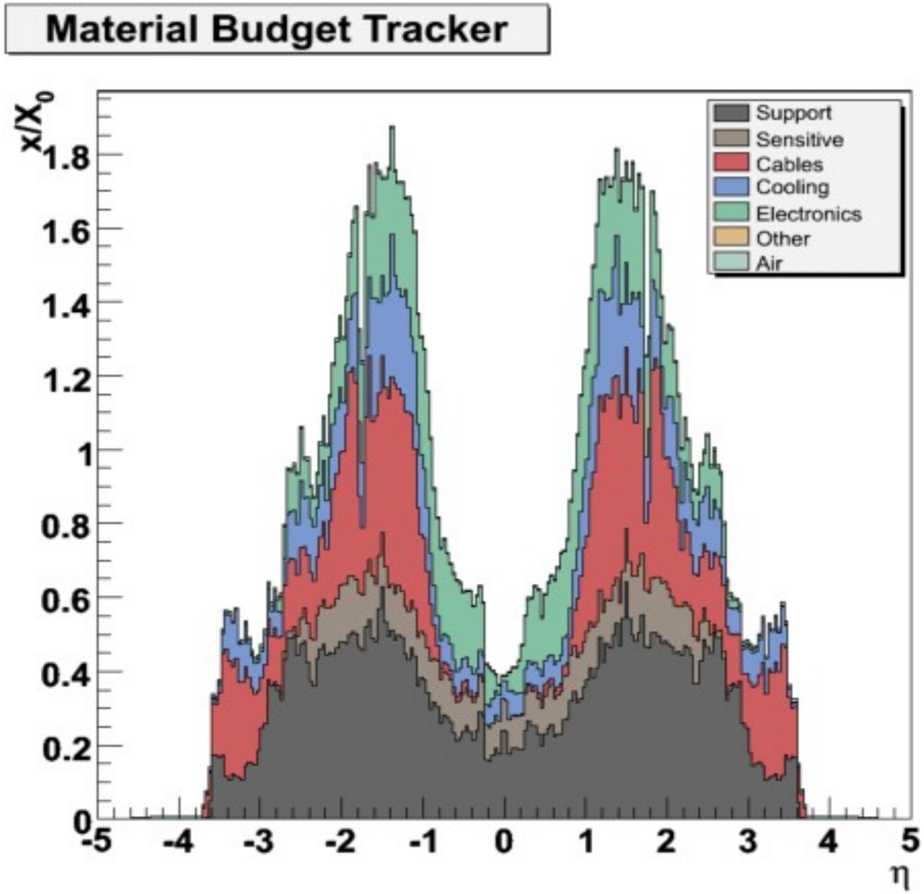
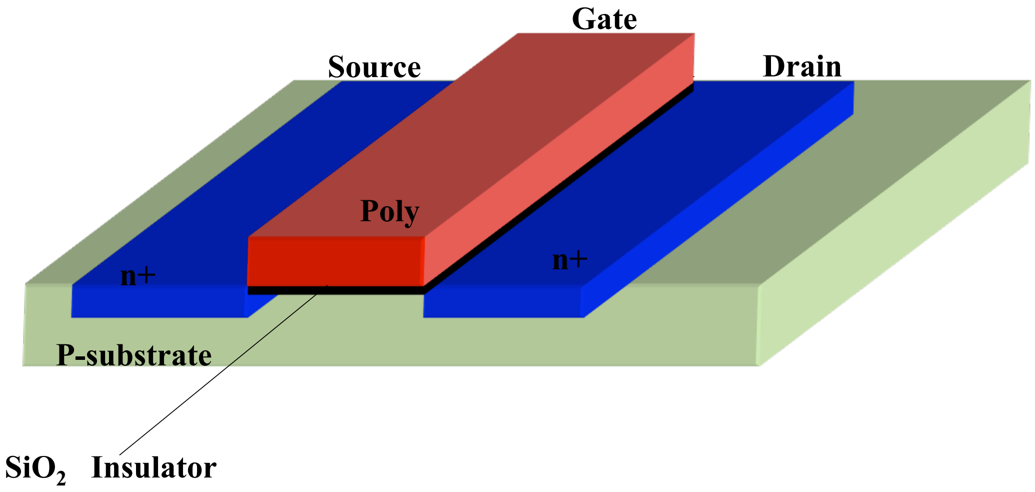


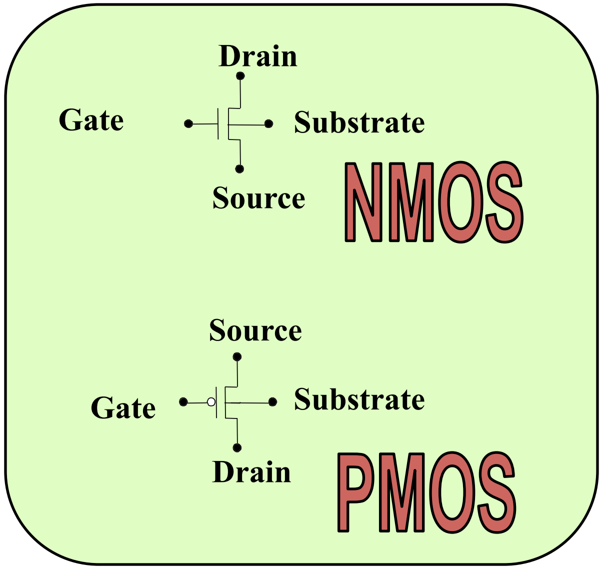
Potential for improvements

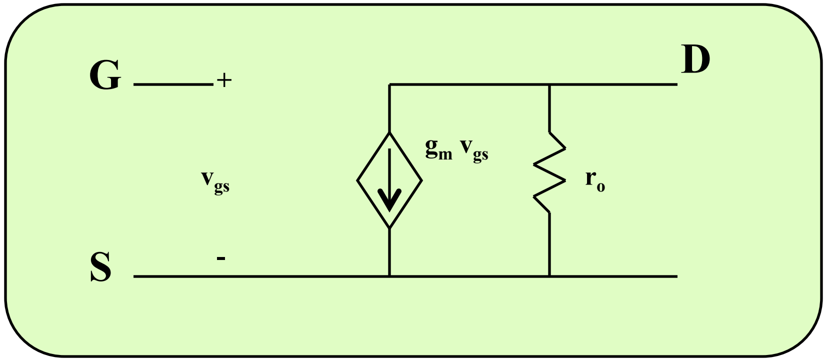
- FE: Low
  - intrinsic speed or resolution of detectors is not expected to improve dramatically
  - FE circuits close to intrinsic noise margins
  - CMOS tech evolution is not going to improve analog (actually probably worse, see later)
  - Only 3D integration can change the game
- A/D Conversion: Medium to Hih
  - conversion energy is still being improved, new architectures introduced, digital helps. Caveat: many companies make ADC IPs, do not design ADC, buy them!
- Digital signal processing: High to very high
  - Little or no “signal processing” is done today in HEP (shaper is analog)
  - Some laudable attempt in the “Altro” project (pedestal correction, tail cancelation etc.)
  - Much more to be done
- Data Processing (i.e. Feature Extraction): Huge
  - Little intelligence in chips: lots of raw (and meaningless!) data shipped out at the cost of embedded BW, power and of expensive links
  - Trigger (i.e. pattern recognition) opportunities
  - Feature extraction could easily be done now

BASIC 30 MINUTES MICROELECTRONICS

MOS transistors







Simple “small-signal” model

What are you interested in?

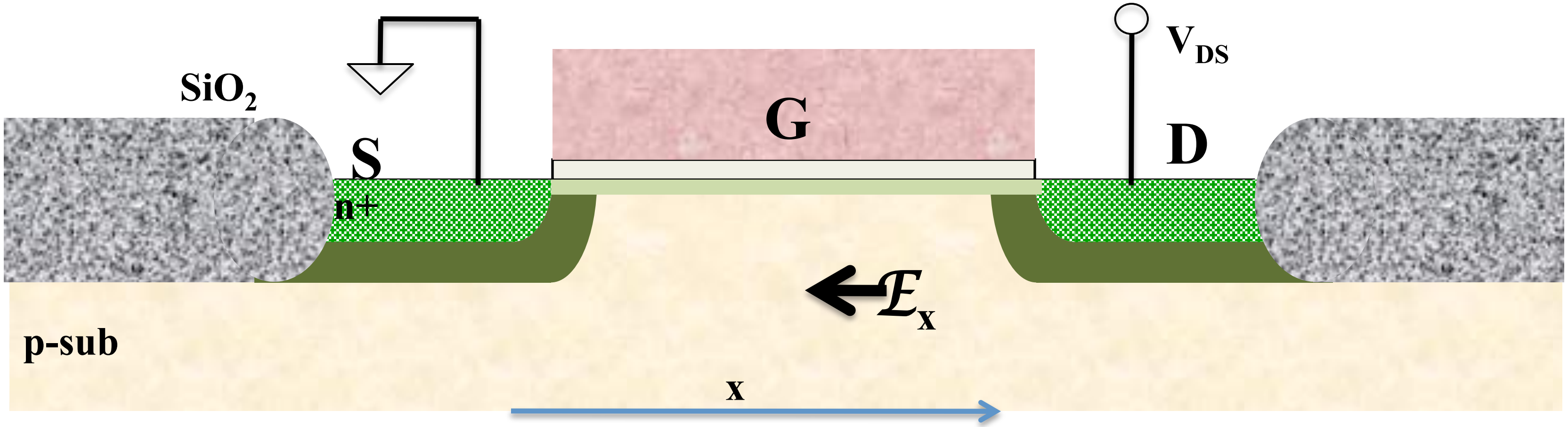
- A MOS transistor is a device with 4 pins;
  - it has two control terminals (the gate and the substrate) and two input/outputs (the source and drain)
    - The substrate is often ignored, but it can have a big effect on the behavior of the transistor
- Want to express an output quantity as a function of some control quantity!

$$O = O\,(p1, p2, \ldots)$$

- It turns out that, for a given device:

$$I_{ds} = I_{ds}\,(V_{gs}, V_{ds}, V_{sb}, \text{process parameters}, \ldots)$$

Simple derivation of MOSFET equations (1)



The current under the transistor is equal to the product of the velocity and the charge moved under the influence of the potential V_{DS} *under the gate*

$$I_d = Q_e(x) \cdot W \cdot v_e(x) \qquad (1)$$

where W *is the width of the transistor and* $Q_e(x)$ *is the charge per unit area.*

MOS Transistors Equations

- Cut-off region

$$I_{ds} = 0 \qquad (V_{gs} - V_t) < 0$$

- Non-saturation region

$$I_{ds} = \frac{\mu\varepsilon}{t_{ox}} \frac{W}{L}((V_{gs} - V_t)V_{ds} - \frac{V_{ds}^2}{2}) \qquad 0 < V_{ds} < (V_{gs} - V_t)$$

- Saturation region

$$I_{ds} = \frac{\mu\varepsilon}{2t_{ox}} \frac{W}{L}(V_{gs} - V_t)^2 \qquad (V_{gs} - V_t) < V_{ds}$$

μ: effective mobility, ε dielectric constant of gate insulator,
t_{ox} thickness of gate oxide
W,L width and length of transistor

… and near the threshold

$$V_t = \Phi_{MS} + 2\Phi_f + \gamma\sqrt{2\Phi_f + V_{SB}}$$

with :

$$\Phi_f = \frac{kT}{q}\ln\left(\frac{N_{SUB}}{n_i}\right)$$

and :

Φ_{MS} = *difference of workfunction between gate material and substrate.*

Drain current in subthreshold :

$$I_D = I_{D0}\exp\left(\frac{V_{GS} - V_{th}}{nV_T}\right)$$

Remember!

$$I_{ds} = \frac{\mu\varepsilon}{t_{ox}} \frac{W}{L} ((V_{gs} - V_t)V_{ds} - \frac{V_{ds}^2}{2})$$

$Non-saturation$

$$I_{ds} = \frac{\mu\varepsilon}{2t_{ox}} \frac{W}{L} (V_{gs} - V_t)^2$$

$Saturation\ region$

Manufacturing parameters,
can't be changed on a given technology

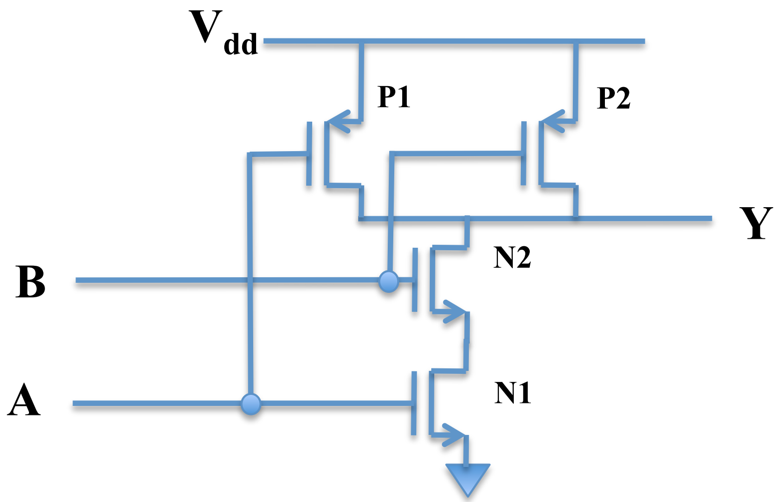
Geometric parameters
Defined at layout time

Electrical parameters
Depend on circuit behavior

How are MOSFETs used

- Digital circuits:
  - in CMOS circuits, transistors behave as switches and could be modeled as simple on-off devices
  - Main requirements: speed, current drive, (low) power, (small) size.
- Analog circuits:
  - the most important function in analog is "gain", i.e. the translation of a "small" signal into a "larger" signal
  - Main requirements: high gain, accuracy, (low) noise, (low) power…

Example in digital



A	B	N1	N2	P1	P2	Y
0	0	open	open	closed	closed	V_{dd}
0	V_{dd}	open	closed	open	closed	V_{dd}
V_{dd}	0	closed	open	closed	open	V_{dd}
V_{dd}	V_{dd}	closed	closed	open	open	0

Analog: the basic equations revisted

$$I_{ds} = \frac{\mu\varepsilon}{2t_{ox}} \frac{W}{L} (V_{gs} - V_t)^2$$

Saturation region

Once the transistor is chosen this is fixed!

The translation of input -> output depends only on this term

Analog: what does one want (mostly)

$$I_{ideal} = f(V_{gs}) \quad such\ that \quad \frac{df(V_{gs})}{dV_{gs}}\ is\ "large"$$

$$g_m = \frac{dI_{ds}}{dV_{gs}} = \frac{\mu\varepsilon}{t_{ox}} \quad \frac{W}{L} \quad (V_{gs} - V_t) \qquad in\ saturation\ region$$

$$g_m = \frac{2I_{ds}}{V_{gs} - V_t}$$

The mysterious “*weak inversion*” region

$$If\ we\ are\ looking\ for\ a\ region\ with\ high\ gain,$$
$$observe\ that\ when\ V_{gs} \cong V_t$$

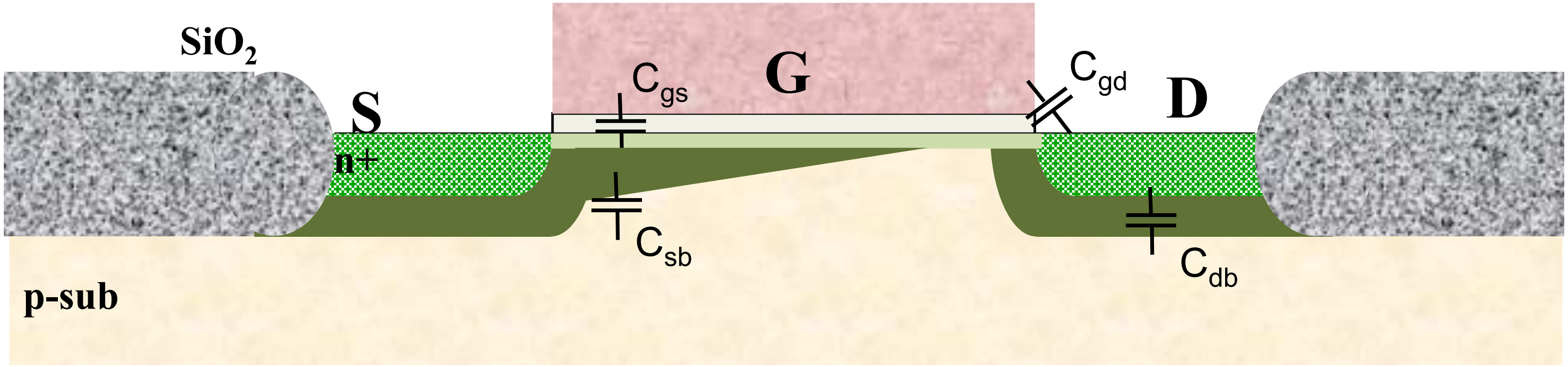
$$I_{ds_{wi}} = I_{wi0} \frac{W}{L} e^{\frac{V_{gs}-V_t}{nkT} q}$$

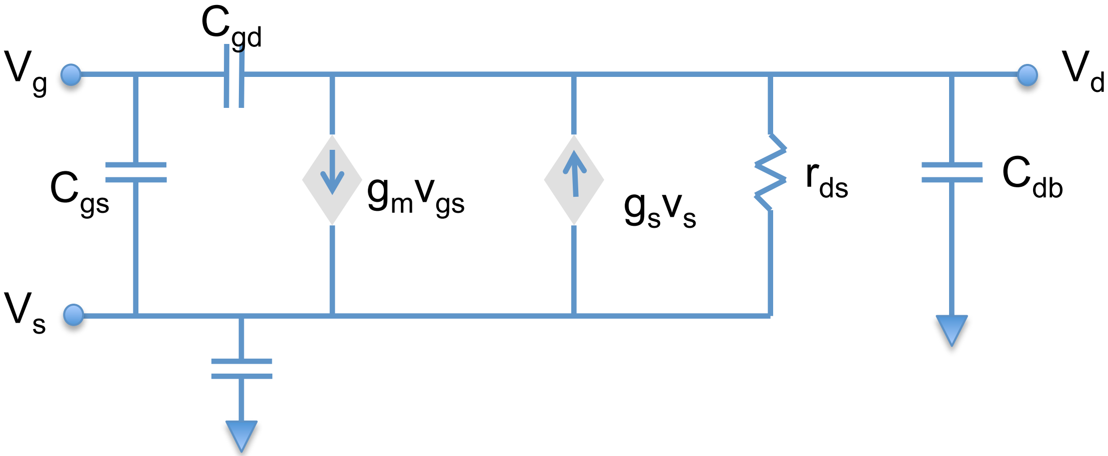
$$but\ unfortunately\ I_{wi0}\ is\ a\ small\ number,$$
$$therefore\ what\ we\ really\ want:$$

$$I_{ideal} = f(V_{gs}) \quad such\ that \quad \frac{df(V_{gs})}{dV_{gs}}\ is\ "large"$$

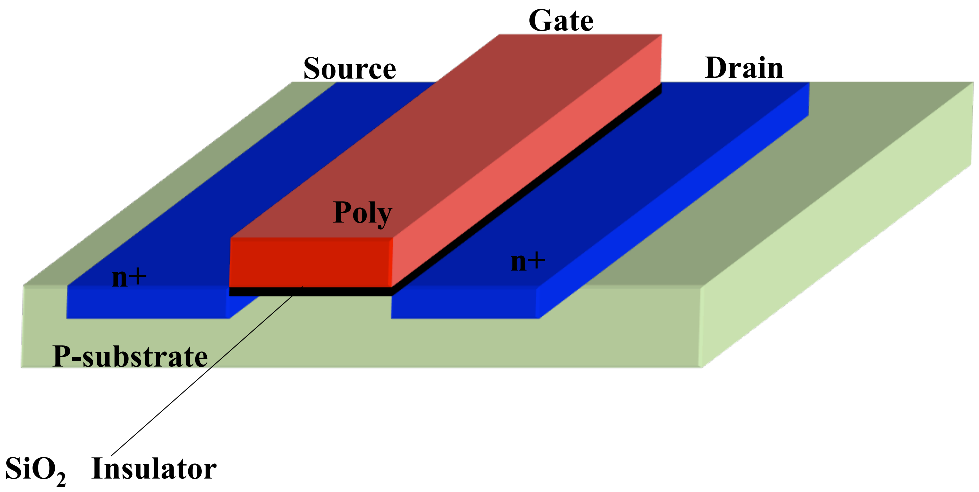
$$AND \quad f(Vgs) \quad is\ also\ large\ enough$$

The real transistor





Why do we care so much about nm?



- Smaller dimensions give:
  - – Shorter transit time
    - Faster circuit
  - – Lower parasitic capacitance
    - Faster circuit
    - Lower power ($P \propto C V^2$)
  - – More transistors/unit area
    - More functionality can be built into chips

Reality check

- Beware: these formulas are just about decent for devices down to about one micron channel length, but are fairly approximate for the modern deep submicron generations (< 0.35 μm).

- In reality only very rough first order calculations are performed by hand, only the general tendencies are correct, once you know a few more details…

Detail # 1: channel length modulation

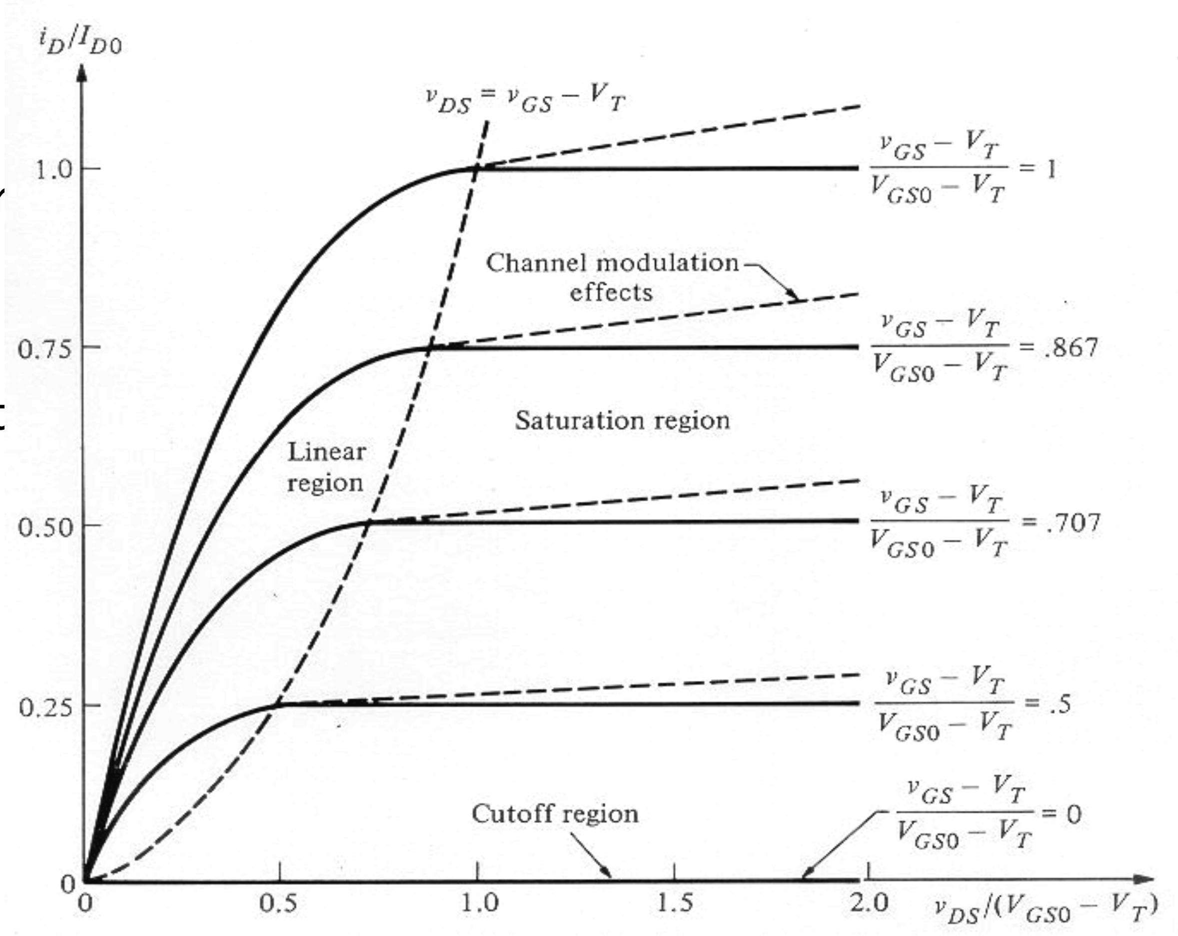
Increasing V_{DS} increases also the size of the drain depletion region which effectively shortens the length of the channel, increasing the transistor current in a way which is better described by the equation:

$$I_d' = I_d\left(1 + \lambda V_{DS}\right)$$

with : $$\frac{\Delta L}{L} = \lambda V_{DS}$$

MOS output characteristics

- **Linear region**:
  $V_{ds}<V_{gs}-V_T$
  - Voltage controlled resistor
- **Saturation region**:
  $V_{ds}>V_{gs}-V_T$
  - Voltage controlled current source
- Curves deviate from the ideal current source behavior due to:
  - Channel modulation effects



Detail #2: velocity saturation

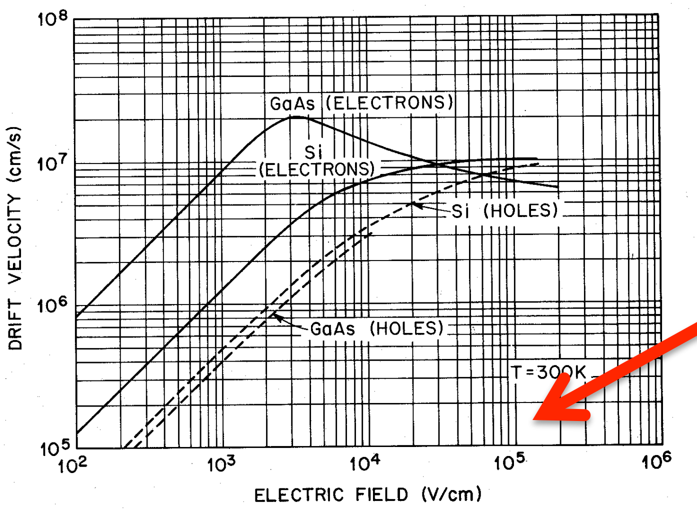


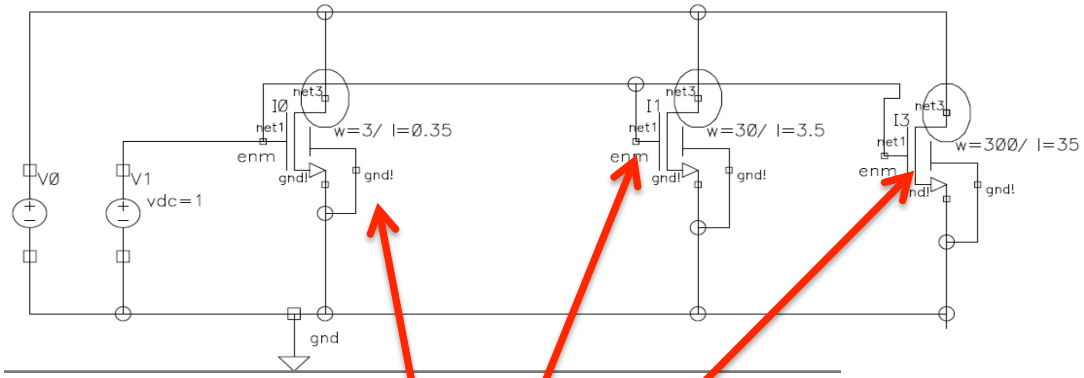
Fig. 23 Drift velocity versus electric field in GaAs and Si.[12, 13] Note that for *n*-type GaAs, there is a region of negative differential mobility.

Modern transistors operate here.

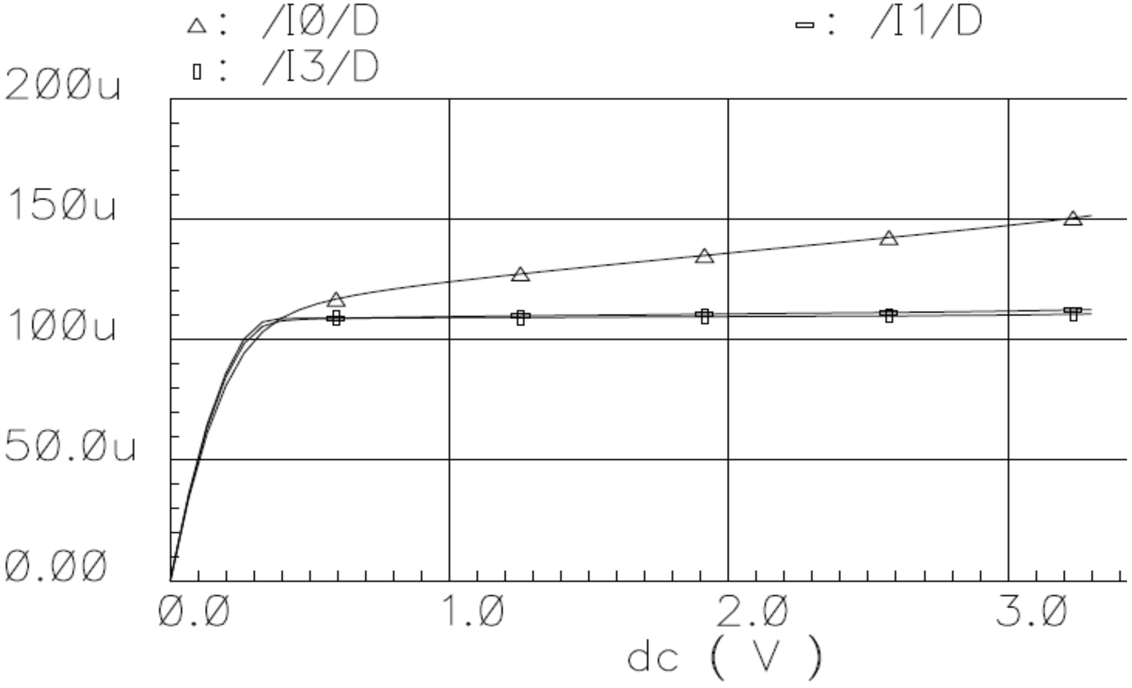
Example: L=0.25 mm, V_{ds} = 2.5V
gives a field of: 2.5/.25e-6 =1e5 V/cm

- Beyond a certain value of the electric field, electrons (and holes) are not further accelerated by an increase in the V_{DS} voltage

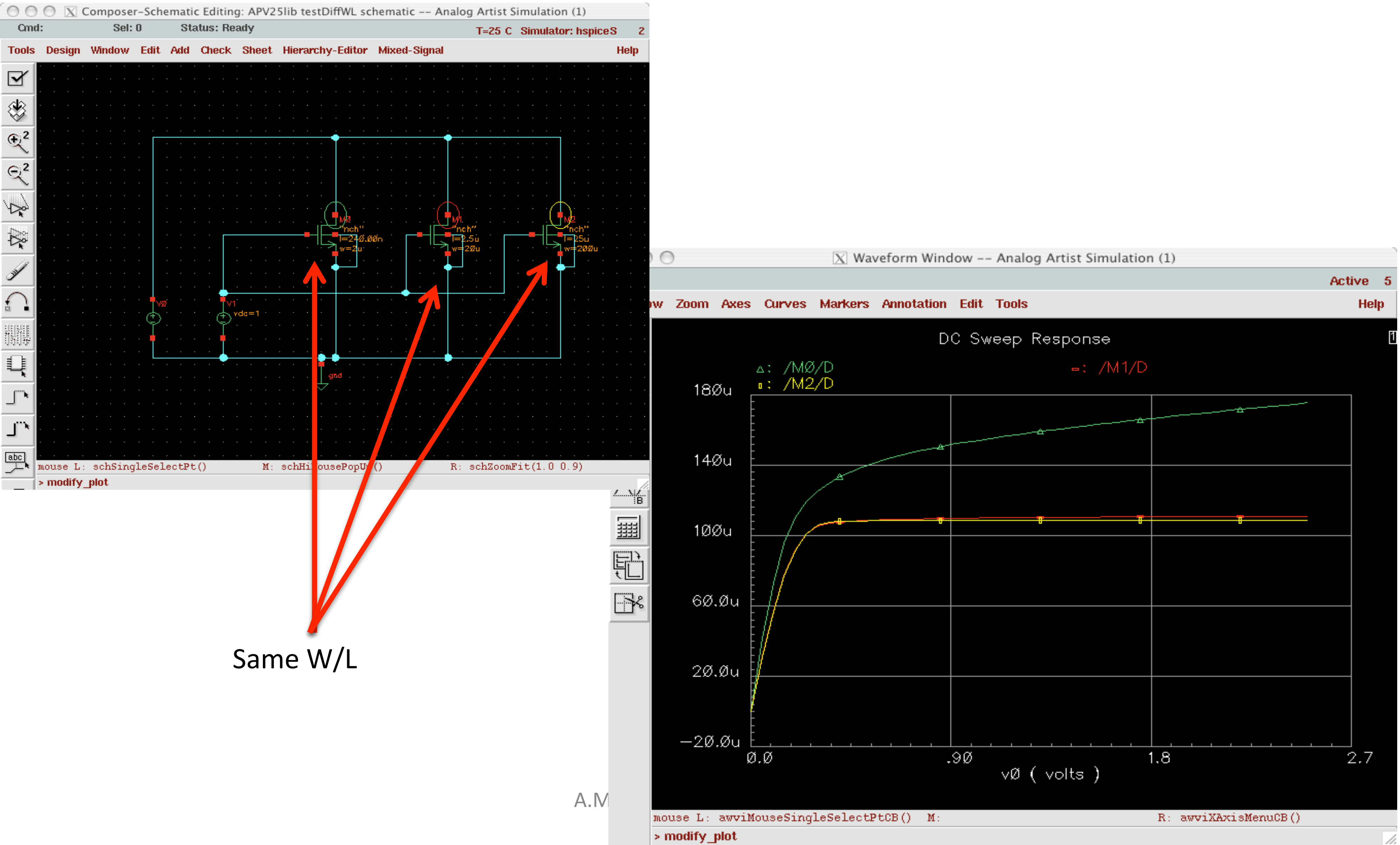
The transistor at .35 μm



Same W/L

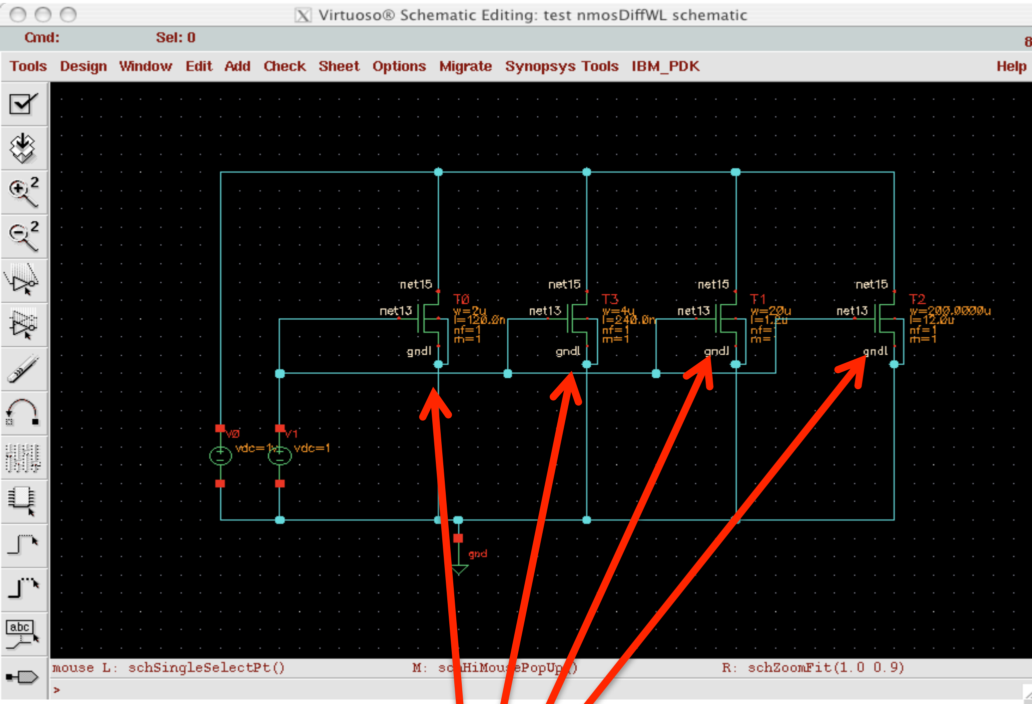


… at .25 um

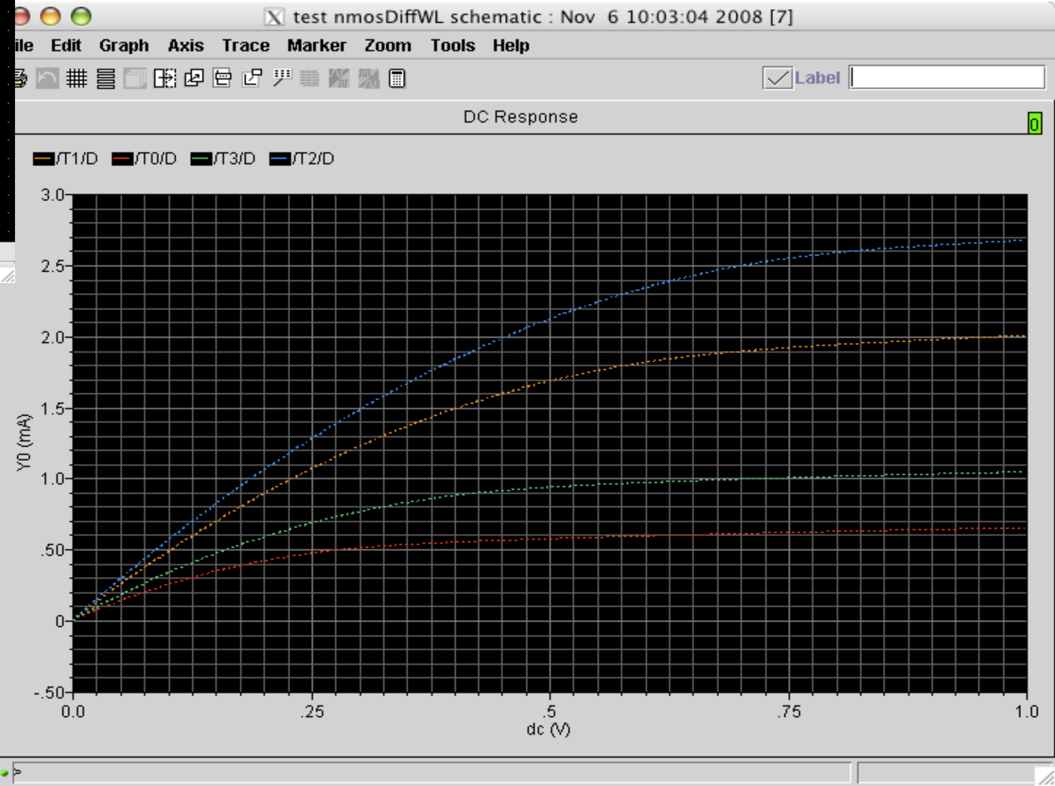


Same W/L

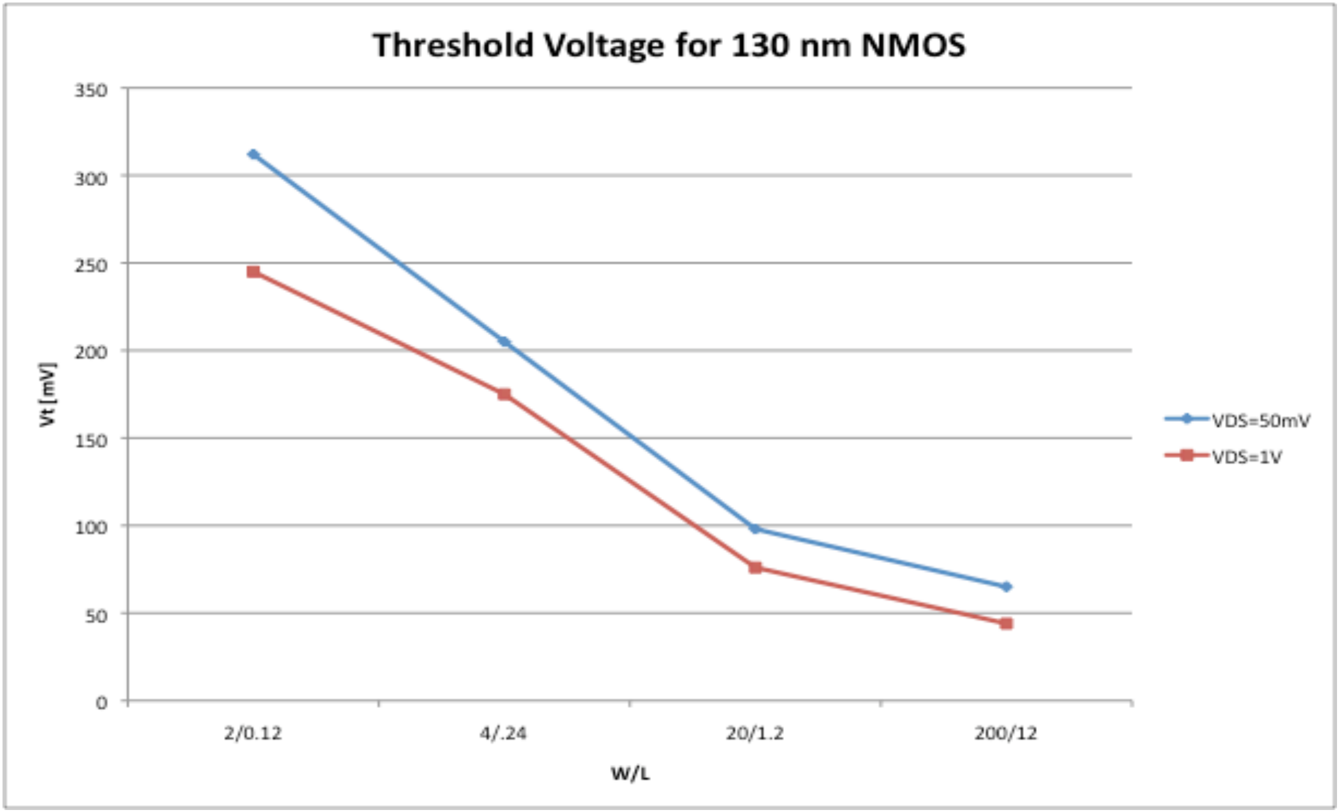
… at 130nm



Same W/L

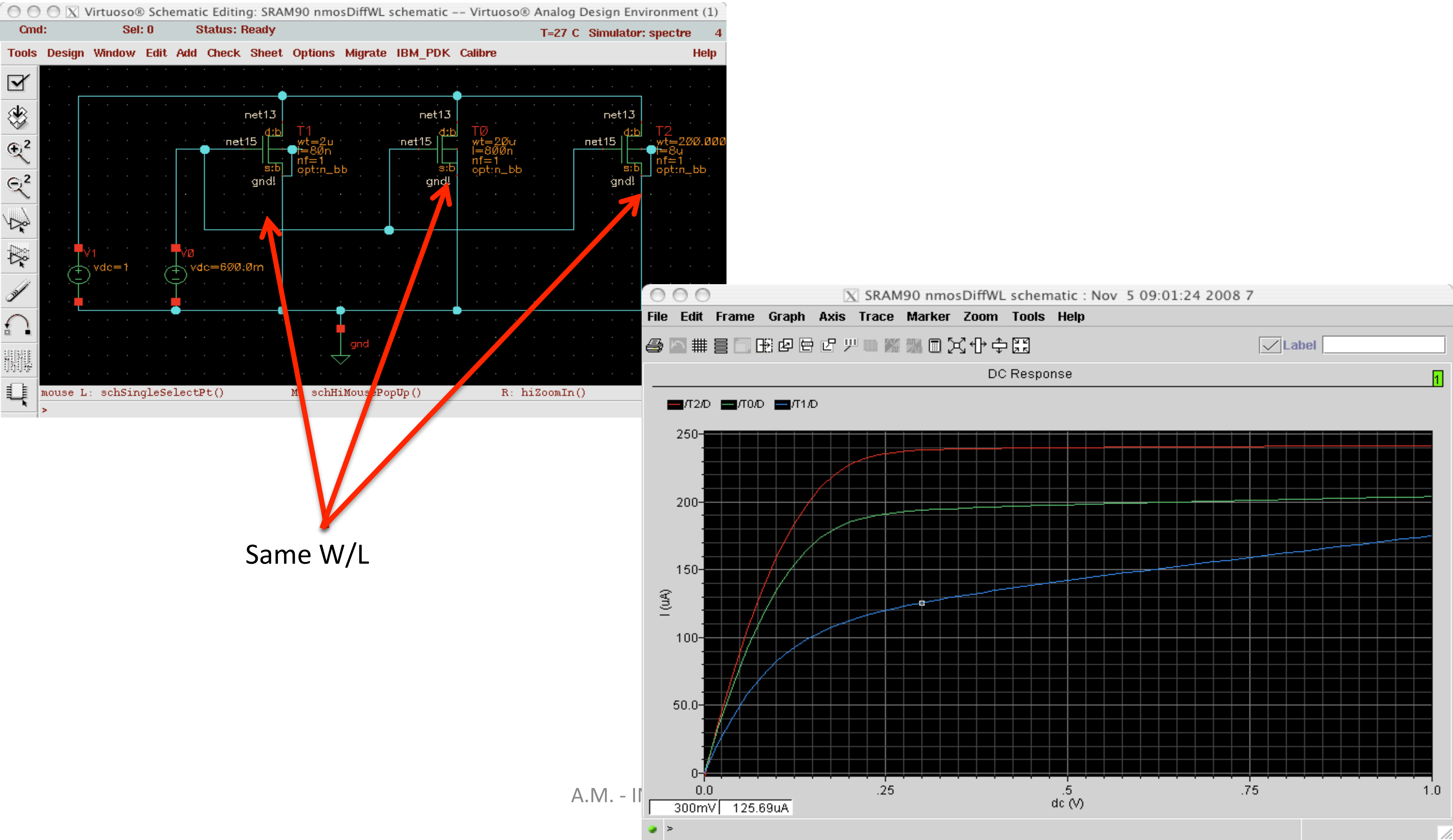


Short channel effects: V_t variation



V_t defined as V_{GS} when I_d=300nA

… and at 90nm

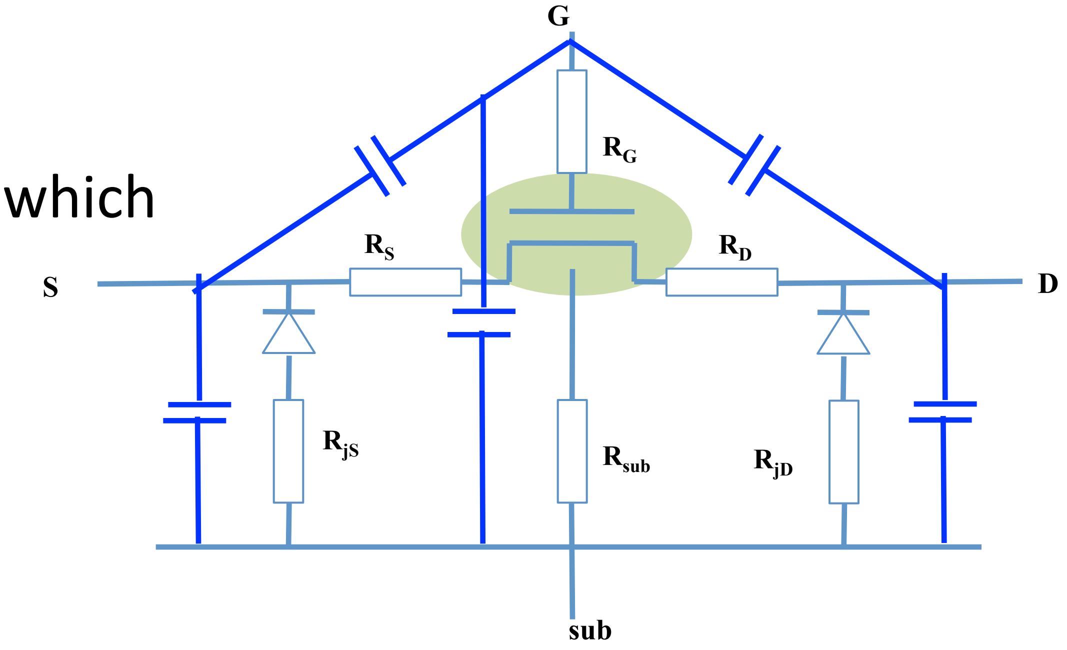


Same W/L

Further complications: RF Models

At high speed and for analog applications, the MOS models must further be complemented by additional important details which are necessary to describe the device accurately:

- Parasitic capacitors
- Parasitic resistors



Modeling tools

- Complexity of behavior of deep-submicron transistors is taken care by "models" in tools like Hspice, Spectre etc.
- These are essentially all derived from the old glorious "Spice" electrical simulator
- These models are to some extent numerical approximations to measured data more than real "physical models" and contain many (> 100) parameters to try to match the behavior of measured devices

$$I_d = I(\text{Voltages, Temp, } {\scriptstyle \text{Process(small\_size\_effects)}})$$

$$I_d = I(\text{Voltages, Temp, } {\Large \text{Process(small\_size\_effects)}})$$

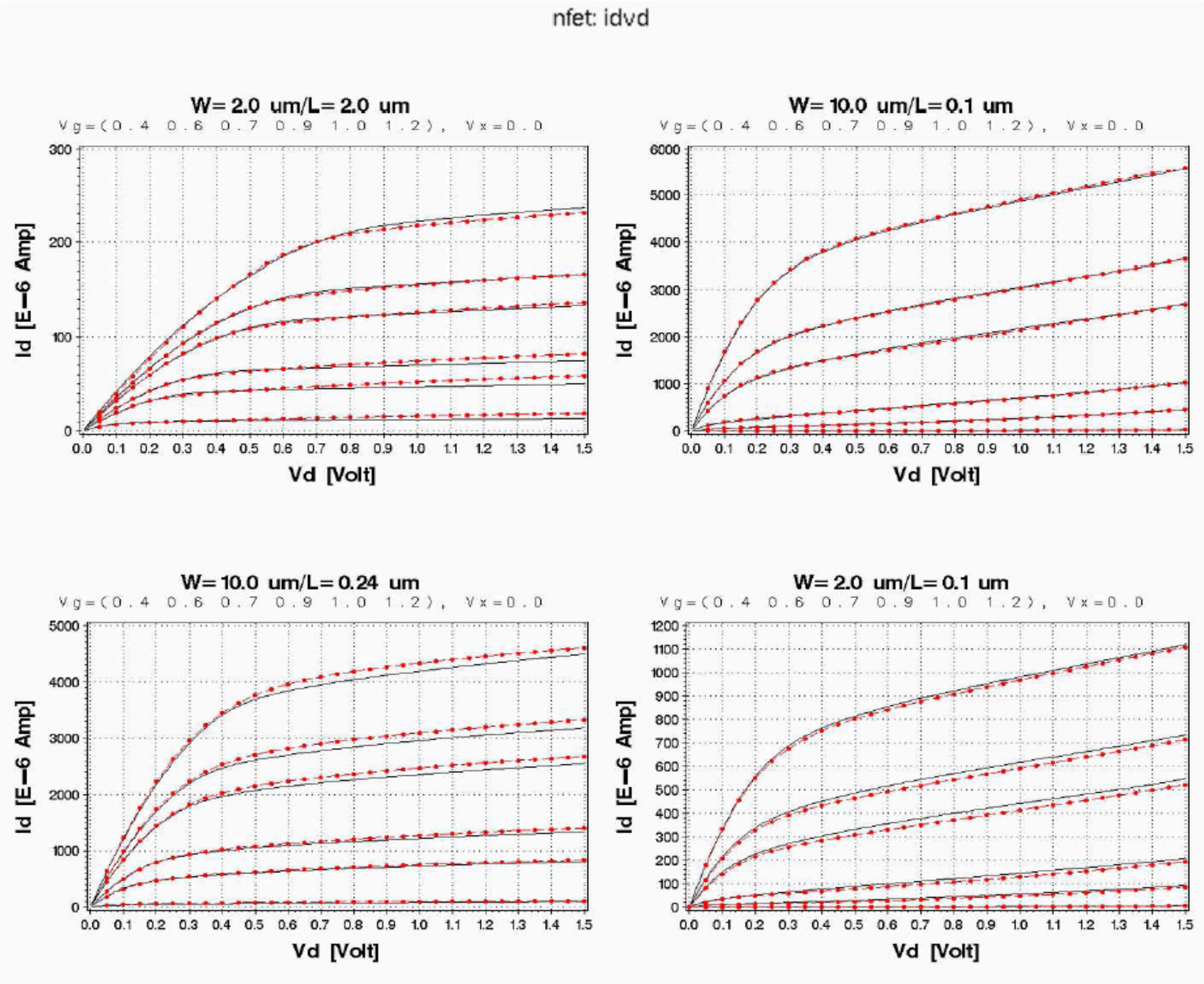
Example model for .18 um technology

```
 T66D SPICE BSIM3 VERSION 3.1 PARAMETERS
SPICE 3f5 Level 8, Star-HSPICE Level 49, UTMOST Level 8
* DATE: Aug 24/06
* LOT: t66d                  WAF: 6002
* Temperature_parameters=Default
.MODEL CMOSN NMOS (                                LEVEL    = 49
+VERSION = 3.1            TNOM     = 27            TOX      = 4E-9
+XJ      = 1E-7           NCH      = 2.3549E17     VTH0     = 0.3748918
+K1      = 0.5810791      K2       = 5.190537E-3   K3       = 0.0251112
+K3B     = 1.9548261      W0       = 1E-7          NLX      = 1.704106E-7
+DVT0W   = 0              DVT1W    = 0             DVT2W    = 0
+DVT0    = 1.3341776      DVT1     = 0.4208392     DVT2     = 0.0592963
+U0      = 270.6031975    UA       = -1.397081E-9  UB       = 2.427846E-18
+UC      = 7.90533E-11    VSAT     = 9.474445E4    A0       = 1.9252432
+AGS     = 0.4453175      B0       = 3.575132E-8   B1       = 4.519153E-6
+KETA    = -0.0104469     A1       = 0.8           A2       = 0.6706014
+RDSW    = 116.5959526    PRWG     = 0.3690724     PRWB     = -0.2
+WR      = 1              WINT     = 3.397749E-10  LINT     = 1.754665E-8
+XL      = 0              XW       = -1E-8         DWG      = -4.586166E-9
+DWB     = 5.274214E-9    VOFF     = -0.0975545    NFACTOR = 2.4290125
+CIT     = 0              CDSC     = 2.4E-4        CDSCD    = 0
+CDSCB   = 0              ETA0     = 2.73419E-3    ETAB     = 4.431962E-6
+DSUB    = 0.0157531      PCLM     = 0.7131944     PDIBLC1 = 0.1207863
+PDIBLC2 = 3.061733E-3    PDIBLCB = -0.1           DROUT    = 0.6529592
+PSCBE1  = 8E10           PSCBE2   = 1.720071E-9   PVAG     = 2.810889E-3
+DELTA   = 0.01           RSH      = 6.7           MOBMOD   = 1
+PRT     = 0              UTE      = -1.5          KT1      = -0.11
+KT1L    = 0              KT2      = 0.022         UA1      = 4.31E-9
+UB1     = -7.61E-18      UC1      = -5.6E-11      AT       = 3.3E4
+WL      = 0              WLN      = 1             WW       = 0
+WWN     = 1              WWL      = 0             LL       = 0
+LLN     = 1              LW       = 0             LWN      = 1
+LWL     = 0              CAPMOD   = 2             XPART    = 0.5
+CGDO    = 8.06E-10       CGSO     = 8.06E-10      CGBO     = 1E-12
+CJ      = 9.608408E-4    PB       = 0.8           MJ       = 0.3788997
+CJSW    = 2.73327E-10    PBSW     = 0.7255769     MJSW     = 0.11073
+CJSWG   = 3.3E-10        PBSWG    = 0.7255769     MJSWG    = 0.11073
+CF      = 0              PVTH0    = -1.371522E-3  PRDSW    = -2.3260605
+PK2     = 6.322009E-4    WKETA    = -2.59017E-5   LKETA    = -0.0117759
+PU0     = 4.4811269      PUA      = 1.856785E-12  PUB      = 0
+PVSAT   = 1.333082E3     PETA0    = 4.733753E-5   PKETA    = 1.350718E-4     )
```

and models are not perfect…

Example model vs hardware comparison
for a 90 nm technology

NFET

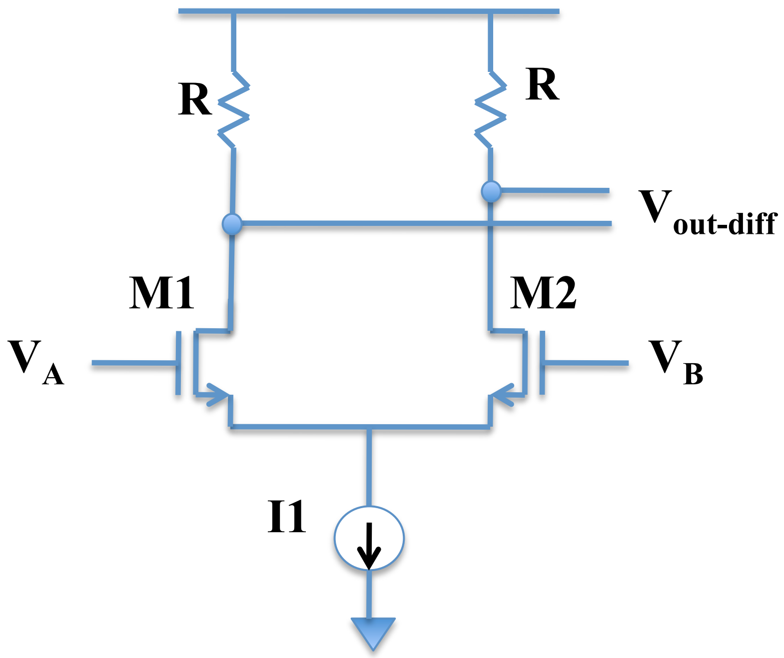


Process variations (1)

- Manufacturing a 90nm device in a foundry requires close to 1,000 processing steps

- Minute differences in these steps can lead to significantly different electrical characteristics between devices:
  - On a single chip
    - on-chip matching
  - On chips on the same wafer
  - On chips on different wafers

Process variation example



- The diff pair has M1 and M2 identical devices
- When $V_A = V_B$ then $V_{out} = 0$
- If $I_d(M1) \neq I_d(M2)$ because of mismatch then

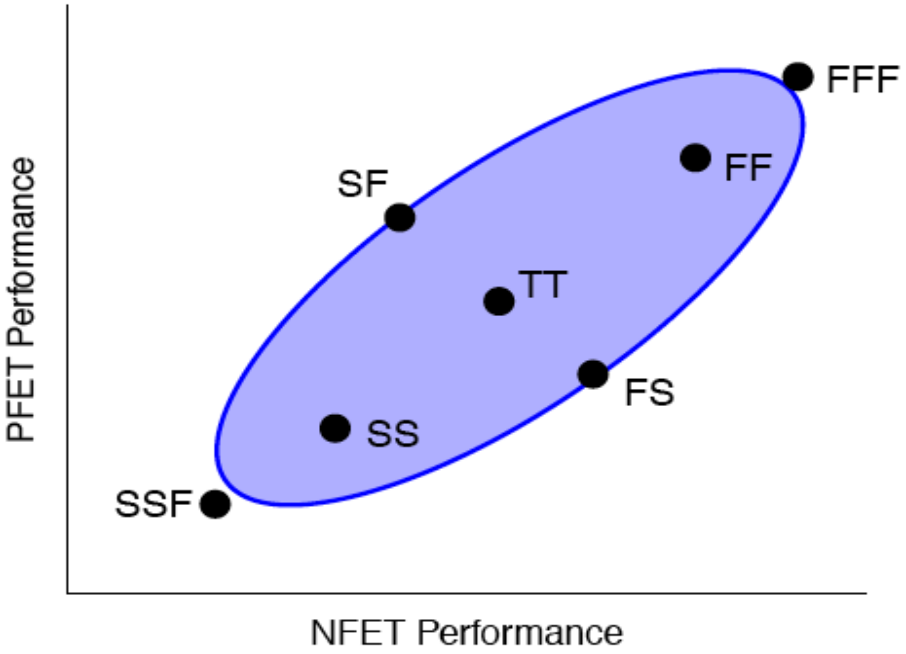
  $V_{out} \neq 0$

  and the amplifier acts as if there was a fixed offset voltage connected to one of the inputs

Process variations (2)

- Designer must cope with a multi-dimensional world of variations to make sure that all chips work robustly

- In addition, variations in temperature and supply voltage must be carefully taken into account

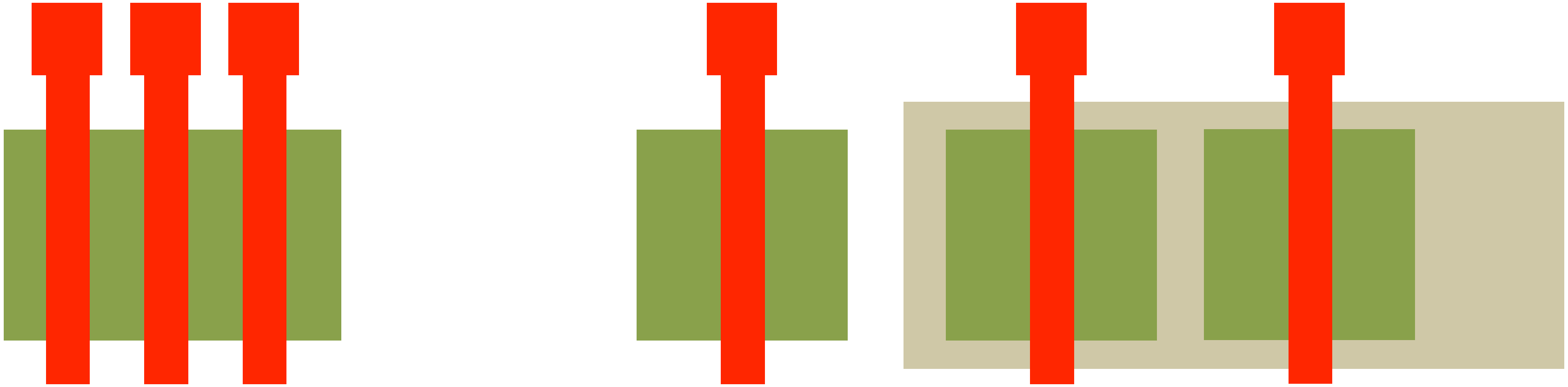


Process variations (3)

- Process variations can affect:
  - devices (NMOS and PMOS independently)
    - $V_{t,}$ and some processes have multiple V_t options
    - mobility
    - intrinsic transistor parasitics (and therefore speed)
  - interconnect
    - spacing of thin lines affects C and R of metal lines (maybe differently in different layers!)
  - passives
    - capacitors
    - resistors

Process variations (4)

- Proximity effects
  - Identical devices (transistor, capacitors and resistors) may behave differently depending on how they are laid-out relatively to neighbor



MOS transistor: Threshold equation

- Threshold:

$$V_t = V_{FB} + 2\Phi_B + \frac{\sqrt{2\varepsilon q N_A (2\Phi_B + V_{sb})}}{C_{ox}} + V_{q-trapped}$$

Threshold depends on:

- physics constants
- doping concentration
- source to bulk voltage
- thickness of gate insulator
- radiation damage

Relevant for HEP

TRENDS AND ISSUES

Why can't scaling continue forever?

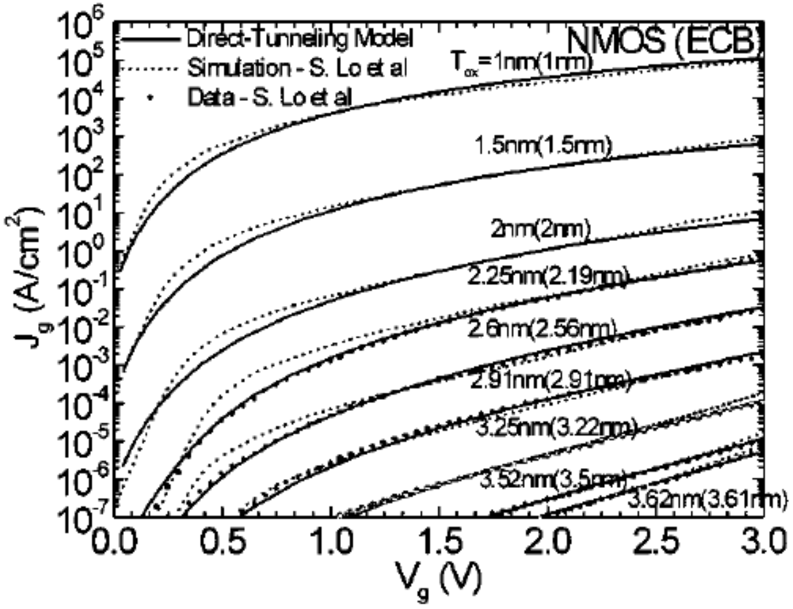
- Technological Reasons
  - – Historically these reasons have a lifetime of 3-5 years…
- Fundamental reasons from Physics
  - – Well known since > 30 years
- Economic reasons
  - – Depend on the next "killer" application

Technological reasons

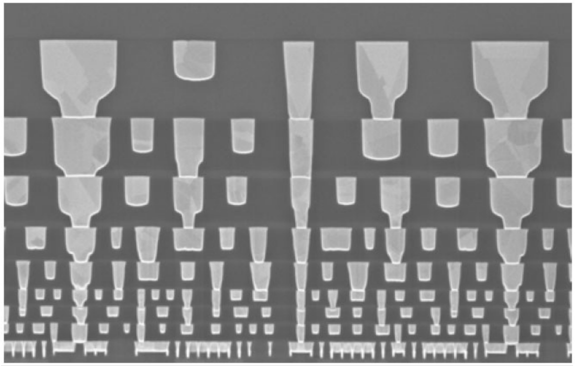
- Lithography limitations
  - How to print structures much smaller than the wavelength of the light used?
- Material limitations
  - Leakage currents through gate oxides
  - Electron velocity saturates
- Material properties
  - resistance in wires gets larger with smaller wires
  - capacitance between wires gets higher with closer wires

Leakage current in thin oxides

W.C. Lee, C. Hu, “Modeling CMOS Tunneling Currents Through Ultrathin Gate Oxide Due to Conduction- and Valence-Band Electron and Hole Tunneling”,
IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 48, NO. 7, JULY 2001

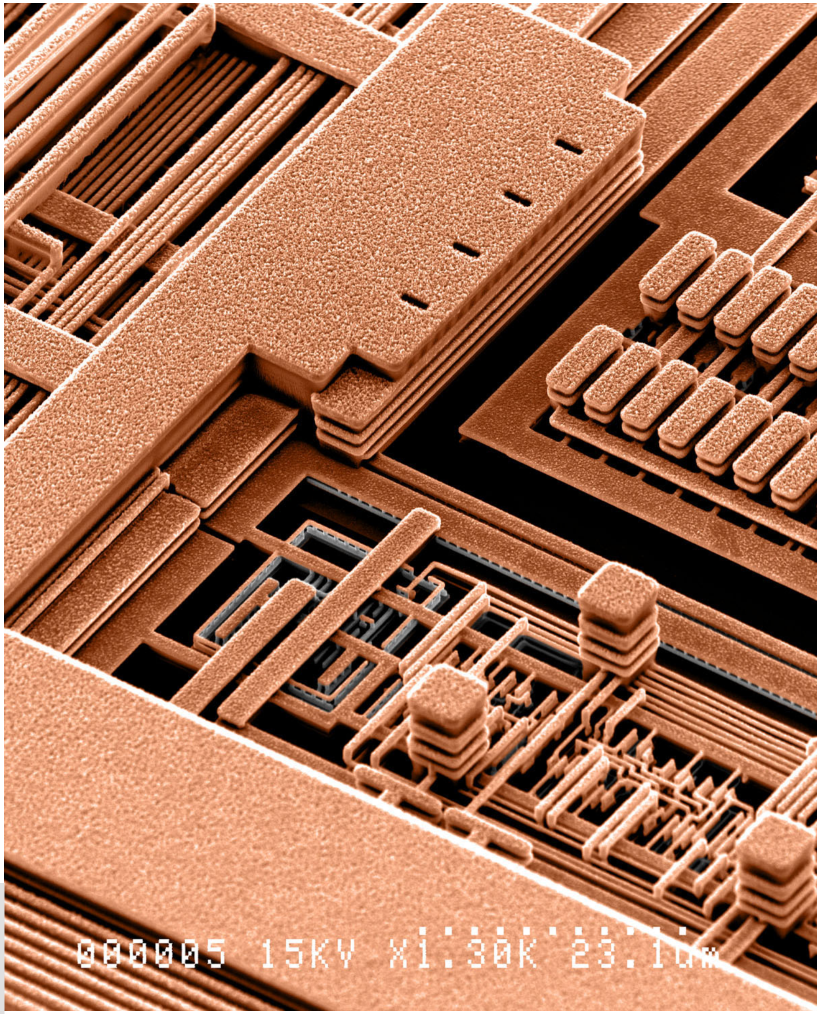


Wire Resistance



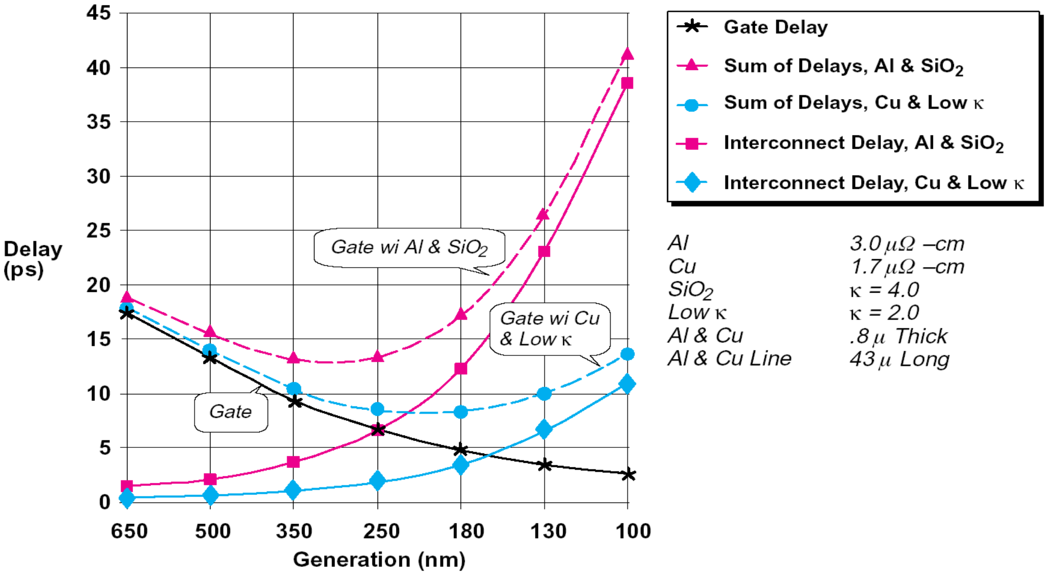
Intel wires in 32nm process

S. Natarajan et al. “A 32nm Logic Technology Featuring…”, IEDM 2008



IBM Cu wires
for 180 nm process

Parasitic capacitance



- Scaling of wires reaches an optimal of about 2pF/cm at 0.25-0.18 mm
- After that it gets substantially worse

Source: SIA 1997

Fundamental reasons

- At the very bottom the thermodynamic limit is [1]:

$$E_{min} = (\ln 2) * kT = 4\ 10^{-21} J$$

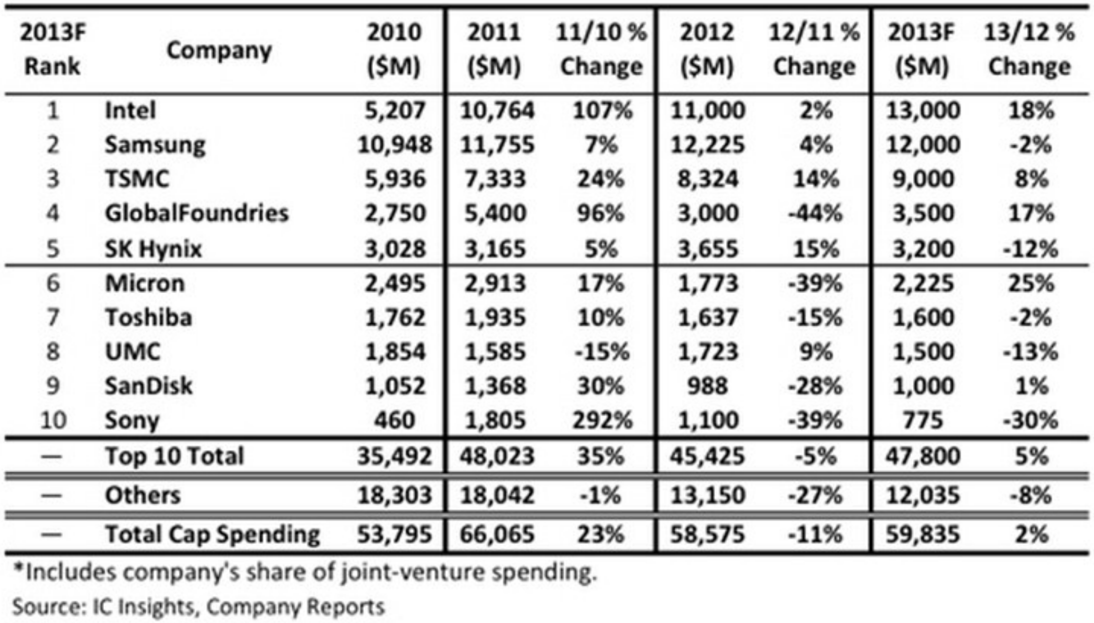
- Sub-threshold slope
  - Threshold voltage in MOS devices can not be scaled and supply voltage can not be scaled forever
- Atomic scale of transistors
  - Number of dopant atoms is getting small and Poisson’s law matters
    - matching becomes nightmarish
- Quantum mechanical leakage currents

---

[1] see: J. Meindl, J. Davis. “*The* Fundamental Limit on Binary Switching Energy for Terascale Integration (TSI)”, IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 35, NO. 10, OCTOBER 2000

Economic reasons

- If you spend 10B$ for new fabs, how many chips do you have to sells and with which profit margin to amortize your investment?



2013F Rank	Company	2010 ($M)	2011 ($M)	11/10 % Change	2012 ($M)	12/11 % Change	2013F ($M)	13/12 % Change
1	Intel	5,207	10,764	107%	11,000	2%	13,000	18%
2	Samsung	10,948	11,755	7%	12,225	4%	12,000	-2%
3	TSMC	5,936	7,333	24%	8,324	14%	9,000	8%
4	GlobalFoundries	2,750	5,400	96%	3,000	-44%	3,500	17%
5	SK Hynix	3,028	3,165	5%	3,655	15%	3,200	-12%
6	Micron	2,495	2,913	17%	1,773	-39%	2,225	25%
7	Toshiba	1,762	1,935	10%	1,637	-15%	1,600	-2%
8	UMC	1,854	1,585	-15%	1,723	9%	1,500	-13%
9	SanDisk	1,052	1,368	30%	988	-28%	1,000	1%
10	Sony	460	1,805	292%	1,100	-39%	775	-30%
—	Top 10 Total	35,492	48,023	35%	45,425	-5%	47,800	5%
—	Others	18,303	18,042	-1%	13,150	-27%	12,035	-8%
—	Total Cap Spending	53,795	66,065	23%	58,575	-11%	59,835	2%

*Includes company's share of joint-venture spending.

Source: IC Insights, Company Reports

CMOS Technology Roadmap

SLHC Designs to be frozen here

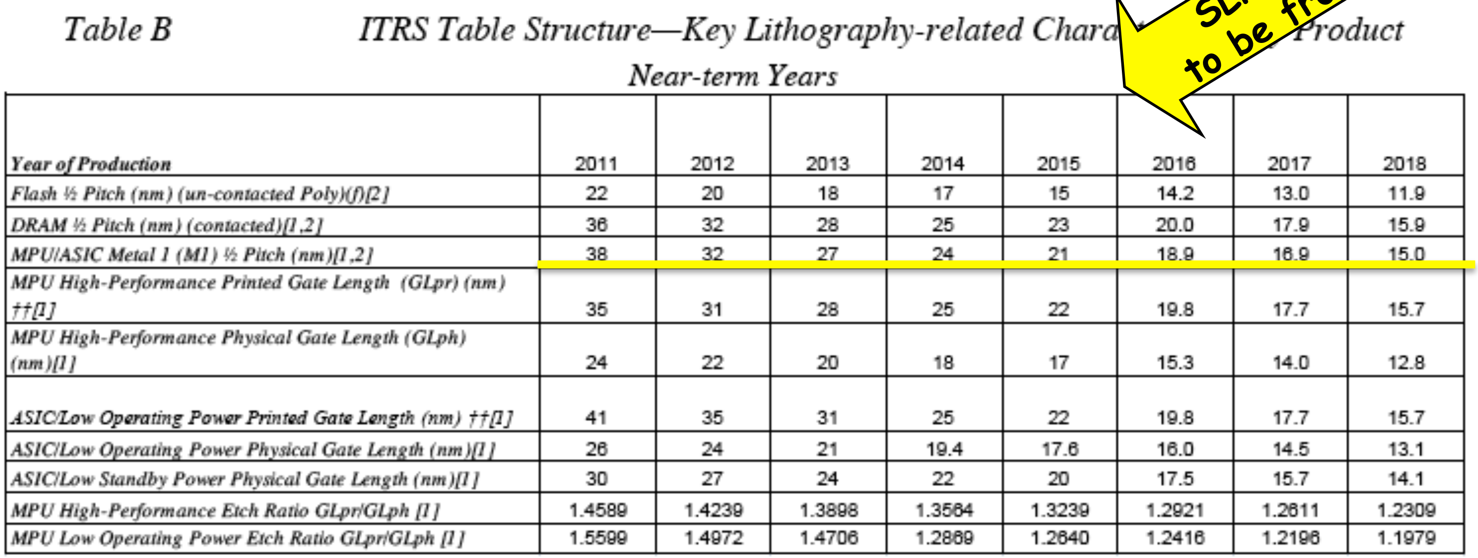


Table B *ITRS Table Structure—Key Lithography-related Chara* *Product*

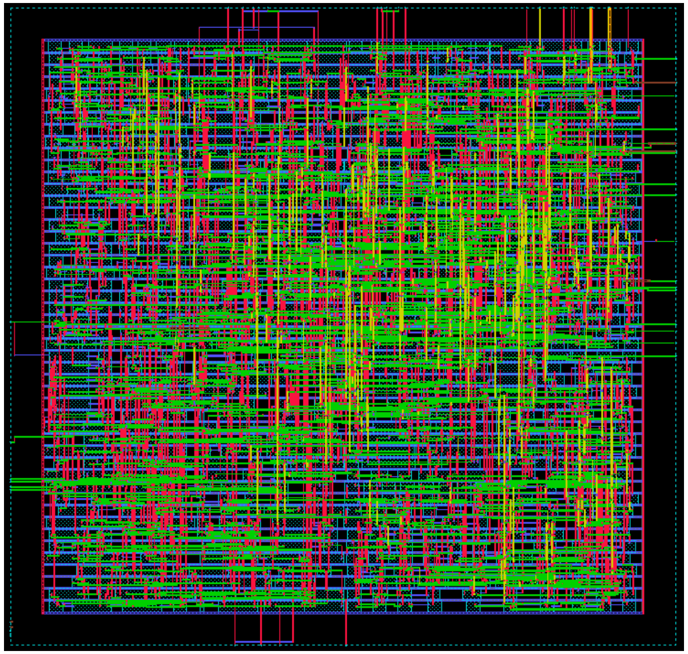
Near-term Years

Year of Production	2011	2012	2013	2014	2015	2016	2017	2018
Flash ½ Pitch (nm) (un-contacted Poly)(f)[2]	22	20	18	17	15	14.2	13.0	11.9
DRAM ½ Pitch (nm) (contacted)[1,2]	36	32	28	25	23	20.0	17.9	15.9
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)[1,2]	38	32	27	24	21	18.9	16.9	15.0
MPU High-Performance Printed Gate Length (GLpr) (nm) ††[1]	35	31	28	25	22	19.8	17.7	15.7
MPU High-Performance Physical Gate Length (GLph) (nm)[1]	24	22	20	18	17	15.3	14.0	12.8
ASIC/Low Operating Power Printed Gate Length (nm) ††[1]	41	35	31	25	22	19.8	17.7	15.7
ASIC/Low Operating Power Physical Gate Length (nm)[1]	26	24	21	19.4	17.6	16.0	14.5	13.1
ASIC/Low Standby Power Physical Gate Length (nm)[1]	30	27	24	22	20	17.5	15.7	14.1
MPU High-Performance Etch Ratio GLpr/GLph [1]	1.4589	1.4239	1.3898	1.3564	1.3239	1.2921	1.2611	1.2309
MPU Low Operating Power Etch Ratio GLpr/GLph [1]	1.5599	1.4972	1.4706	1.2869	1.2640	1.2416	1.2196	1.1979

From ITRS 2011 Executive Summary

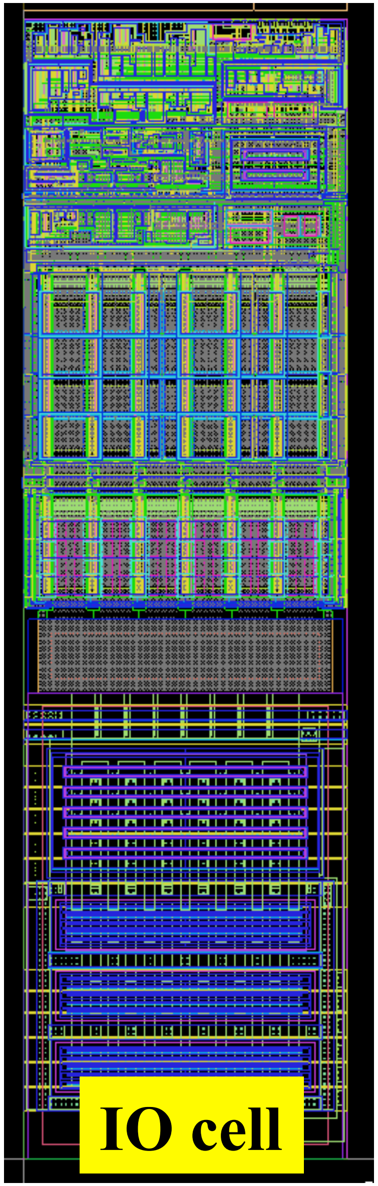
There is no doubt that industry ~~will be~~ is well ahead of the requirements from the HEP community, including HL-LHC, ILC etc.

Integration potential: Example in 130 nm



12 bit microprocessor core runs @ 330 MHz

Scale is the same



Interfacing to the "standard" world

- USB 2.0 OTG
  - ~ 20-60K Gates [1]
- Ethernet 10-100-1000 MAC
  - 20,560 gates [2]

- Notice that:
  - 1 mm^2 in 130 nm contains ~ 200K gates
  - 1 mm^2 in 65 nm contains ~ 800K gates
- …and
  - Production cost of 1 mm^2 in 130nm < 0.1 $
  - Production cost of 1 mm^2 in 65 nm < 0.15 $

---

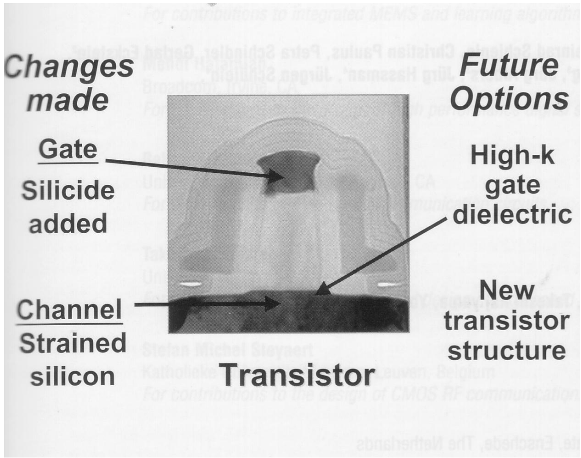
[1] http://www.faraday-tech.com/techDocument/FOTG200_ProdBrief_v1.2.pdf

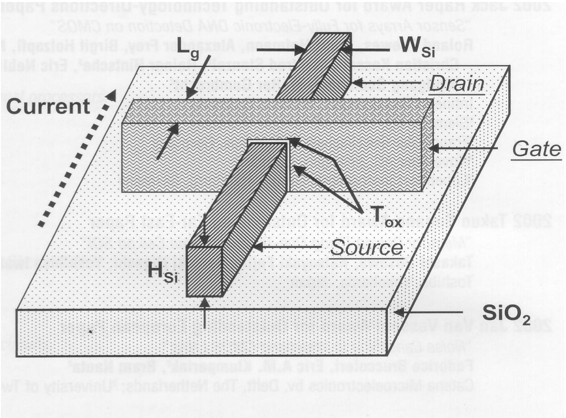
[2] http://opencores.org/project,ethernet_tri_mode

How many more generations?

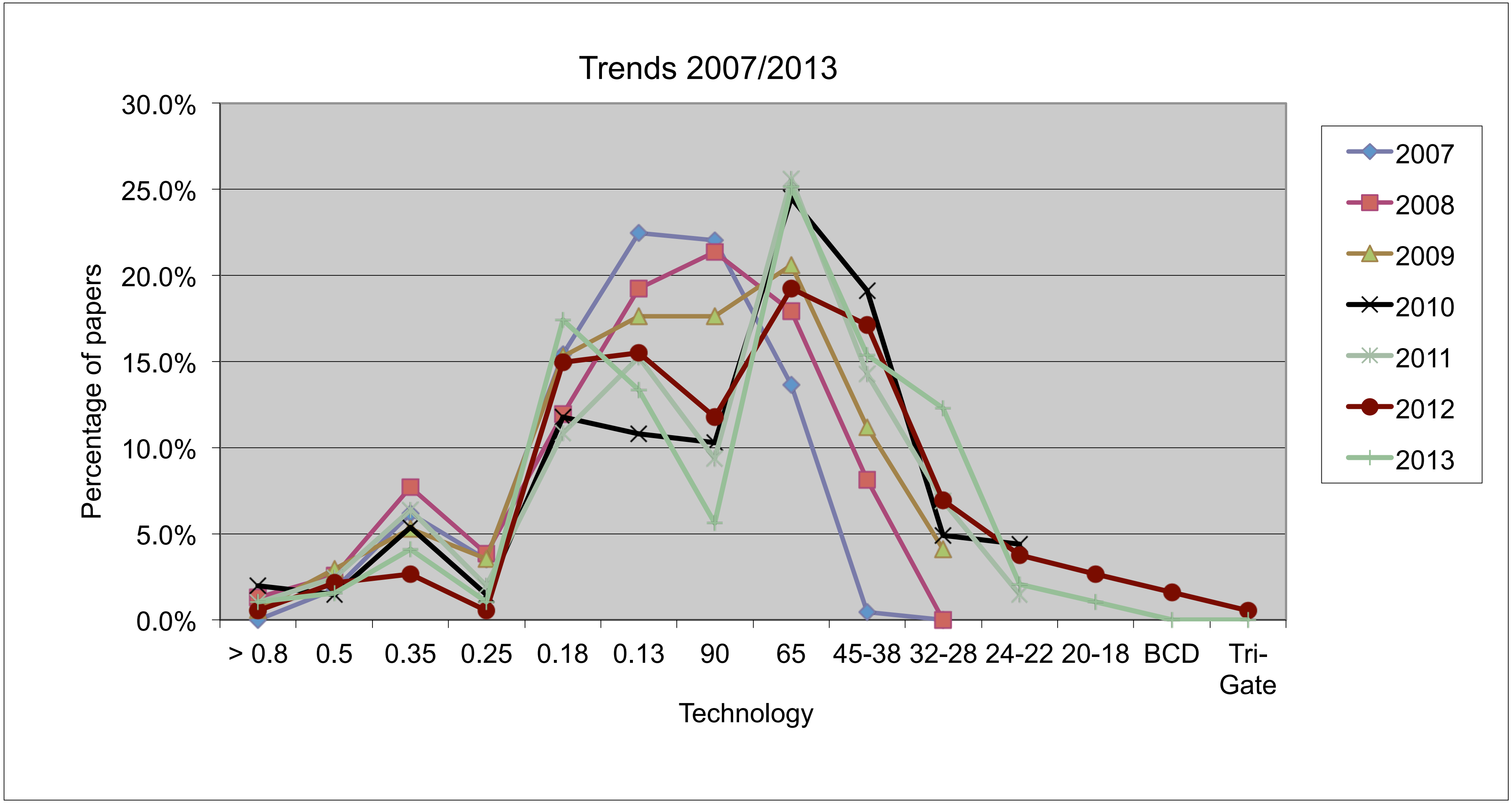
"The end of the planar FET is close, but perhaps one or two generations can be added if newer transistors can be made, for example the 'FINFET'"

G. Moore, 2003

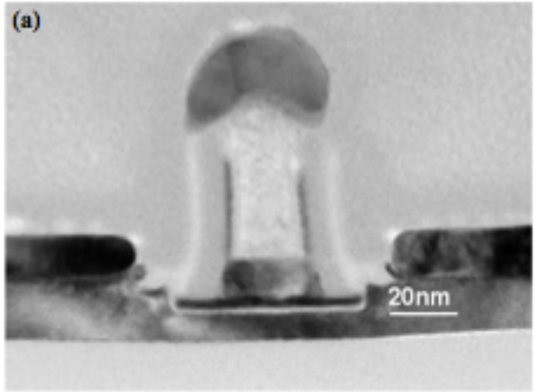




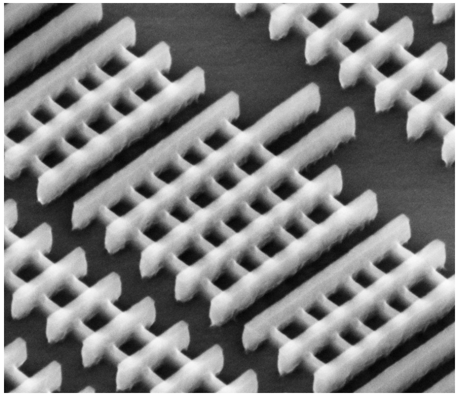
Technologies used in ISSCC papers



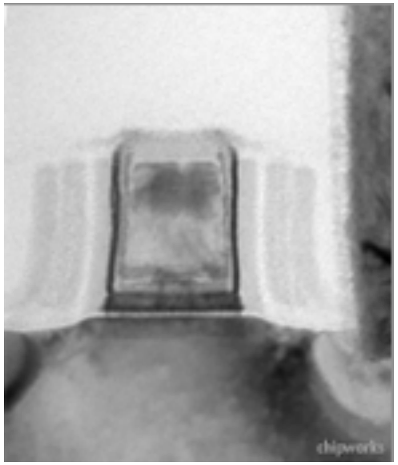
Some advanced devices



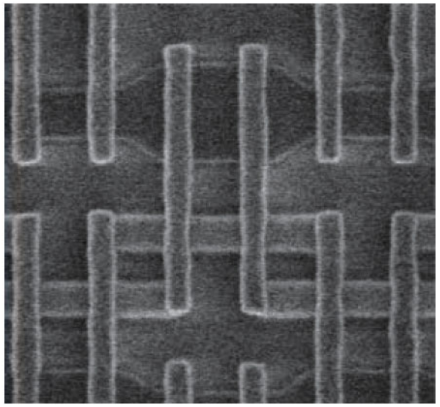
20 nm FDSOI from ST



22 nm TriGate from Intel



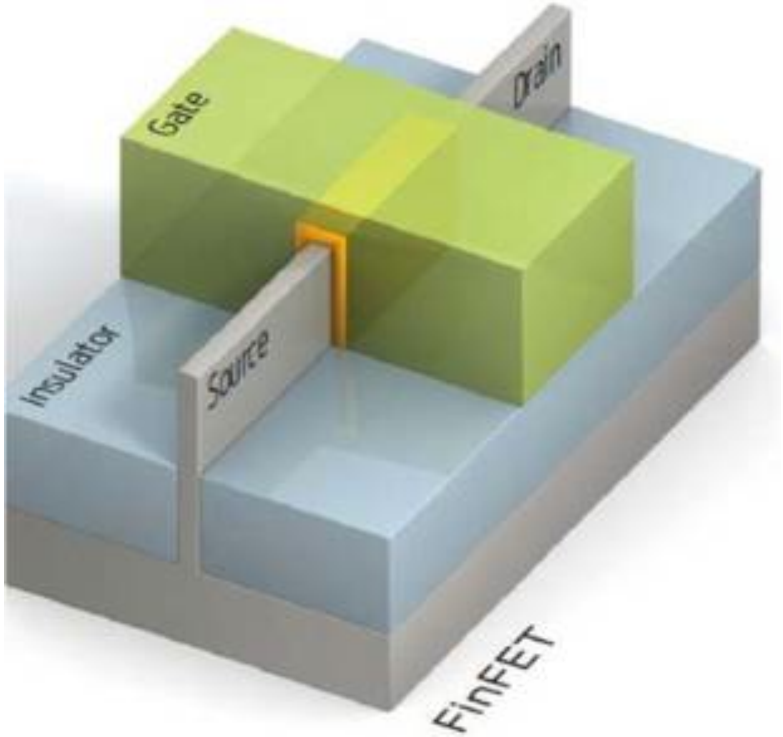
28 nm planar from TSMC



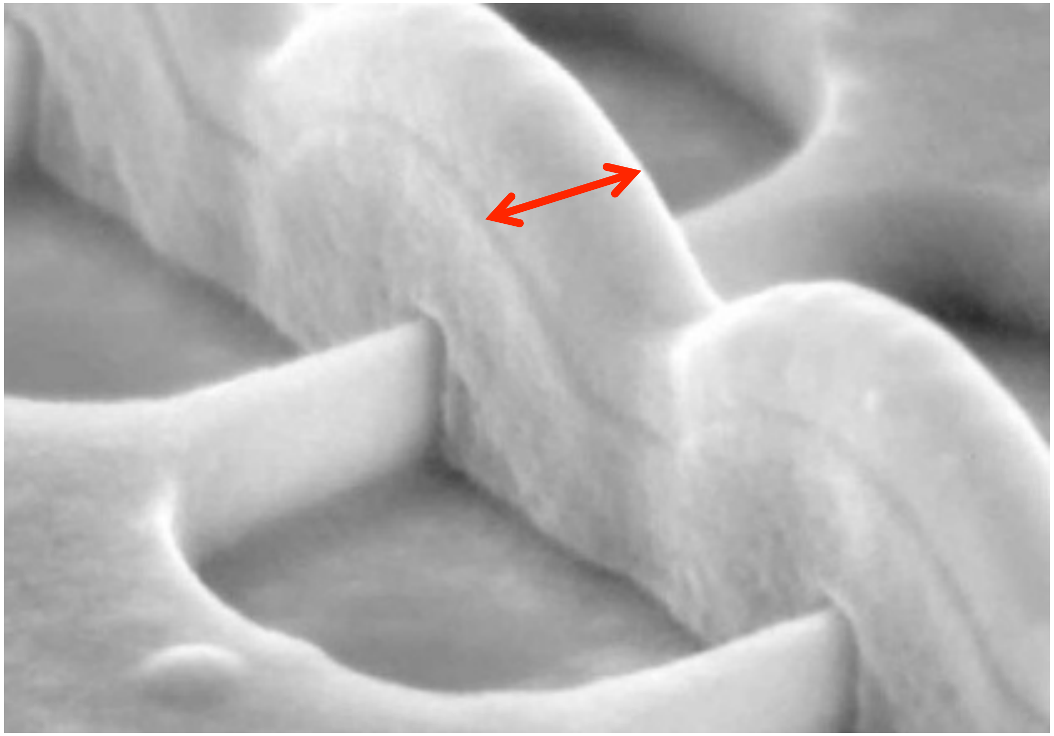
32 nm SOI from IBM

Various sources

16 nm FINFET

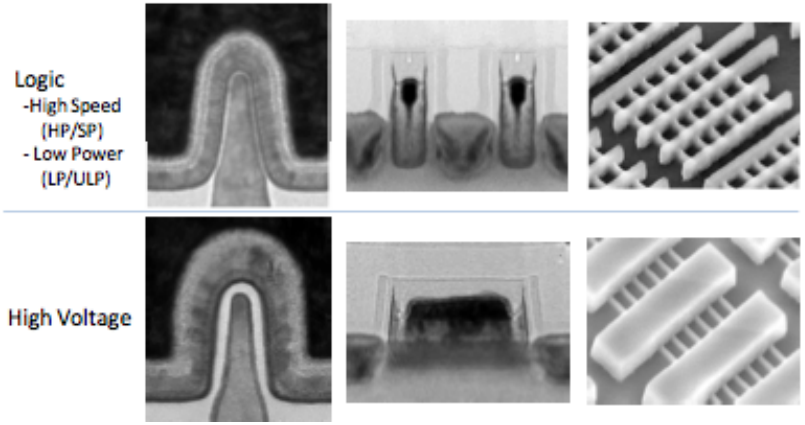


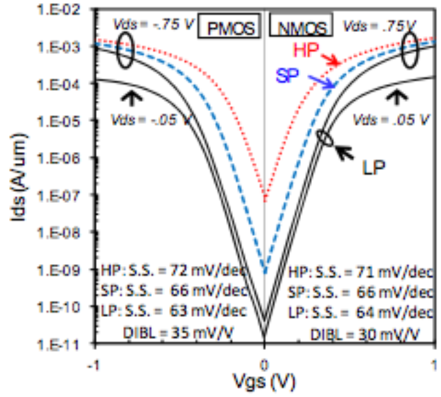
16 nm

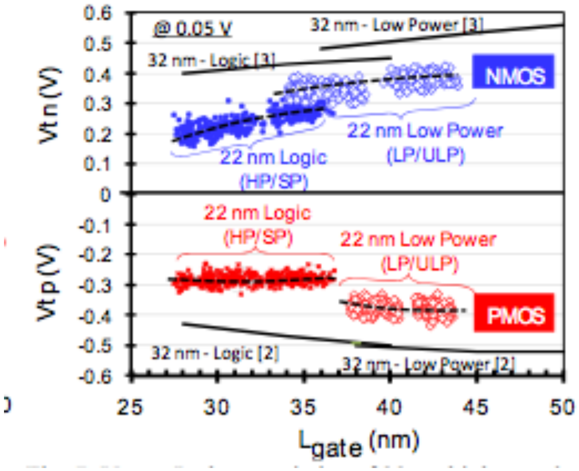


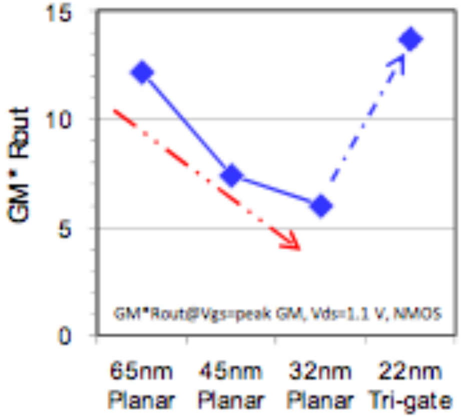
Source: TSMC

… and still, devices behave very well





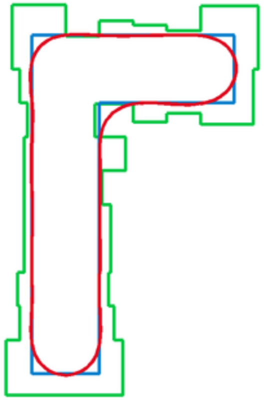


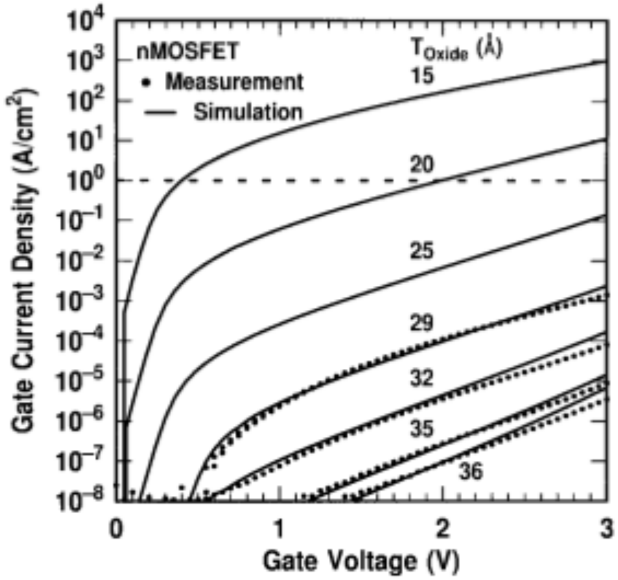


©permission IEEE, C.-H. Jan et al., A 22nm SoC Platform..., IEDM12-44,

Technology enablers

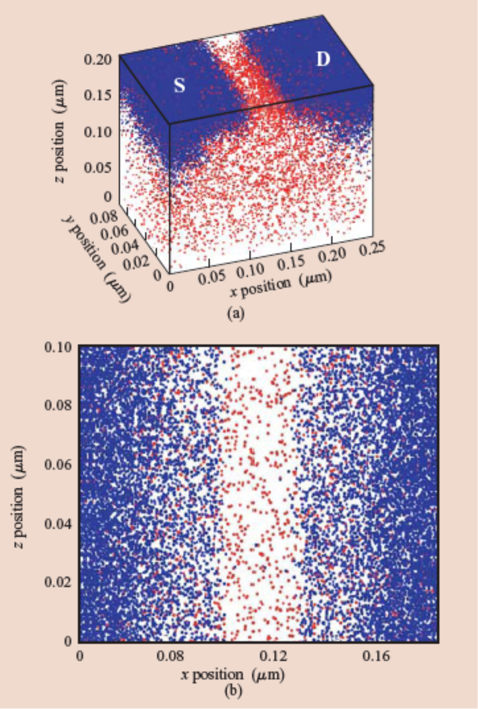
- Lithography
  - Solution: turn the problem up-side-down to work to your advantage!
  - OPC
    - Correct mask and process distortions by synthesizing masks and not by introducing shorter wavelength
  - Double and multiple patterning
    - Build images by superimposing patterns
- New materials
  - SOI wafers (reduce parasitic capacitances)
  - Si-Ge and channel stress (enhance mobility)
  - Gate oxide materials (need to avoid leakage currents)
  - Metal gates (avoid problem of poly depletion), lower F





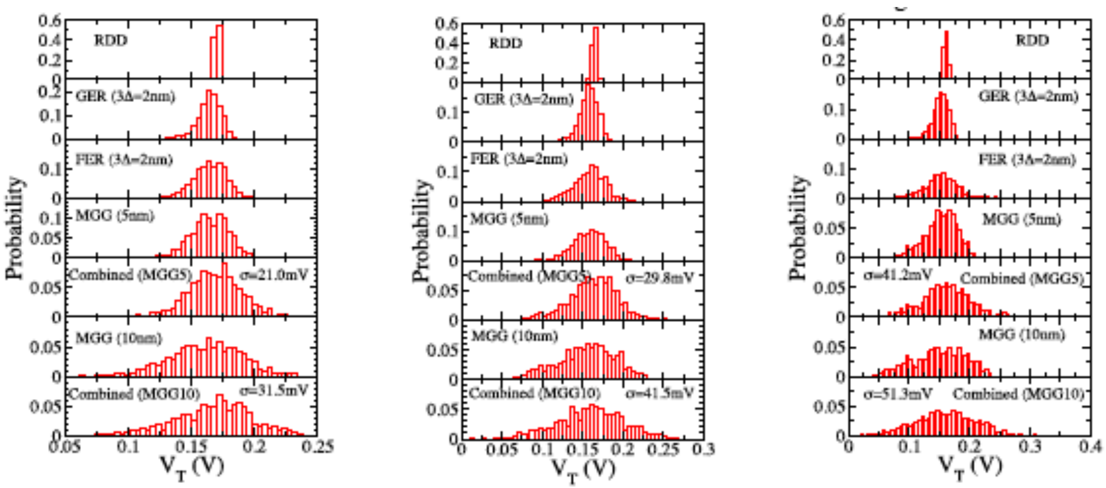
© permission IEEE, S.H. Lo et al.,Quantum-Mechanical Modeling… IEEE JSSC 18,5, 1997

Atomic Scale Variability



Atomistic view of dopants in 50nm transistor

from K. Bernstein et al.,
IBM J. Res. & Dev. Vol. 50 No. 4/5, 2006



Distribution of Vt on three generations of FinFETS, 20nm, 14nm, 10nm

from X. Wang et al.,
IEDM 2011,

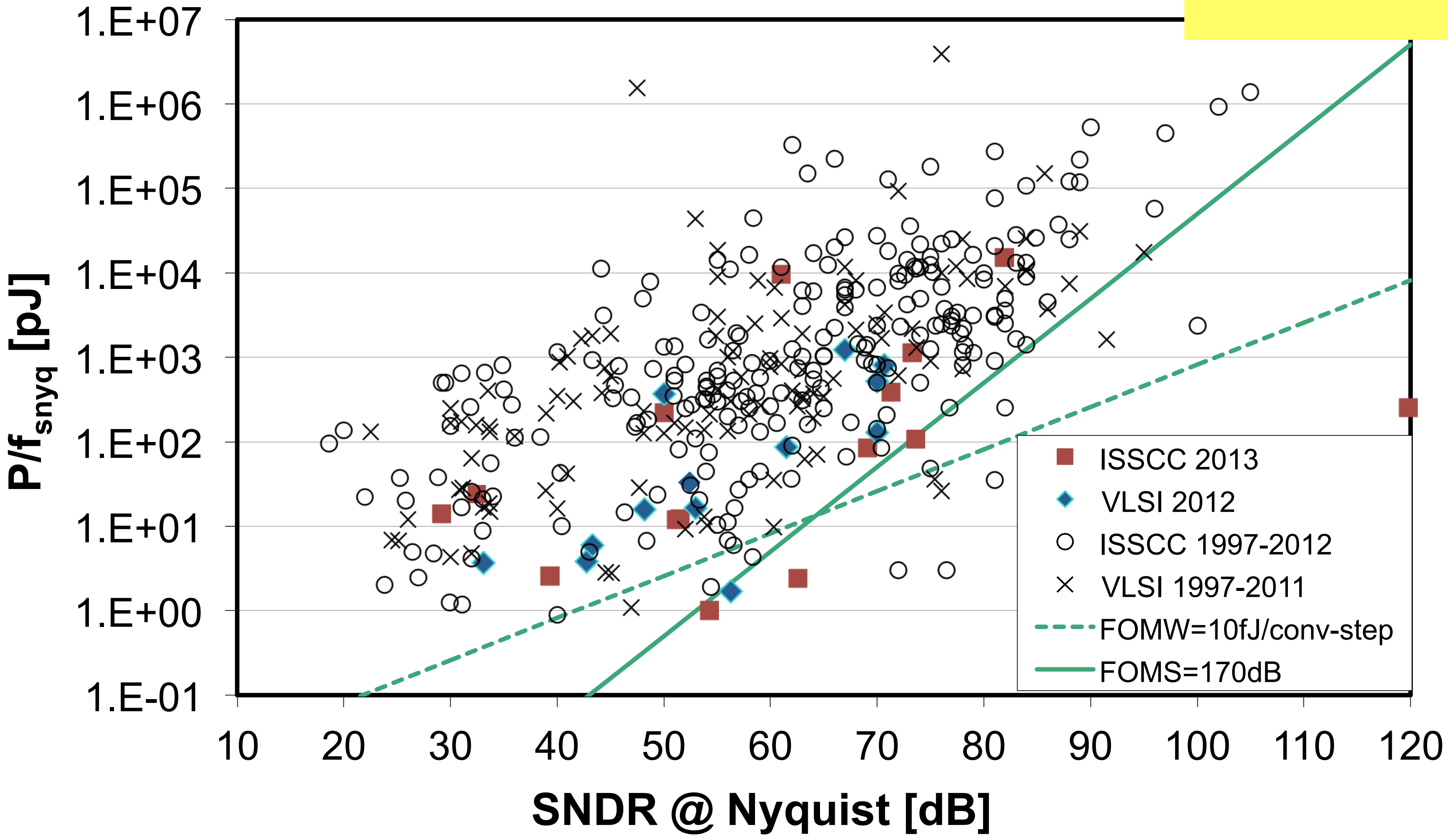
Some looming difficulties

- Device variability
  - transistors have atomic dimensions: dopants are in "countable" number, oxides are few atomic layers thick
- Slow lithography
  - short wavelength powerful light sources are hard to make
- Cost of new foundry
  - Sub-20nm fab > 5B$
- Design complexity
  - number of devices (all must work, both functionally and physically!)
  - variability implies huge simulations

Advances in ADCs

$$FM = \frac{Power}{Freq * 2 \wedge ENOB}$$

$$ENOB = \frac{(SNDR - 1.76)}{6.02}$$



Courtesy of Prof. B. Murmann, Stanford University

Improvements in ADC

- For Tracker
  - Assuming FM for ADC of: 2.5e-13 J/op
  - f_{sample} = 40 MHz
  - N_{bit} = 6 (with ENOB = 5)
  - 128 channels/chip
  - Total Conversion Power: 40 mW
    - to be compared to today's total FE chip power of ~320 mW
- For Calorimeter
  - Assuming FM for ADC of: 2.5e-13 J/op
  - f_{sample} = 40 MHz
  - 14 bit converter
  - Conversion: 82 mW
    - To be compared with 125 mW today for a 12 bit device [CMS ecal]

The places to read and publish are:

IEEE TRANSACTIONS ON
ELECTRON DEVICES

A PUBLICATION OF THE IEEE ELECTRON DEVICES SOCIETY

APRIL 2005 VOLUME 52 NUMBER 4 IETDAI (ISSN 0018-9383)

(Contents Continued on Back Cover)

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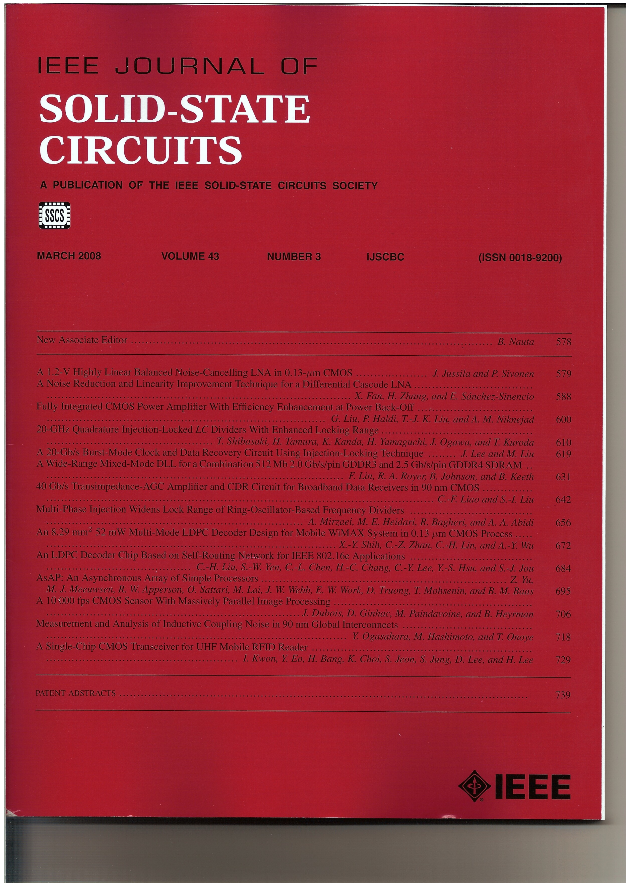

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A PUBLICATION OF THE IEEE SOLID-STATE CIRCUITS SOCIETY

SSCS

MARCH 2008 VOLUME 43 NUMBER 3 IJSCBC (ISSN 0018-9200)

IEEE

…and the conferences are:

2013 INTERNATIONAL ELECTRON DEVICES MEETING

Washington, DC

With a history stretching back nearly 60 years, the IEEE International Electron Devices Meeting (IEDM) is the world's pre-eminent forum for reporting technological breakthroughs in the areas of semiconductor and electronic device technology, design, manufacturing, physics, and modeling. IEDM is the flagship conference for nanometer-scale CMOS transistor technology, advanced memory, displays, sensors, MEMS devices, novel quantum and nano-scale devices and phenomenology, optoelectronics, devices for power and energy harvesting, high-speed devices, as well as process technology and device modeling and simulation. The conference scope not only encompasses devices in silicon, compound and organic semiconductors, but also in emerging material systems. IEDM is truly an international conference, with strong representation from speakers from around the globe.

In 2013 there is once again an increased emphasis on circuit and device interaction. With ever increasing transistor count, nanometer design rules and layout restrictions, circuit-device interaction is becoming critical to providing viable technology solutions. This new emphasis includes technology/circuit co-optimization, power/performance/area analyses, design for manufacturing and process control, as well as CMOS platform technology and scaling.

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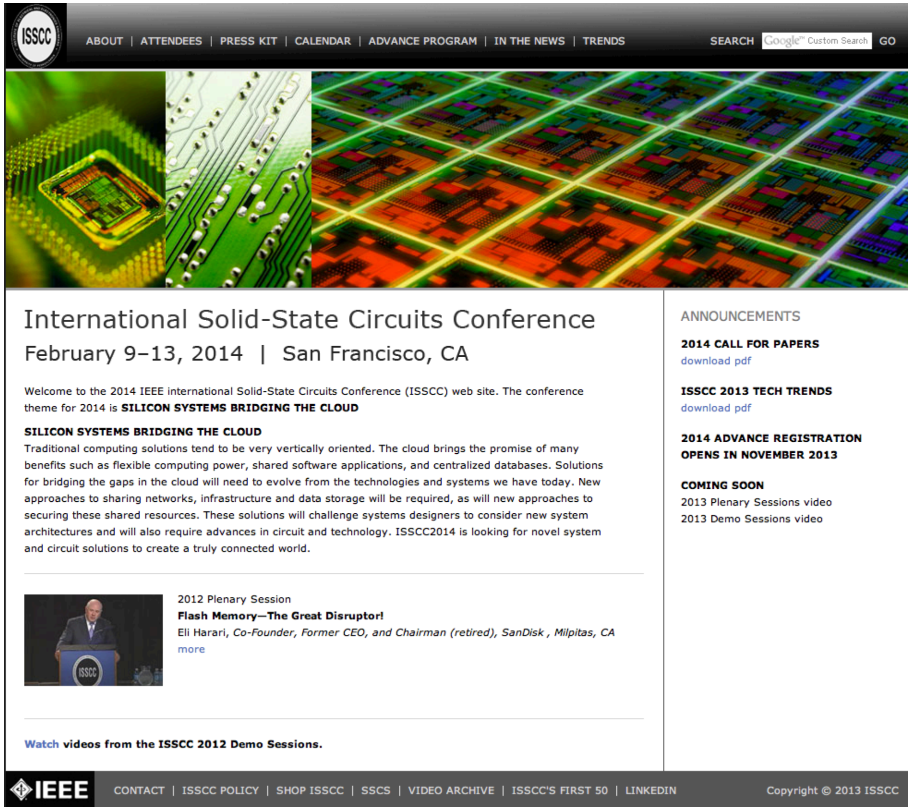

International Solid-State Circuits Conference

February 9–13, 2014 | San Francisco, CA

Welcome to the 2014 IEEE international Solid-State Circuits Conference (ISSCC) web site. The conference theme for 2014 is **SILICON SYSTEMS BRIDGING THE CLOUD**

SILICON SYSTEMS BRIDGING THE CLOUD

Traditional computing solutions tend to be very vertically oriented. The cloud brings the promise of many benefits such as flexible computing power, shared software applications, and centralized databases. Solutions for bridging the gaps in the cloud will need to evolve from the technologies and systems we have today. New approaches to sharing networks, infrastructure and data storage will be required, as will new approaches to securing these shared resources. These solutions will challenge systems designers to consider new system architectures and will also require advances in circuit and technology. ISSCC2014 is looking for novel system and circuit solutions to create a truly connected world.

2012 Plenary Session

Flash Memory—The Great Disruptor!

Eli Harari, *Co-Founder, Former CEO, and Chairman (retired), SanDisk , Milpitas, CA*

more

Watch **videos from the ISSCC 2012 Demo Sessions.**

ANNOUNCEMENTS

2014 CALL FOR PAPERS
download pdf

ISSCC 2013 TECH TRENDS
download pdf

2014 ADVANCE REGISTRATION OPENS IN NOVEMBER 2013

COMING SOON
2013 Plenary Sessions video
2013 Demo Sessions video

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Reading suggestions

(if you read only one book of electronics in your career, start from:)

- Y. Tsividis, C. McAndrew, *Operation and Modeling of the MOS Transistor*, OUP 2011
- B. Razavi, *Fundamentals of Microelectronics*, Wiley 2008
- T.C. Carusone, D.A. Johns, K.W. Martin, *Analog Integrated Circuit Design*, Wiley 2012
- History of microelectronics technology
  - M. Riordan, “Crystal Fire: The Birth of the Information Age”
  - A. Grove, “Only the Paranoid Survive”

Techno Movies

https://dl.dropboxusercontent.com/u/2961692/VLSI%20Movies/1%20-%20The%20Birth%20of%20the%20Transistor%20-%201%20of%204.mp4
https://dl.dropboxusercontent.com/u/2961692/VLSI%20Movies/1%20-%20The%20Birth%20of%20the%20Transistor%20-%202%20of%204.mp4
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https://dl.dropboxusercontent.com/u/2961692/VLSI%20Movies/Microchip%20production%20part%202.flv
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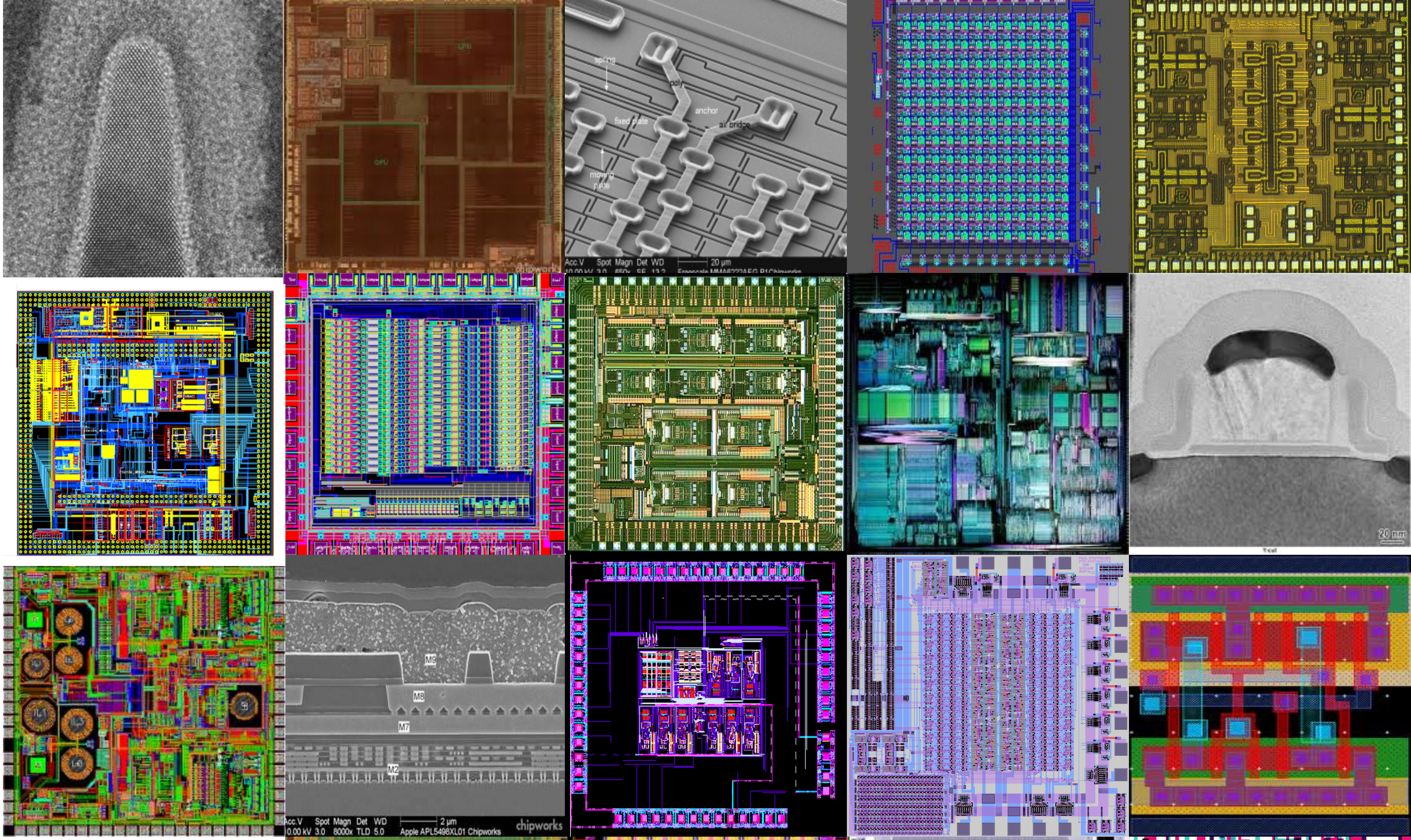
Thank you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GPU
chipworks
spring
poly
anchor
air bridge
fixed plate
moving plate
Acc.V Spot Magn Det WD 20 µm
Freescale MMA6222AEG R1 Chipworks
20 nm
M9
M8
M7
M2
Acc.V Spot Magn Det WD 2 µm
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