FPGA Based L1 Pixel Trigger

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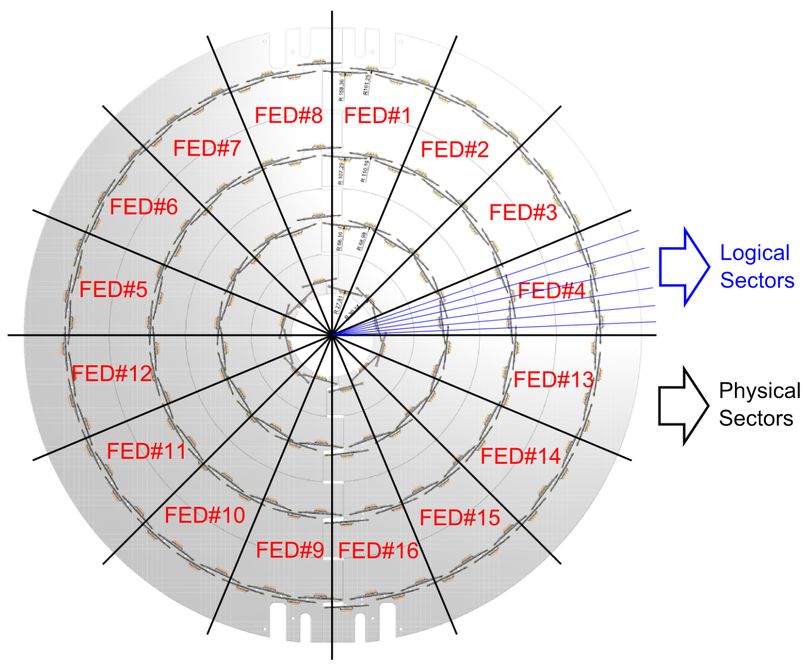
Overview

In order to improve the performance of the trigger of data acquisition in the FED, i.e. to select only the data associated with events, a pixel-level trigger is proposed. The method aims to analyze trajectories of particles that go through the pixels and identify paths that form an almost straight line. Two algorithms have been employed: the Combinatorial and the Straight Line Algorithm. The Straight Line Algorithm was devised as a simpler solution that also requires less hardware resources to process data. The concept of logical sectors is also introduced and its major benefit is the significant reduction in the amount of data that needs to be processed. A true parallel FPGA approach is proposed and the simulated results demonstrate the great processing power of this tool.

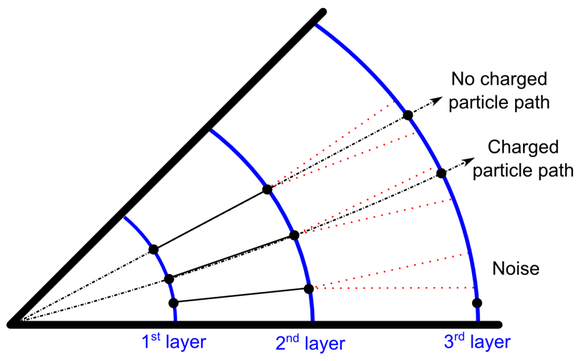
Time and Sector Slicing Algorithm

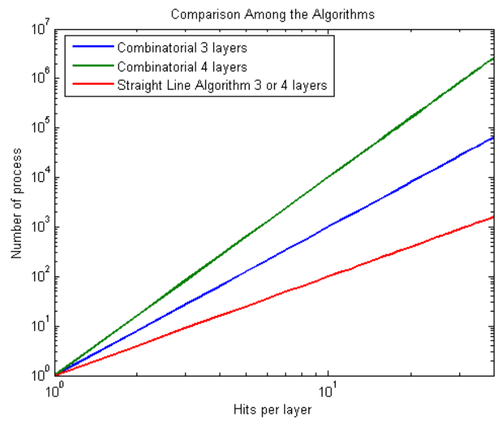
Divide and conquer!



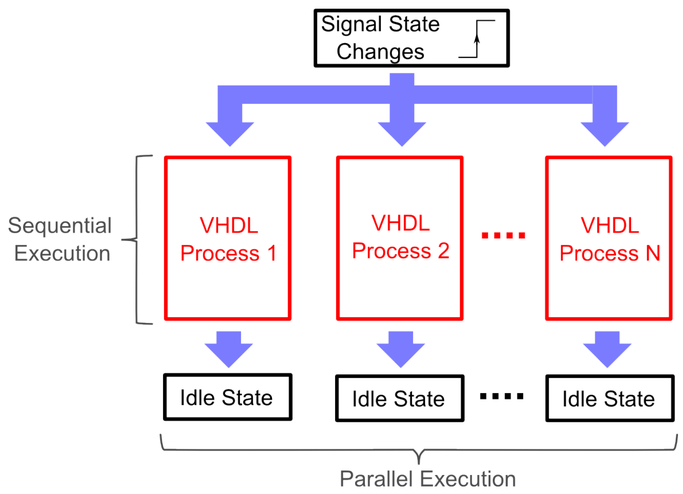
- A Physical Sector is determined by a FED
- The Logical Sectors proposed by this research constitute subdivisions of a Physical Sector
- It is a useful method to reduce the amount of data to be analyzed
- Less processes in a combinatorial analysis

Straight Line Algorithm



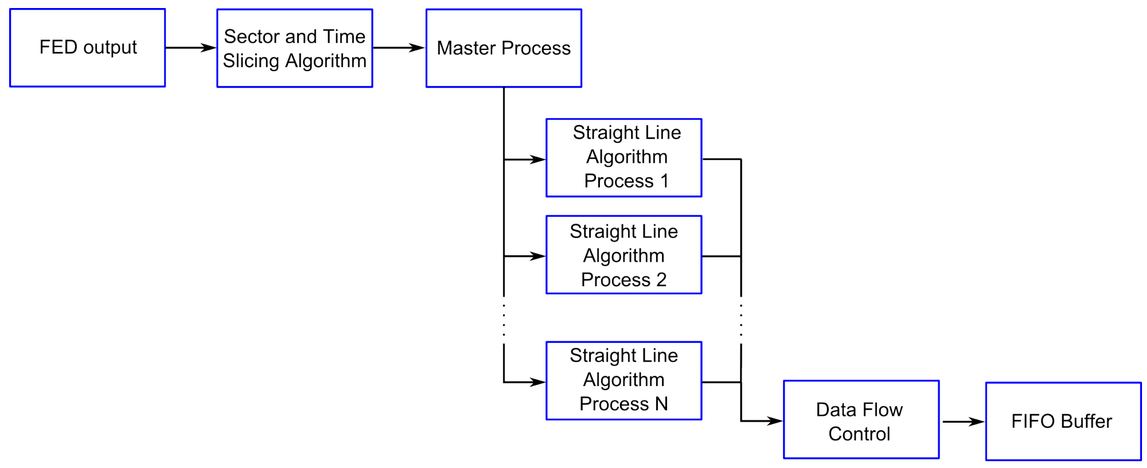


- An event produces rectilinear traces
- Due to the existence of charged particles, certain deviation should be considered
- Two methods: Combinatorial and Straight Line Algorithm (Proposed)
- In a Combinatorial Algorithm: $N = H^L$
- In the Straight Line Algorithm: $N = H^2$
  where N is the number of processes, H is Hits per layer and L is the number of layers



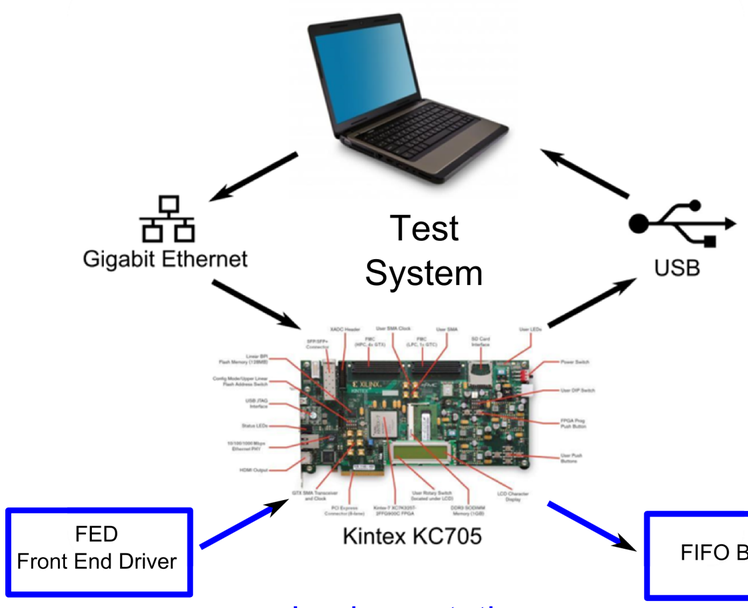
- Different processes are executed in parallel
- The code inside each process is executed sequentially
- Any state change of a signal located in the sensibility list causes an execution of a process

Data Flow



- Data from FED is read by the FPGA and organized by Events and Logical Sector
- The master process distributes tasks to the other processes
- Every Straight Line Algorithm process runs in parallel
- There is a Data Flow Controller to avoid collisions while writing in the FIFO

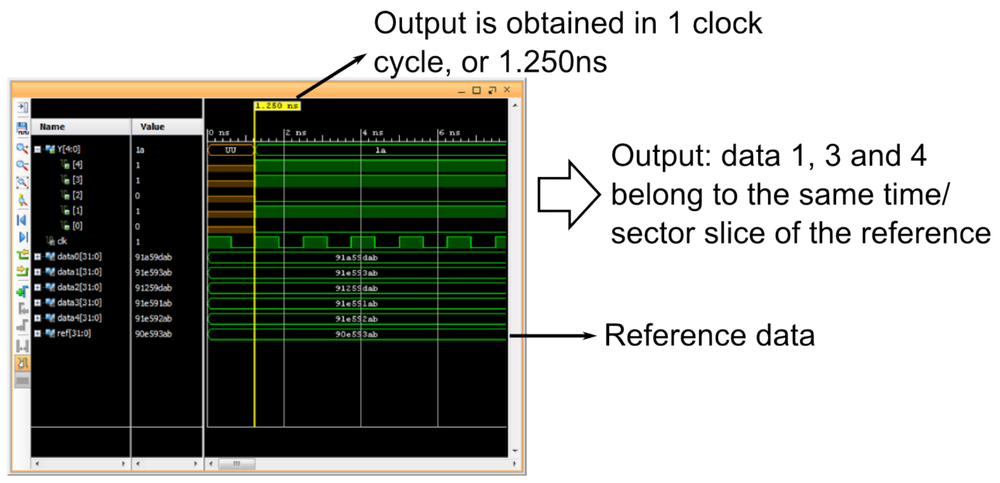
Test and Implementation



Implementation

- In the test system, a computer feeds the FPGA with real data
- The bandwidth is determined by the Gigabit Ethernet interface
- This test can achieve $1/5$ of the FED throughput
- The system with FED: throughput of 40 million packages per second, each packet being 64bits long
- An event can produce information of 250 pixels in an FED $\rightarrow$ Necessity of Logical Sections

Results



- The FPGA behavioral simulation runs on an $800MHz$ Clock
- Considering the data throughput, the FPGA has $25\eta s$ to process the stack $\rightarrow$ 20 clock cycles
- Only one clock cycle was used to process the algorithms of time and sector slicing
- 19 cycles remain available for the Straight Line Algorithm

Acknowledgements

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References

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[2] M. Barbero, “Development of a Radiation-Hard Pixel Read Out Chip with Trigger Capability”, (2003).
[3] CMS Collaboration, “CMS Technical Design Report for the Pixel Detector Upgrade”, (2012).