Intelligent front-end for pixel based instruments: front-end and novel ideas

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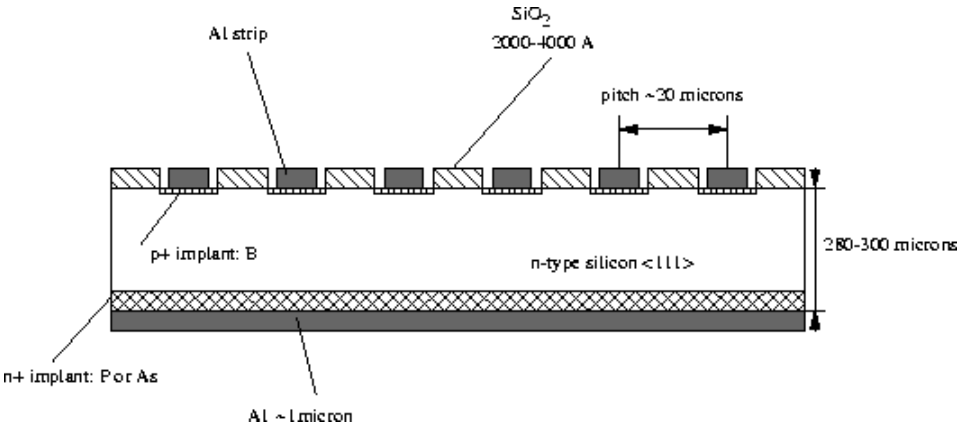
Outline

- Generalities on readout electronics (mostly) for pixel detectors: signal processing, readout chip floorplan, interconnection, technologies
- Enabling technologies for intelligent pixel detectors: evolution of technologies for readout chips, CMOS technologies, vertical integration
- Some examples of intelligent pixel detectors: in-pixel functionalities, pixel level sparsification

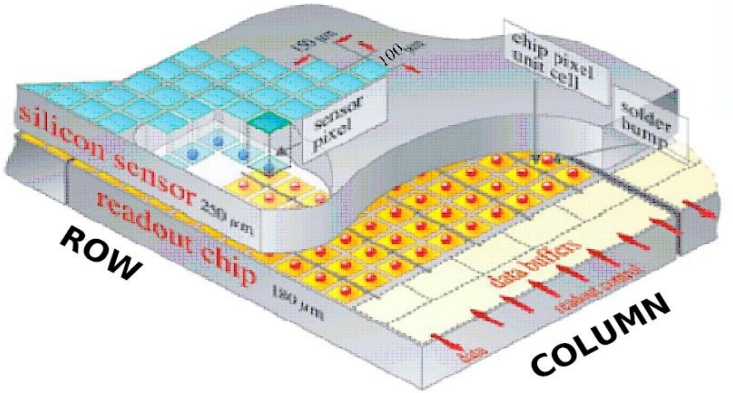
Radiation detectors

- Radiation detection systems may be used to measure
  - the amount of energy released by a particle (a charged one, or a photon) while passing through the sensor volume
  - the position (in one or two dimensions) of a particle passing through the surface of a detector (to be intended as a set of sensors with a given geometrical arrangement)
  - the time of arrival of a particle
  - the number of particles hitting the detector, or the total energy released by those particles in a given position
- Semiconductor microstrip and pixel detectors are used to measure the position of a particle hitting the detector surface (they are also called position-sensitive detectors)

Microstrip detectors



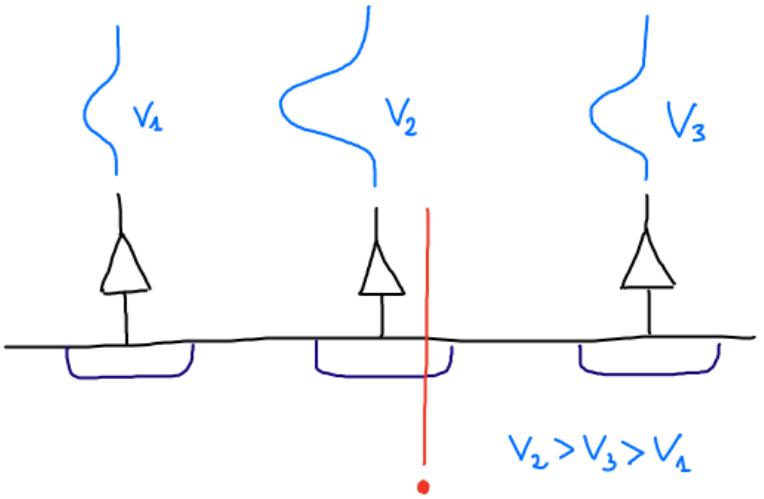
Pixel detectors



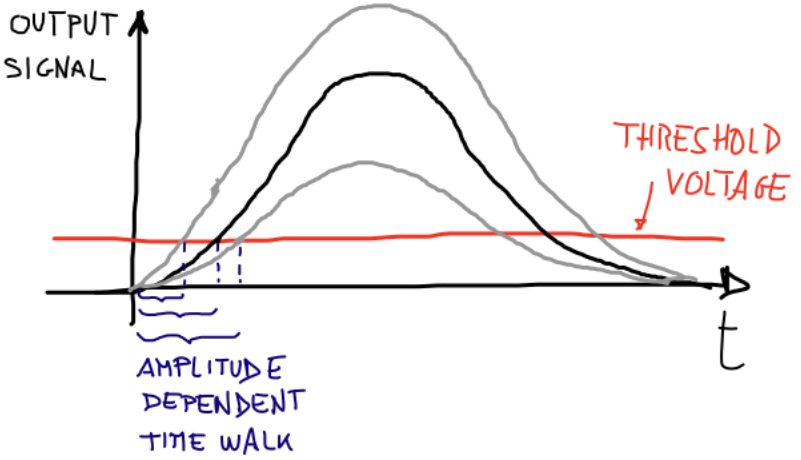
Analog signal processing

- Depending on the application and on the required spatial resolution, semiconductor microstrip and pixel detectors, together with the relevant readout electronics, may be required to provide also information on the amount of energy the particle has released in the sensor volume (amplitude measurement)
- The signal from a capacitive detector is first read out by an analog processing channel, which in its optimum version includes a charge preamplifier and a shaper for signal-to-noise ratio optimization
- A discriminator is generally used to compare the signal at the shaper output to a preset threshold voltage, therefore providing information about the presence of an interesting event (hit/no hit information)

Center of mass of a cluster



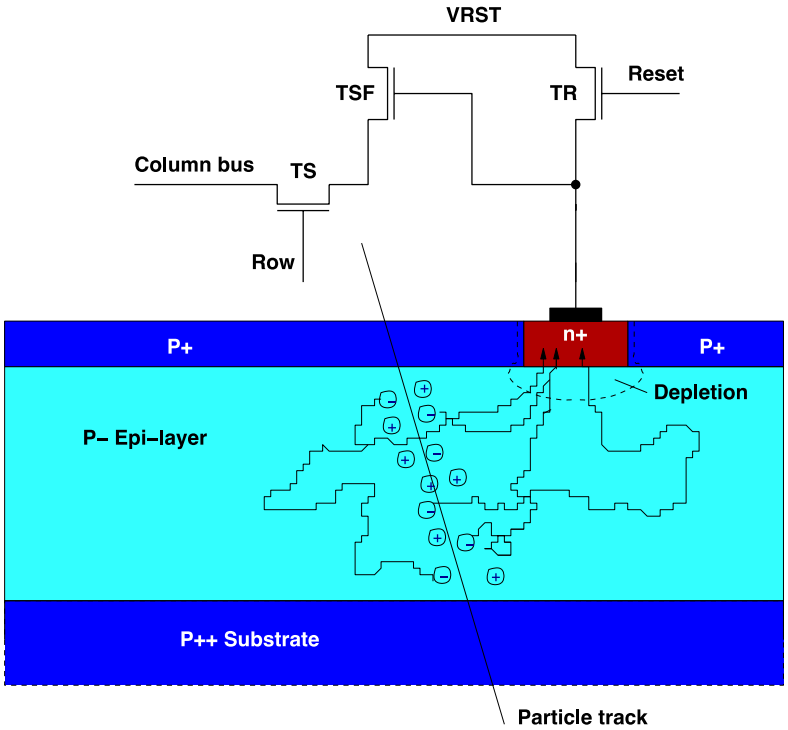
Hit time calculation



Readout architectures

- The digital hit signal at the discriminator output must be further processed by circuitry in the pixel or at the chip periphery; processing may just involve reading out the single hit/no hit bit of information or using it to perform more complex operations
- Choice of the set of operations to be performed on the data collected in a detector before sending them out (implemented in the readout architecture) depends on the target application
- Also the design approach (hybrid vs monolithic) and the available technology may impact on the design of the readout chip; evolution (scaling down) of CMOS technologies and, in general, of microelectronic processes (vertical integration) may help improve performance and include more functionalities in the readout circuits

Monolithic sensor



Functionalities and intelligence

- The task of the front-end is measuring the charge delivered by a capacitive source with the best accuracy compatible with the intrinsic noise of the readout circuit and with the constraints set by the application

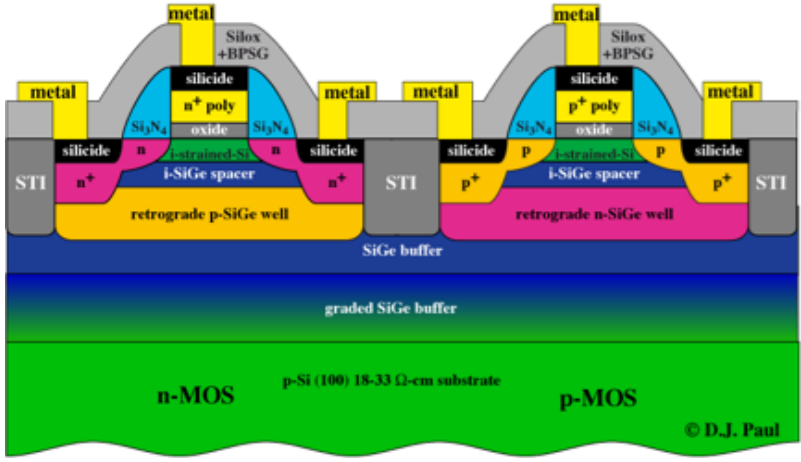
noise – power – speed - area

- Finding the best compromise may imply using additional blocks (in the pixel or at the chip level), adding functionalities, extend the set of operations performed on chip
- On-chip intelligence generally includes the set of functions performed directly on data, inside the pixel, at the chip level or in a more complicated chip assembly: A-to-D conversion, zero suppression, data sparsification, buffering, encoding, lossless compression, error correction, serialization, track discrimination, histogramming
- Other blocks, not necessarily acting on the signal, are used to improve the performance of the in-pixel readout channel or of the chip as a whole, for example by adjusting or calibrating some parameters or by transferring to the chip what was previously done outside: threshold correction circuits, gain calibration, polarity selection, baseline restoration, DC-DC conversion, clock generation, I/O communication, logic level conversion

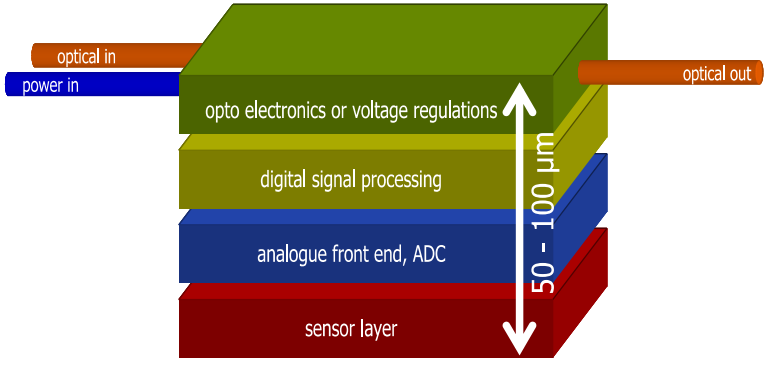
Application needs and technologies

- The driving force for the increasing functional density of readout chips for radiation detectors is given by the need for:
  - higher granularity (smaller pileup, capability for track separation)
  - higher speed (capability for processing hits at a higher rate)
  - data reduction (to limit the bandwidth requirements for transmission to DAQ)
  - higher degree of radiation hardness
- The advance in readout chip design is mainly enabled by
  - evolution of CMOS processes
  - development of interconnection techniques and vertical integration technologies

CMOS technology



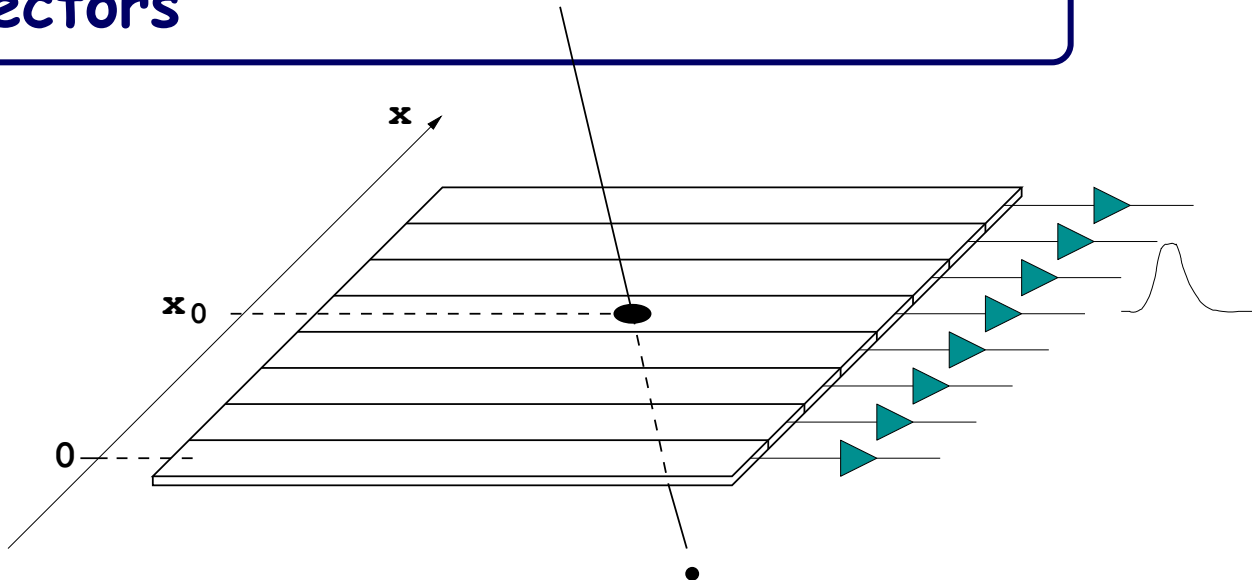
3D integration



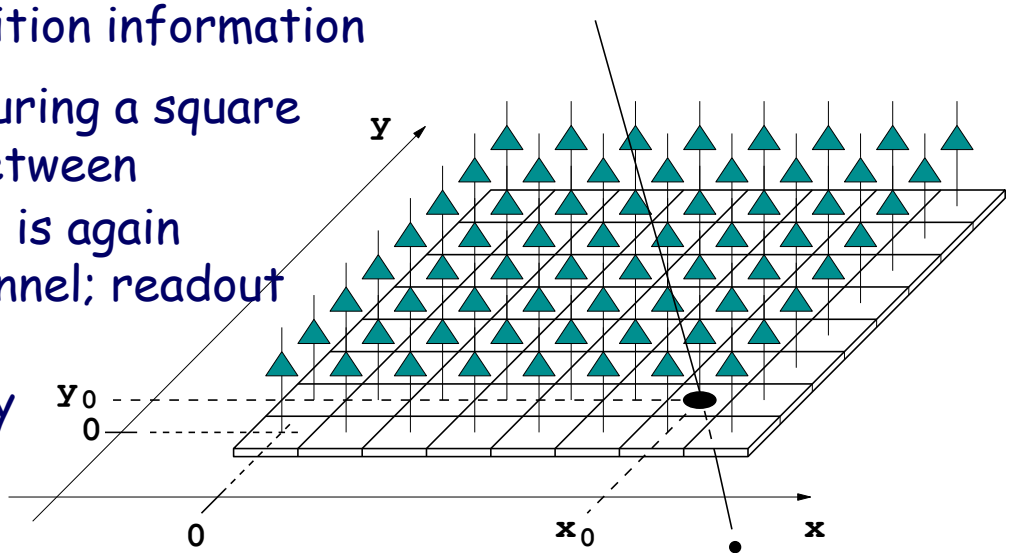
Generalities on readout electronics for pixel detectors

Microstrip and pixel detectors

- In a microstrip detector, each sensor element has the shape of an elongated strip (up to a few cm long) and is read out by a dedicated processing channel; readout channels are arranged in arrays of several tens or hundreds of elements; typical pitch is in the order of a few tens of μm up to 100 μm; a microstrip detector provides monodimensional position information

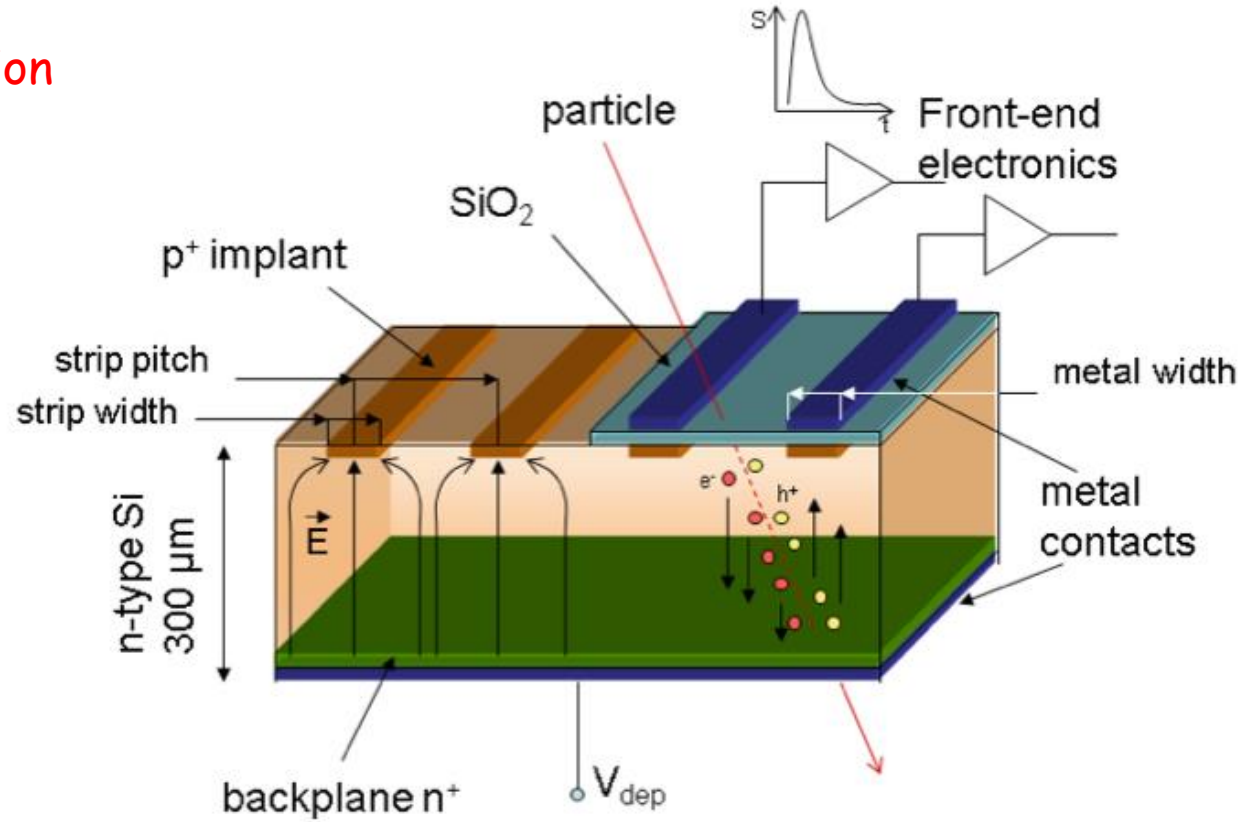


- In a pixel detector, each element, featuring a square or rectangular shape (pitch may vary between several tens and a few hundreds of μm) is again read out by a dedicated processing channel; readout channels are arranged in matrices including a few thousands of elementary cells; a pixel detector provides bidimensional position information



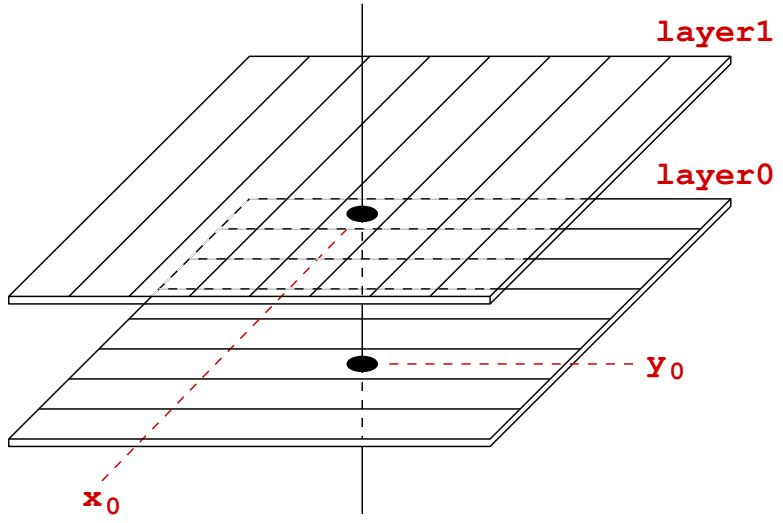
Detectors in high resistivity silicon

- In a microstrip, a large area diode is divided into many small regions, readout separately; production of strip detectors may follow the method of planar diodes using the somewhat more complicated geometrical strip structure
- Each small strip diode consists of a shallow p+ region on a very lowly doped n-substrate
- Full depletion and almost complete and fast collection of the charge released in the sensor substrate may be achieved by applying a reverse voltage of a few tens to a hundred volts



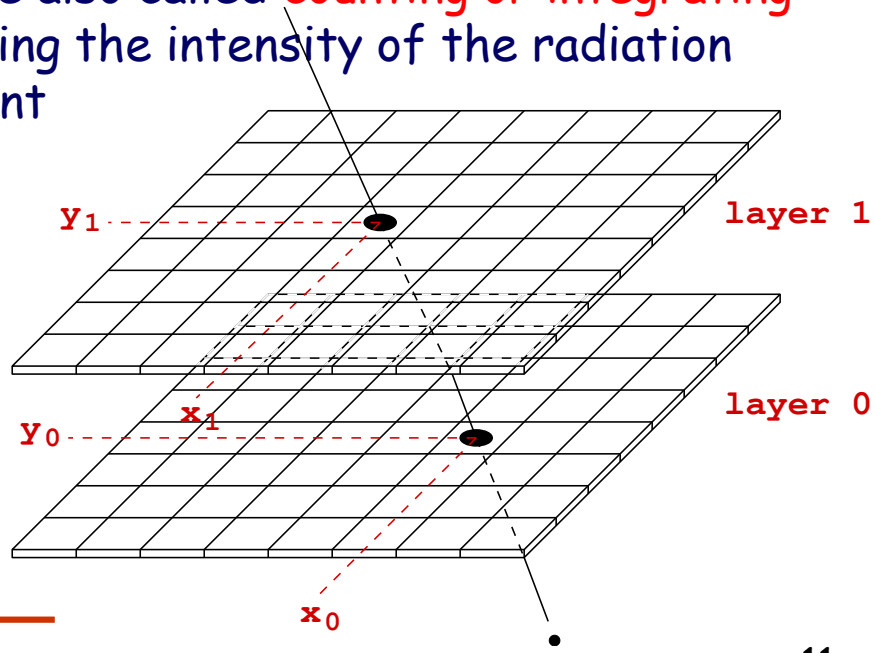
Position and momentum measurement

- A double microstrip detector layer may be used to obtain bidimensional information on the position of the impinging particle (also double-sided microstrip detectors are available)



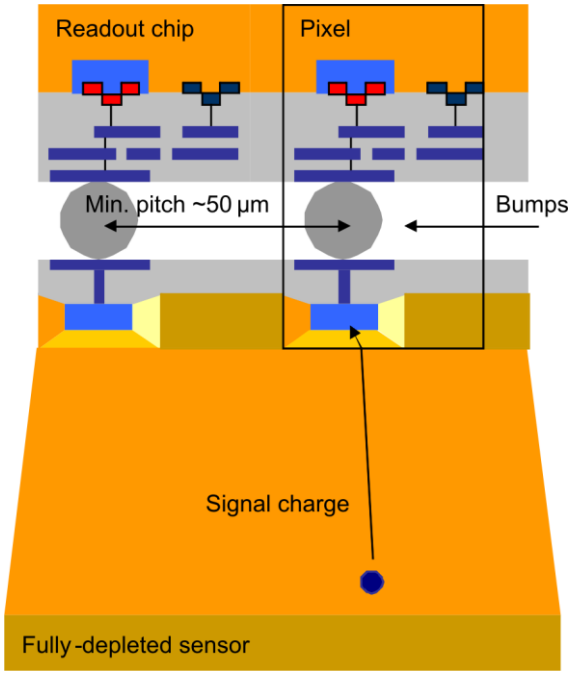
- A single pixel detector layer is sufficient in imaging applications, where the detector has to count the number of striking particles (typically photons, these are also called counting or integrating detectors) in each element, therefore providing the intensity of the radiation hitting the detector surface at any single point

- A double pixel detector layer may be used to obtain information on the momentum (in particular, the direction) of the impinging particle; tracking detectors usually employ multiple layers to improve resolution



Hybrid and monolithic approach

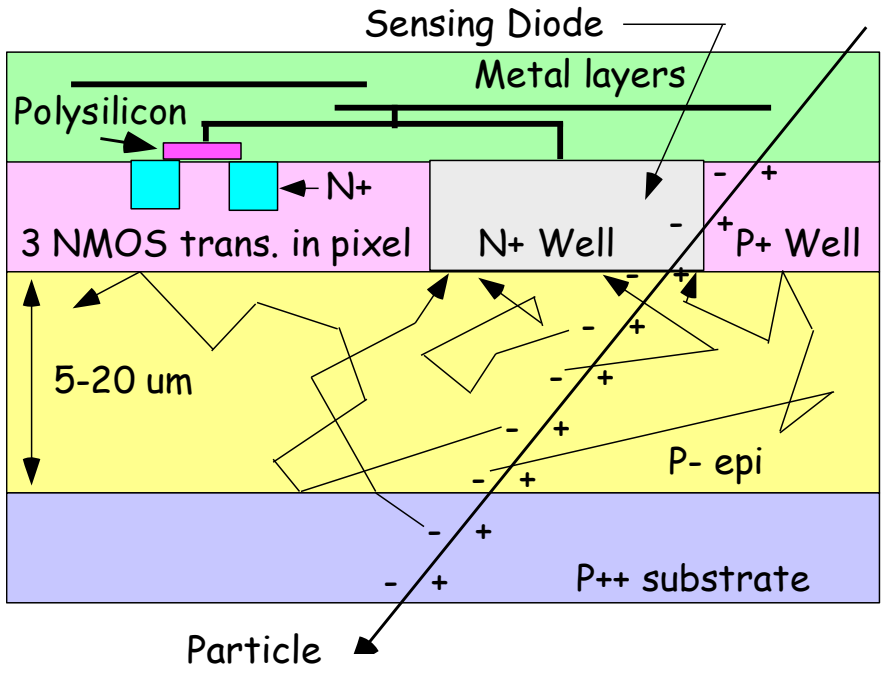
- In semiconductor microstrip and pixel detectors, each microstrip or pixel is read out by a processing channel which generally includes both analog and logic blocks
- In most cases, front-end electronics is integrated in a different piece of silicon from the detector; actually processes for detector fabrication (detector-grade) are quite different from processes for fabrication of microelectronic circuits (electronics-grade)
- Detector and front-end electronics have to be externally interconnected; microstrip detectors are typically connected to the front-end electronics through wire bonding techniques; bump bonding is instead the mainstream technology for pixel detector-to-electronics interconnection



- Sometimes, detectors are monolithically integrated with the front-end electronics; a choice has to be made, in this case, between electronics-grade processes (with possible limitations to the detector performance) and detector-grade processes (with possible degradation in the front-end electronics properties)

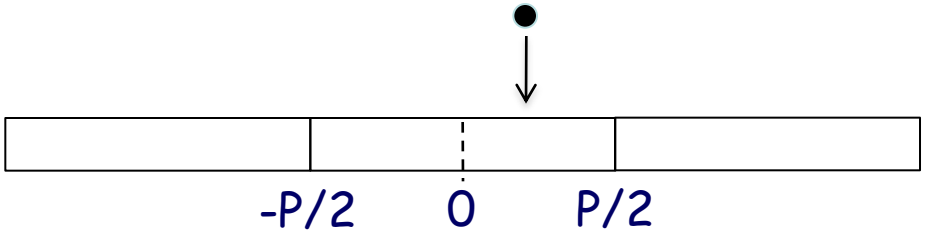
CMOS monolithic sensors

- CMOS MAPS operation is based on the presence of a (relatively) high resistivity (about 10 to 1000 Ω•cm) epitaxial layer, 5 to 20 μm thick (available in so called opto technologies); they are widely used as imaging devices in the visible spectrum; their operation have been adapted to particle tracking in high energy physics experiments and electron microscopy
  - The impinging particle releases electron-hole pairs along its track and, in particular, in the epitaxial layer; this holds also for photons in the visible spectrum, which simply have a shorter range in silicon
  - The epitaxial layer, which is sandwiched between the low resistivity substrate and surface P+ wells, acts as a potential well; therefore, the charge released in the epitaxial layer is confined in the region and can diffuse to one of the N+ collecting electrodes (at least the fraction of charge which does not recombine)



Point resolution

- There is a trend to reduce the pitch of semiconductor detectors to improve resolution; this has an impact on the readout electronics, which has to be designed in such a way to fit into interelectrode spacing



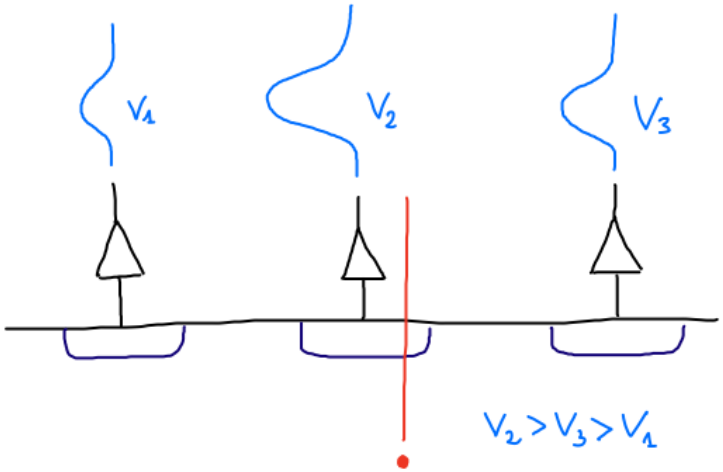
Let us consider the case of simple binary readout (recording just which strip or pixel is hit); the position resolution of a detector with electrode spacing **P** can be calculated as follows

$$s^2 = \left\langle \left(x - \langle x \rangle\right)^2 \right\rangle = \langle x^2 \rangle - \langle x \rangle^2 =$$

$$\int_{-P/2}^{P/2} r x^2 \, dx = \frac{P^2}{12}, \quad r = \frac{1}{P}, \quad \langle x \rangle = 0$$

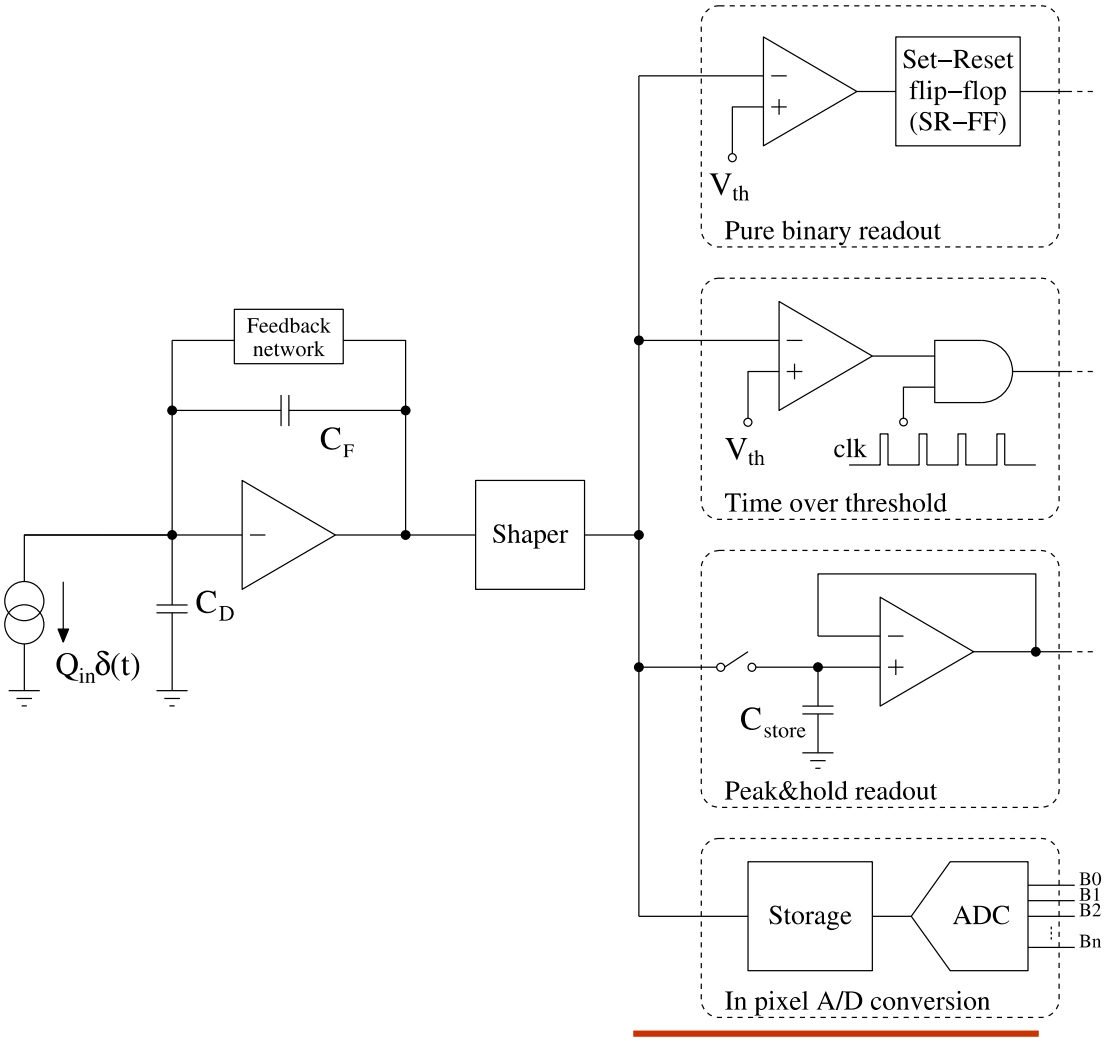
Resolution has to be intended here as the root mean square error made when position x=0 is assigned to a particle hitting the detector between –P/2 and P/2

Resolution may be improved by measuring the signal amplitude in a cluster of sensors (not just hit/no hit information) and calculating the center of mass of the cluster



Hit information processing

- Once a hit has been detected, amplitude analog information at the shaper output can be discarded or retrieved in one of four possible ways



Pure binary readout; analog information is discarded, just hit/no hit information is provided by the readout chip for each channel

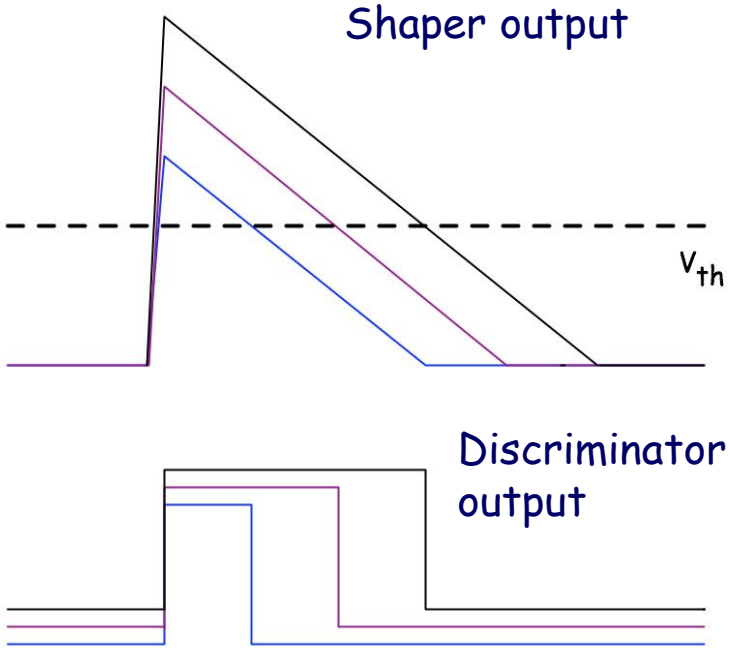
Time over Threshold (ToT); amplitude is converted to a time duration by comparing the shaper output to a preset threshold

Peak & hold; peak voltage at the shaper output is sampled and transferred to the chip periphery

In-pixel A/D conversion; peak voltage at the shaper output is sampled, converted to a digital word and transferred to the chip periphery

Time over Threshold (ToT)

- The Time over Threshold (ToT) technique provides a direct amplitude-to-time conversion; the signal at the shaper output is compared to a fixed voltage at the input of a threshold discriminator; the signal at the output of the discriminator is a digital pulse, whose duration is equal to the time during which the signal at the shaper output exceeds the threshold; digitization is easily achieved by computing the logic AND between the discriminator pulse and a reference clock and by counting the number of clock pulses

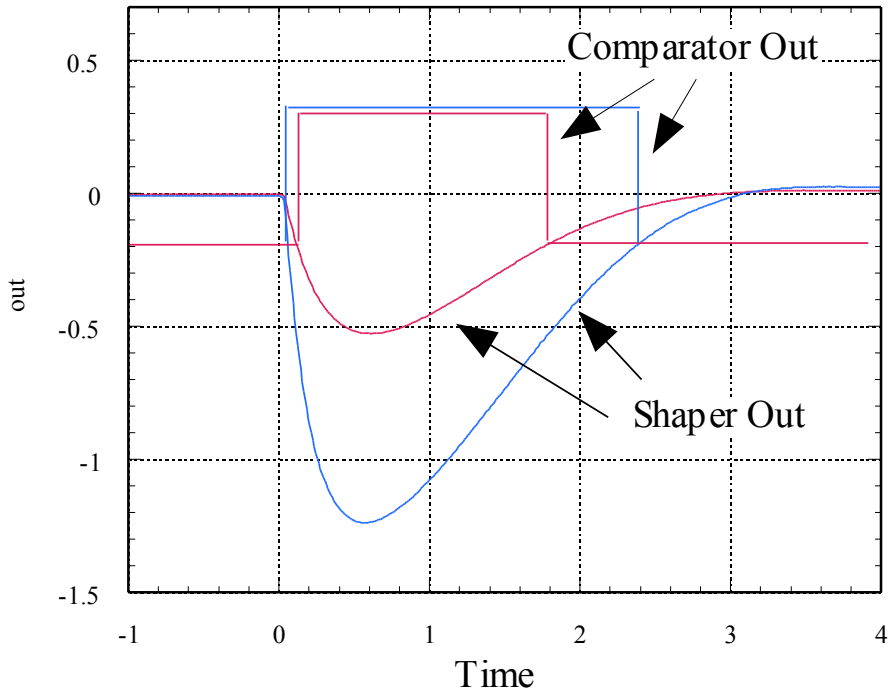


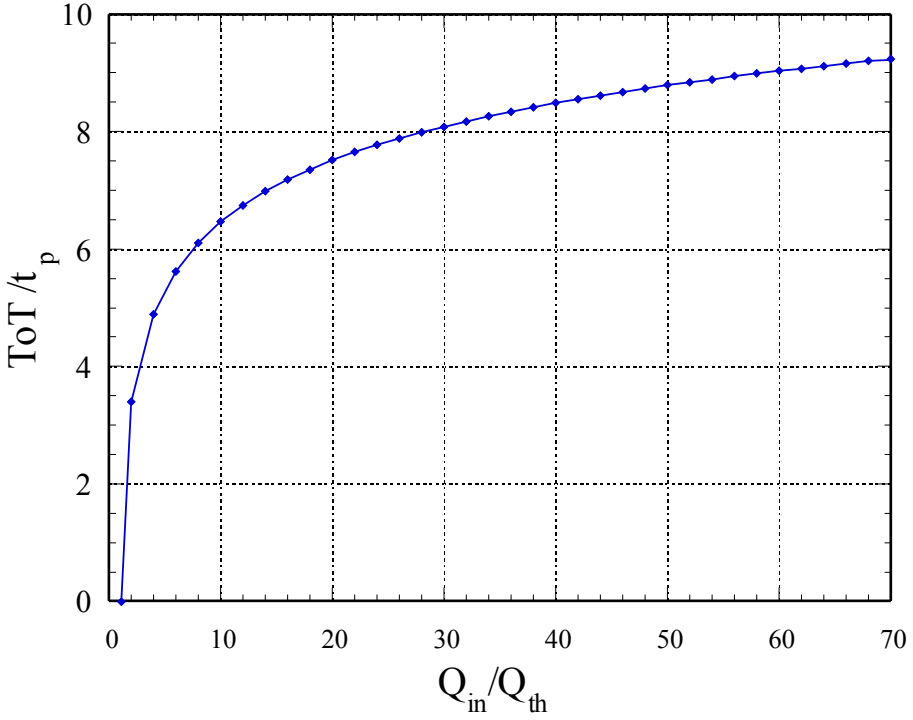
- If the signal at the shaper output returns to the baseline with a constant slope, then a linear relationship exists between the peak amplitude at the shaper output and the ToT duration (the rise time of the shaper output signal is assumed to be negligible)

$$ToT = \frac{V_{peak} - V_{th}}{\left| \frac{dV_{shaper}}{dt} \right|}$$

Range compression with Time over Threshold (ToT)

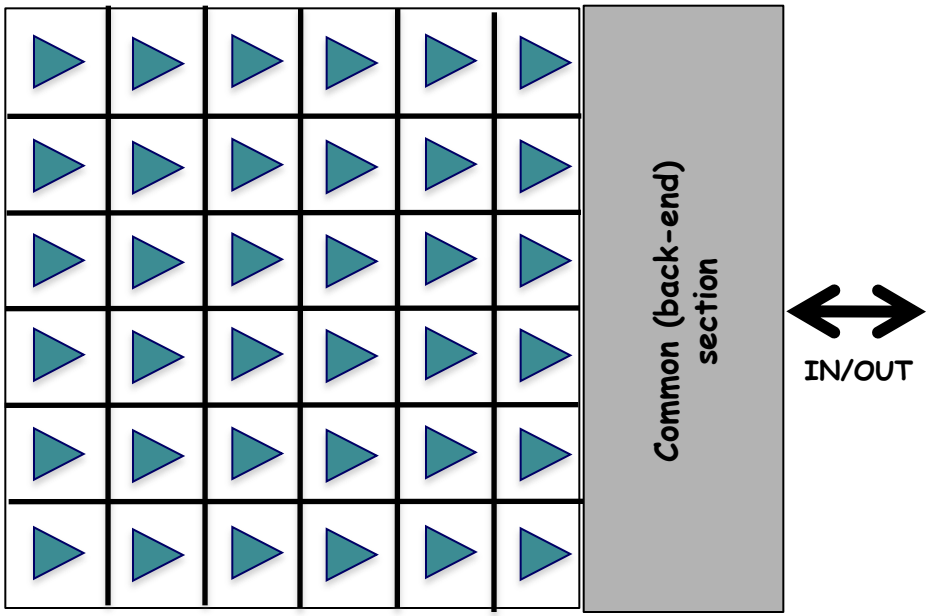
- In the case of linear (constant shape) filtering, the peak voltage-to-ToT duration relationship becomes a non linear one; in particular, a compression of the characteristic may be achieved in such a way that both high resolution at small input charge and high dynamic range can be obtained





General features of readout chips

- A readout chip for semiconductor detectors includes both analog and digital blocks; it contains a section where a cell is periodically replicated based on the detector chip geometry, and a common (completely digital) section servicing all the cells
- The analog front-end performs the task of amplifying and suitably shaping the charge signal in order to maximize the signal to noise ratio
- Digital blocks may perform several tasks, like data selection (sparsification), zero suppression, hit counting, analog-to-digital conversion, time stamping, data storing, buffering and serialization (or parallelization)

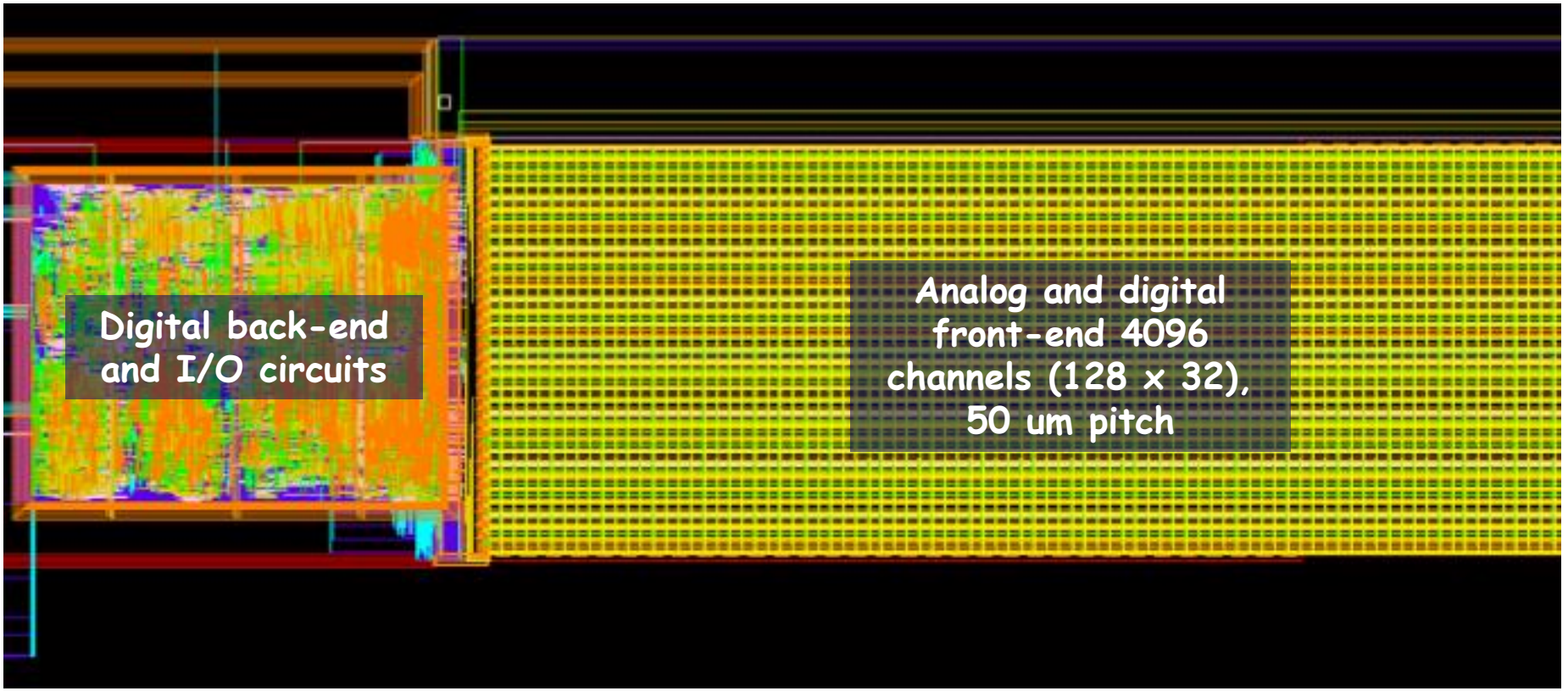


Front-end section (one cell for-each sensor element)

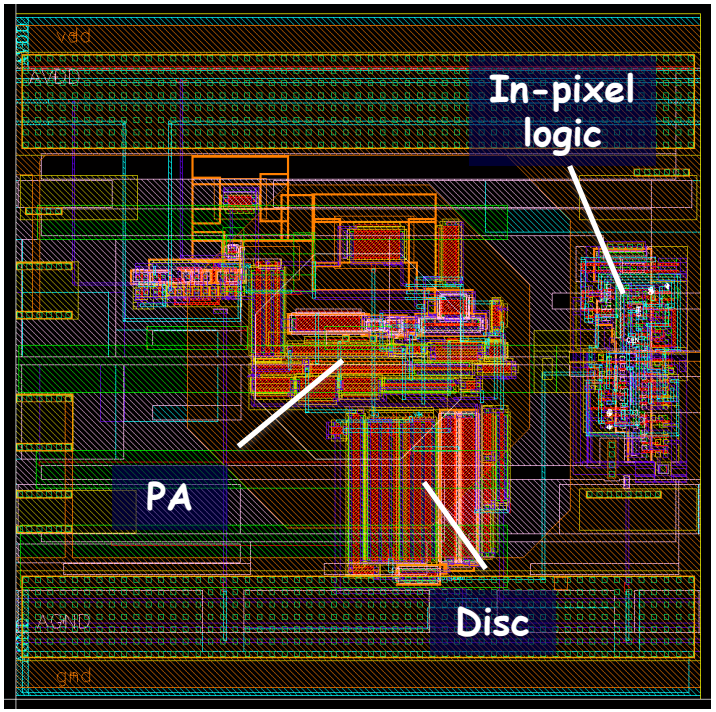
- A readout chip has to provide digital information in a form that requires the least readout bandwidth and processing time possible before being stored in a disk; therefore, as many functions as possible are moved from the acquisition system to the chip itself

SuperPix0 chip for hybrid pixel detectors

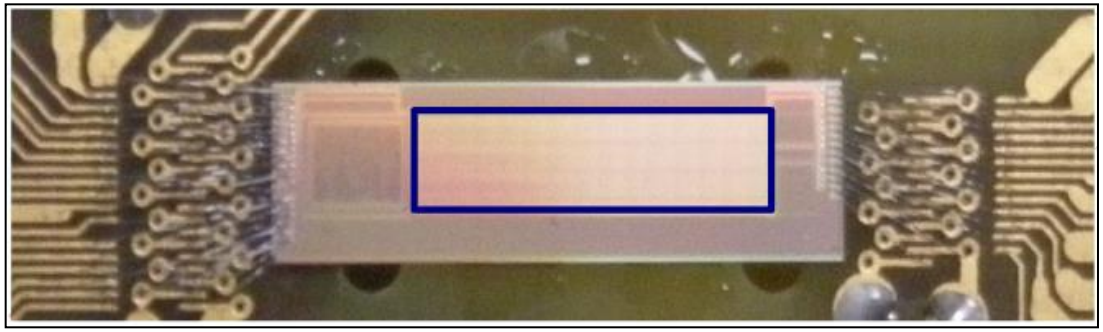
- Fabricated in a 130 nm CMOS technology – mixed signal chip for hybrid pixel
- Sparsified readout based on a macropixel structure

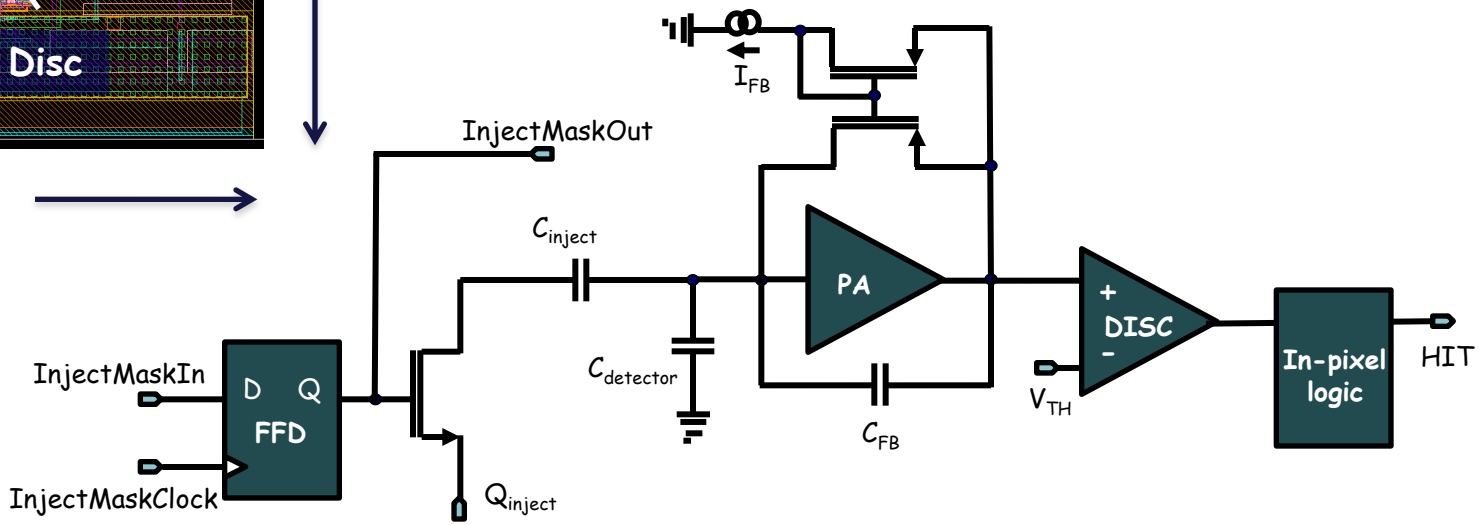


SuperPix0 cell



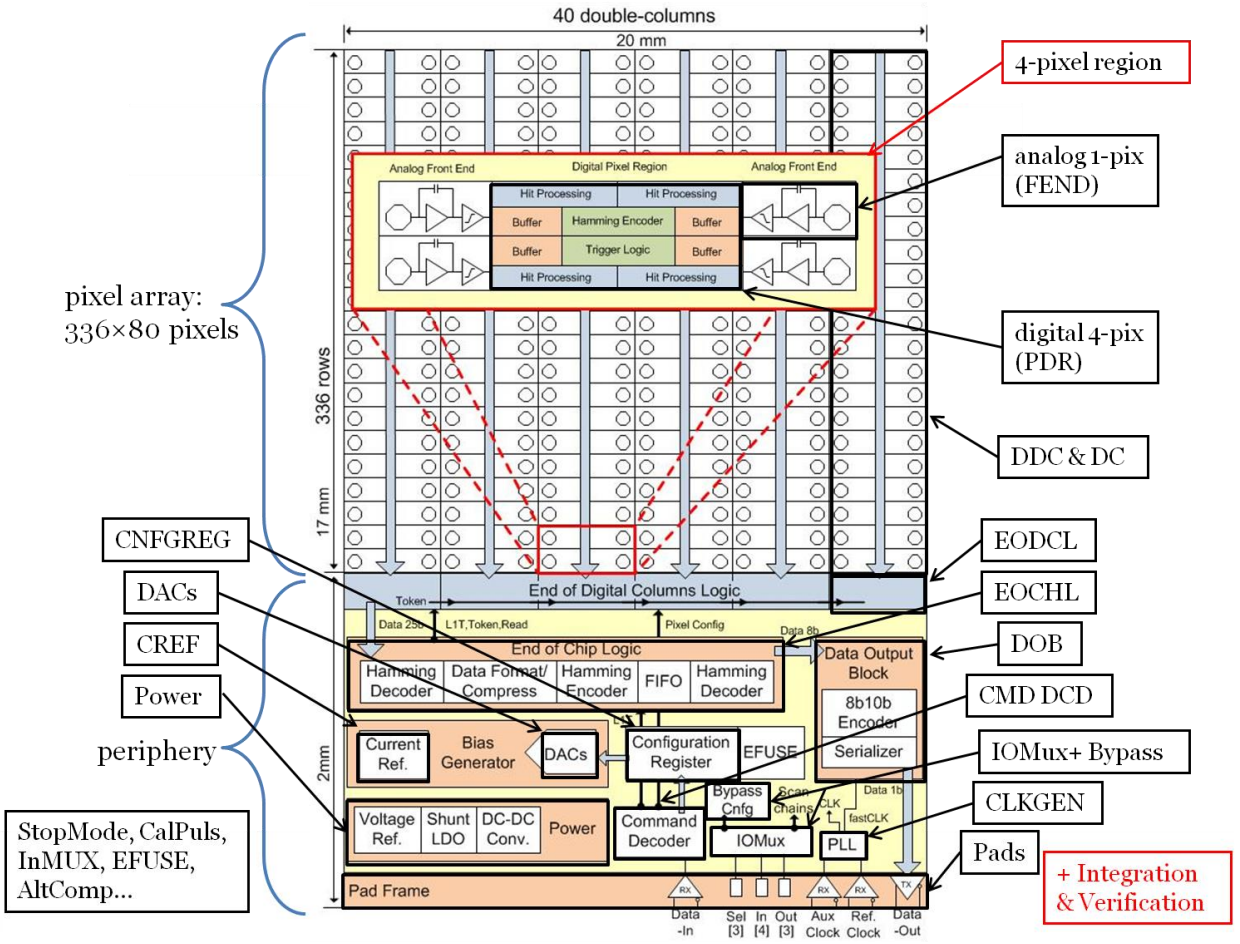
Photograph of the prototype

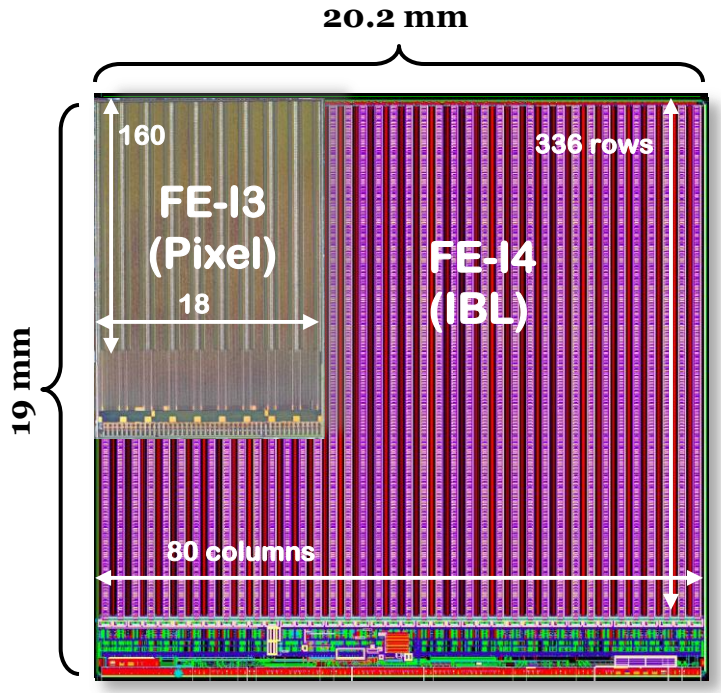




FE-I4 chip for the ATLAS IBL

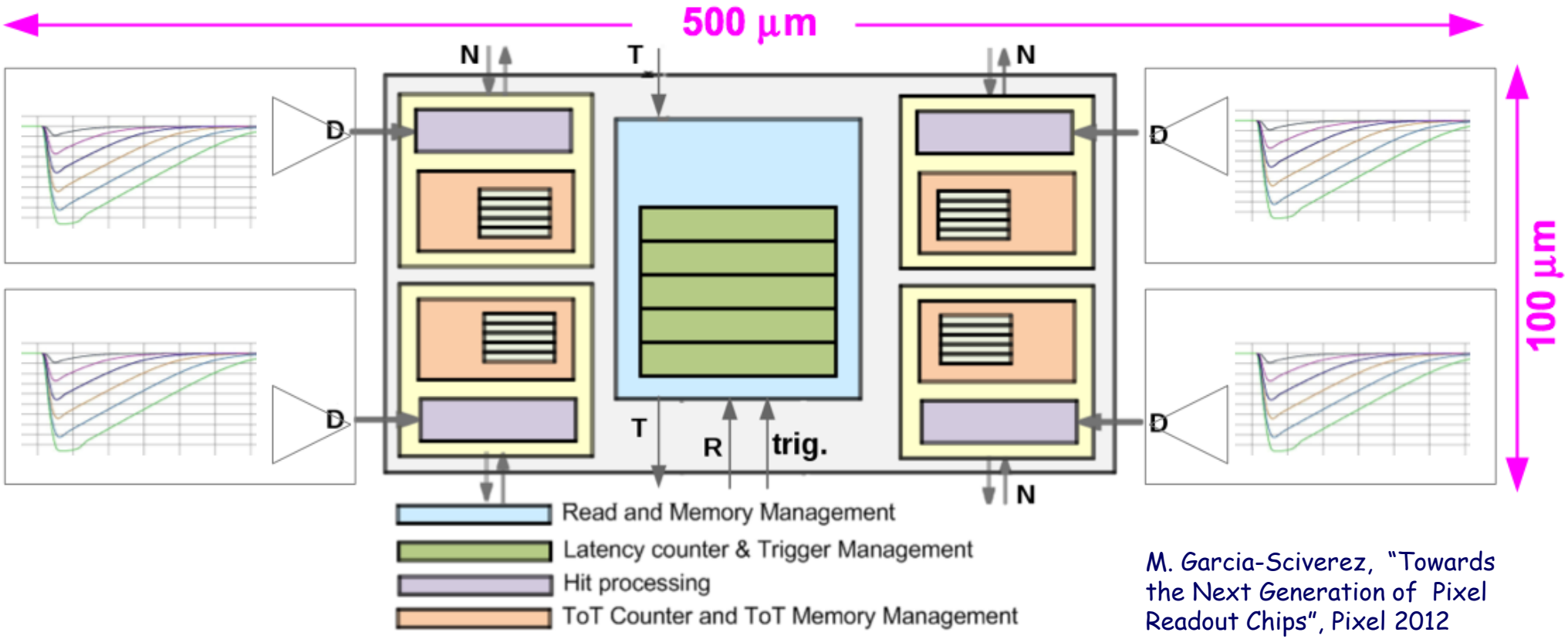
- CMOS 130 nm mixed-signal chip





- Power regulation
- Command decoding and trigger management
- Internal signal monitoring and diagnostic recording and reporting
- Data formatting and high speed serialized output, including clock generation

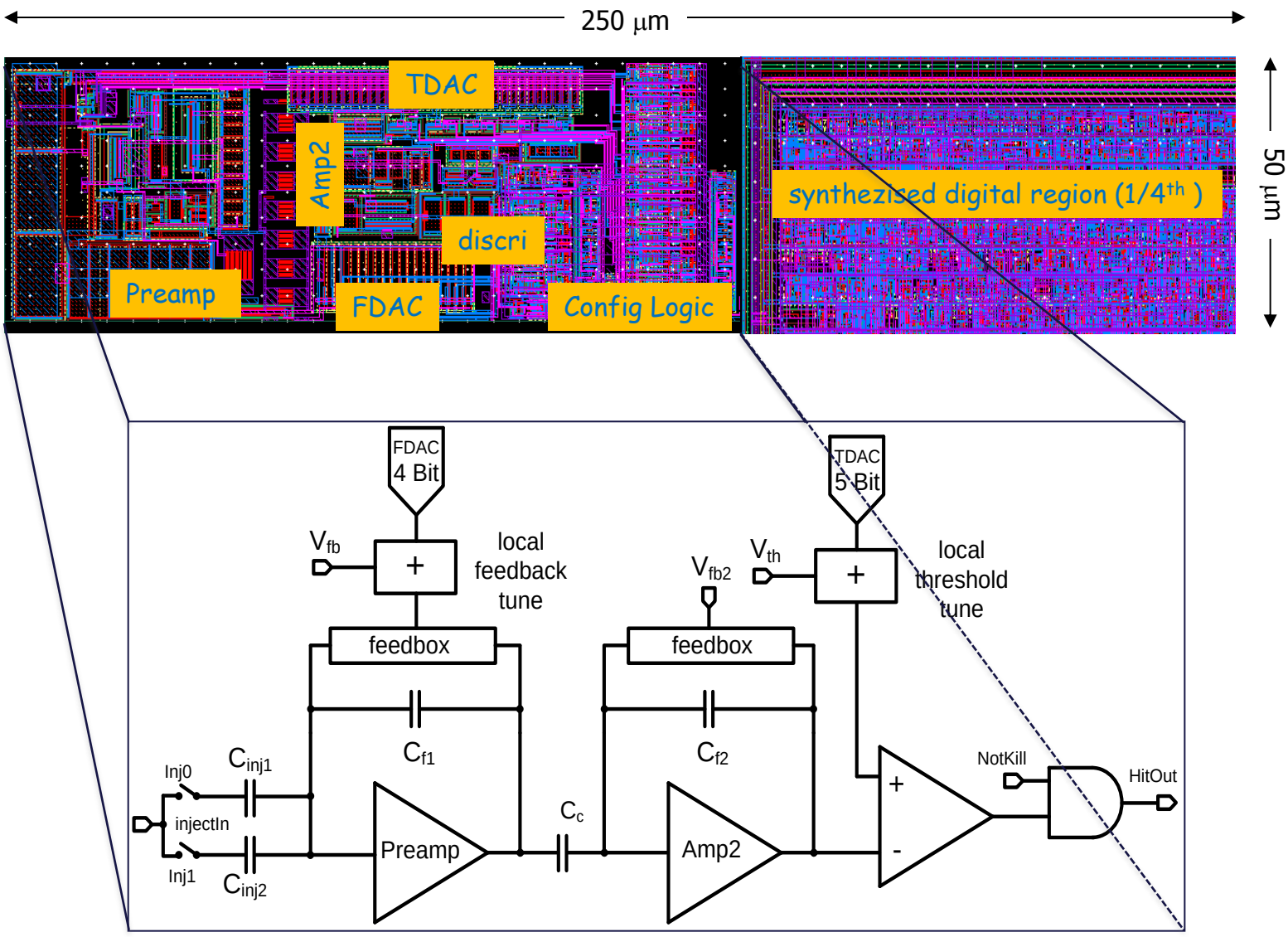
FE-I4 chip digital core



M. Garcia-Sciverez, "Towards the Next Generation of Pixel Readout Chips", Pixel 2012 Conference

- TOT and threshold encoding
- Local association and hit storage
- Triggered hit retrieval with time stamp matching

FE-I4 elementary cell



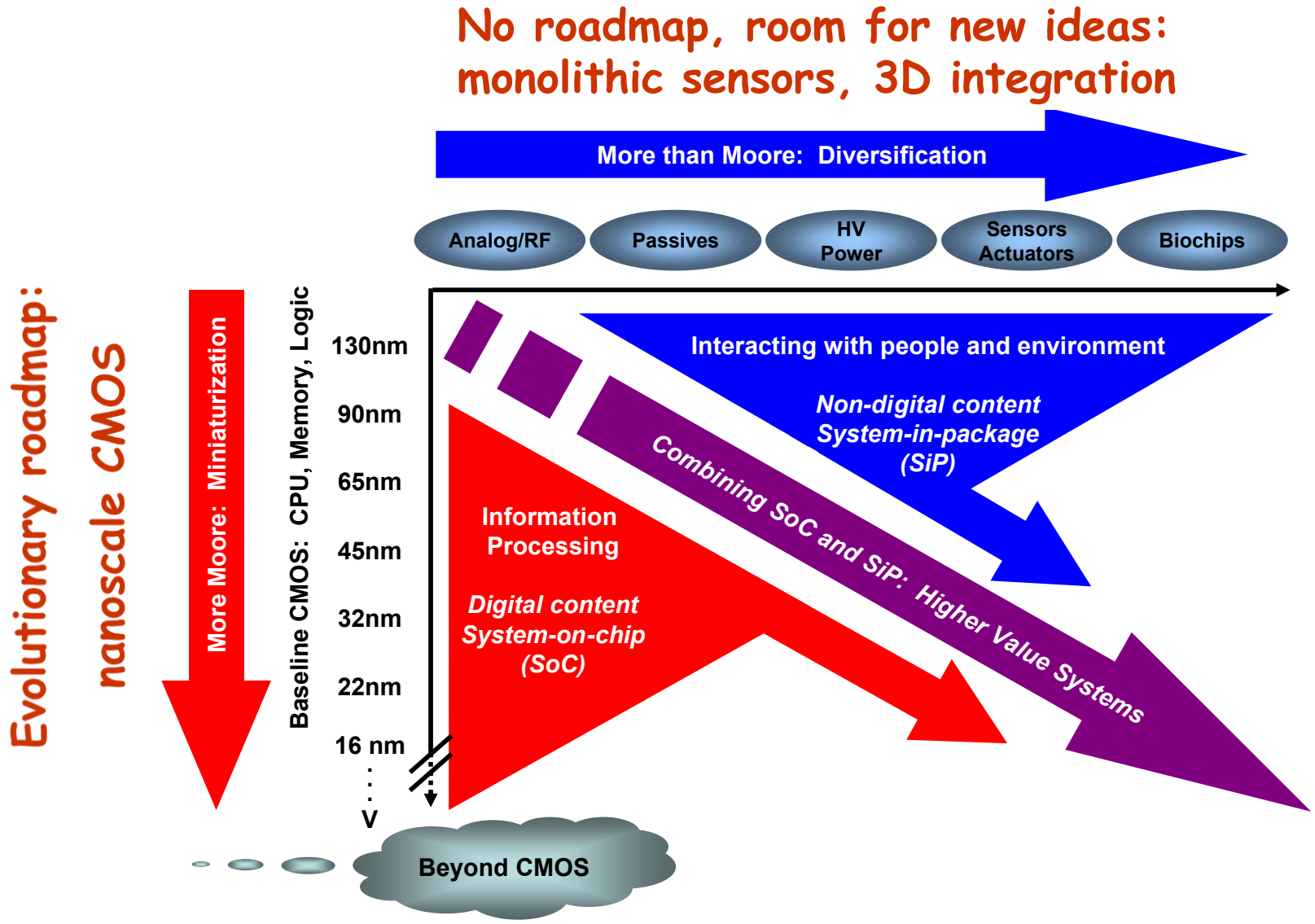
Enabling technologies for intelligent pixel detectors

Nanoscale CMOS and 3D integration

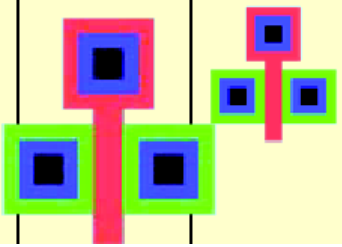
- New applications of semiconductor detectors in high energy physics (silicon vertex trackers) and photon science (high-resolution imagers) set demanding and often conflicting requirements on the front-end electronics
  - more electronic intelligence squeezed in smaller pixel cells
  - larger amount of data stored in the chips and then transmitted outside
  - lower power
  - higher radiation levels
  - minimum amount of material and dead areas

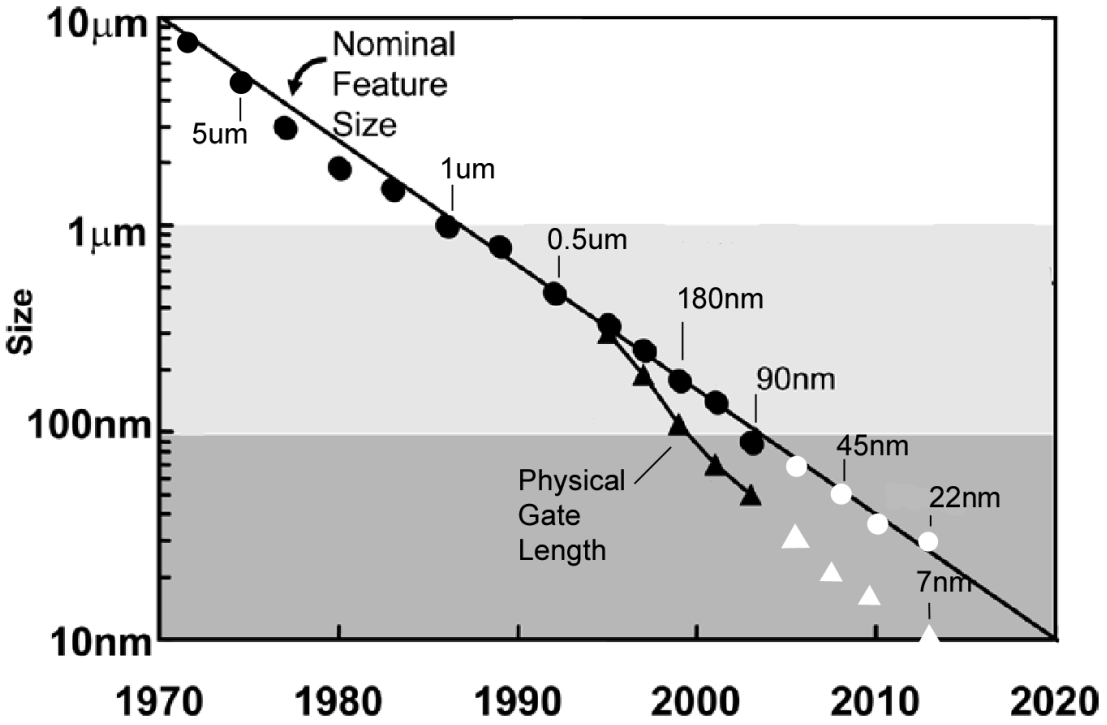
- The potential of current microelectronic processes (including interconnections) has to be exploited, in particular
  - standard, nanoscale CMOS technology
  - vertical integration technology

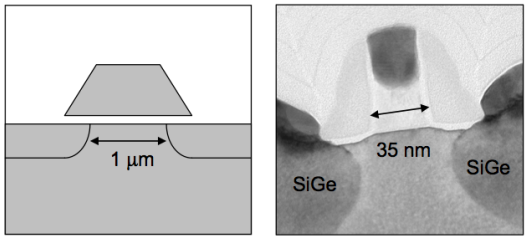
Evolution of microelectronic technology



Industry scaling roadmap for CMOS

Feature Size [nm]	2000	1200	800	500	350	250	130	65	35	20
Minimum NMOS										



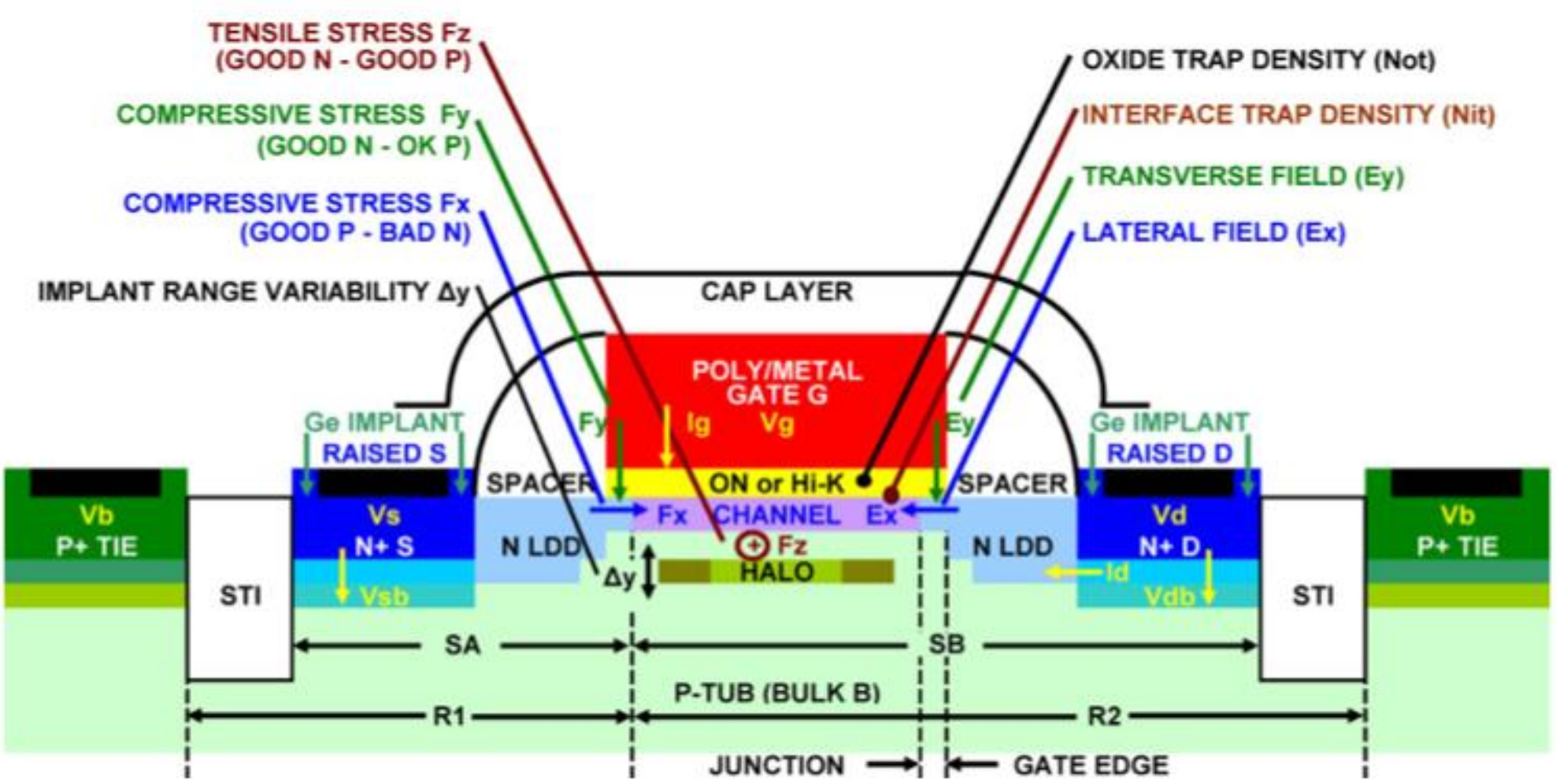


	Dennard 1974	Intel 2005
Gate Length:	1.0 µm	35 nm
Gate Oxide Thickness:	35 nm	1.2 nm
Operating Voltage:	4.0 V	1.2 V

Classical scaling ended in the early 2000s due to gate oxide leakage limits

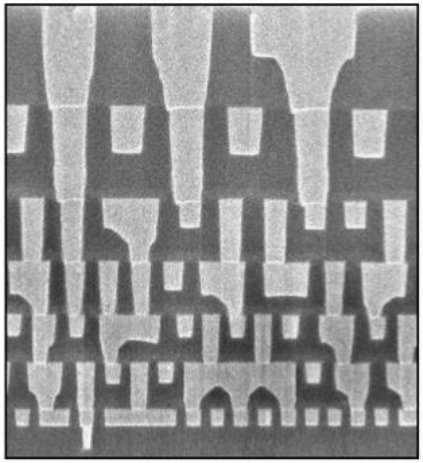
Bohr, "the new Era of Scaling in a SoC world", 2009 ISSC

Nanoscale MOSFET devices

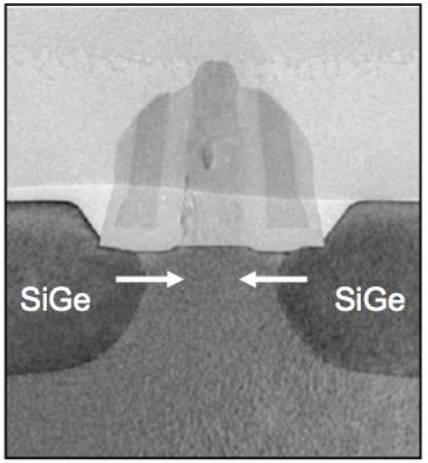


Lewyn et al, "Analog circuit design in nanoscale CMOS technologies", Proc. IEEE, Vol. 97, no. 10, Oct. 2009.

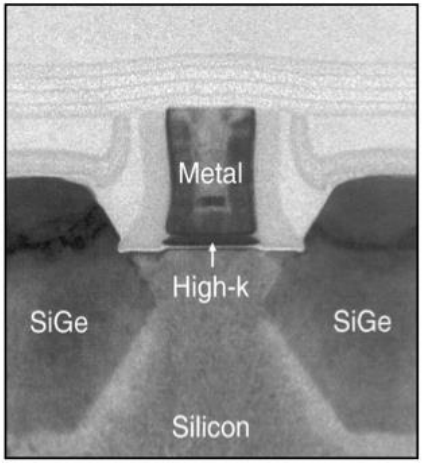
Technology innovations for device scaling



Copper + Low-k



Strained Silicon



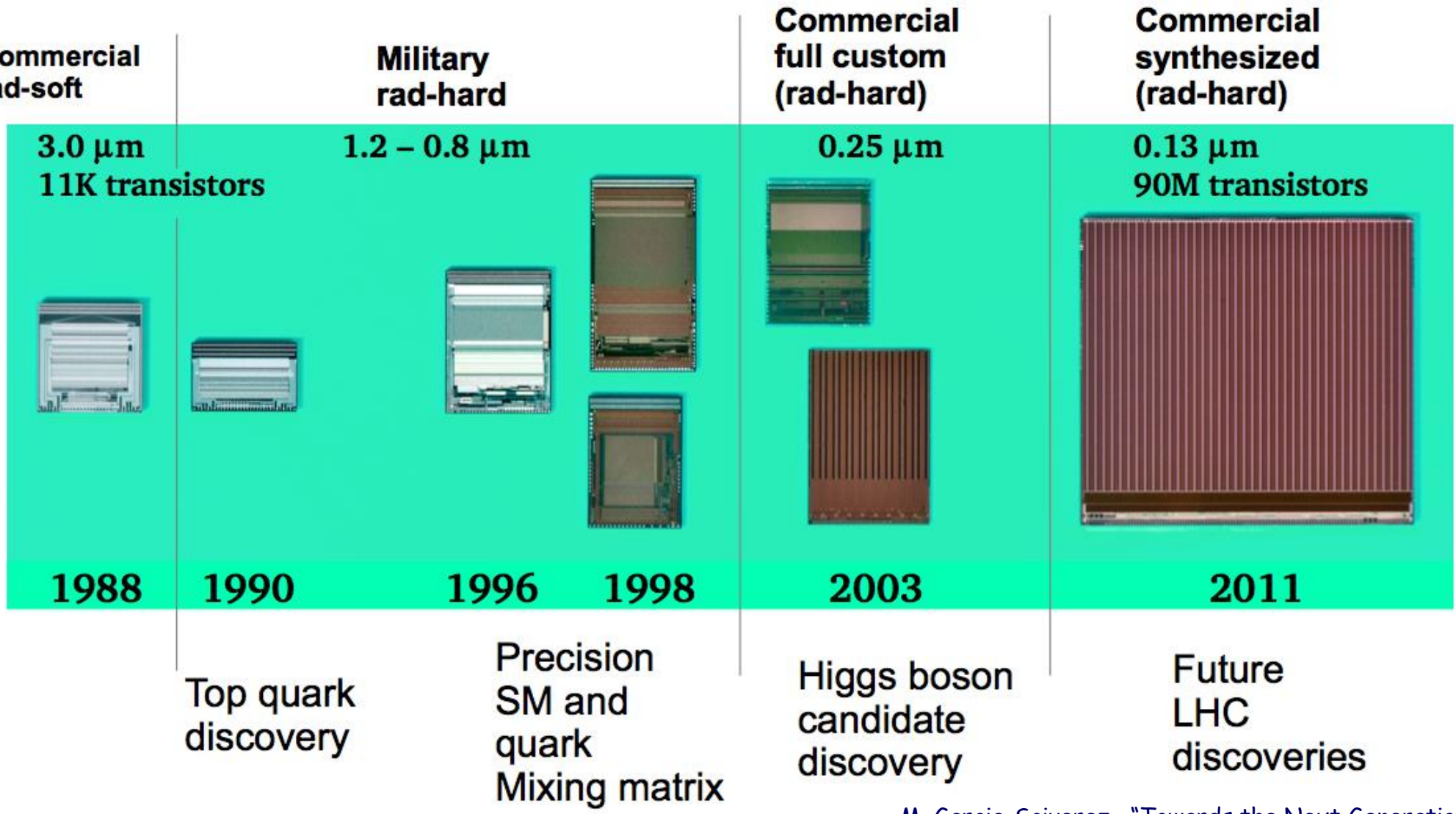
High-k + Metal Gate

- Copper has replaced aluminum as a means to increase conductivity while a series of ever lower-k dielectrics has been introduced to reduce wire capacitance
- Mechanical stress (compressive or tensile strain) is introduced in the silicon channel to enhance carrier mobility and drive current
- Gate dielectric is made thicker (still reducing gate capacitance) by using materials with higher dielectric constant than SiO_2

Reasons for CMOS scaling

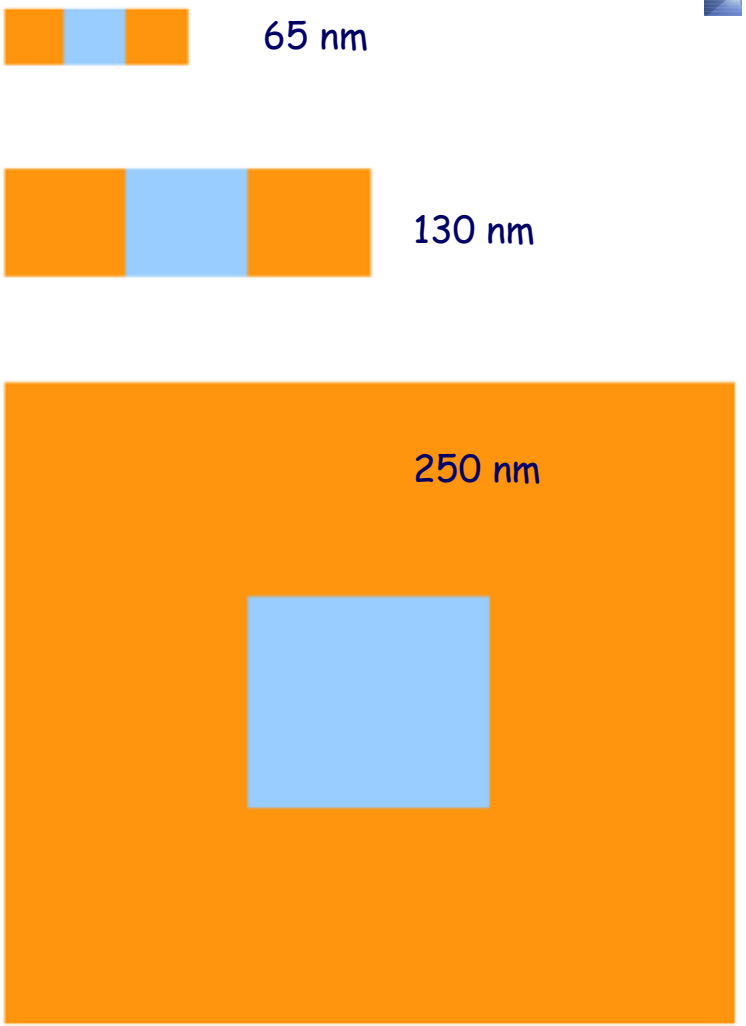
- Industrial microelectronic technologies are today well beyond the 100 nm frontier, bringing CMOS into the nanoscale era
- Digital performance (speed, density, power dissipation) are driving the evolution of CMOS technologies towards a continuous shrinking of physical feature sizes
- **Analog performance** remains essential for the processing of signals delivered by semiconductor detectors
- Front-end electronics may benefit from scaling in terms of functional density (small pitch pixels) and digital performance - analog design is a challenge (reduced supply voltage and dynamic range, statistical doping effects, ……)
- For a full integration of analog and digital circuits in the most modern semiconductor technologies, design advances are needed to exploit the full potential: digital signal processing may be used to overcome analog limitations, analog circuits may be used to monitor the performance of digital circuits and their power consumption

Chips for vertex detectors at colliders

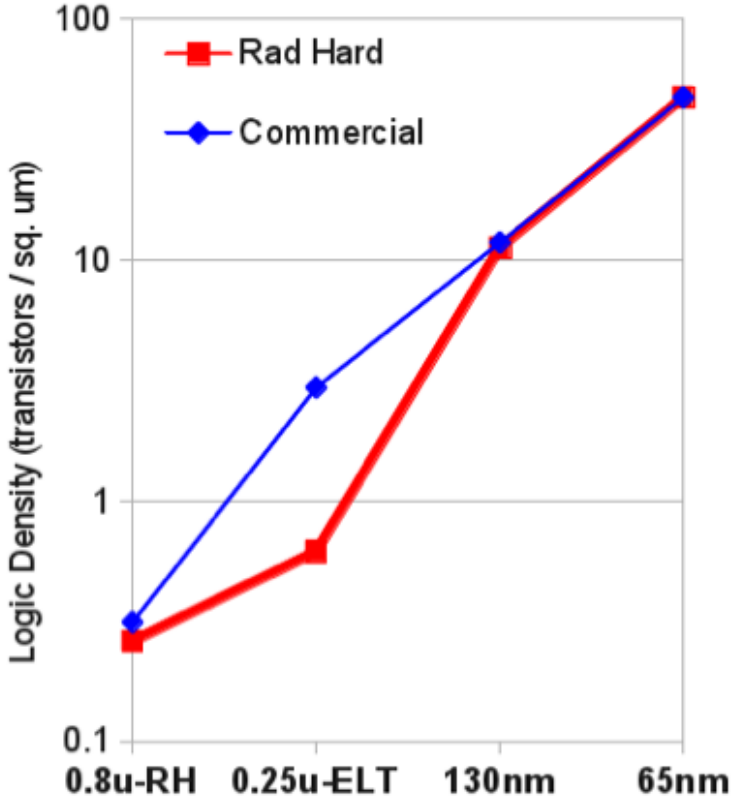


M. Garcia-Sciverez, "Towards the Next Generation of Pixel Readout Chips", Pixel 2012 Conference

Rad-hard logic in detector front-end chips

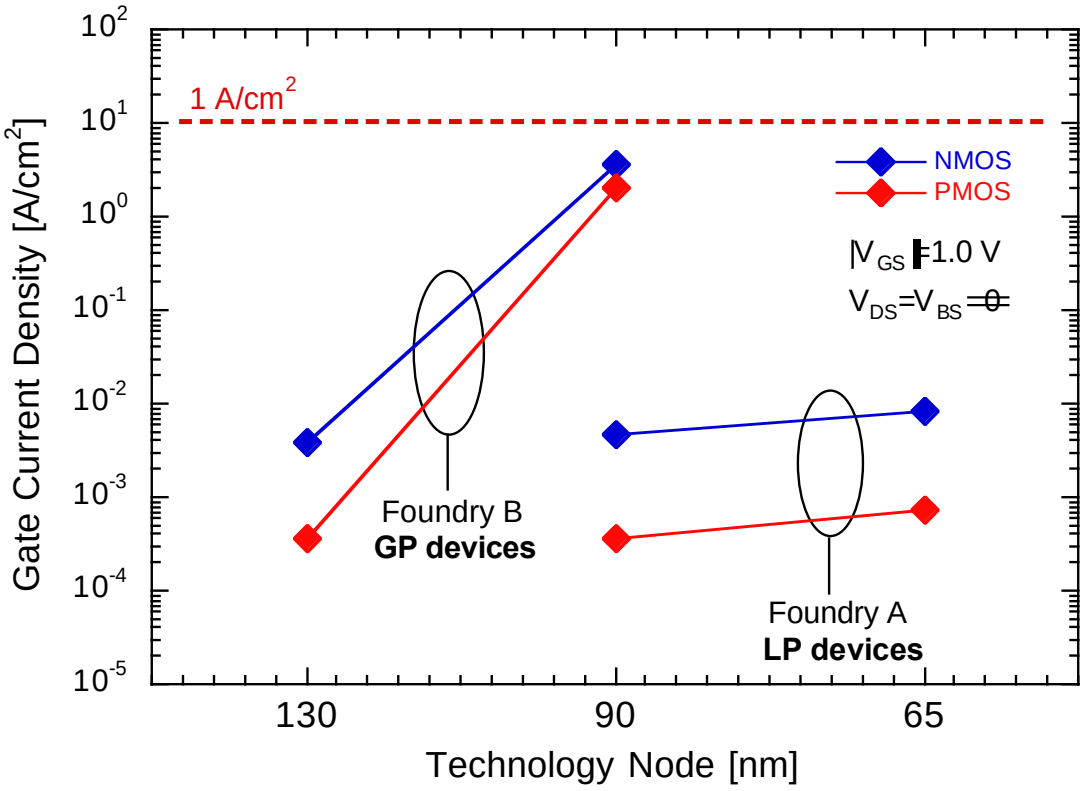


- Logic circuits in radiation detectors front-end chips lagged Moore's law due to the need for enclosed layout transistors (ELT), but are now catching up

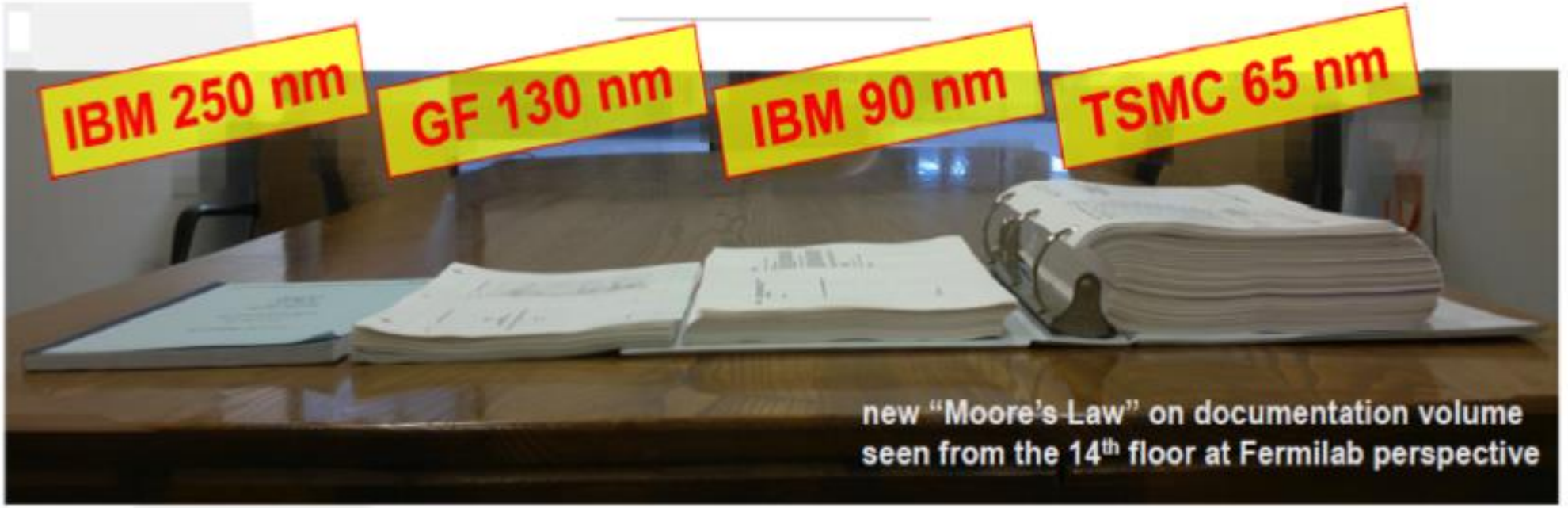


CMOS 65 nm low-power

- After the 250 nm (LHC) and the 130 nm node (LHC upgrades, XFEL,…), our community appears to be very interested in the 65 nm CMOS generation: several prototypes have been already fabricated and tested
- Among the wide choice of options of this technology, the low-power (LP) flavor is less aggressive than other variants (thicker gate oxide, smaller gate leakage, higher voltage), and is more attractive for mixed-signal chips where analog performance is an essential feature
- LP devices are optimized for a reduced leakage (larger equivalent oxide thickness, different level of nitridation with respect to other flavours, different silicon stress)



Moore's law for DRMs

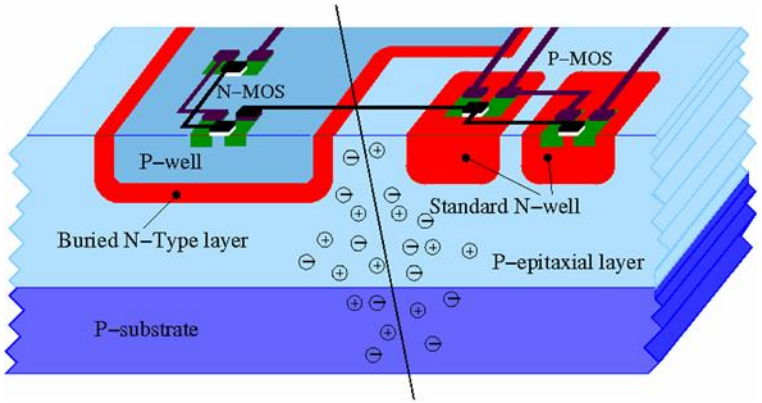


G. Deptuch

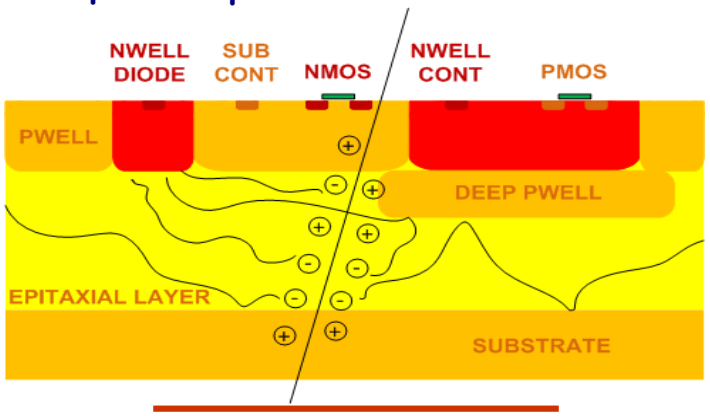
CMOS sensors with hybrid pixel features

- Some (more or less standard) properties of less scaled CMOS technologies have been exploited to add some new functionalities to monolithic active pixel sensors

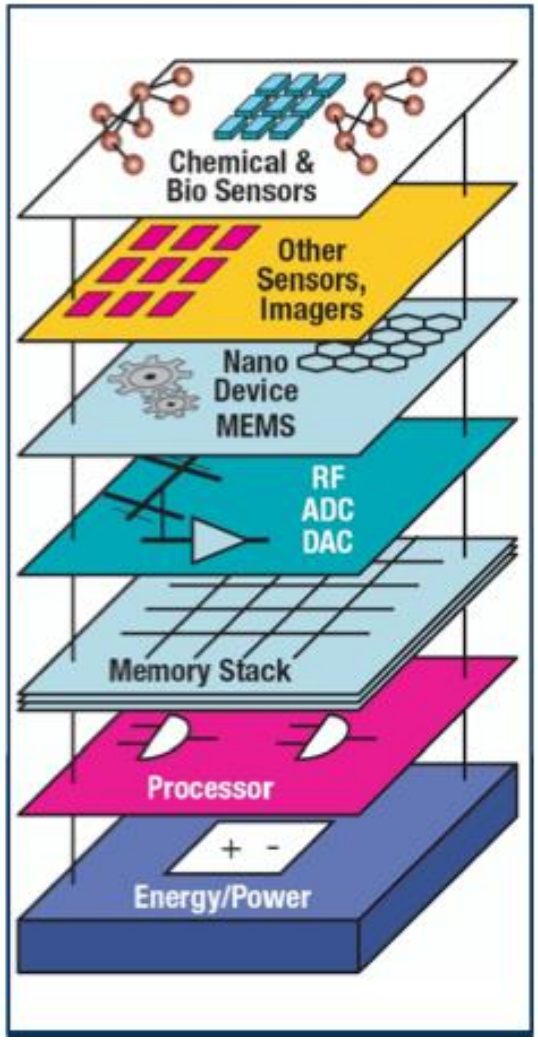
  - deep N-well monolithic sensor



  - monolithic sensor in a quadruple well CMOS technology



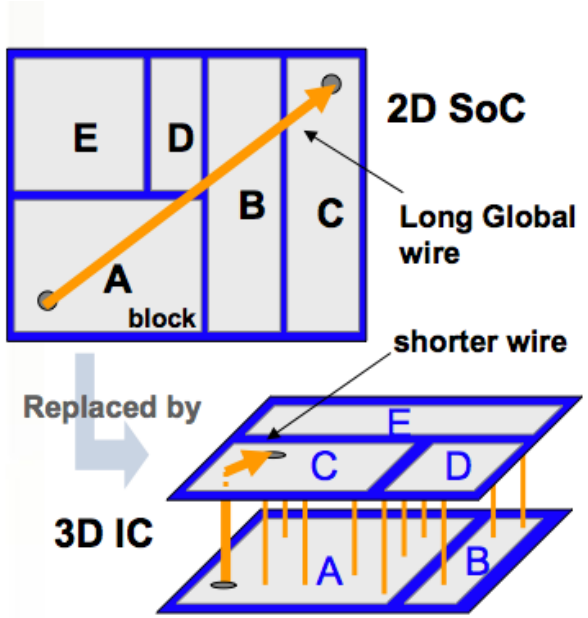
3D integration of microelectronic circuits and sensors



- 3D integration is an emerging technology that can form highly integrated systems by vertically stacking and connecting various materials, technologies and functional components together
- Intense research activity ongoing in academia and industry: MIT Lincoln Labs, IBM, INTEL, SEMATECH, Tezzaron in the US, CEA-LETI, Fraunhofer Institute and IMEC in Europe, T-Micro in Japan
- Presently pursued applications
  - vertically integrated, high resolution CMOS imagers
  - 3D stacked flash memories
  - 3D integration of processor and memory subsystems

J.-Q. Lu, K. Rose, and S. Vitkavage, "3D Integration: Why, what, who, when?," Future Fab Int., no. 23, pp. 25–27, 2007.

Advantages of 3D integration

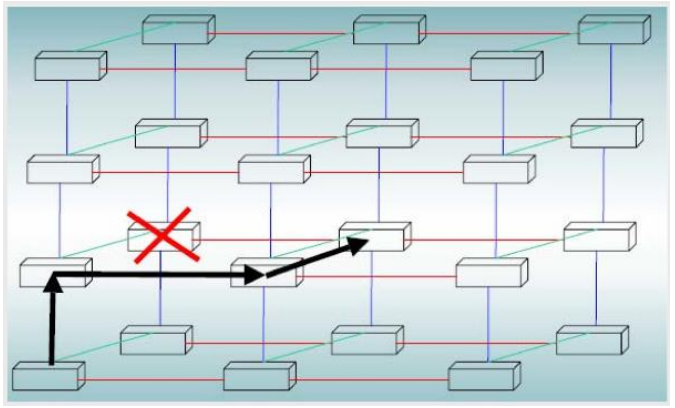


- Replace long horizontal with short vertical interconnects, addressing
  - power dissipation (more than 50% of dynamic power consumption is due to interconnects in modern processes)
  - RC delay (increasing exponentially from technology node to node)
  - crosstalk (more of an issue in mixed signal circuits)
  - form factor

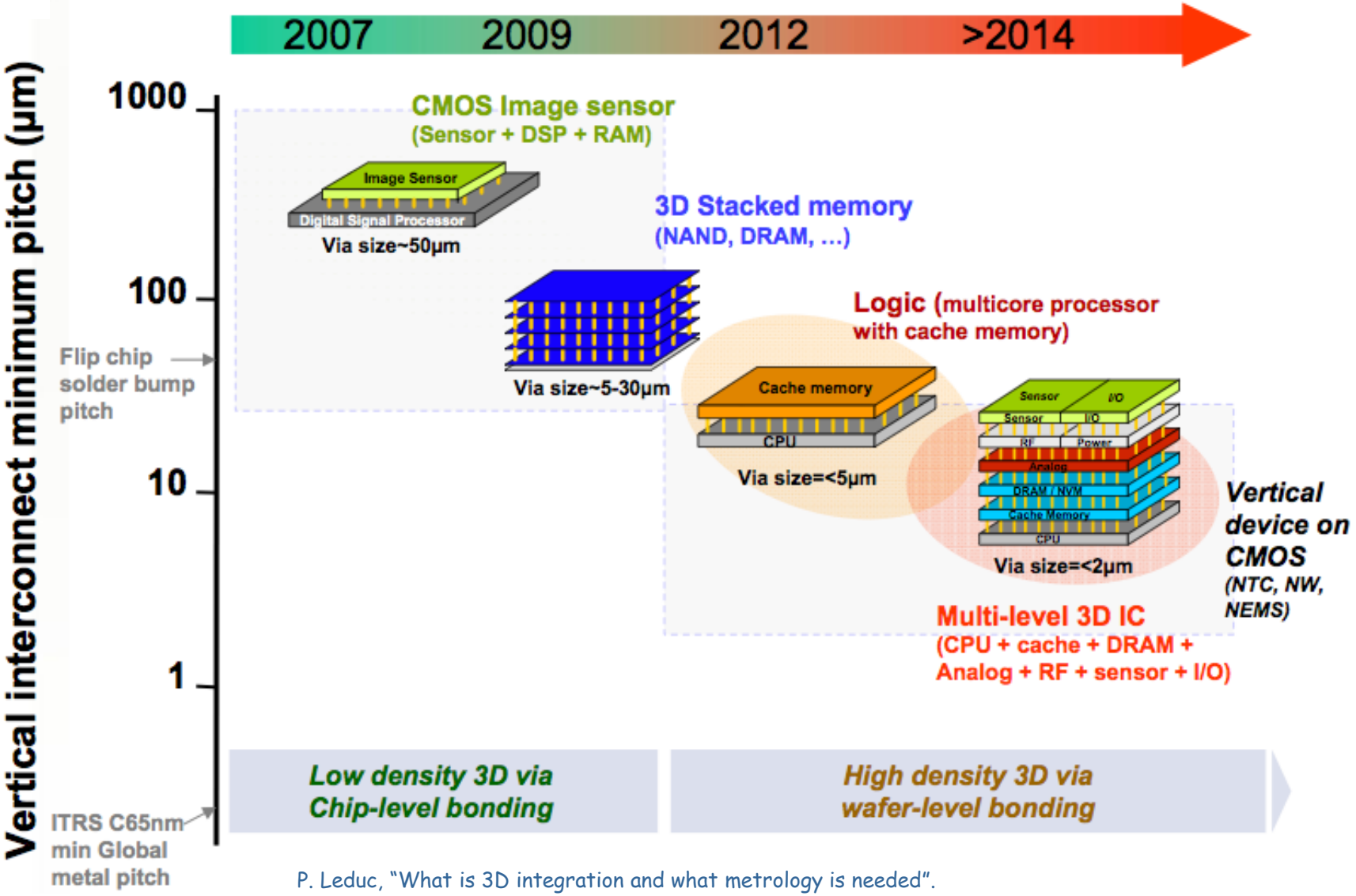
$$P_{dyn} = C\, V_{DD}^2\, f$$

switching capacitance (diffusion, gate, interconnects)

- Enable the integration of heterogeneous devices and technologies (memory, logic, RF, analog, sensors,…)
  - cost reduction (as compared to SoC)
  - new functionalities can be implemented
- Enable higher fault resistance thanks to the high connectivity of 3D ICs



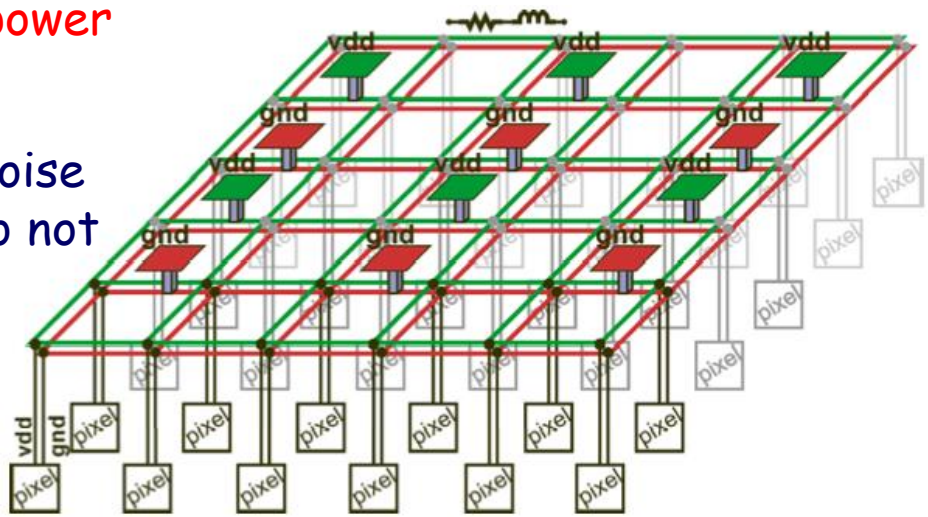
Applications of 3D integration

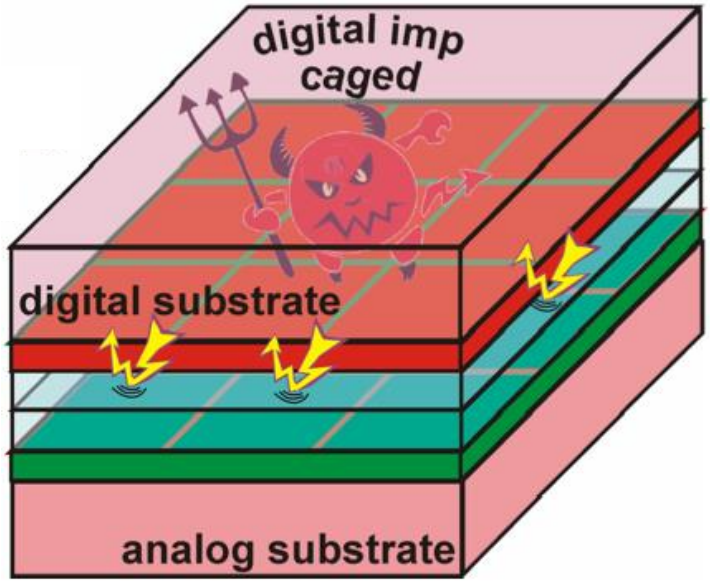


P. Leduc, "What is 3D integration and what metrology is needed".

Benefits for pixel detectors

- More efficient and uniform ground and power distribution (against voltage drops)
- Separation of digital activity from low-noise analog part (analog and digital circuits do not share the same substrate)





G. Deptuch, "Front-end electronics 4 3D technologies," Vertically Integrated Pixel Sensors Workshop, Pavia, Italy, April 22-24 2010

- Post-process thinning (3D wafers obtained by fusion techniques are as rigid as monolithic structures) ➔ less material
- Dead area reduction (readout electronics can be designed with virtually no peripheral circuits ➔ 4-side buttable detectors)

3D-IC Consortium and AIDA

- International laboratories and universities with interest in HEP formed a consortium for the development of 3D ICs (http://3dic.fnal.gov)
- The Consortium made a considerable effort to organize and finalize the first multiproject run (share the costs by sharing the area) in the Tezzaron/Chartered 130 nm 3D technology

✓ Consortium was comprised of 17 members from 7 countries

VIPIX Collaboration
- Fermilab, Batavia
- University of Bergamo
- University of Pavia
- University of Perugia
- INFN Bologna
- INFN Pisa
- INFN Rome

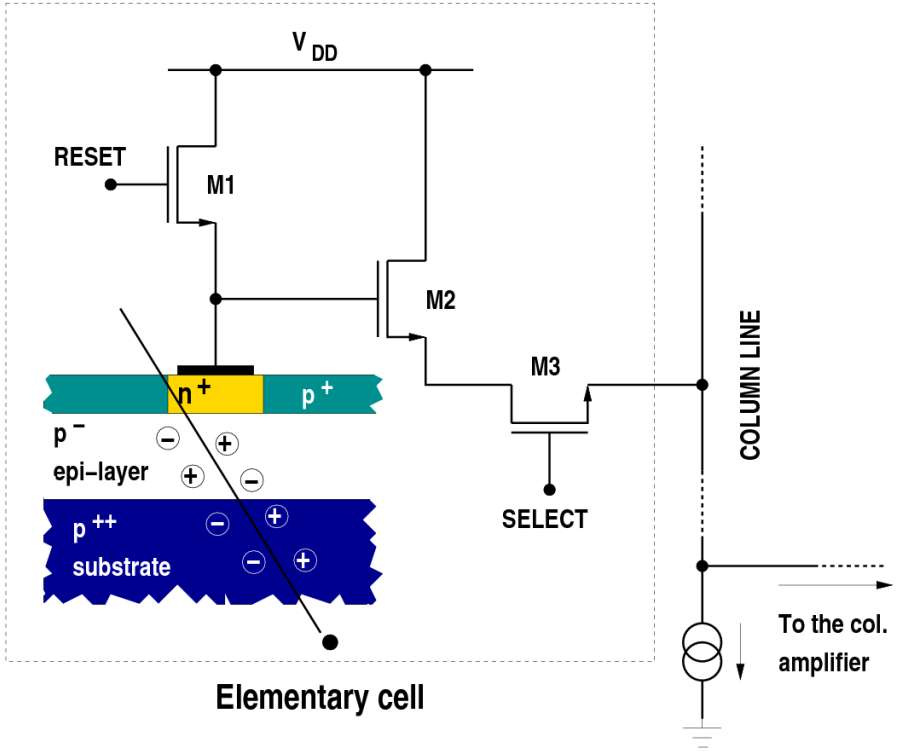
- CPPM, Marseilles
- IPHC, Strasbourg
- IRFU Saclay
- LAL, Orsay
- LPNHE, Paris
- CMP, Grenoble
- University of Sherbrooke
- University of Bonn
- AGH University of Science &Technology, Poland
- Universitat de Barcelona

✓ Benefits:
- Sharing of designs
- Development of special software programs
- Development of libraries and test structures
- Design review
- Sharing of results
- Frequent meetings
- Cost reduction

- The WP3 of the AIDA project (Advanced European Infrastructures for Detectors at Accelerators) aims at establishing a network activity to enable access to vertical integration technologies

Some examples of intelligent pixel detectors

Monolithic active pixel sensors in CMOS technology



Elementary cell

P-type, high resistivity, epitaxial layer acts as a potential well for electrons
(Feasibility with non epitaxial CMOS processes has been demonstrated by Dulinski et al., *IEEE TNS* **51** (2004) 1613)

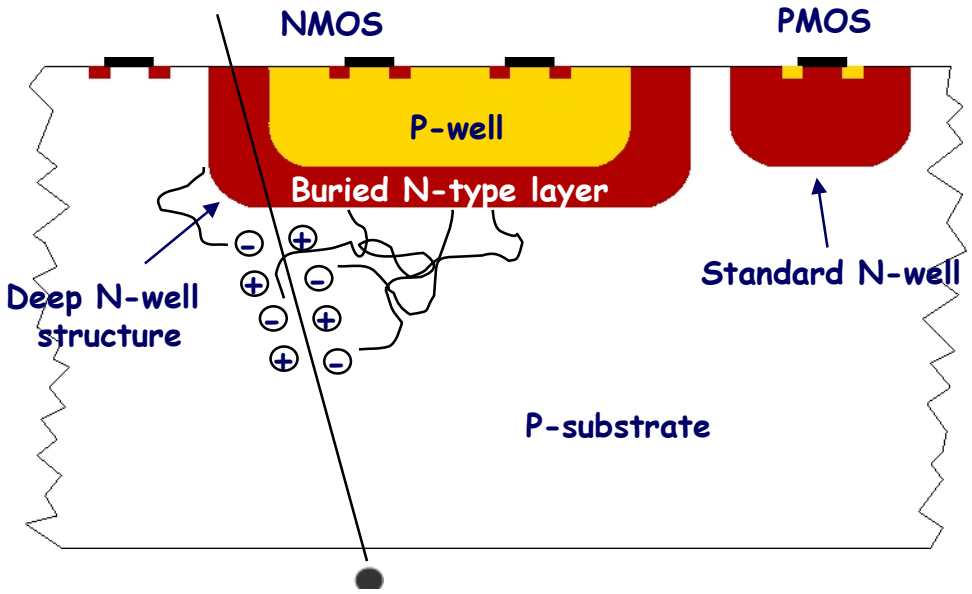
Electrons diffuse until they reach the n-well/epi-layer junction

Charge-to-voltage conversion is provided by sensor capacitance

Extremely simple, mostly 3T, in-pixel readout configuration (no PMOS allowed) (Examples of advanced functions integrated at the pixel level are available in the literature: G. Deptuch et al., NIM A512 (2003) 299)

- CMOS MAPS might be thinned down to a few tens of microns with no significant degradation in charge collection
- Functional density and circuit complexity at the pixel level may be limited by fill factor constraints and PMOS unavailability

DNW MAPS

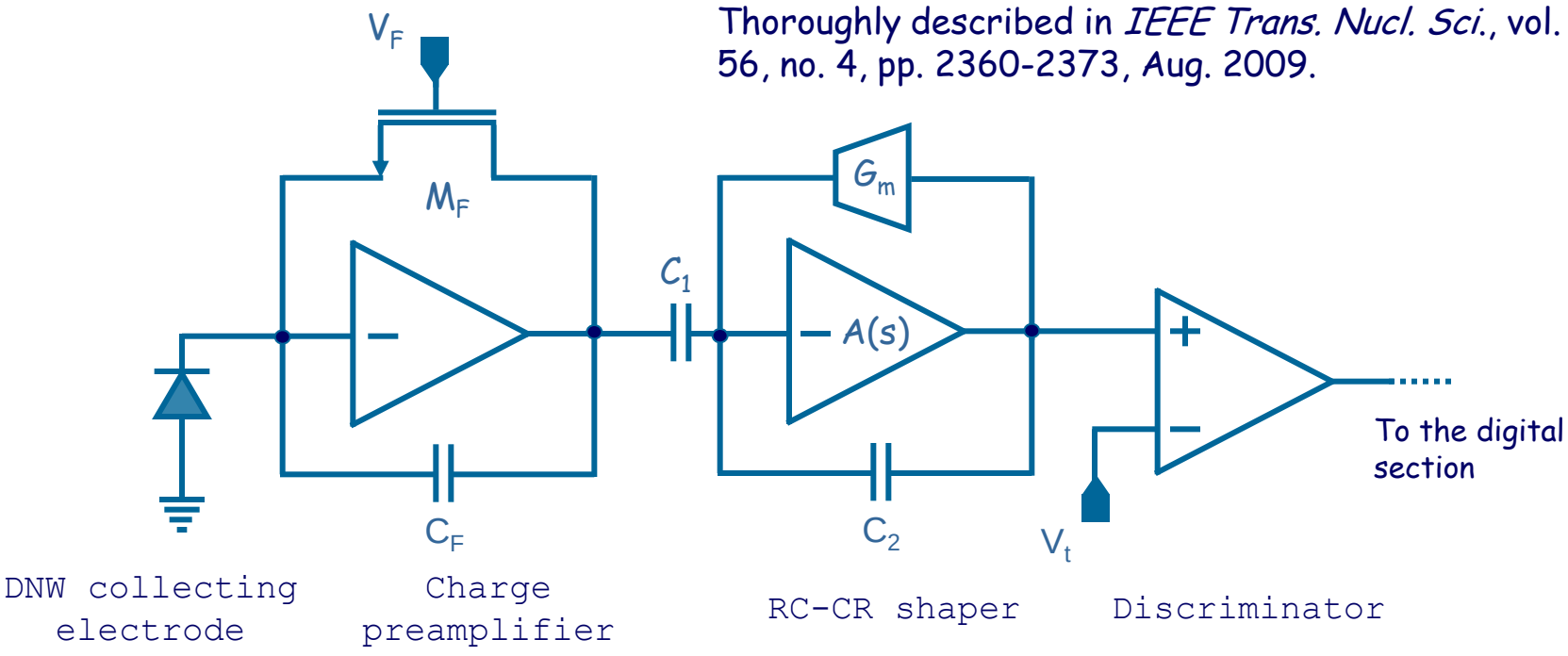


- MAPS may satisfy the requirements (resolution, multiple scattering) of the experiments at the future high luminosity colliders
- DNW monolithic sensors were proposed to improve readout speed through sparsification techniques

- A DNW is used to collect the charge released in the substrate
- A classical readout channel for capacitive detectors is used for Q-V conversion → gain decoupled from electrode capacitance
- NMOS devices of the analog section are built in the deep N-well
- Using a large detector area, PMOS devices may be included in the front-end design → charge collection inefficiency depending on the ratio of the DNW area to the area of all the N-wells (deep and standard)

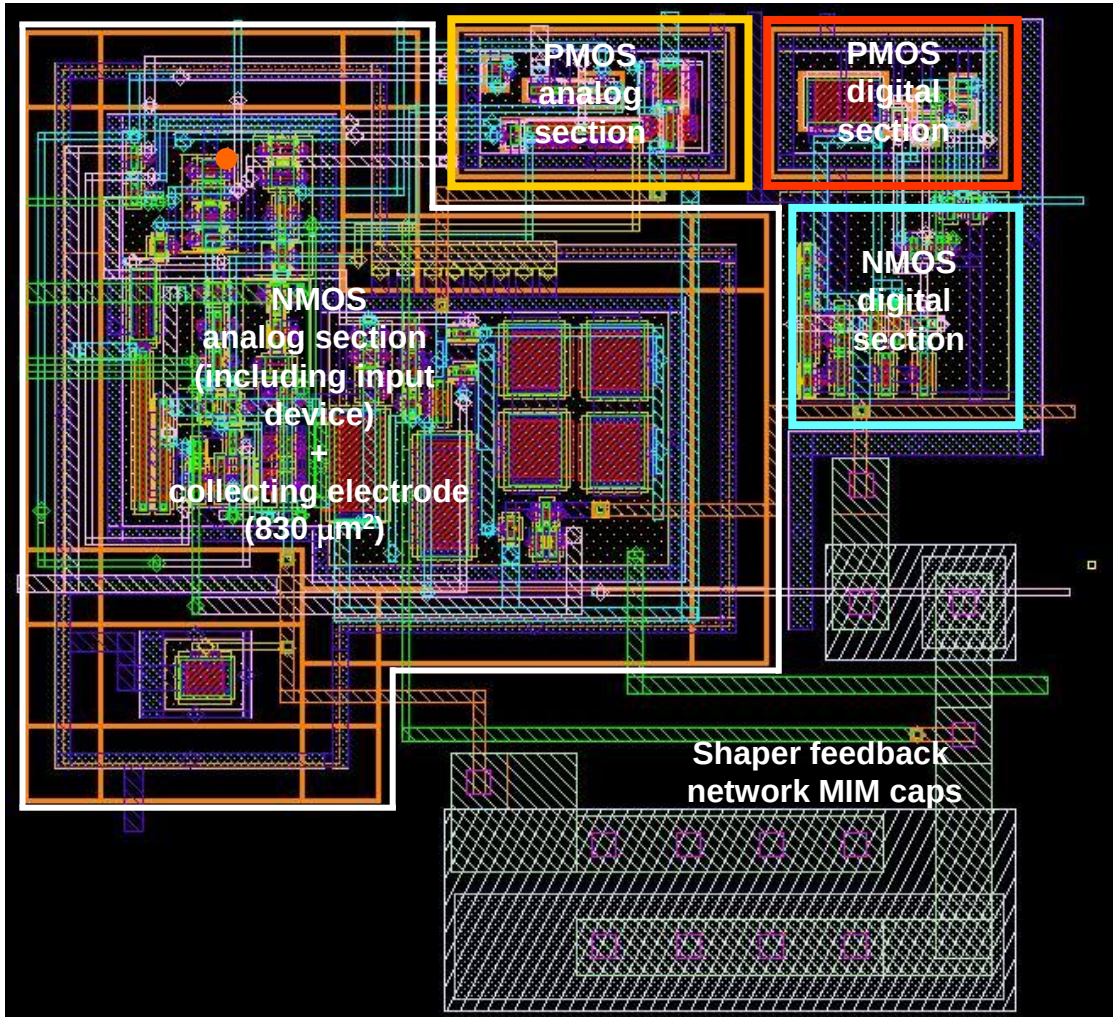
DNW MAPS front-end architecture

Thoroughly described in *IEEE Trans. Nucl. Sci.*, vol. 56, no. 4, pp. 2360-2373, Aug. 2009.



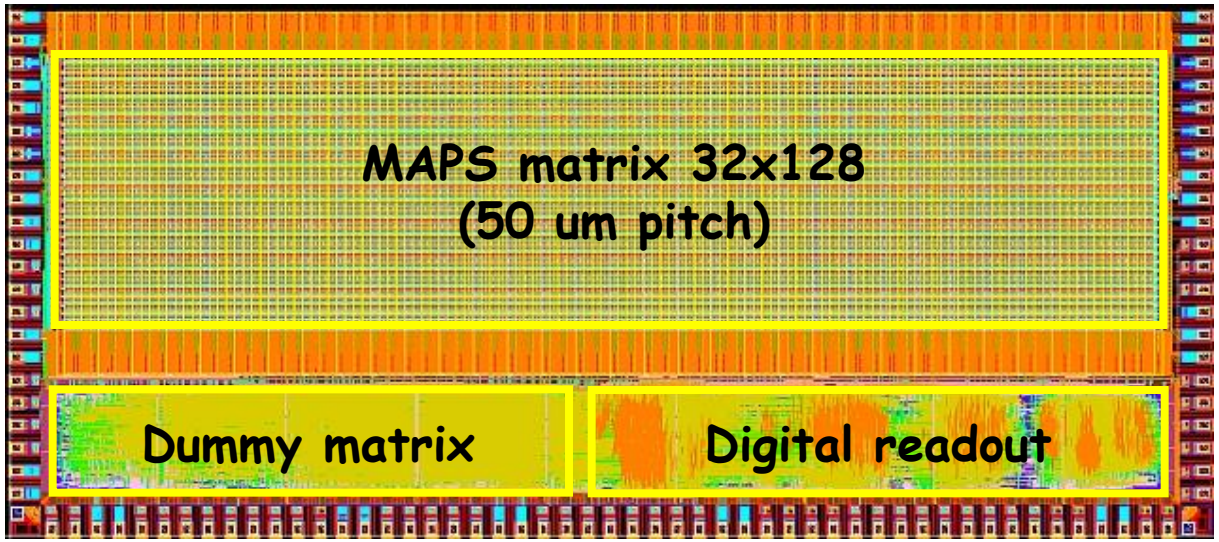
- Sensor and front-end (analog and digital, not shown) electronics integrated in a 50 μm pitch pixel (130 nm CMOS technology)
- Continuous time shaping, selectable peaking time (200 and 400 ns), 30 μW/channel power dissipation, C_D≈300 fF, W/L=14/0.25 for the preampli input device

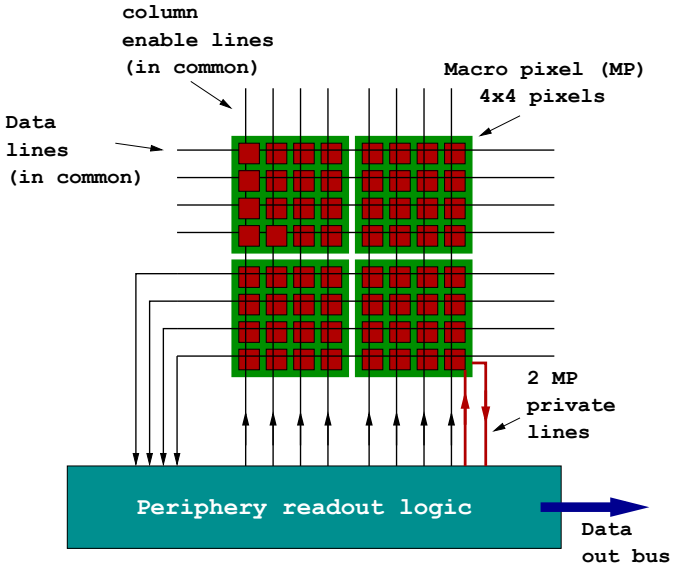
Layout of the elementary cell (Apsel series)



MAPS matrix with data driven readout

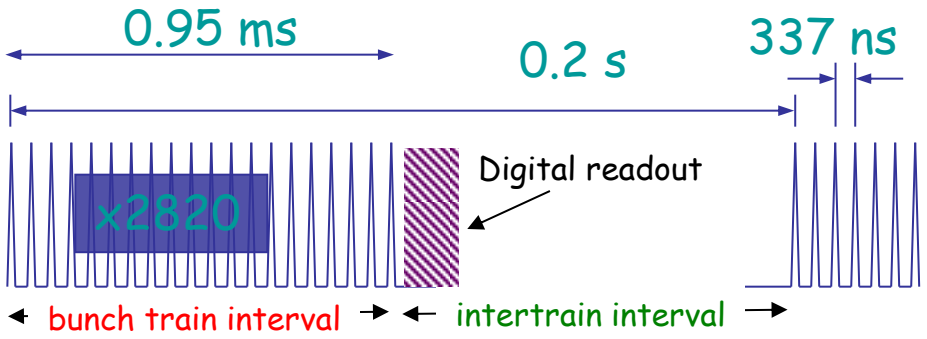
- A dedicated readout architecture to perform on-chip data sparsification has been implemented in the Apsel4D prototype
  - time stamps are generated in the chip periphery and associated to hits
  - matrix logically organized in macro-pixels (MP, 4x4 pixels)
  - two lines from the periphery to each MP (one to communicate the arrival of a hit, the other to freeze, reset and re-enable a hit MP)
  - data are brought out of the matrix through horizontal lines running along each row and shared among the pixels in the row





Beam structure at the ILC experiments

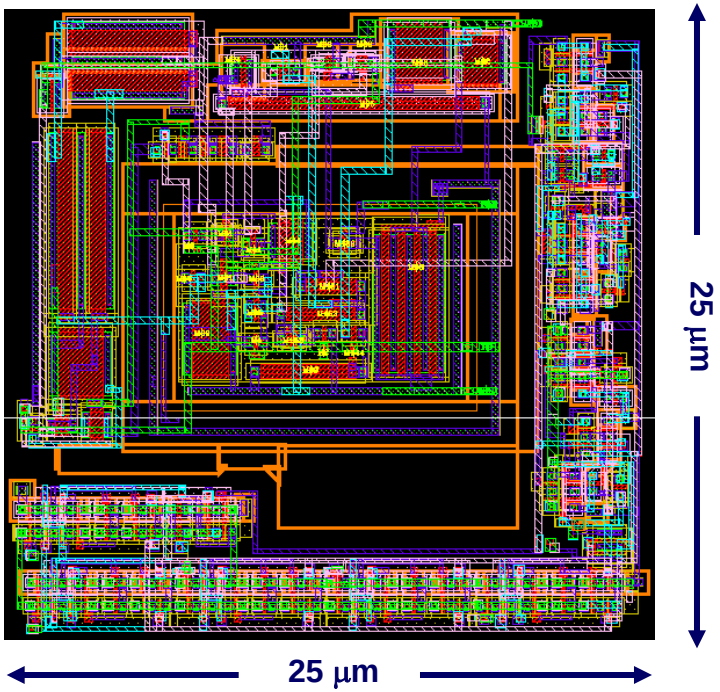
- The International Linear Collider (ILC) is a linear e^+ e^- accelerator, which will be operated at 500 GeV/1 TeV
  - The beam structure at the ILC will feature 2820 bunches per train, each lasting slightly less than 1 ms, with an interbunch period of 330 ns and a repetition rate of 5 Hz
  - The operation of many monolithic pixel readout chips has been tailored on the beam structure of the ILC; therefore, in some of these chips, an acquisition interval (corresponding to the bunch train period) and a readout interval (corresponding to the intertrain period) have been envisioned



DNW MAPS for the ILC (SDR series)

- A different DNW MAPS version has been developed (in a 130 nm CMOS process) for applications to the ILC vertex detector, requiring relatively small point resolution (5 μm or better); this translates to severe constraints on the pixel pitch, which was reduced to 25 μm with respect to the Apsel series MAPS (50 μm)

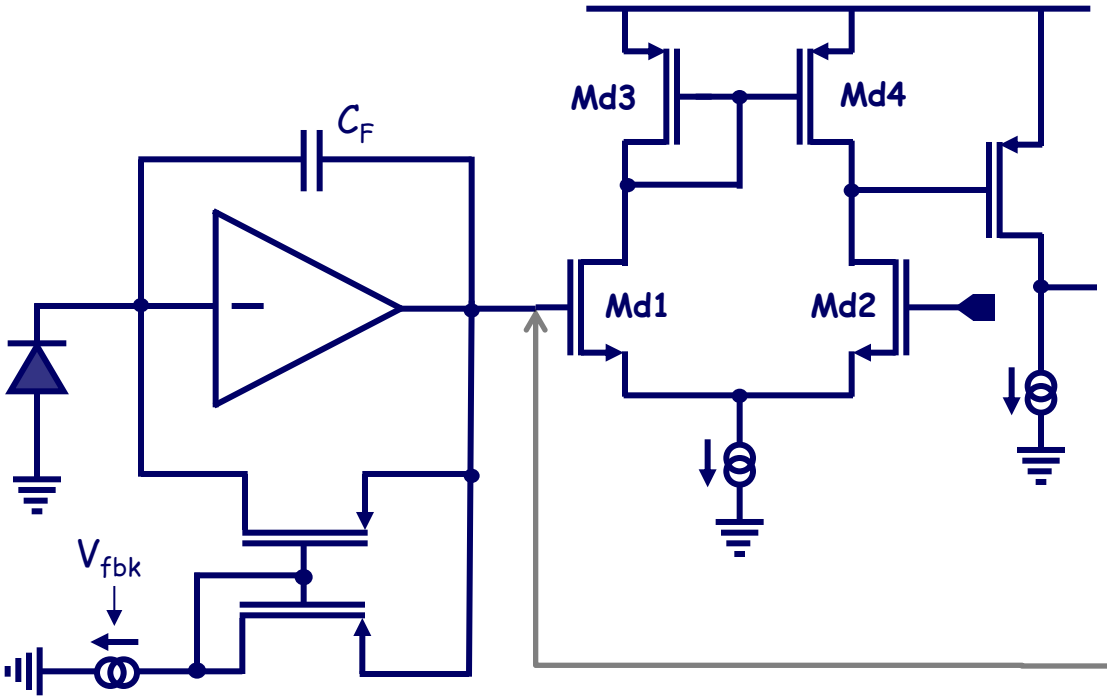
Layout of the elementary cell of the SDR0 MAPS chip

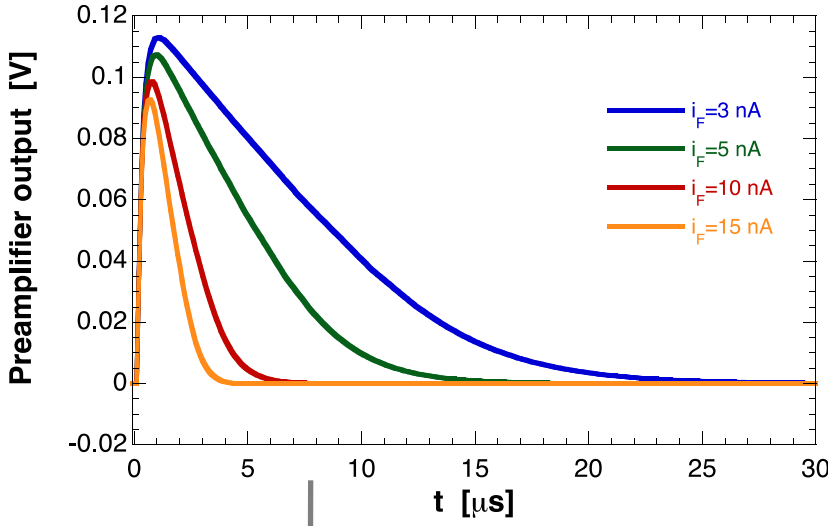


Shaperless front-end for DNW MAPS (SDR series)

- The analog front-end has to be simplified taking into account the reduced dimensions of the elementary cell; the signal processor only includes a charge preamplifier, whose bandwidth is purposely limited to reduce noise

Charge preamplifier Discriminator

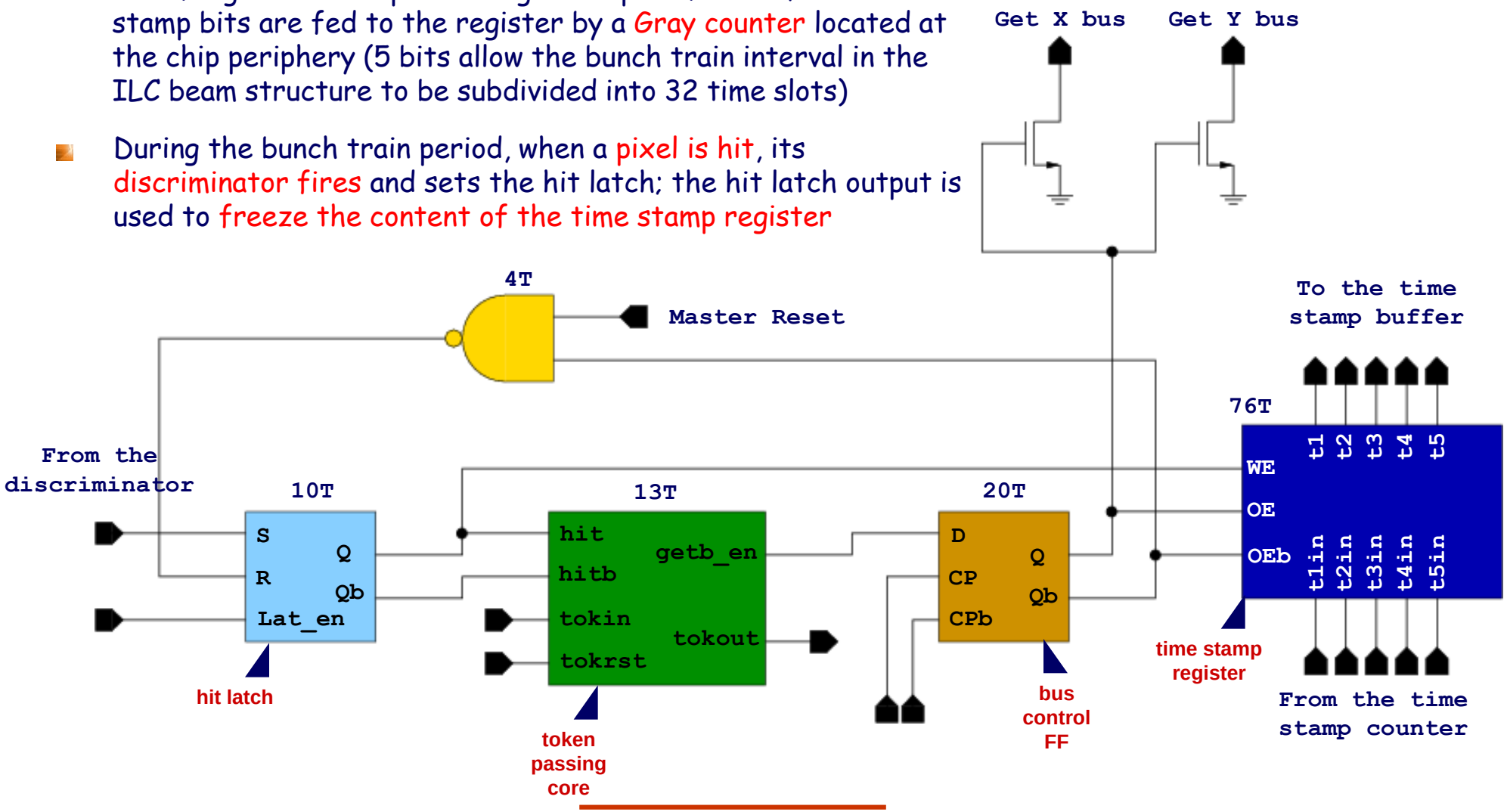




Digital front-end (SDR series)

Implemented by INFN Pavia from a FNAL idea

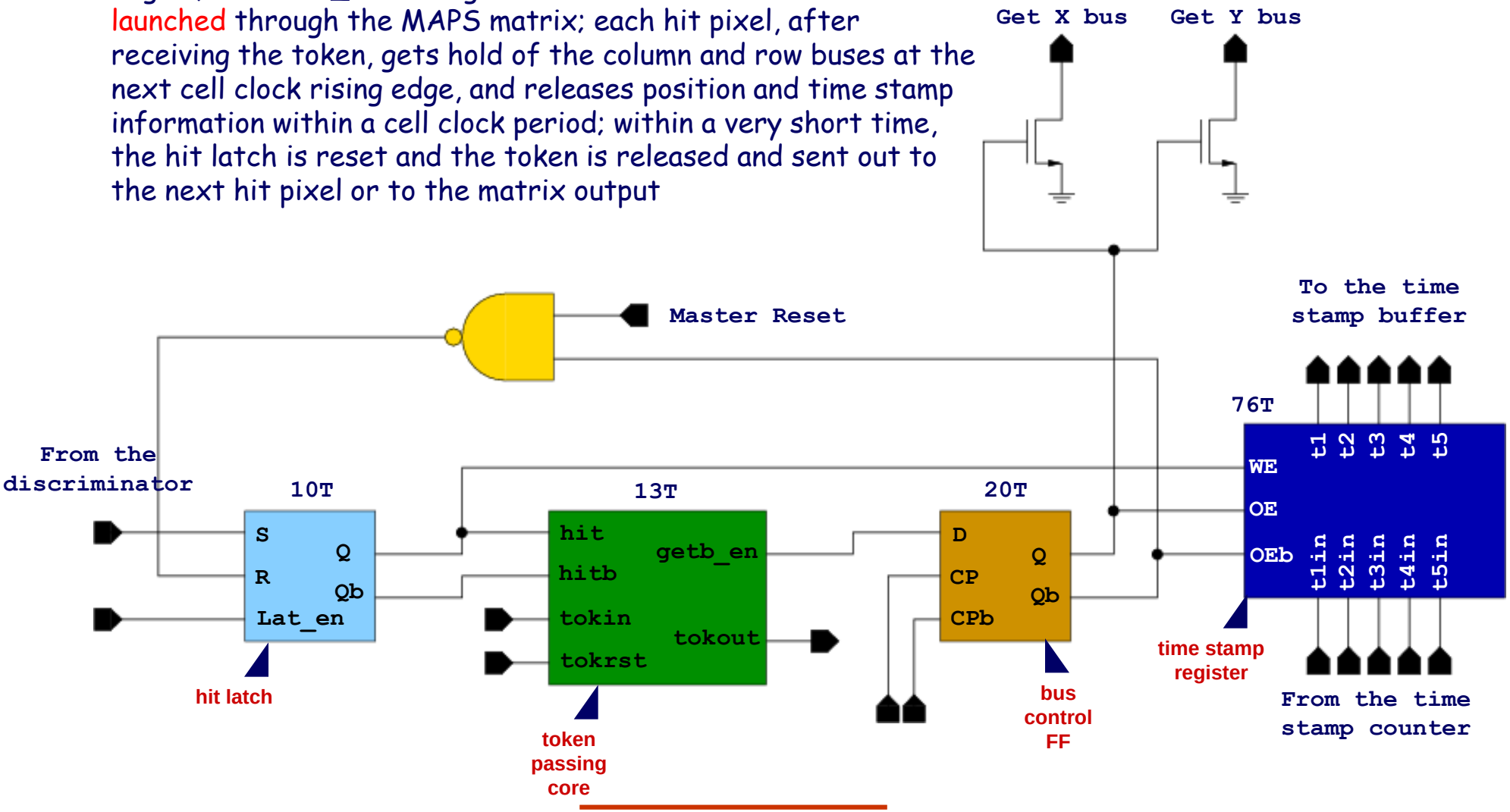
- The elementary cell includes a 5-bit time stamp register and a set of logic blocks implementing data sparsification; the 5 time stamp bits are fed to the register by a Gray counter located at the chip periphery (5 bits allow the bunch train interval in the ILC beam structure to be subdivided into 32 time slots)
- During the bunch train period, when a pixel is hit, its discriminator fires and sets the hit latch; the hit latch output is used to freeze the content of the time stamp register



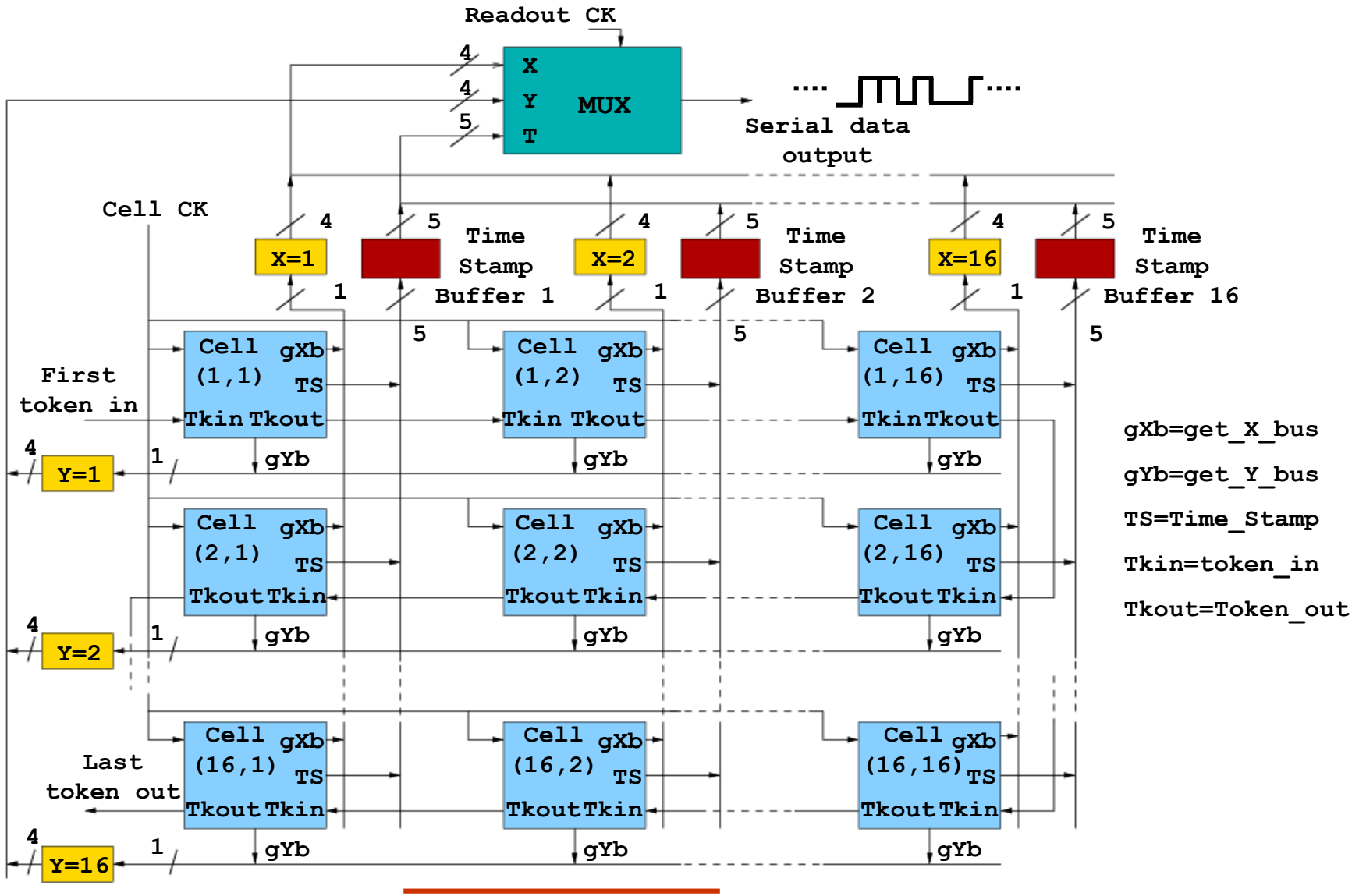
Digital front-end (SDR series)

Implemented by INFN Pavia from a FNAL idea

- At the end of the bunch train period, when the readout phase begins, the latch_enable signal is switched off and the token is launched through the MAPS matrix; each hit pixel, after receiving the token, gets hold of the column and row buses at the next cell clock rising edge, and releases position and time stamp information within a cell clock period; within a very short time, the hit latch is reset and the token is released and sent out to the next hit pixel or to the matrix output

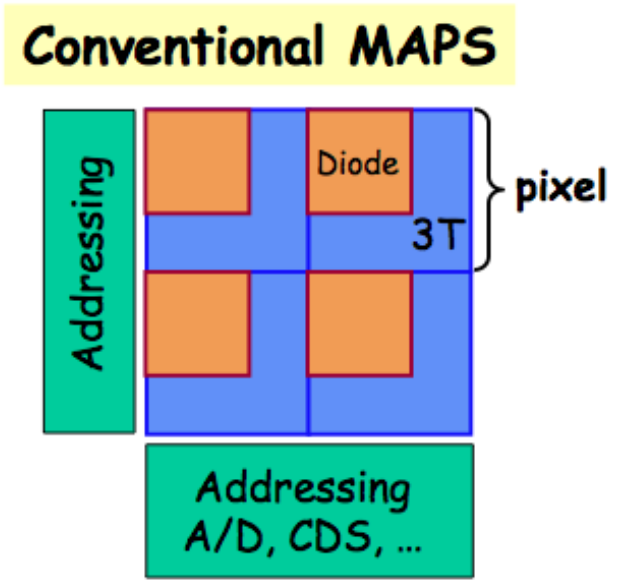


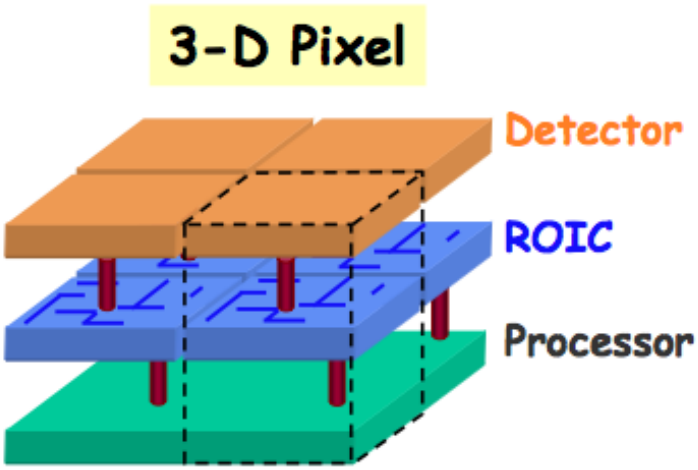
Token passing readout for DNW MAPS (SDR series)



3D pixel sensors

- Vertical integration processes represent a technological leap in the design of monolithic radiation sensors
- In a conventional monolithic sensor
  - the sensor and the front-end electronics share pixel area, with a consequent loss in collection efficiency and/or fill factor; for the front-end electronics and sensor to coexist in the pixel, non optimized design solutions for both have to be accepted
  - control and support electronics is placed outside the imaging area, where they form a dead region for the sensor
- In the 3D version of a monolithic pixel sensor
  - the sensor area can be fully active, resulting in a four-side buttable chip;
  - circuit density and functionality is increased due to the availability of multiple layers of electronics
  - each layer of the detector can be optimized from the standpoint of the fabrication process

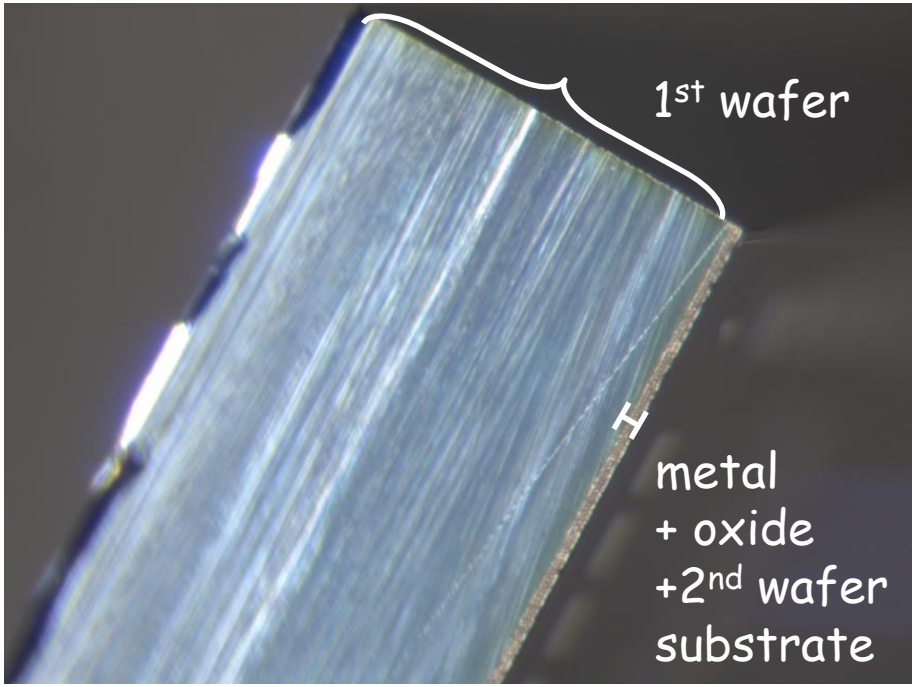




Key technologies for wafer level 3D integration

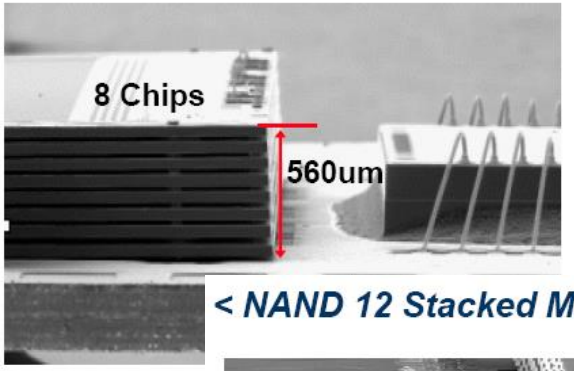
- Several process sequences have been developed to fabricate wafer stacks; many of them depend on the following enabling technologies
  - Through silicon via (TSV) formation: fabrication of electrically isolated connections through the silicon substrate; the diameter of the TSV is dependent on the degree of access to an individual stratum, which in turn depends on the application
  - Thinning of the strata: stacked layers may be thinned to below 50 µm in memory stacks, 25 µm for CMOS silicon circuits and to below 5 µm for SOI circuits
  - Alignment: a precision better than 1 µm is required
  - Wafer bonding: may be obtained through oxide to oxide fusion, direct copper fusion, copper/tin bonding or polymer bonding; bonding can be made between two wafers, between a die and a wafer or between two dice
- Wafers to be bonded may come from the same process (homogeneous integration) or be based on different technologies (heterogeneous integration); if the different layers of the circuits perform qualitatively different tasks (for example, sensing and signal processing) then the most suitable technology can be chosen for each layer

Vertical integration processes

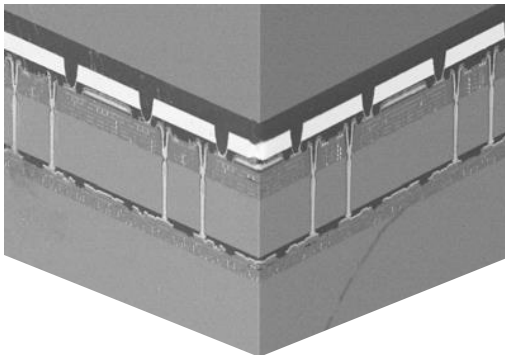


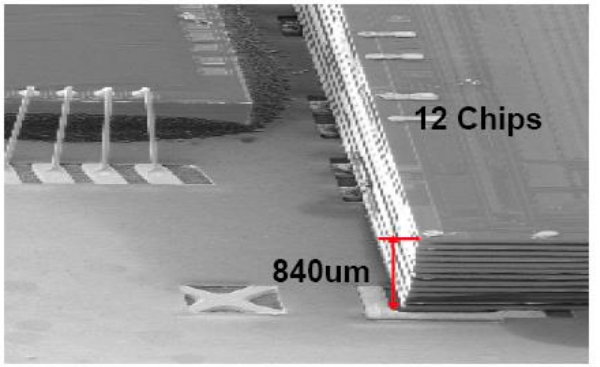
< 2 layer MAPS for particle tracking >

< NAND 8 Stacked Memory Card >



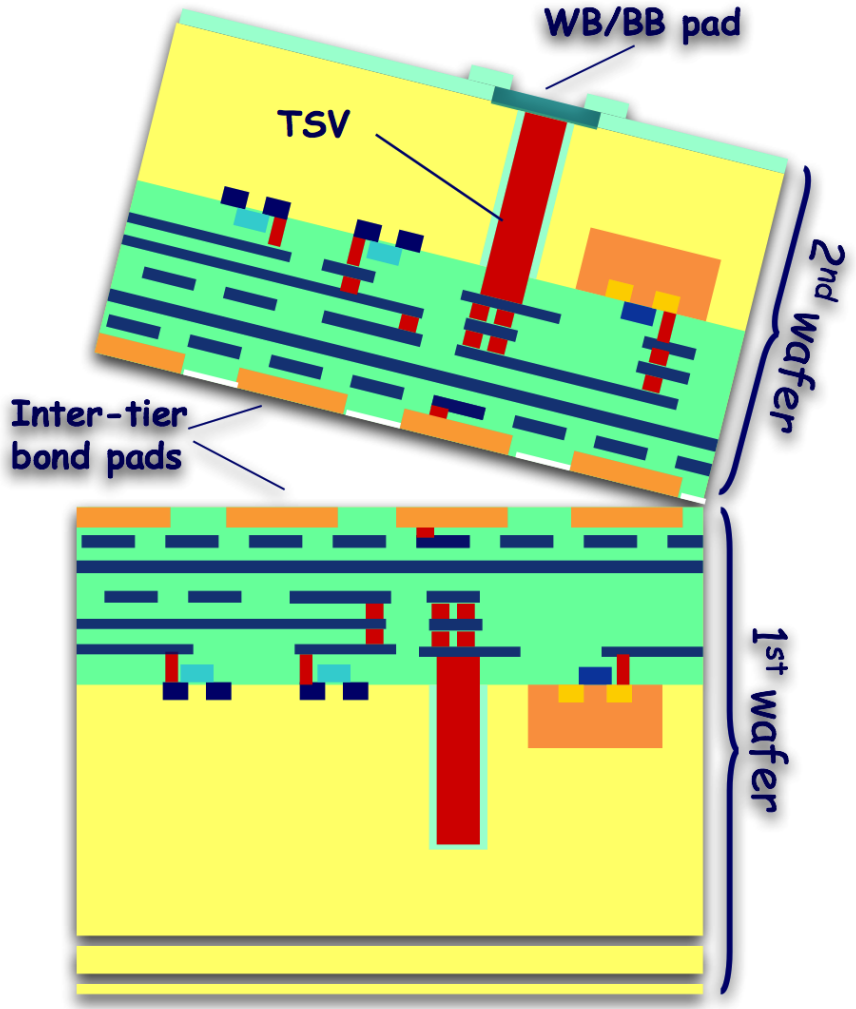
< NAND 12 Stacked Memory Card >





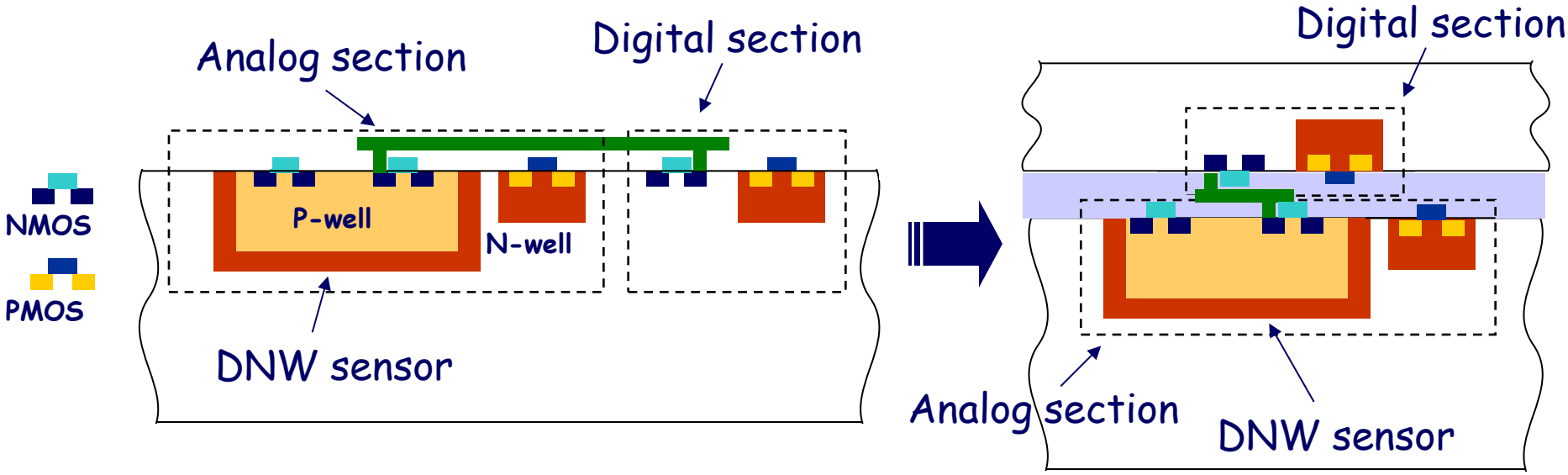
Tezzaron/Chartered homogeneous 3D integration

- In wafer-level, three-dimensional processes, multiple strata of planar devices are stacked and interconnected using through silicon vias (TSV)
- 3D processes rely upon a set of enabling steps
  - TSV formation
  - Substrate thinning (below 50 μm)
  - Inter-layer alignment and mechanical/electrical bonding
- Tezzaron Semiconductor technology (via middle approach) can be used to vertically integrate two layers specifically processed by Chartered, now Globalfoundries (130 nm CMOS, 1 poly, 6 metal layers, 2 top metals, dual gate option, N- and PMOS available with different V_{th})



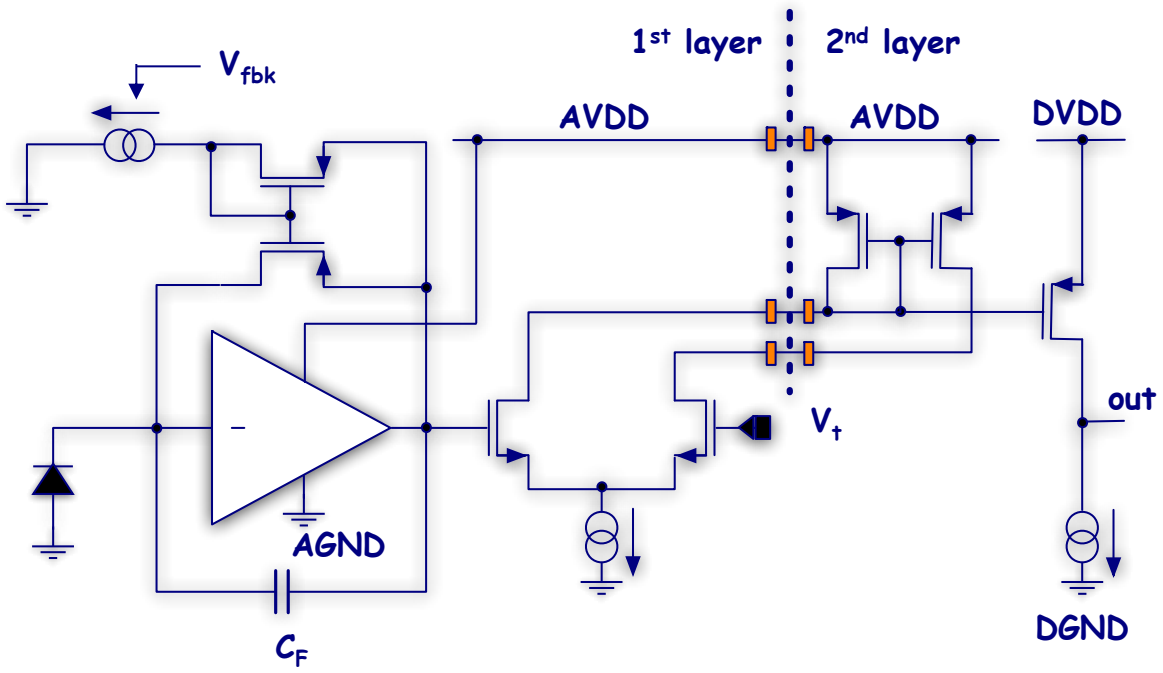
Migration to a 3D process (SDR series)

- Use of a 3D process makes it possible to separate analog from digital section to minimize cross-talk between digital blocks and sensor/analog circuits

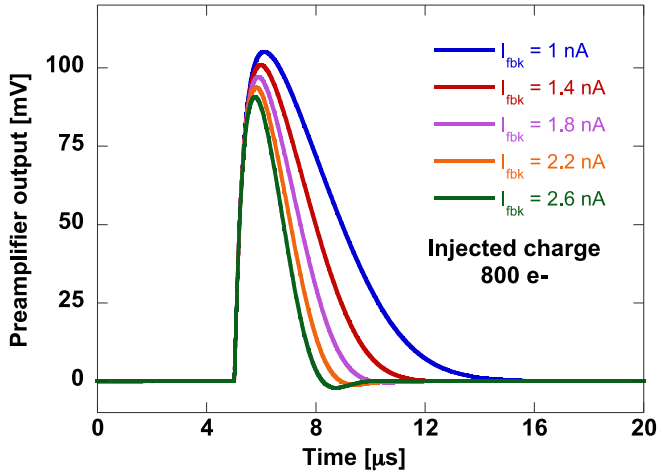


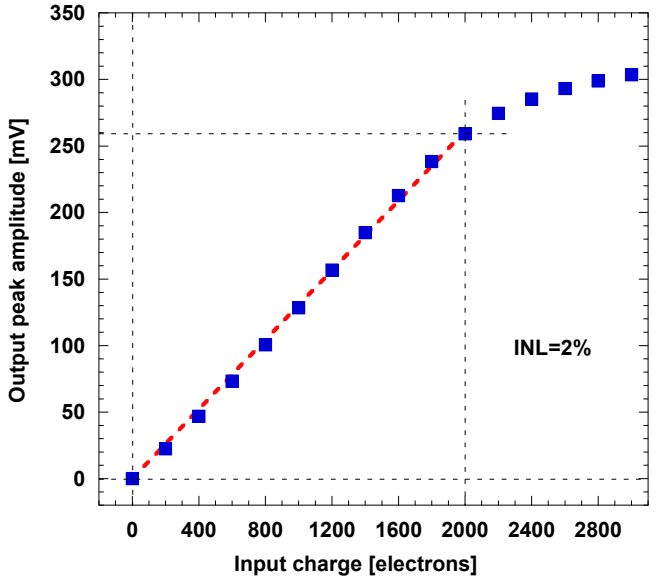
- Tier 1: collecting electrode (deep N-well/P-substrate junction) and analog front-end and discriminator
- Tier 2: digital front-end (2 latches for hit storage, pixel-level digital blocks for sparsification, 2 time stamp registers, kill mask) and digital back-end (X and Y registers, time stamp line drivers, serializer)

Analog FE and discriminator: the SDR1 3D MAPS



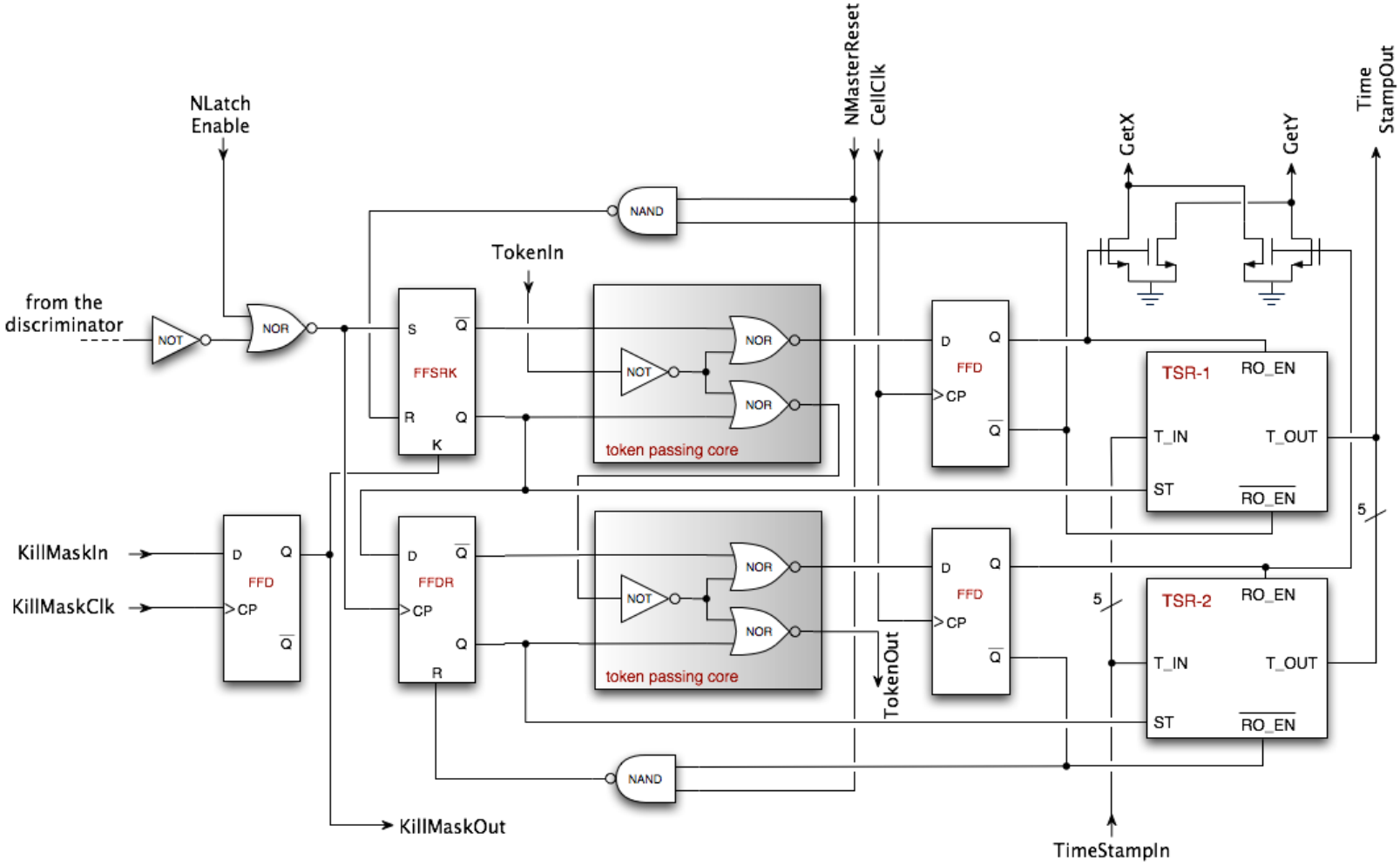
- 20 μm pitch
- W/L=20/0.18
- I_D=1.4 μA, power dissipation=5 μW
- C_D=200 fF
- ~1 μs peaking time
- Power cycling capabilities
- Charge sensitivity (G_Q): 800 mV/fC
- Equivalent noise charge (ENC): 35 e-
- Threshold dispersion (ΔQ_t): 36 e- (28 e- from the SFE, 22 e- from the discriminator)





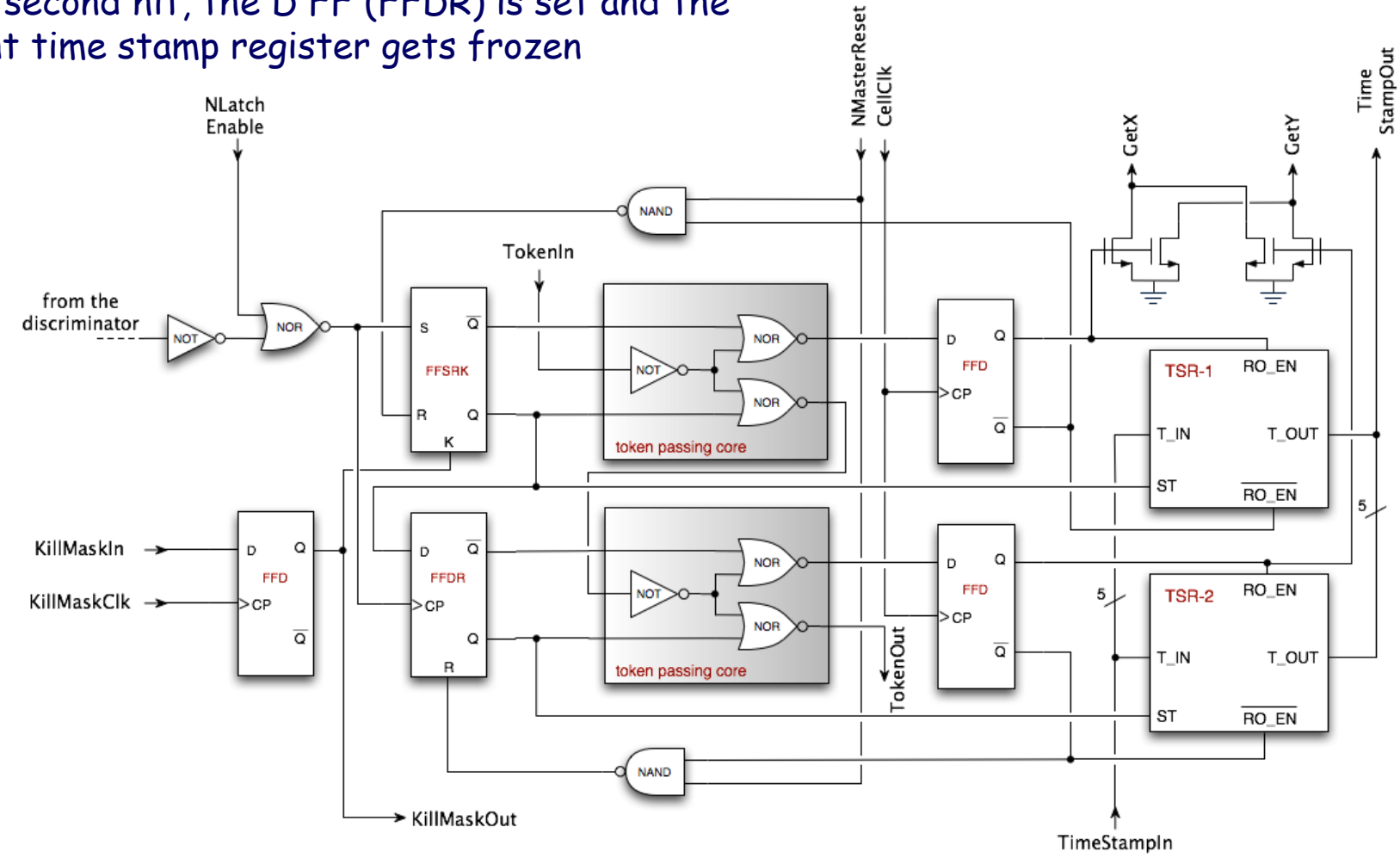
Digital front-end

- Digital front-end complexity can be increased; double hit detection, two 5-bit time stamps and a kill mask can be included

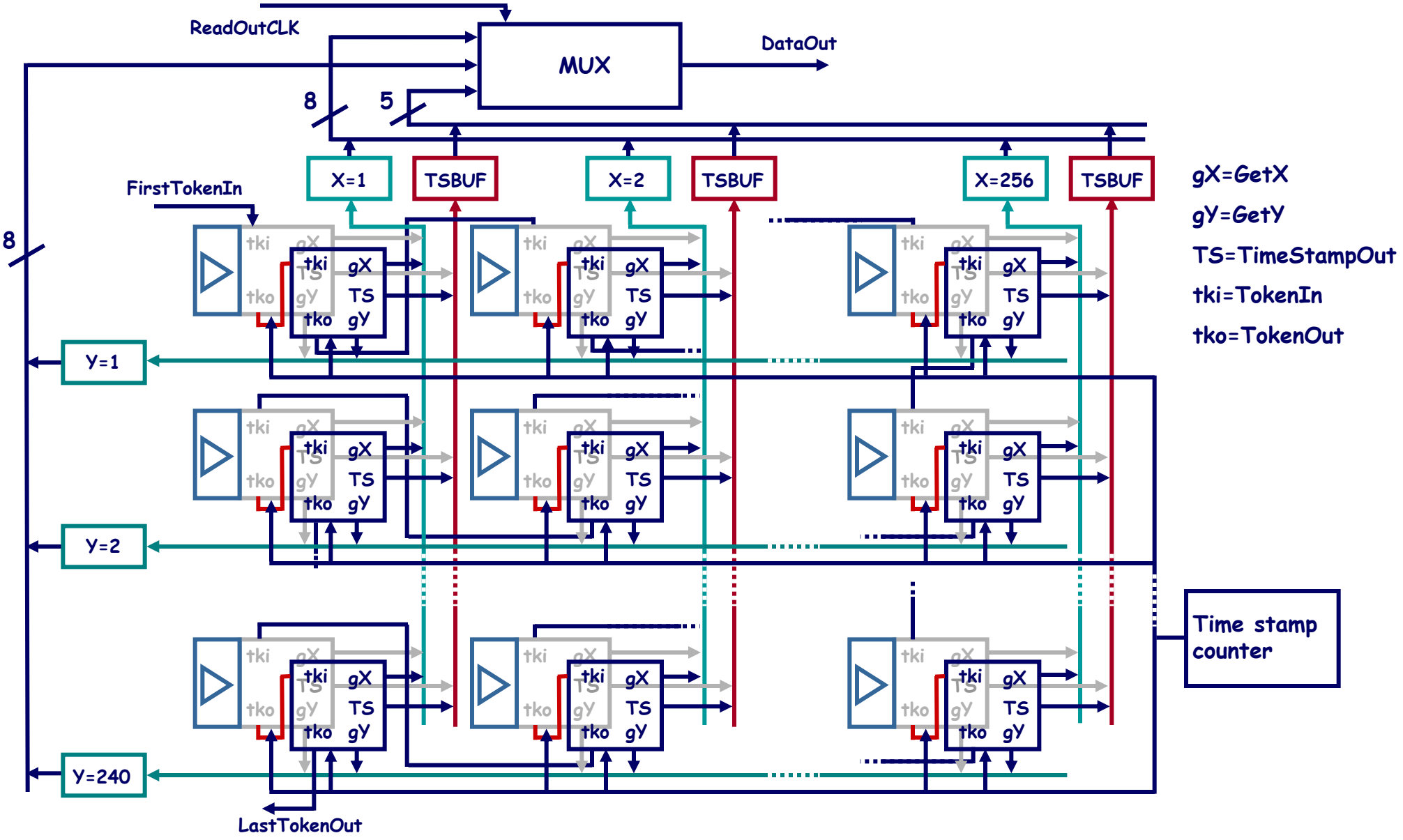


Digital front-end

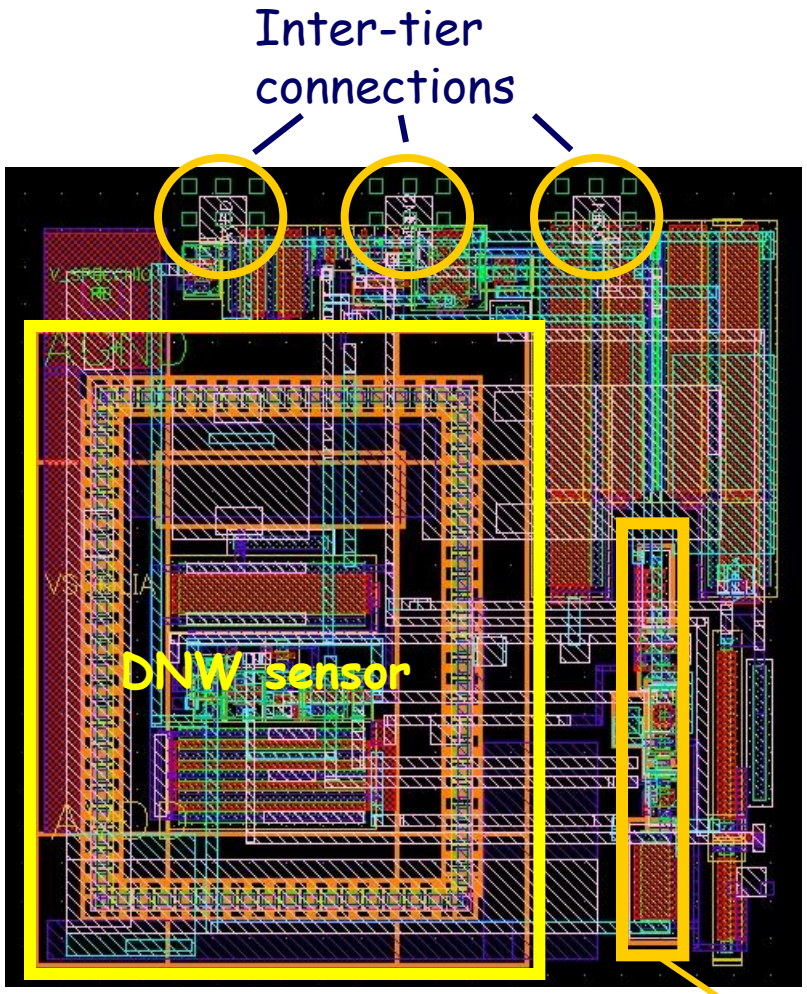
- During the bunch train period, the SR FF (FFSRK) is set, and the relevant time stamp register gets frozen, when the pixel is hit for the first time
- Upon a second hit, the D FF (FFDR) is set and the relevant time stamp register gets frozen



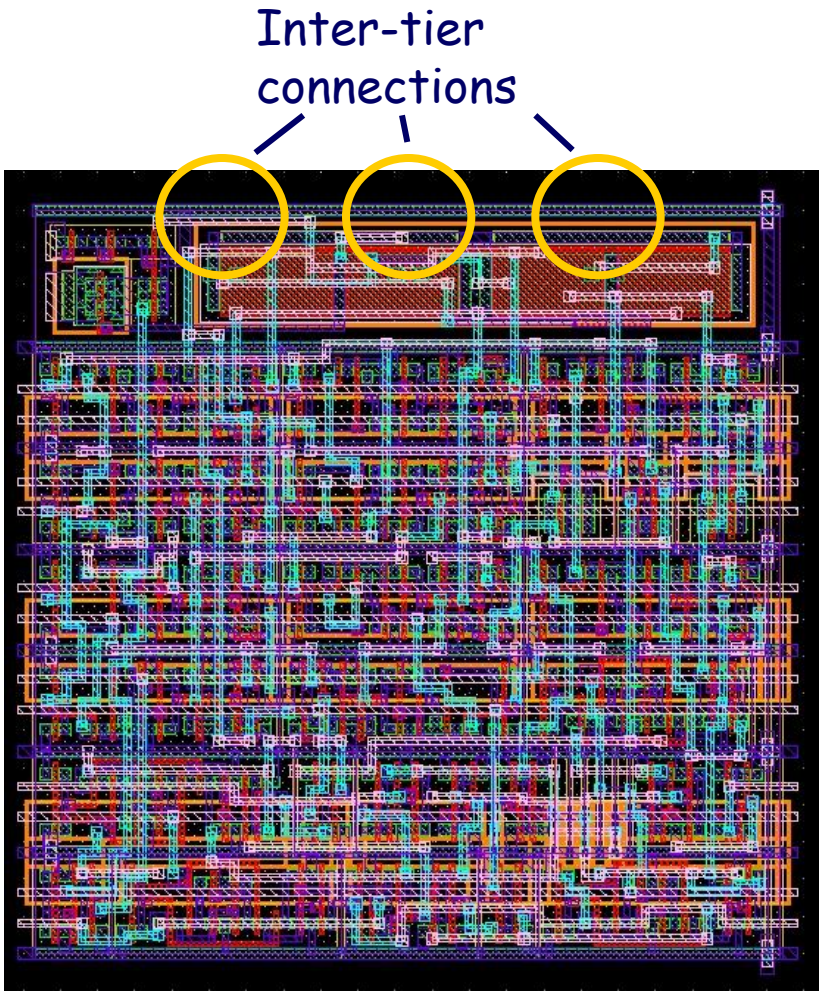
Token passing readout architecture



Elementary cell layout: bottom and top tiers



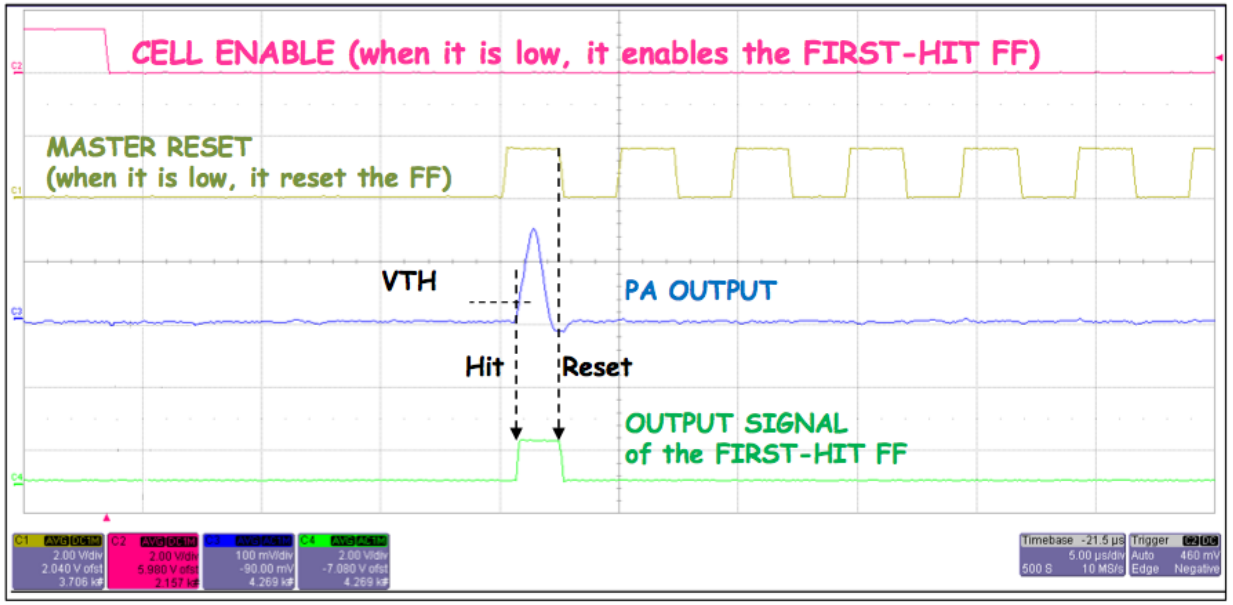
Analog section and
discriminator NMOS

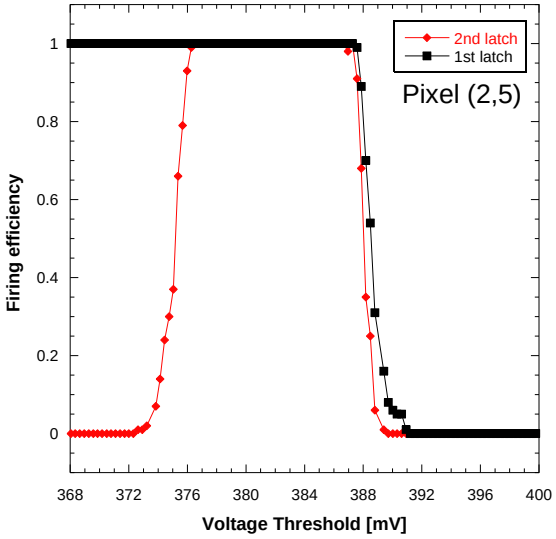


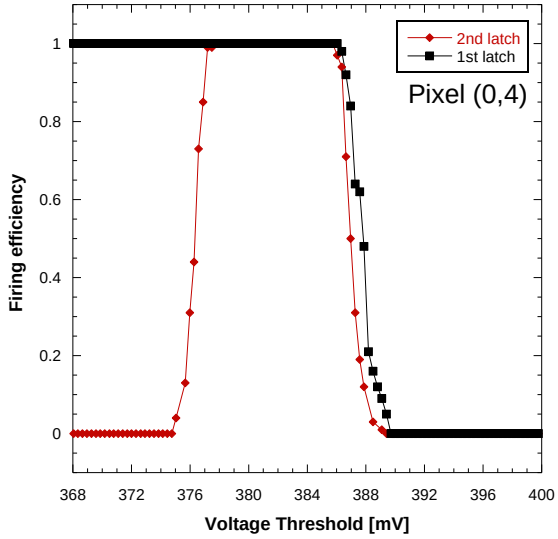
Digital section and
discriminator PMOS

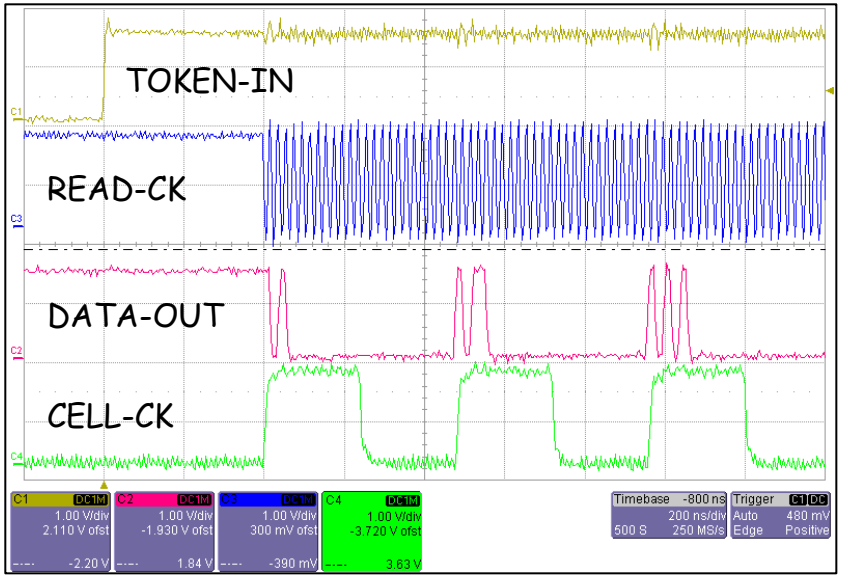
SDR1 test results

- 3D interconnection and token-based digital readout electronics fully functional
- No coupling between the digital and analog sections

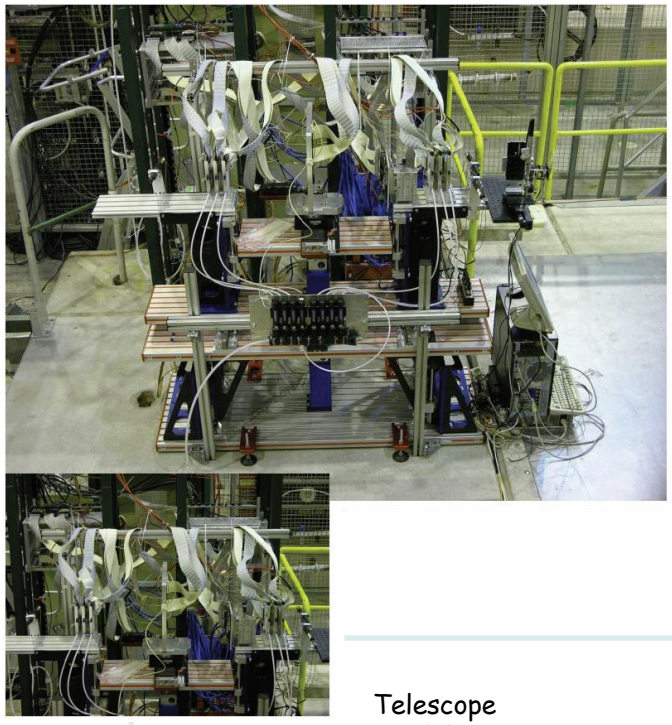


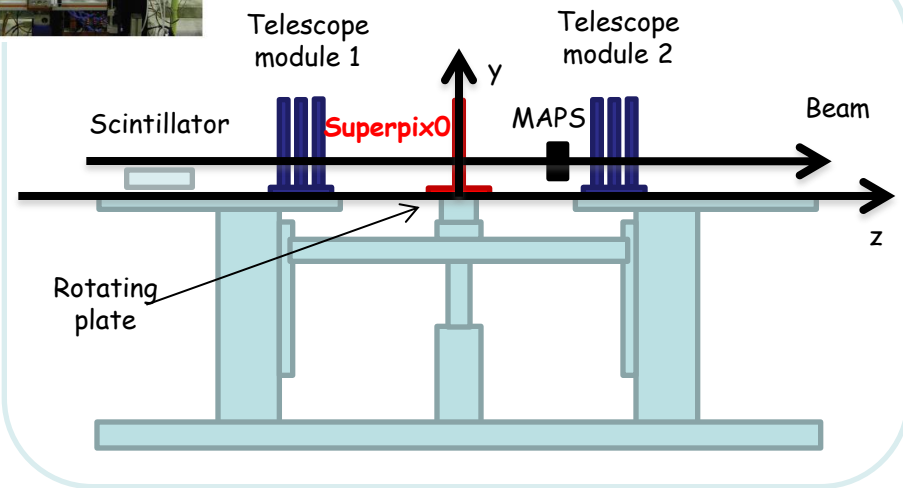


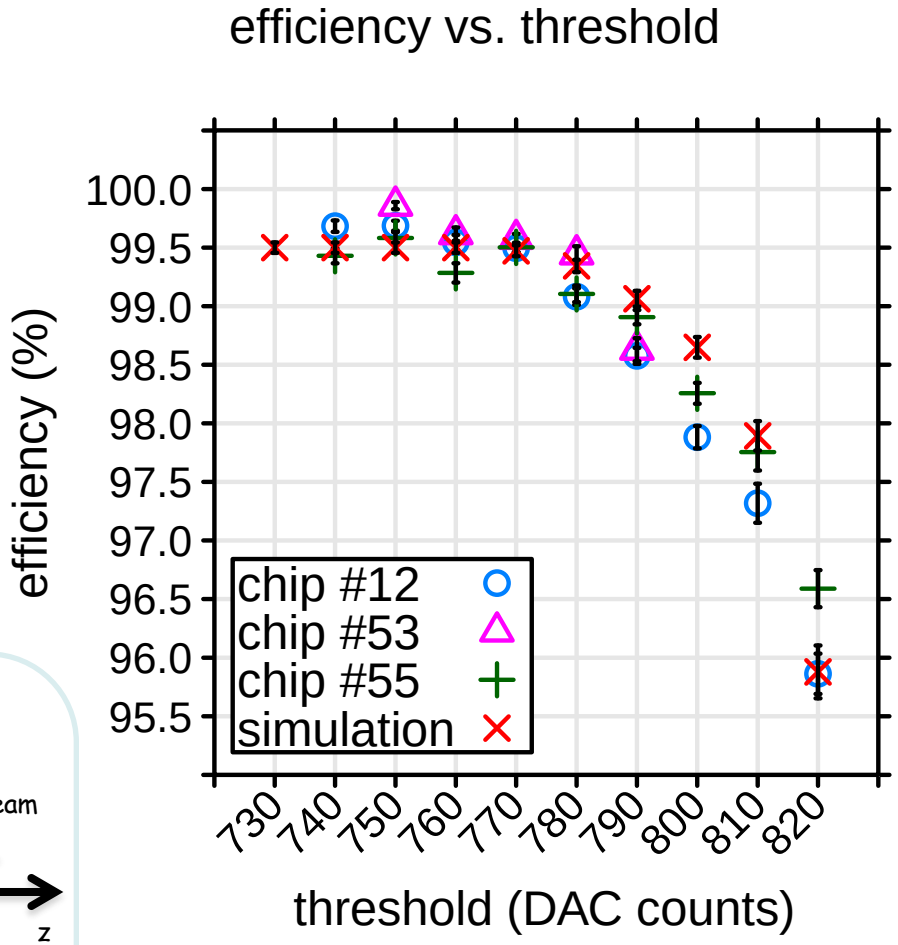




3D MAPS: test beam results



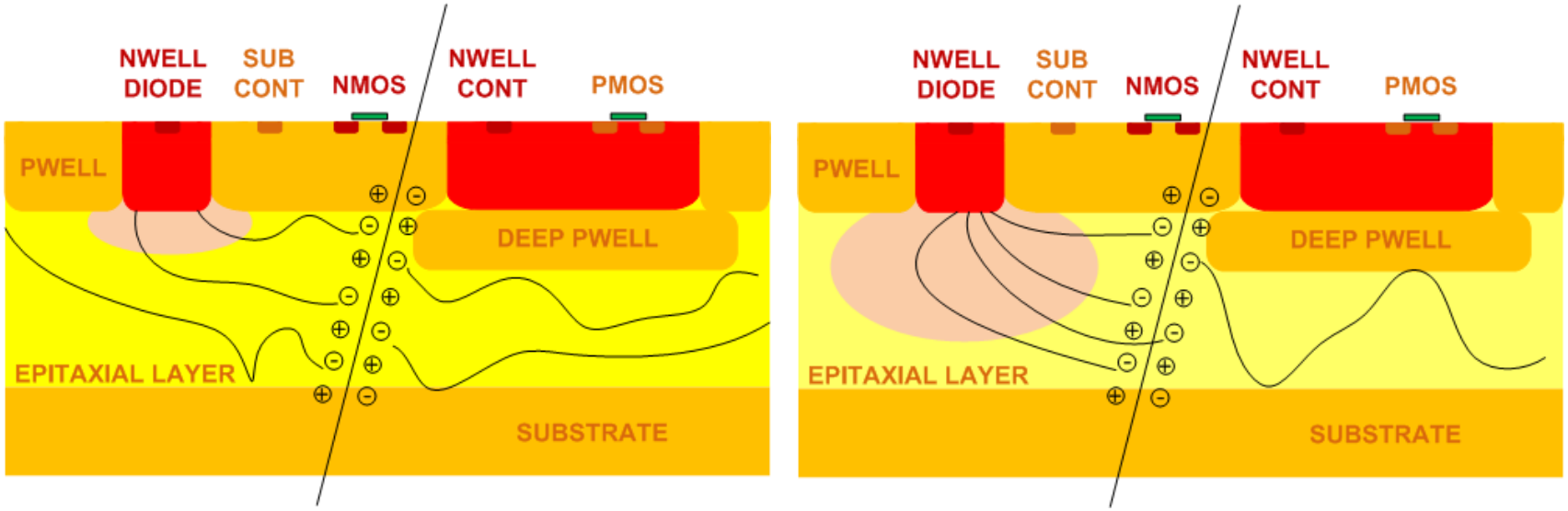




- 3D technology may provide some advantage to DNW MAPS in terms of detection efficiency

Quadruple well CMOS technology

- Charge collection efficiency of MAPS structures developed in a standard CMOS process can be affected by the presence of competitive N-wells needed for in-pixel logic suited for a fast readout
- In a quadruple well CMOS process, a deep P-well is used to shield the N-wells from the sensitive layer of the device
- Different epitaxial layer options - high resistivity epitaxial layer (1 kΩ·cm) expected to provide better charge collection properties and higher bulk damage tolerance

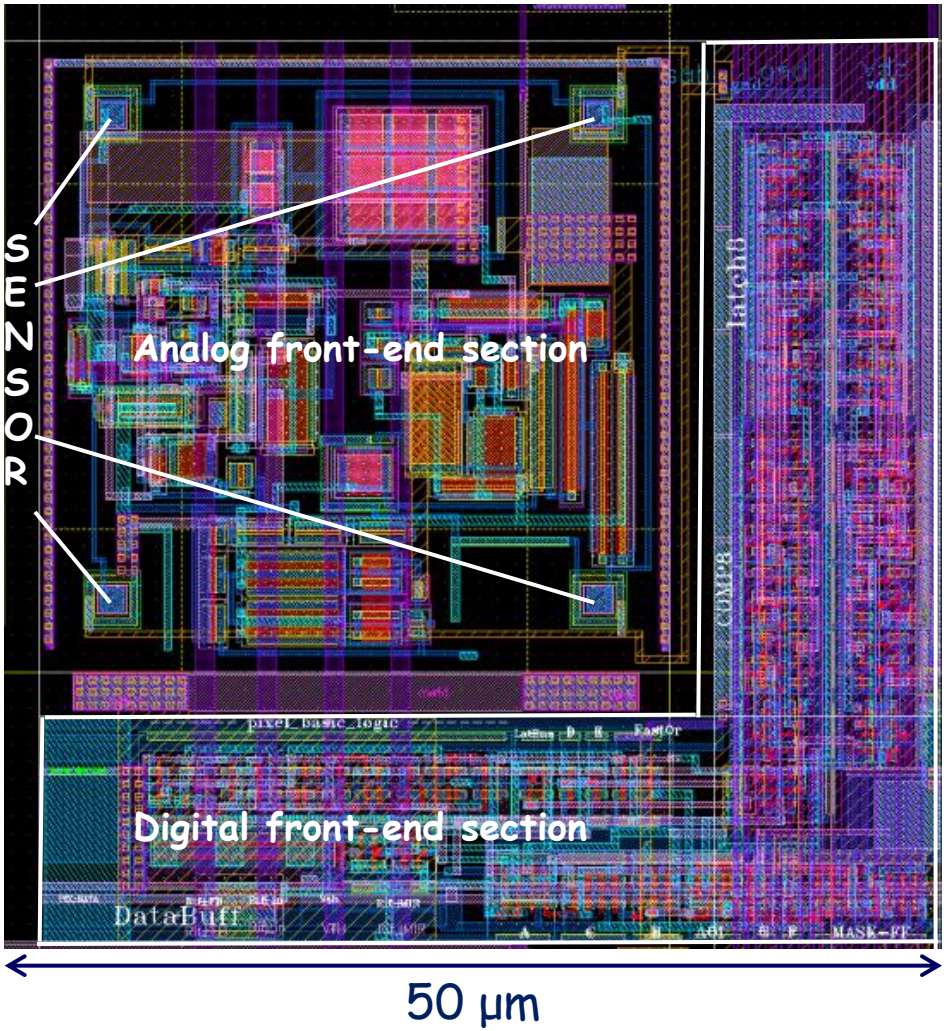


Standard resistivity epitaxial layer

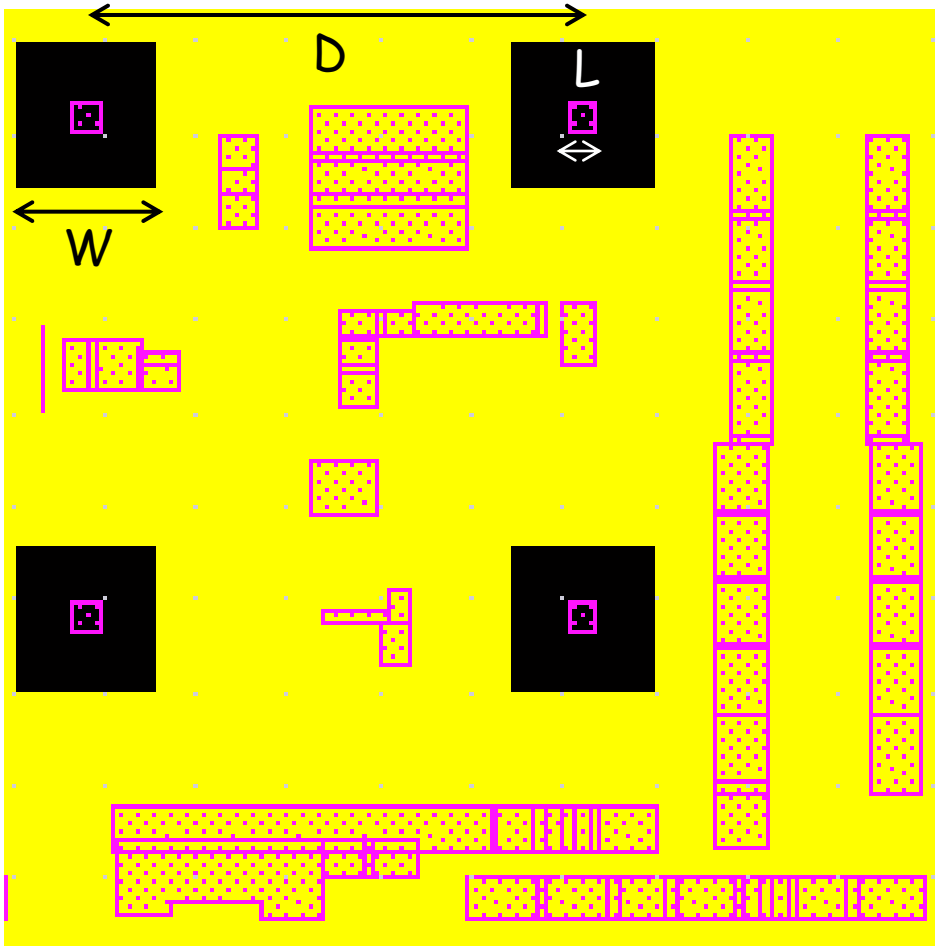
High resistivity epitaxial layer

Apsel4well pixel layout

Pixel layout w/o DPW layer

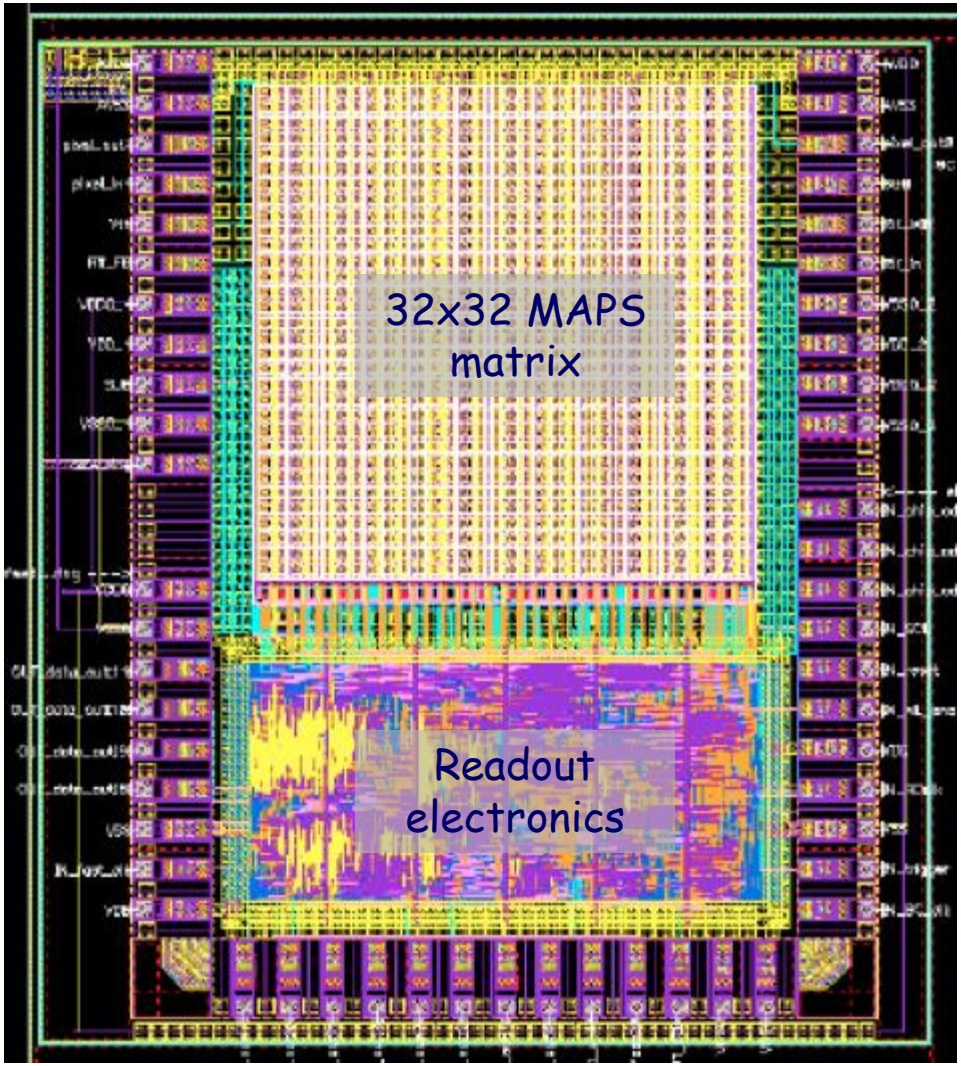


DPW (yellow) and NW (pink) layers

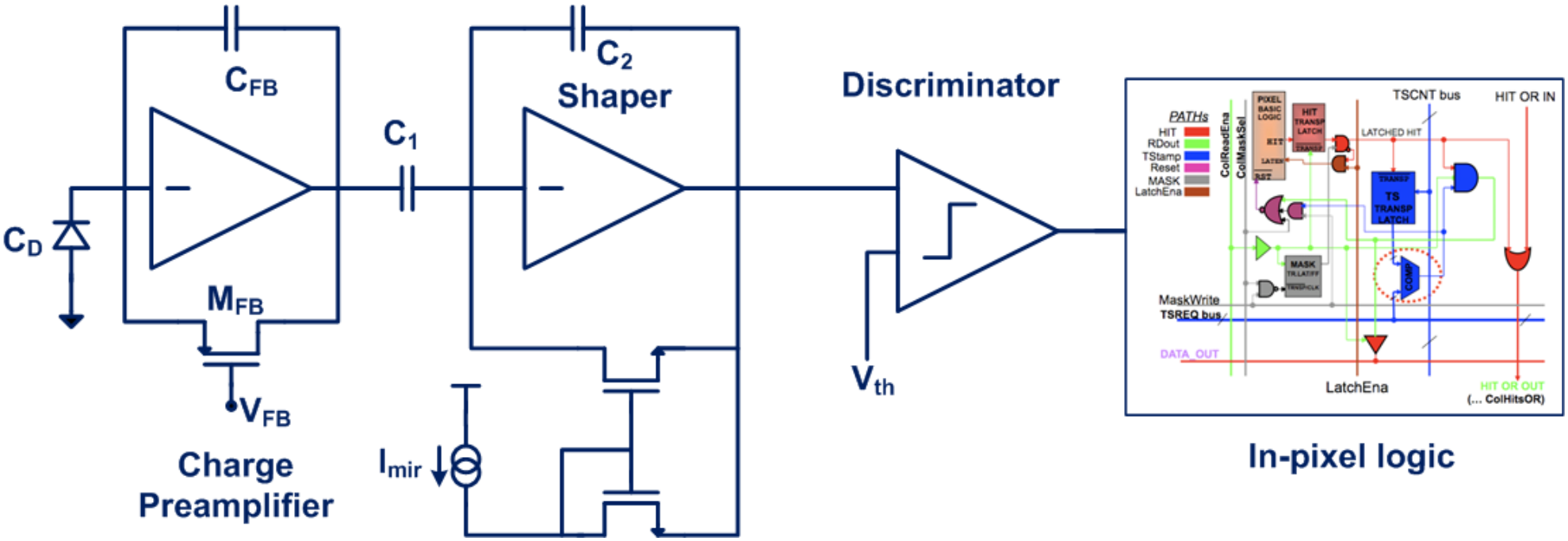


W=8 µm L=1.5 µm D=27 µm

Apsel4well detector



Apsel4well pixel layout



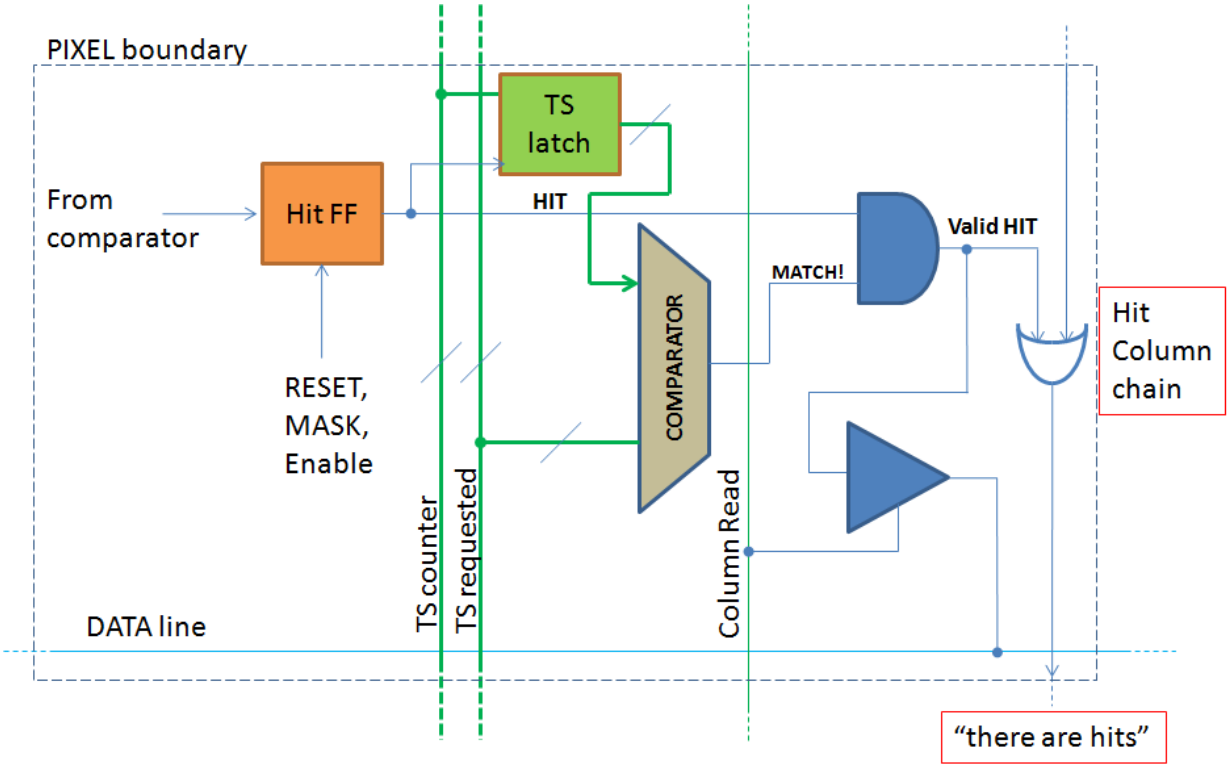
In-pixel logic

- 4 interconnected N-well diffusions as collecting electrode
- Charge PA, shaper and threshold discriminator
- In-pixel logic with time stamping capabilities, readout can be data-push or triggered

In-pixel logic

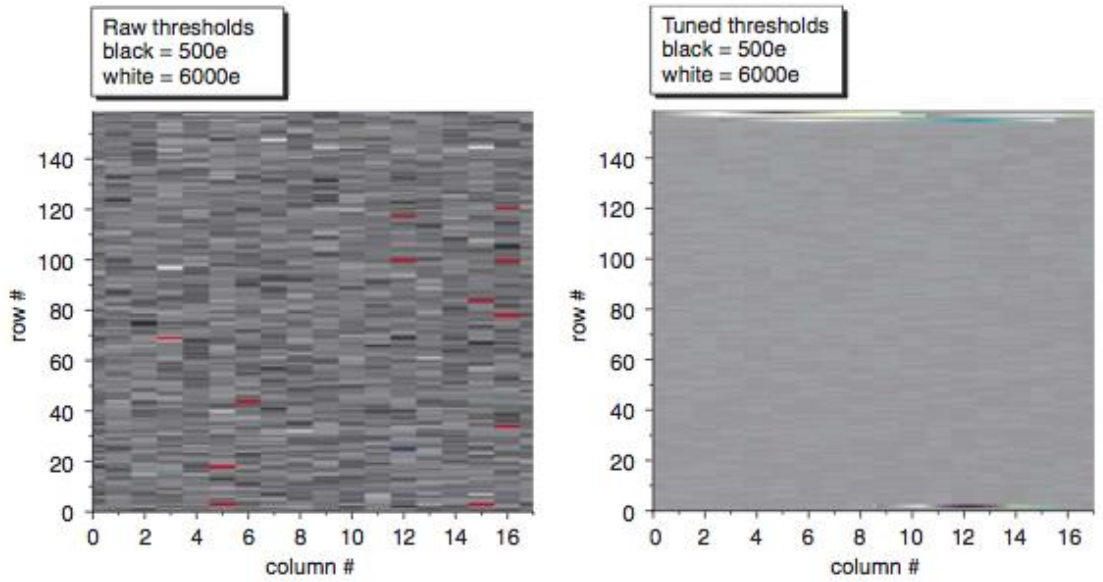
- Complex in-pixel logic can be implemented without reducing the pixel collection efficiency. Readout can be data push or triggered (only selected time stamps are read out)

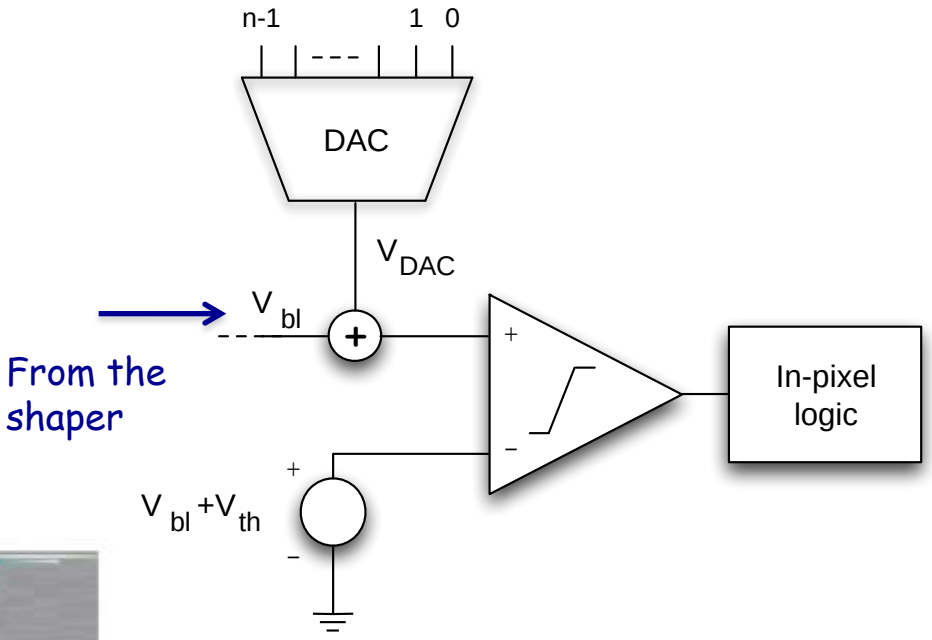
- Timestamp (TS) is broadcast to pixels and each pixel latches the current TS when fires
- Matrix readout is TS ordered
  - A readout TS enters the pixel and a HIT-OR-OUT is generated for columns with hits associated to that TS
  - mA column is read only if HIT-OR-OUT=1
  - DATA_OUT is generated for pixels in the active columns with hits associated to that TS.



Ancillary electronics in readout chips

- Readout chips for semiconductor detectors also include several blocks aiming to optimize chip operation
  - Threshold dispersion is one of the most important parameters affecting detection efficiency in a readout chip; it arises from systematic and random variations in device parameters; as a consequence of threshold dispersion, two binary channels with identical input charge may feature different responses (one fires, the other one does not)





- D/A converters, with the relevant registers (one set for each channel) are used for finely tuning the threshold and reducing the channel dispersion

Ancillary electronics in readout chips

- Readout chips for semiconductor detectors also include several blocks aiming to optimize chip operation
  - The possibility to inject a well known amount of charge at exactly the same input node of the charge preamplifier where the real sensor will be bonded is often required in a readout chip for a twofold purpose:

    1. to make an extensive (involving all the channels) and possibly automatic functional test of the chip;
    2. to enable channel-by-channel gain calibration and threshold dispersion optimization, again possibly through an automatic procedure;

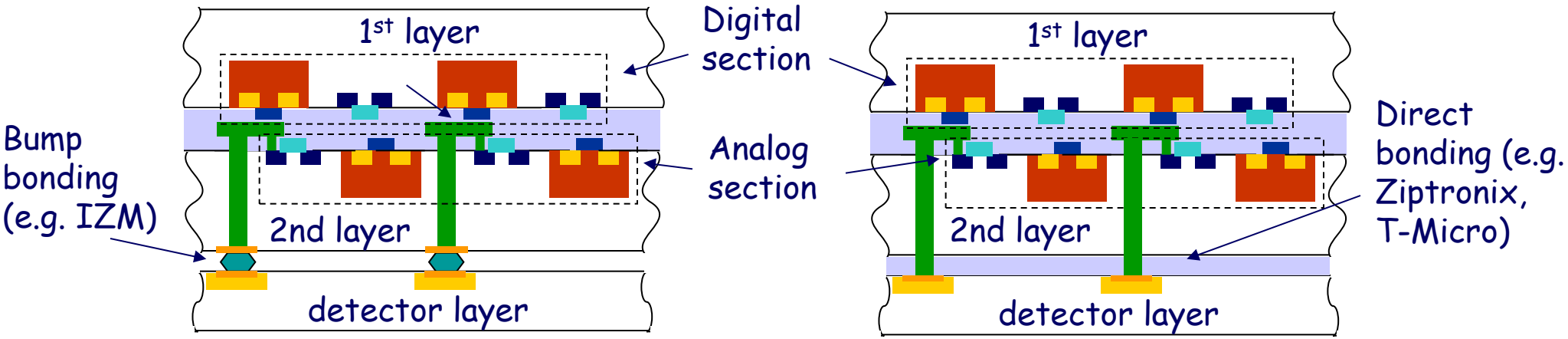
    the test signal amplitude is generally controlled by means of a programmable DAC register

  - In a multichannel circuit, like the ones used for pixel or microstrip readout, some cells may happen to be malfunctioning or exceedingly noisy, therefore appearing as always firing; since such channels do not provide any useful information, they could be switched off or simply disconnected from the readout flow to free some bandwidth; this is generally achieved by loading a kill mask during the chip configuration phase, indicating which channels should be marked as dead

  - Off chip data transmission is generally performed using low voltage differential signaling (LVDS) levels (faster and more robust against common mode noise); therefore, CMOS-to-LVDS and LVDS-to-CMOS conversion circuits are needed for communication from and to the chip

3D hybrid pixels

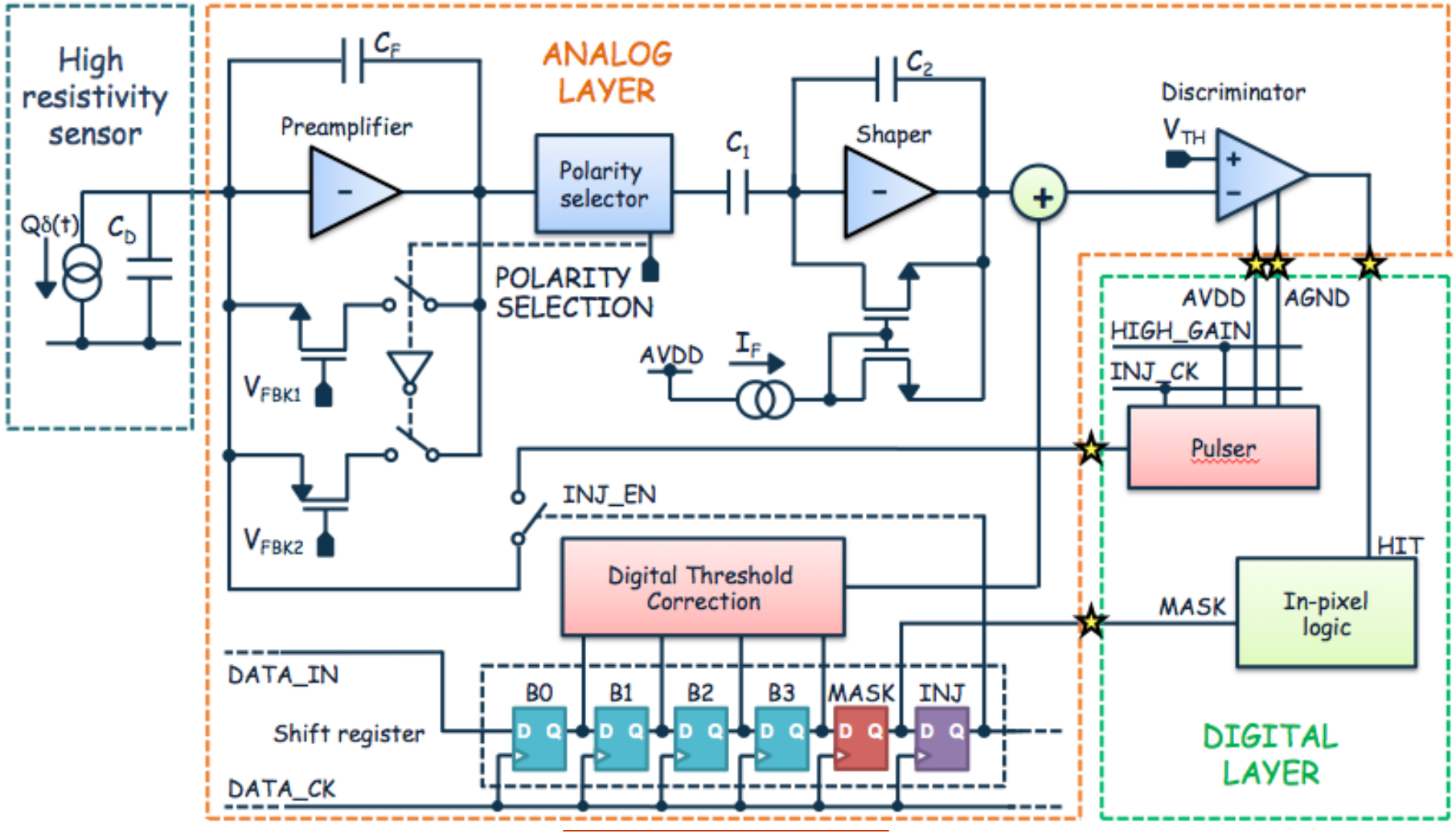
- Development of a 3D front-end chip to be vertically integrated with fully depleted detectors through some more (bump bonding) or less (direct bonding) standard technique



- Connection through direct bonding techniques may provide some advantage:
  - less material in the detector region
  - more mechanical stability for possible post processing steps (e.g., thinning)

Superpix1 front-end chip for hybrid pixel detectors

- 2-tier design (130 nm CMOS process), 50 um pitch



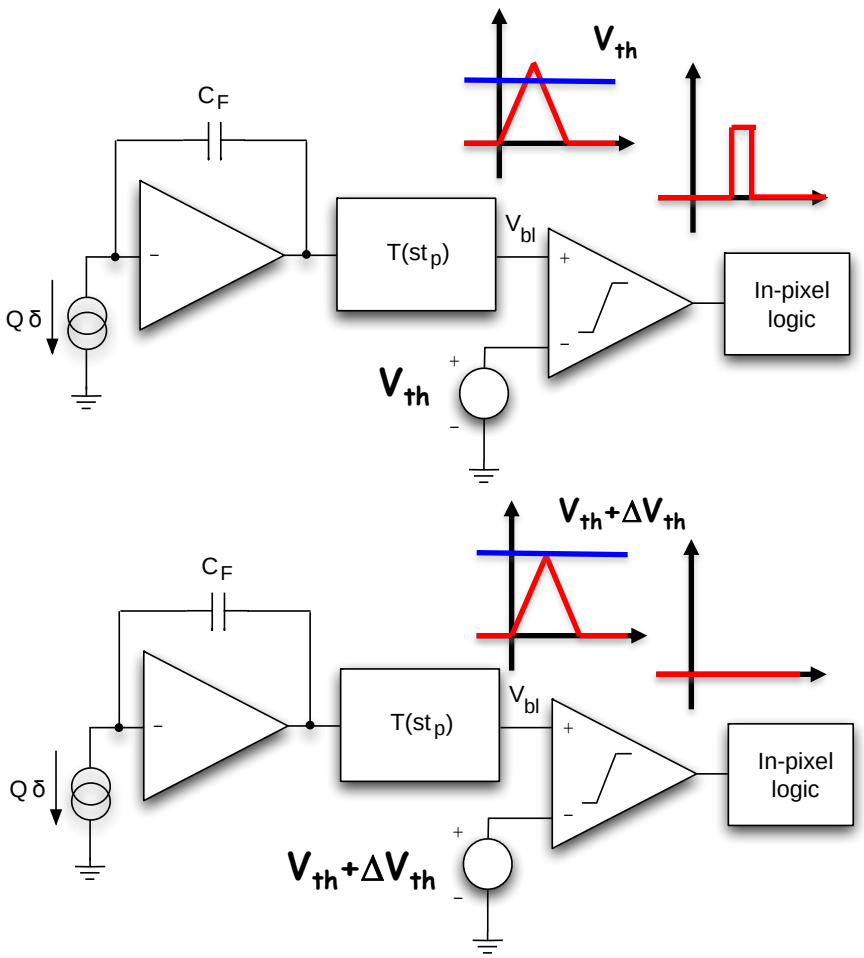
Superpix1 analog front-end features

Main front-end design features	
Preamplifier Input Device [μm/μm]	18/0.25
Analog Power Dissipation [μW/pixel]	13.5
Peaking Time (Q_{inject} =16000 e-) [ns]	250
Charge sensitivity [mV/fC]	48
ENC @C_D = 150 fF [e- rms]	180
Threshold dispersion (before/after correction) [e- rms]	560/65

The threshold dispersion issue

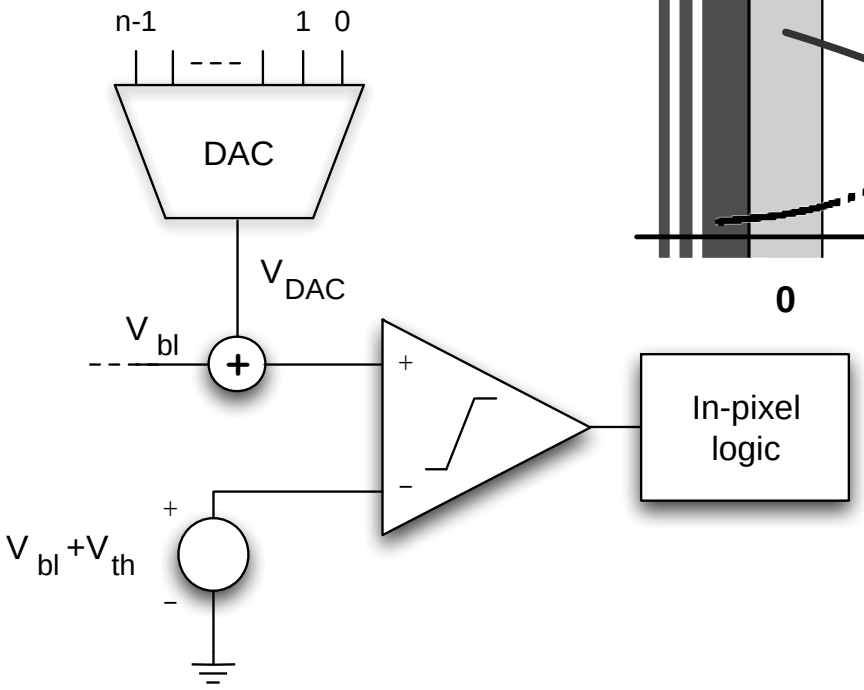
- In a multichannel binary readout circuit, random and systematic variations of process (doping) and geometrical (device dimensions, thickness of the various involved layers) parameters may be responsible for introducing non uniformities in the parallel path followed by the signals

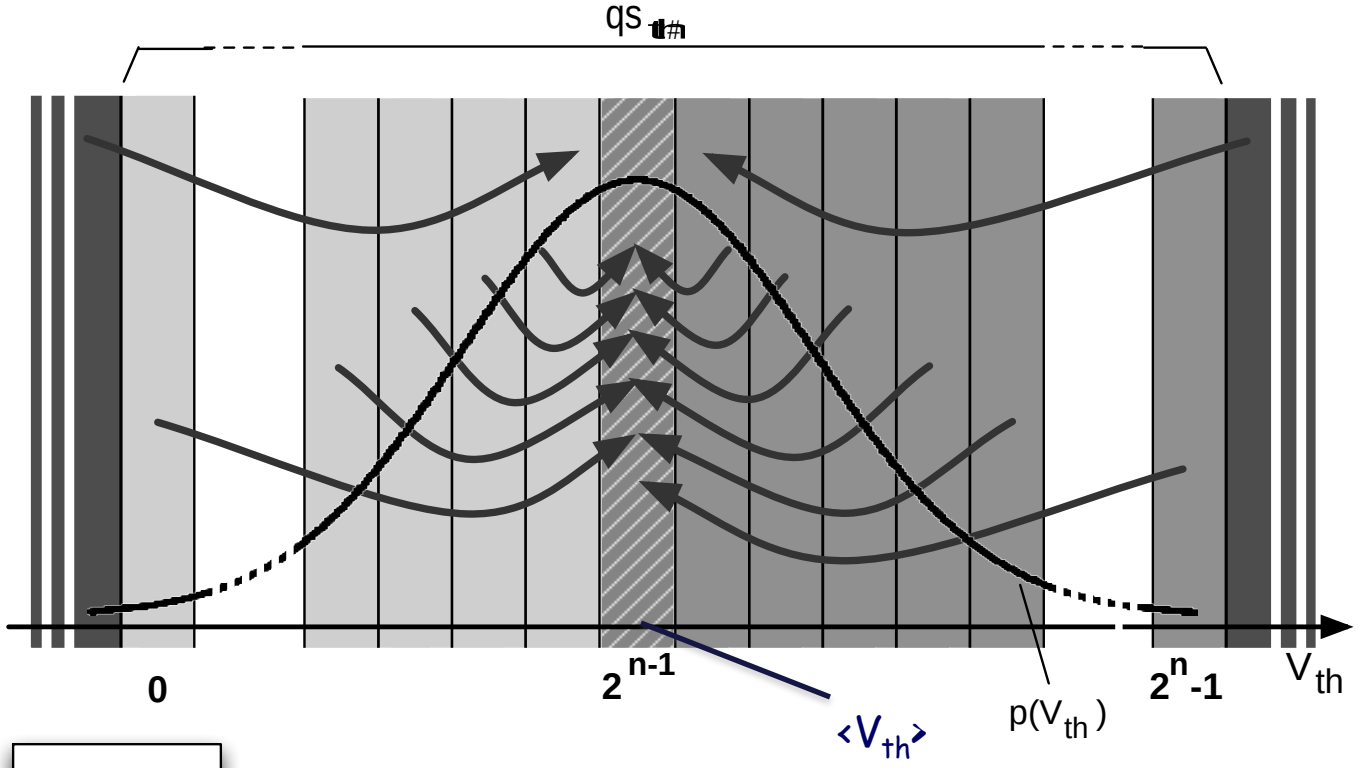
- Two channels, nominally identical to each other and featuring a common threshold at the inverting input of the discriminator, may provide different responses to the same charge pulse at the preamplifier input



Threshold correction analysis

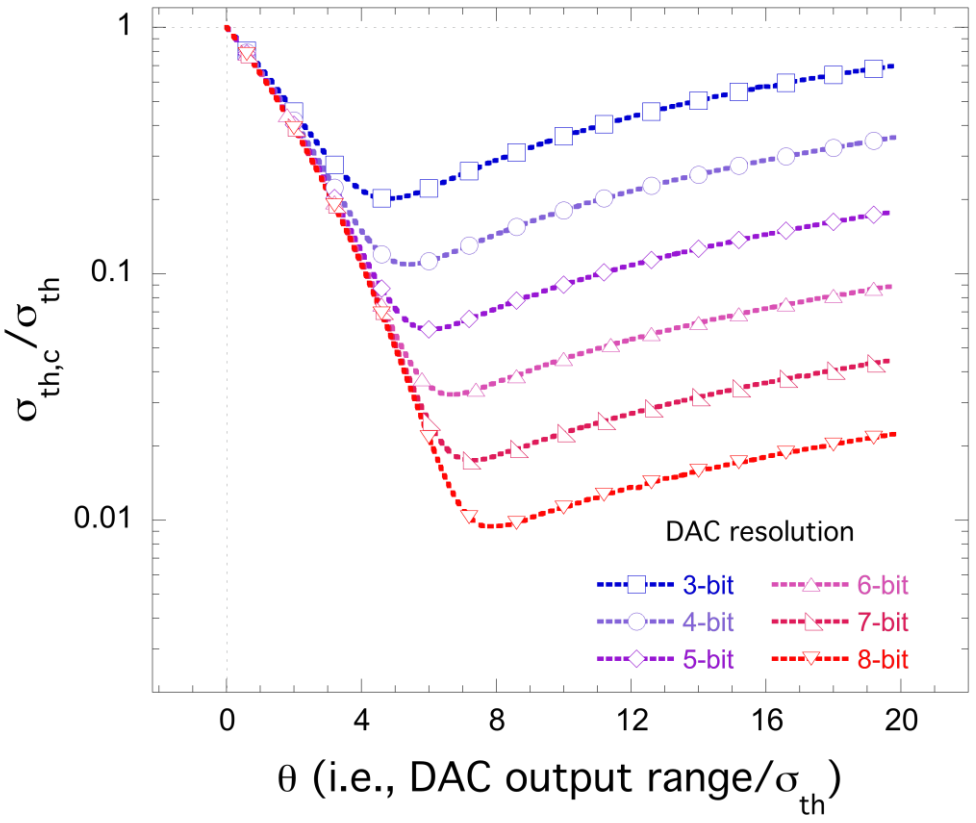
- The output range of the DAC, $\theta\sigma_{th}$ (σ_{th} being the threshold dispersion before correction), is subdivided in 2^n intervals

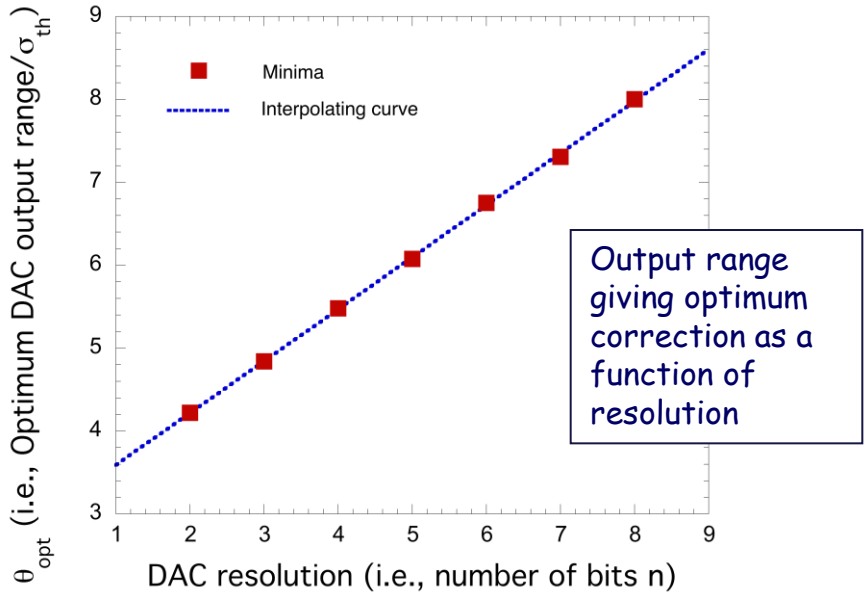




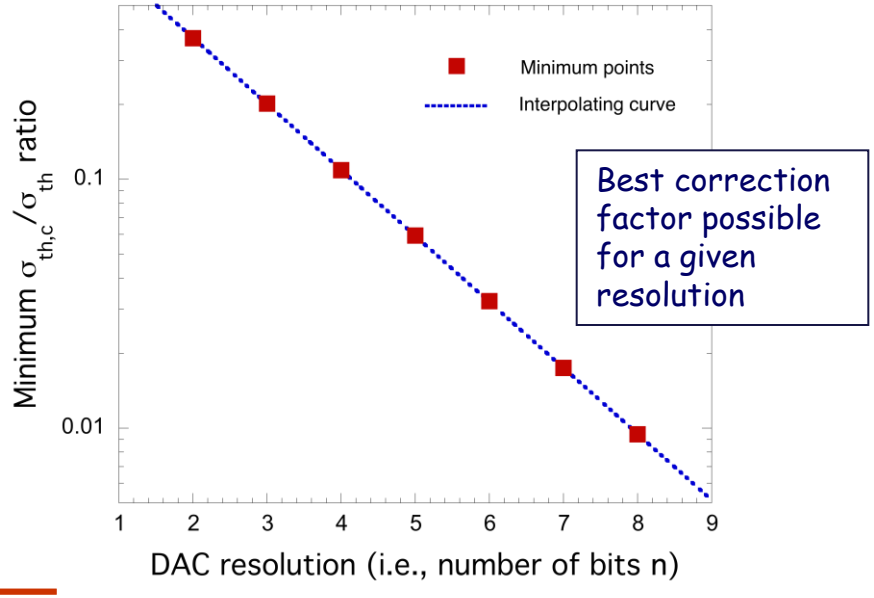
- In each cell, the threshold correction is obtained by programming the DAC so as to shift the actual threshold as close as possible to $\langle V_{th} \rangle$

Optimum DAC configuration for threshold correction





Output range giving optimum correction as a function of resolution



Best correction factor possible for a given resolution

- Given the DAC resolution, there exists a value of the output dynamic range optimizing the operation of the circuit

Threshold correction

Threshold tuning procedure

With threshold scan techniques the threshold voltage is measured for each channel

↓

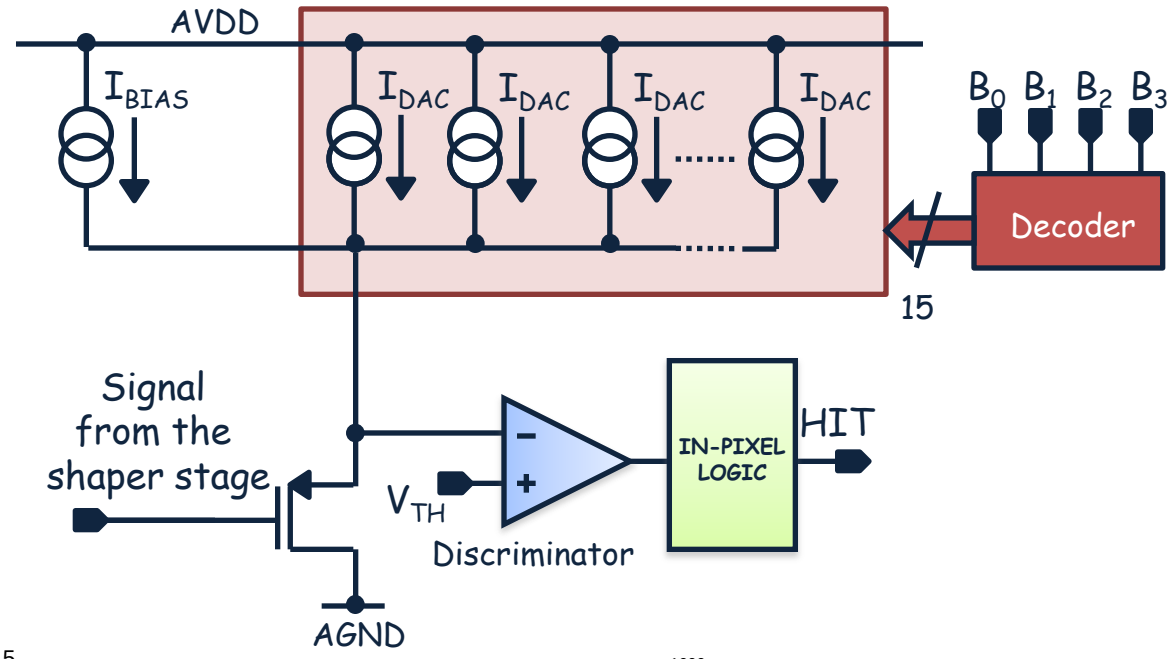
The average threshold voltage value is calculated

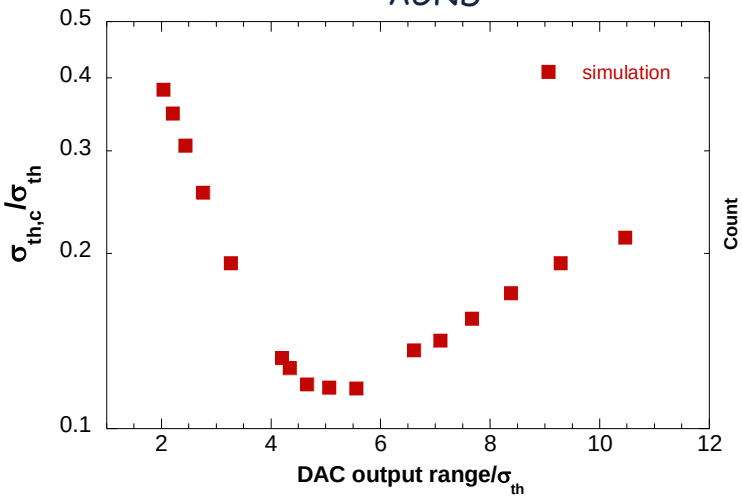
↓

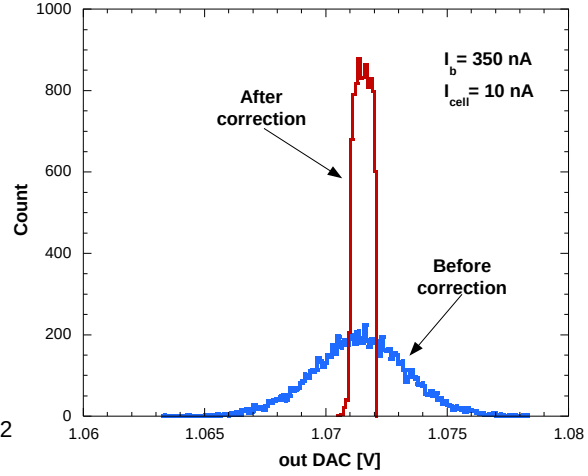
For each channel, the difference between its threshold and the average value defines the bit sequence

↓

The bit correction sequence is loaded during the programming phase

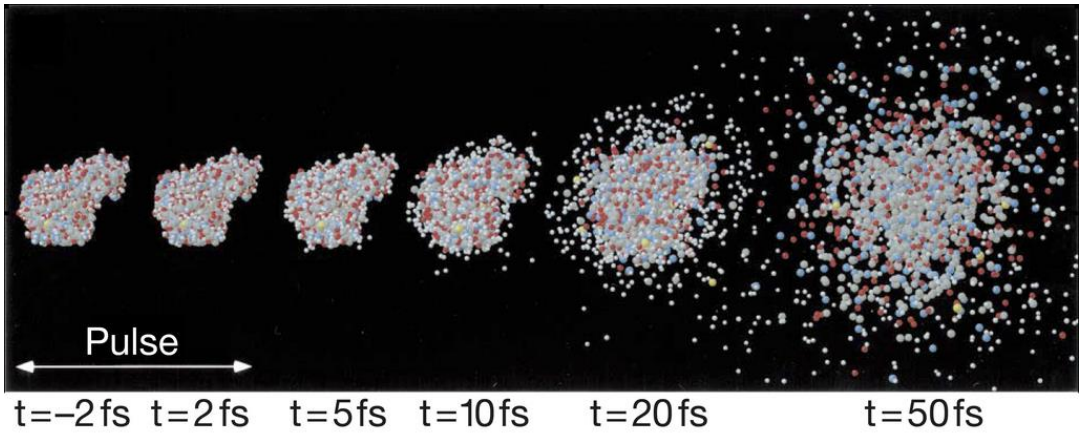






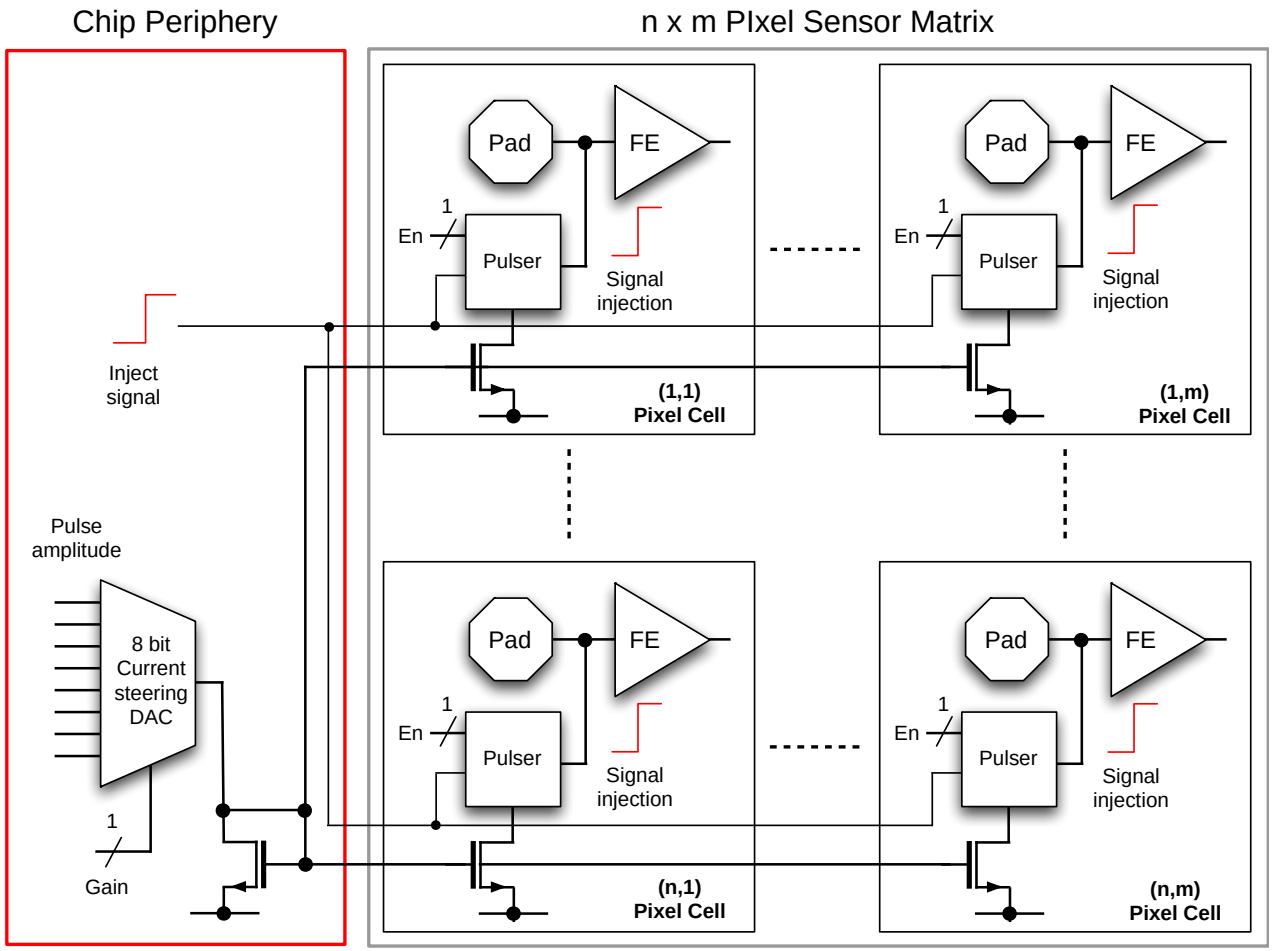
Requirements for applications at FELs

- Free electron lasers are bound to become the predominant tool for the investigation of natural phenomena in several fields: structural biology, chemistry, material science, atomic and molecular science
- FELs emit high intensity beam of ultrafast X-rays
  - energy range: 100 eV to 10 keV (λ from 10 nm to 0.1 nm)
  - pulse duration: tens of femtoseconds to picoseconds
  - repetition rate: 100 Hz (continuous mode) to 5 MHz (burst mode)
- A wide dynamic range is foreseen for the signal emerging from the X-ray interaction with the samples under test – 1 to 10000 photons (➔ 80 dB) and single photon sensitivity ➔ severe requirements for the front-end channel noise and sensitivity properties and for the ADC resolution



Gain calibration circuit

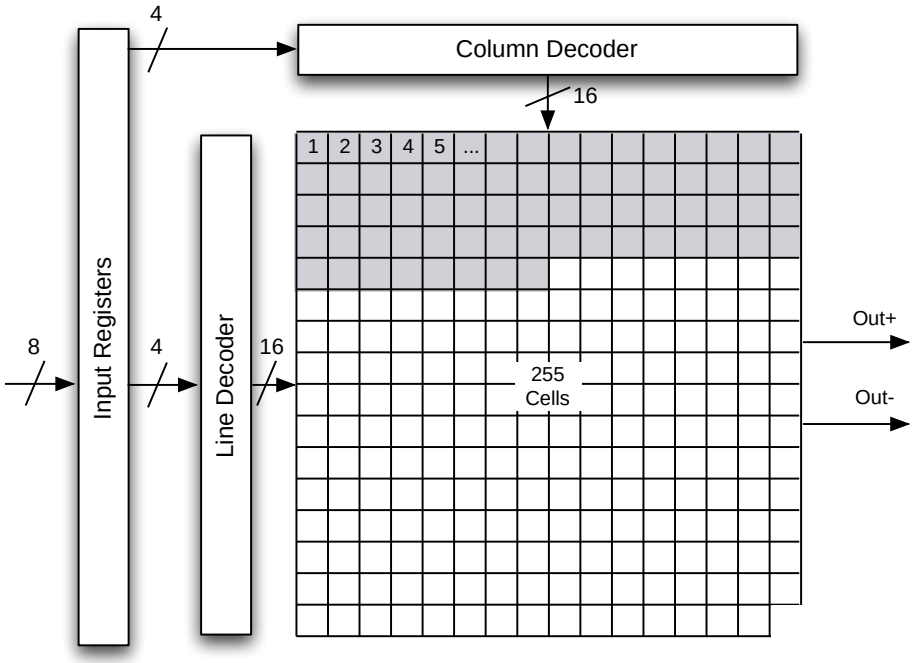
- Developed for the DSSC (DEPFET sensor with signal compression) chip
- Programmable internal pulser for application to a 2D X-ray imager
- 8-bit resolution needed to meet the sensitivity requirements for the front-end channel

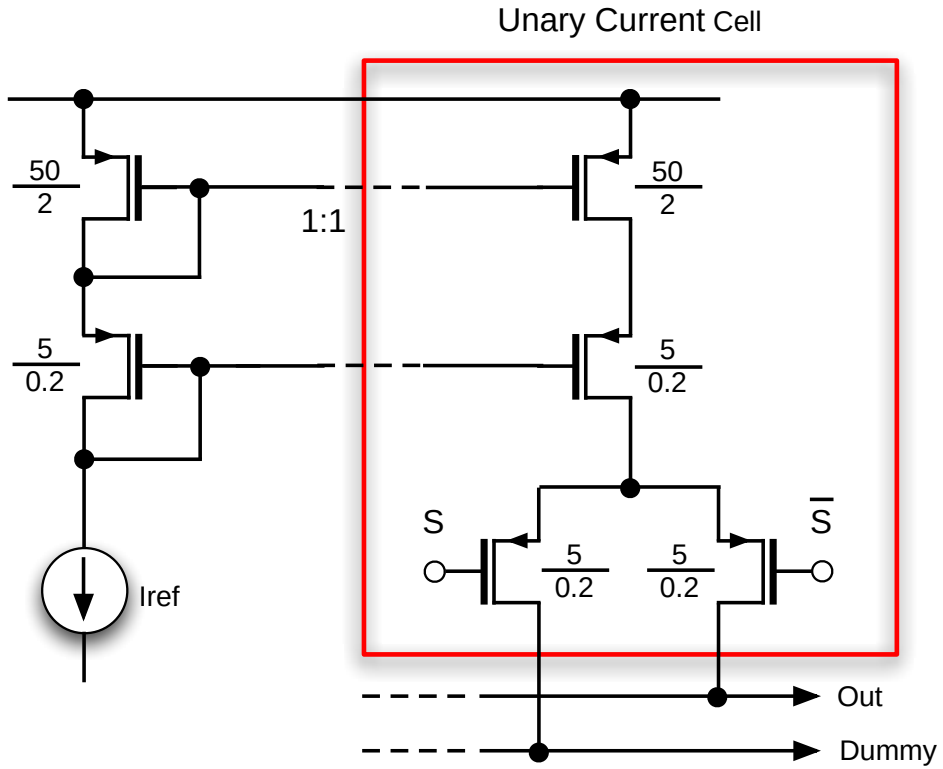


M. Manghisoni et al., "High Accuracy Injection Circuit for Pixel-Level Calibration of Readout Electronics", 2010 IEEE NSS Conference Record

Pulser configuration

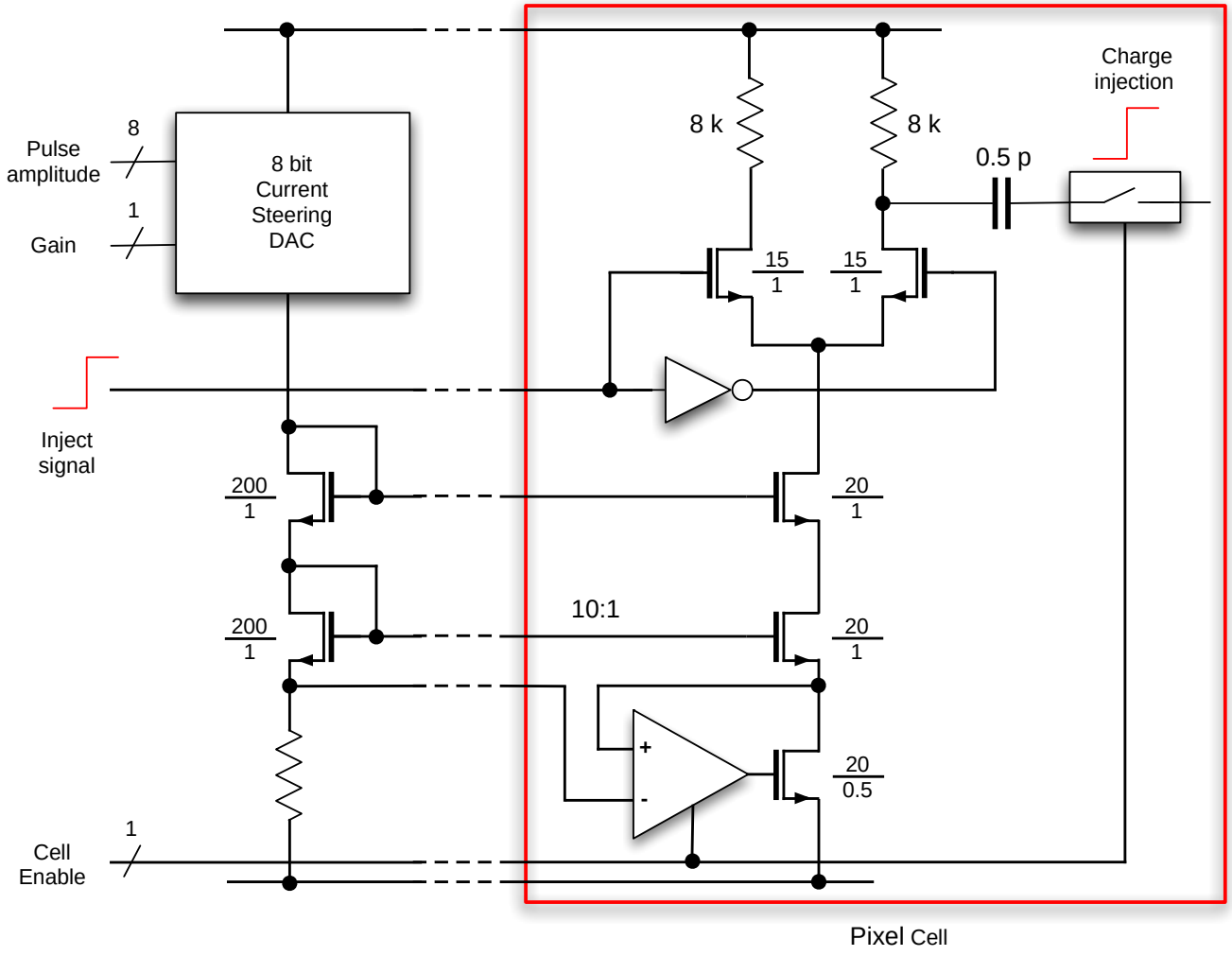
- Unary current source architecture with 255 cells arranged in a two-dimensional array (16x16)
- Thermometric selection of current cells





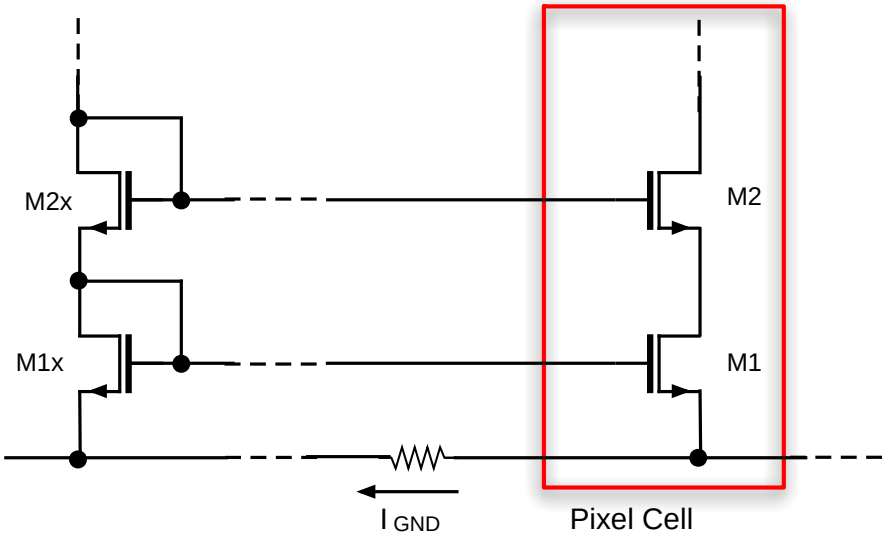
Pulser operation

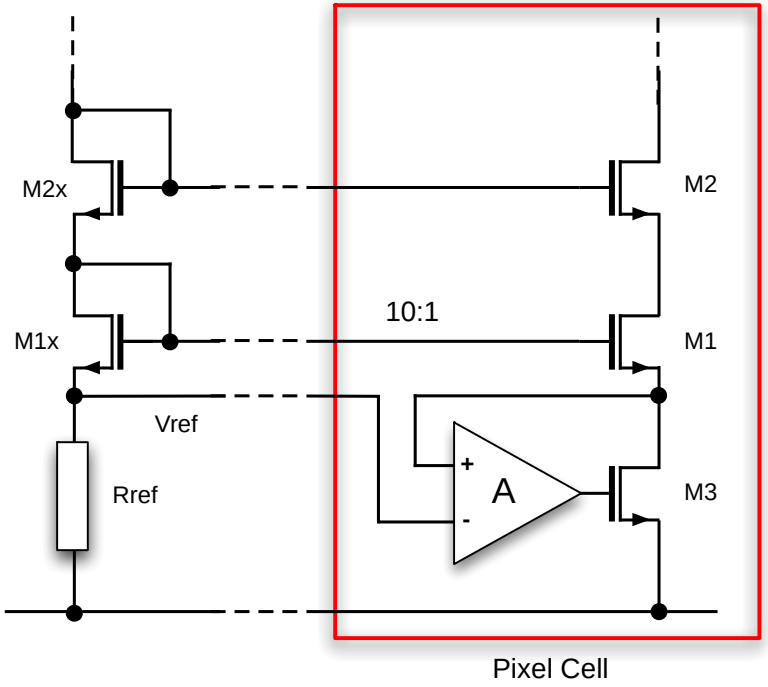
- DAC current is mirrored into each pixel by means of a 10:1 mirror
- Mirrored current is switched from one branch of the differential stage to the other to produce a voltage step at one terminal of the injection capacitance
- Charge injection into each pixel cell is disabled both by opening a switch in series with the injection capacitance and by turning off the mirror current



Voltage drop along power and ground lines

- Resistivity on the power and ground lines may be responsible for an unwanted voltage drop ➔ non-uniformity in the behavior of nominally identical circuits

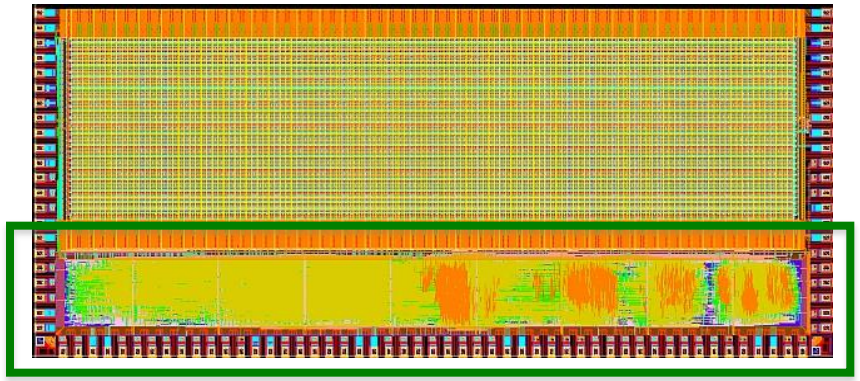




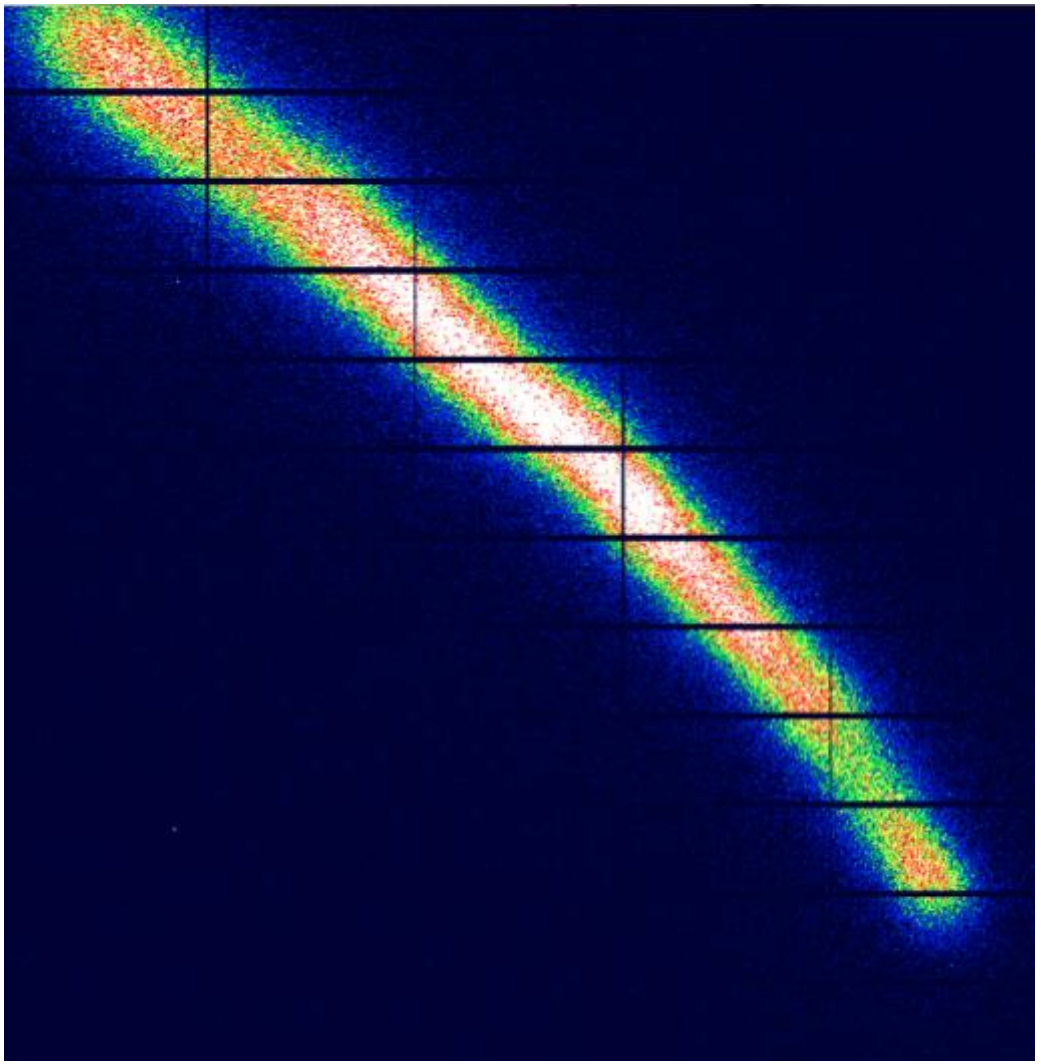
- V_{GS} voltage in M1 is forced to be the same as in M1x by virtue of the large gain A of the amplifier

Dead area issue in radiation detectors

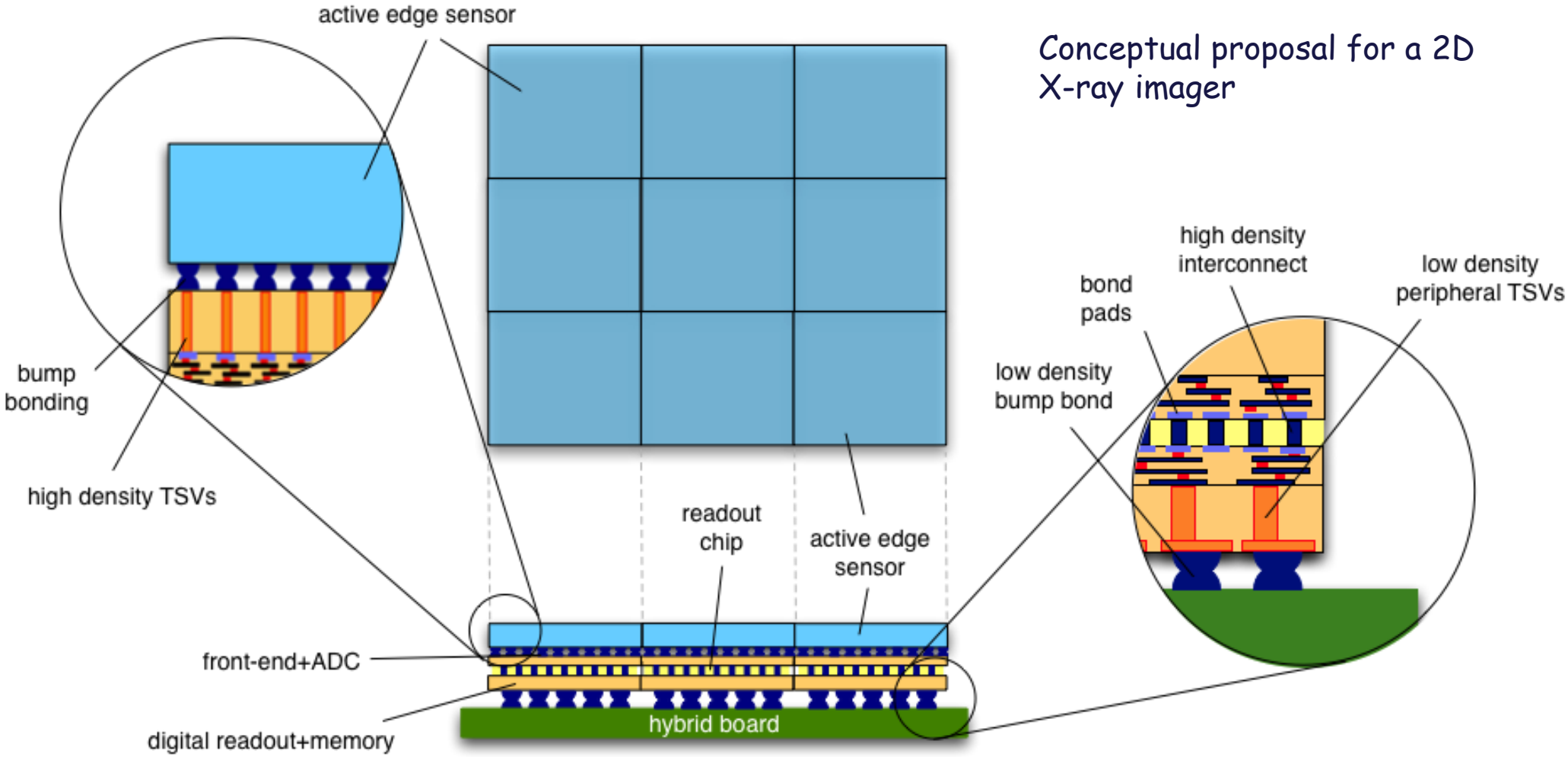
- Modules of limited size
- Gap between modules ➔ missing data



- Dead area generally corresponding to the area taken by the readout circuits at the periphery of the chip
- The sensing layer itself may include some dead area (e.g., guard rings)



Enabling technologies for 4-side buttable modules



Conceptual proposal for a 2D X-ray imager

Conclusion

- Pixel detector requirements for next generation experiments at high luminosity colliders and X-ray sources are extremely challenging
  - high granularity ➔ small room for electronic circuits
  - high hit rate ➔ high speed, on-chip memory
  - data reduction ➔ hit discrimination capability
  - radiation hardness
- More functionalities need to be built into the readout chip to satisfy the specifications
  - front-end performance improvement
  - data selection and hit discrimination (bandwidth reduction)
- Technology evolution (both in the 'more Moore' and the 'more than Moore' sense) makes it possible to follow the trend and, actually, has a role in enhancing it, leaving room for creativity and continuous innovation

Acknowledgment

Most of the developments discussed in this lecture come from the work of my present or former colleagues at University of Bergamo, University of Pavia and INFN, to whom I am grateful:

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I also would like to thank the groups of Marcello Giorgi in Pisa and of Mauro Villa in Bologna, who collaborated in the development of the DNW and quadruple well monolithic sensor chips

Bibliography

- L. Rossi et al., "Pixel detectors. From fundamentals to applications". Springer, Berlin, 2006.
- R. Ballabriga, M. Campbell, E.H.M. Heijne, X. Llopart, L. Tlustos, "The Medipix3 Prototype, a Pixel Readout Chip Working in Single Photon Counting Mode With Improved Spectrometric Performance", *IEEE Trans. Nucl. Sci.*, Vol. 54, No. 5, Oct. 2007, pp. 1824-1829.
- I. Peric, L. Blanquart, G. Comes, P. Denes, K. Einsweiler, P. Fischer et al., "The FEI3 readout chip for the ATLAS pixel detector", *Nucl. Instrum. Methods*, Vol. A565, 2006, pp. 178-187.
- R. Horisberger, "Readout architectures for Pixel detectors", *Nucl. Instrum. Methods*, Vol. A465, 2001, pp. 148-152.
- P. Fischer, "An area efficient 128 channel counter chip", *Nucl. Instrum. Methods*, Vol. A378, 1996, pp. 297-300.
- P. Fischer, "Design considerations for pixel readout chips", *Nucl. Instrum. Methods*, Vol. A501, 2003, pp. 175-182.
- G. Deptuch, J-D Berst, G. Claus, C. Colledani, W. Dulinski, Y. Gornushkin et al., "Design and Testing of Monolithic Active Pixel Sensors for Charged Particle Tracking", *IEEE Trans. Nucl. Sci.*, Vol. 49, No. 2, Apr. 2002, pp. 601-610.
- Y. Degerli, A. Besson, G. Claus, M. Combet, A. Dorokov, W. Dulinski et al., "Development of Binary Readout CMOS Monolithic Sensors for MIP Tracking", *IEEE Trans. Nucl. Sci.*, Vol. 56, No. 1, Feb. 2009, pp. 354-363.
- M.L. Prydderch, N.J. Waltham, R. Turchetta, M.J. French, R. Holt, A. Marshall et al., "A 512 x 512 CMOS Monolithic Active Pixel Sensor with integrated ADCs for space science", *Nucl. Instrum. Methods*, Vol. A512, 2003, pp. 358-367.

Bibliography

- C.D. Arvanitis, S.E. Bohndiek, G. Segneri, C. Venanzi, G. Royle, A. Clark et al., "A Novel Active Pixel Sensor With On-Pixel Analog-to-Digital Converter for Mammography", *2006 IEEE Nuclear Science Symposium Conference Record*, Vol. 6, pp. 3576-3580, 2006.
- L. Rossi et al., "Pixel detectors. From fundamentals to applications". Springer, Berlin, 2006.
- J.J. Velthuis, P.P. Allport, G. Casse, A. Evans, R. Turchetta, G. Villani, "A monolithic active pixel sensor for particle detection in 0.25 μm CMOS technology", *Nucl. Instrum. Methods*, Vol. A560, 2006, pp. 40-43.
- J.P. Crooks, S.E. Bohndiek, C.D. Arvanitis, R. Speller, H. XingLiang, E.G. Villani et al., "A CMOS Image Sensor With In-Pixel ADC, Timestamp and Sparse Readout", IEEE Sensor Journal, Vol. 9, No. 1, Jan. 2009.
- M. Barbero, G. Varner, A. Bozek, T. Browder, F. Fang, M. Hazumi et al., "Development of a B-Factory Monolithic Active Pixel Detector –The Continuous-Acquisition Pixel Prototypes", *IEEE Trans. Nucl. Sci.*, Vol. 52, No. 4, Aug. 2005, pp. 1187-1191.
- G. Traversi, A. Bulgheroni, M. Caccia, M. Jasztrab, M. Manghisoni, E. Pozzati et al., "Design and Performance of a DNW CMOS Active Pixel Sensor for the ILC Vertex Detector", *IEEE Trans. Nucl. Sci.*, vol. 56, no. 5, pp. 3002-3009, Oct. 2009.
- L. Ratti, M. Manghisoni, V. Re, V. Speziali, G. Traversi, S. Bettarini et al., "Monolithic pixel detectors in a 0.13 μm CMOS technology with sensor level continuous time charge amplification and shaping", *Nucl. Instrum. Methods*, vol. A568, 2006, pp. 159-166, 2006.
- G. Lutz, "DEPFET development at the MPI semiconductor laboratory", *Nucl. Instrum. Methods*, vol. A549, 2005, pp. 103-111.
- W. Kucewicz, A. Bulgheroni, M. Caccia, P. Grabiec, J. Marczewski, H. Niemiec, "Development of monolithic active pixel detector in SOI technology", *Nucl. Instrum. Methods*, vol. A541, 2005, pp. 172-177.

Bibliography

- Y. Arai, M. Hazumi, Y. Ikegami, T. Kohriki, O. Tajima, S. Terada, "Monolithic Pixel Detector in a 0.15 μm SOI Technology", *2006 IEEE Nuclear Science Symposium Conference Record*, Vol. 3, pp. 1440-1444, 2006.
- "Handbook of 3D Integration: Technology and Applications of 3D Integrated Circuits". Edited by P. Garrou, C. Bower and P. Ramm. Wiley-VCH, Weinheim, 2008.
- M. Koyanagi, T. Nakamura, Y. Yamada, H. Kikuchi, T. Fukushima, T. Tanaka et al., "Three-Dimensional Integration Technology based on Wafer Bonding With Vertical Buried Interconnection", *IEEE Trans. El. Dev.*, Vol. 53, No. 11, Nov. 2006.
- R. Patti, "Three-Dimensional Integrated Circuits and the Future of System-on-Chip Designs", *Proc. IEEE*, Vol. 94, no. 6, pp. 1214-1224, Jun. 2006.
- A.W. Topol, D.C. La Tulipe, Jr., L. Shi, D.J. Frank, K. Bernstein, S.E. Steen et al., "Three-dimensional Integrated circuits", *IBM J. Res. & Dev.*, Vol. 50, No. 4/5, Jul./Sep. 2006.
- G. Deptuch, M. Demarteau, J. Hoff, R. Lipton, A. Shenai, M. Trimpl et al., "Vertically Integrated Circuits at Fermilab", *2009 IEEE Nuclear Science Symposium Conference Record*, pp. 1907-1915, 2009.
- W. Dulinski, G. Bertolone, R. de Masi, Y. Degerli, A. Dorokhov, F. Morel et al., "Thin, Fully Depleted Monolithic Active Pixel Sensor based on 3D Integration of Heterogeneous CMOS layers", *2009 IEEE Nuclear Science Symposium Conference Record*, pp. 1165-1168, 2009.
- M. Manghisoni, E. Quartieri et al., "High Accuracy Injection Circuit for Pixel-Level Calibration of Readout Electronics", 2010 IEEE Nuclear Science Symposium Conference Record, pp. 1312-1318, Knoxville, USA, October 30 - November 6 2010.
- M. Garcia-Sciveres, "Towards the Next Generation of Pixel Readout Chips", Pixel 2012 Conference, Inawashior, Japan, September 3-7 2012.
- H. Graafsma, "Towards edgeless detector tiles, using 3D-Integration", Heareus Seminar, May 2013.

Vertex detectors in future HEP experiments

- Experiments at the future particle colliders (or upgrade of present colliders) will set severe requirements for the front-end electronics