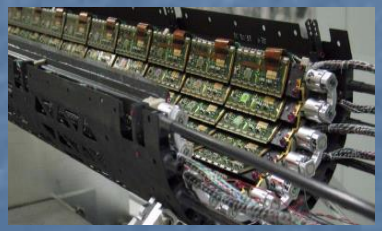
# ATLAS – CMS RD collaboration:

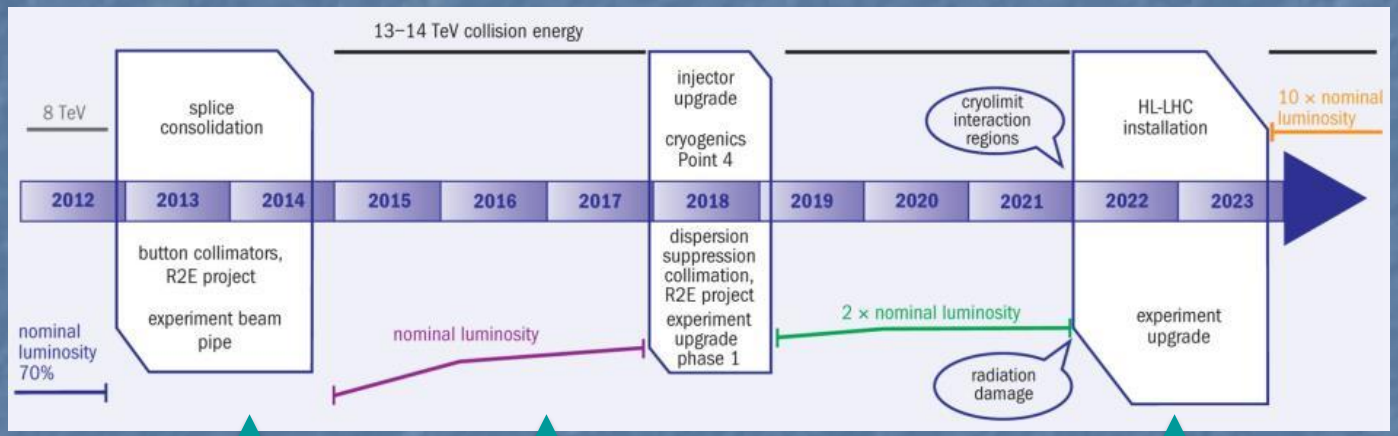
# Pixel readout integrated circuits for extreme rate and radiation

The “pixel 65” collaboration

# Pixel upgrades

- Current LHC pixel detectors have clearly demonstrated the feasibility and power of pixel detectors for tracking in high rate environments
- Phase1 upgrades: Additional pixel layer, ~4 x hit rates
  - ATLAS: Addition of inner B layer with new 130nm pixel ASIC (FEI4)
  - CMS: New pixel detector with modified 250nm pixel ASIC (PSI46DIG)
- **Phase2 upgrades**: ~16 x hit rates, 2-4 x better resolution, 10 x readout rates, 16 x radiation tolerance, Increased forward coverage, less material, , ,
  - Installation: ~ 2022
  - Relies fully on significantly improved performance from next generation pixel chips.






ATLAS Pixel IBL

CMS Pixel phase1

CMS & ATLAS phase 2 pixel upgrades

100MHz/cm$^2$

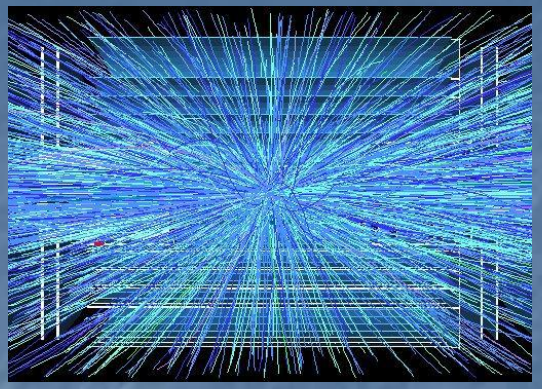
400MHz/cm$^2$

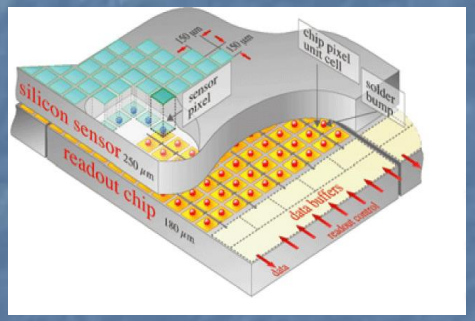
1-2GHz/cm$^2$

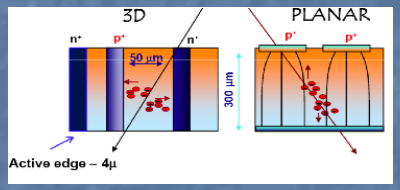
# Phase 2 pixel challenges

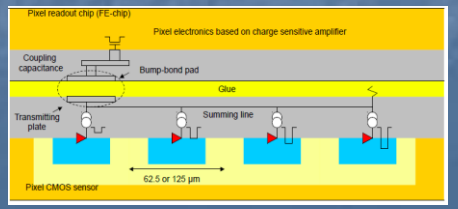
- ATLAS and CMS phase 2 pixel upgrades very challenging
  - Very high particle rates: 500MHz/cm$^2$
    - Hit rates: 1-2 GHz/cm$^2$ (factor 16 higher than current pixel detectors)
  - Smaller pixels: ¼ - ½ (25 – 50 um x 100um)
    - Increased resolution
    - Improved two track separation (jets)
  - Participation in first/second level trigger ?
    A. 40MHz extracted clusters and shape (outer layers) ?
    B. Region of interest readout for second level trigger ?
  - Increased readout rates: 100kHz -> 1MHz
  - Low mass -> Low power

  Very similar requirements (and uncertainties) for ATLAS & CMS
- Unprecedented hostile radiation: 10MGy(1Grad), $10^{16}$ Neu/cm$^2$
  - Hybrid pixel detector with separate readout chip and sensor.
  - Phase2 pixel will get in 1 year what we now get in 10 years
- Pixel sensor(s) not yet determined
  - Planar, 3D, Diamond, HV CMOS, , ,
  - Possibility of using different sensors in different layers
  - Final sensor decision may come relatively late.
- Very complex, high rate and radiation hard pixel readout chips required






ATLAS HVCMOS program

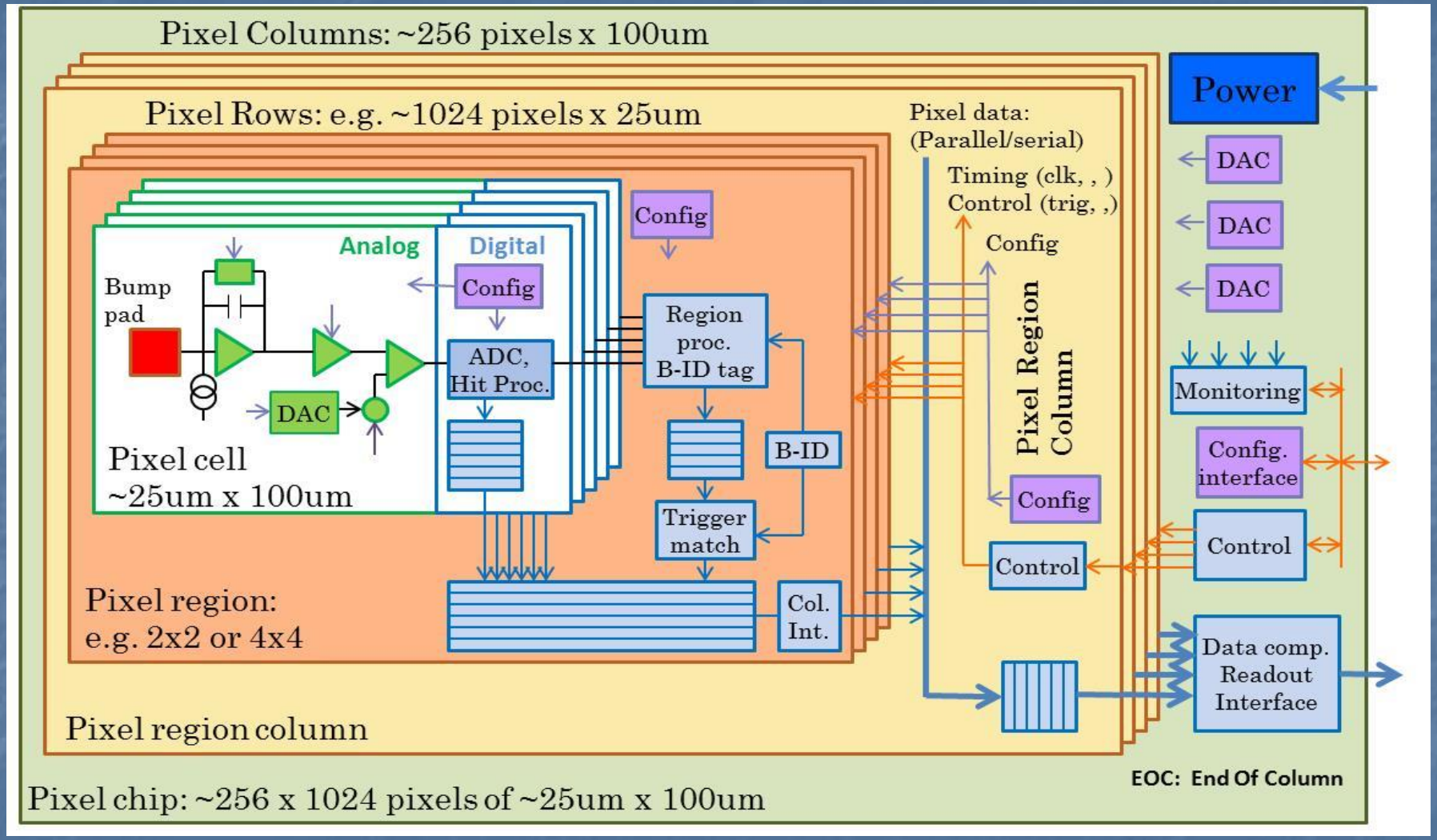
# Pixel chip

- Pixel readout chips critical for schedule to be ready for phase 2 upgrades
  - Technology: Radiation qualification
  - Building blocks: Design, prototyping and test
  - Architecture definition/optimization/verification
  - Chip prototyping, iterations, test, qualification and production
  - System integration
    - System integration tests and test-beams
  - Production and final system integration, test and commissioning
- Phase 2 pixel chip very challenging
  - Radiation
  - Reliability: Several storage nodes will have SEUs every second per chip.
  - High rates
  - Mixed signal with very tight integration of analog and digital
  - Complex: ~256k channel DAQ system on a single chip
  - Large chip: ~2cm x 2cm, ½ - 1 Billion transistors.
  - Very low power: Low power design and on-chip power conversion
- Both experiments have evolved to have similar pixel chip architectures and plans to use same technology for its implementation.
- Experienced chip designers for complex ICs in modern technologies that most work in a extremely harsh radiation environment is a scarce and distributed "resource" in HEP.

# Pixel chip generations

| Generation | Current<br>FEI3, PSI46 | Phase 1<br>FEI4, PSI46DIG | Phase 2 |
|---|---|---|---|
| Pixel size | 100x150um$^2$ (CMS)<br>50x400um$^2$ (ATLAS) | 100x150um$^2$ (CMS)<br>50x250um$^2$ (ATLAS) | 25x100um$^2$ ? |
| Sensor | 2D, ~300um | 2D+3D (ATLAS)<br>2D (CMS) | 2D, 3D, Diamond, MAPS ? |
| Chip size | 7.5x10.5mm$^2$ (ATLAS)<br>8x10mm$^2$ (CMS) | 20x20mm$^2$ (ATLAS)<br>8x10mm$^2$ (CMS) | **> 20 x 20mm$^2$** |
| Transistors | 1.3M (CMS)<br>3.5M (ATLAS) | 87M (ATLAS) | **~1G** |
| Hit rate | **100MHz/cm$^2$** | **400MHz/cm$^2$** | **1-2 GHz/cm$^2$** |
| Hit memory per chip | 0.1Mb | 1Mb | ~16Mb |
| Trigger rate | 100kHz | 100KHz | 200kHz - **1MHz** |
| Trigger latency | 2.5us (ATLAS)<br>3.2us (CMS) | 2.5us (ATLAS)<br>3.2us (CMS) | 6 - **20us** |
| Readout rate | 40Mb/s | 320Mb/s | **1-3Gb/s** |
| Radiation | 1MGy (100Mrad) | 3.5MGy (350Mrad) | **10MGy (1Grad)** |
| Technology | 250nm | 130nm (ATLAS)<br>250 nm (CMS) | **65nm** |
| Architecture | Digital (ATLAS)<br>Analog (CMS) | Digital (ATLAS)<br>Analog (CMS) | Digital |
| Buffer location | EOC | Pixel (ATLAS)<br>EOC (CMS) | Pixel |
| Power | ~1/4 W/cm$^2$ | ~1/4 W/cm$^2$ | **~1/4 W/cm$^2$** |

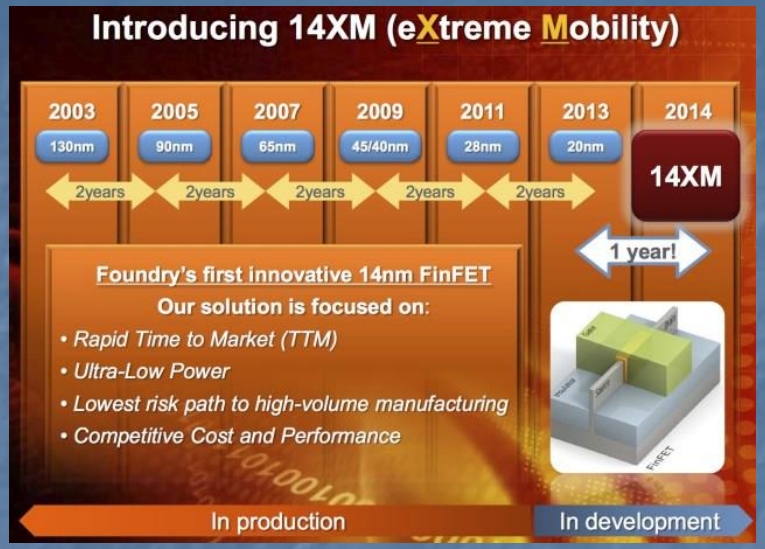
# 3rd generation pixel architecture

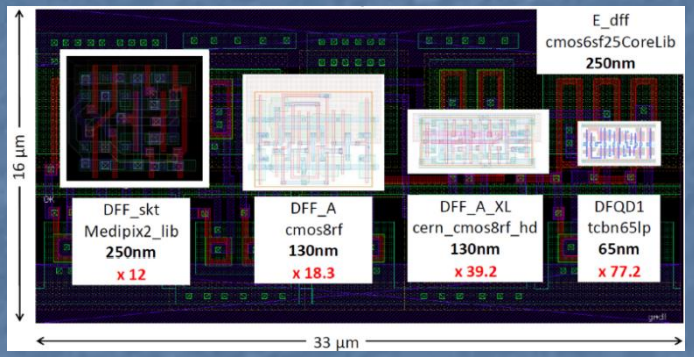



- 95% digital (as FEI4)
- Charge digitization
- ~256k pixel channels per chip
- Pixel regions with buffering
- Data compression in End Of Column

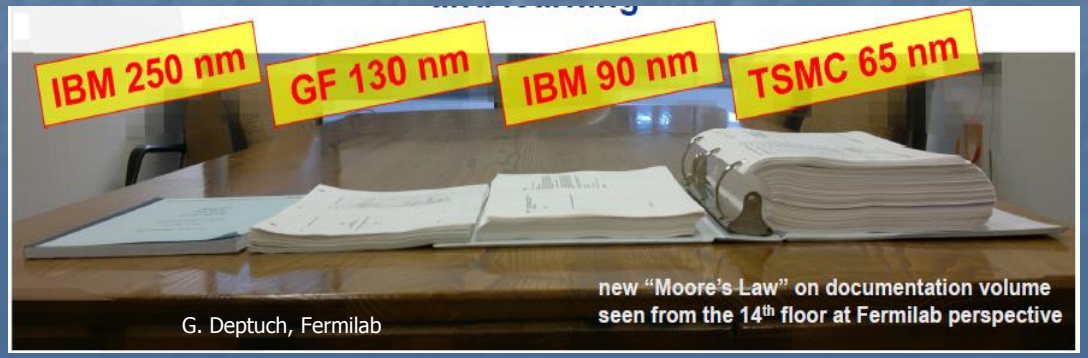
# Why 65nm Technology

- Mature technology:
  - Available since ~2007
- High density and low power
- Long term availability
  - Strong technology node used extensively for industrial/automotive
- Access
  - CERN frame-contract with TSMC and IMEC
    - Design tool set
    - Shared MPW runs
    - Libraries
    - Design exchange within HEP community
- Affordable (MPW from foundry and Europractice, ~1M NRE for full final chips)
- Significantly increased density, speed, , , and complexity !



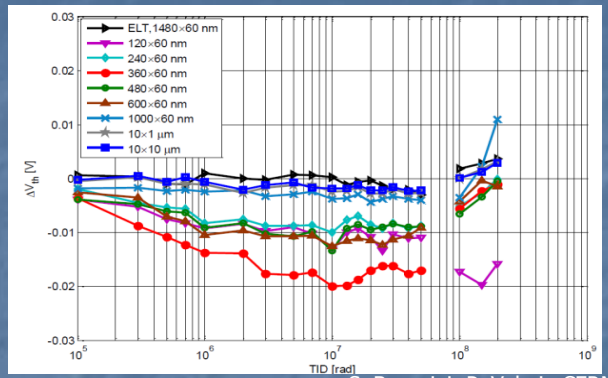

X. Llopart CERN



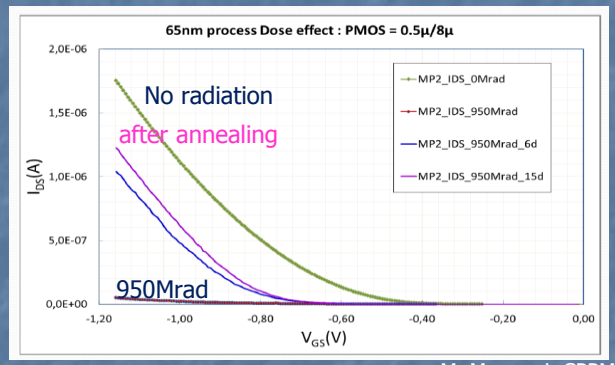

G. Deptuch, Fermilab

# 65nm Technology

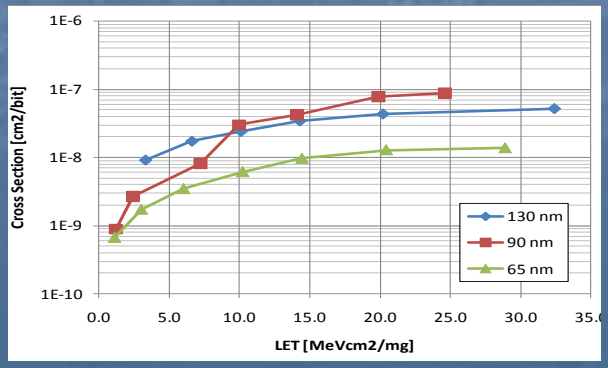
- Radiation hardness
  - Uses thin gate oxide
    - Radiation induced trapped charges removed by tunneling
    - More modern technologies use thick High K gate "oxide" with reduced tunneling/leakage.
  - Verified for up to 200Mrad
  - To be confirmed for 1Grad
    - PMOS transistor drive degradation, Annealing ?
    - If significant degradation then other technologies must be evaluated and/or a replacement strategy must be used for inner pixel layers
  - CMOS normally not affect by NIEL
    - To be confirmed for $10^{16}$ Neu/cm$^2$
    - Certain circuits using "parasitic" bipolars to be redesigned ?
  - SEU tolerance to be build in (as in 130 and 250nm)
    - SEU cross-section reduced with size of storage element, but we will put a lot more per chip
  - All circuits must be designed for radiation environment ( e.g. Modified RAM)




S. Bonacini, P. Valerio CERN




M. Menouni, CPPM



# ATLAS – CMS RD collaboration

- Similar requirements, same technology choice and limited availability of rad hard IC design experts in HEP makes this ideal for a close CMS – ATLAS RD collaboration
  - Even if we do not make a common pixel chip
- Initial 2day workshop between communities confirmed this.
  - Workshop: http://indico.cern.ch/conferenceDisplay.py?confId=208595
- Forming a RD collaboration has attracted additional groups and collaborators
  - Synergy with CLIC pixel (and others): Technology, Rad tol, Tools, etc.
- Institutes: 17
  - ATLAS: Bonn, CERN, CPPM, LBNL, LPNHE Paris, NIKHEF, New Mexico, RAL, UC Santa Cruz.
  - CMS: Bari, Bergamo-Pavia, CERN, Fermilab, Padova, Perugia, Pisa, PSI, RAL, Torino.
- Collaborators: 99, ~50% chip designers
- Collaboration organized by Institute Board (IB) with technical work done in specialized Working Groups (WG)
- Initial work program covers ~3 years to make foundation for final pixel chips
  - Will be extended if appropriate:
    A. Common design ?,
    B. Support to experiment specific designs

# Working groups

| WG | Domain |
|---|---|
| WG1 | Radiation test/qualification |
| Qualification of technology to 10 MGy TID, $10^{16}$ n.eq./cm$^2$. Transistor simulation models after irradiation. Evaluation of logic cell libraries after irradiation. Expertise on radiation effects in 65nm | |
| WG2 | Top level design |
| Design methodology, verification and test of ~5 × $10^8$ transistor IC. Analog integration in large digital chip. Power distribution Synthesis constraints. Clock distribution and optimization | |
| WG3 | Simulation and verification test bench |
| System Verilog simulation and Verification framework. Optimization of global architecture/pixel regions/pixel External system and external physics data. Verification of test chips and evolving designs | |
| WG4 | I/O |
| Definition of readout and control interfaces (e.g. LPGBT). Definition of standardized I/O protocols and performance Implementation of readout and control interface blocks. Standardized interfaces: Control, Readout, etc. | |
| WG5 | Analog design |
| Evaluate and compare alternate amplifier designs. Evaluate and compare charge ADC techniques vs. number of bits (TOT, shared ADC, etc.) | |
| WG6 | IP blocks |
| Define common requirements for IP block design. Evaluate, document, and keep library of IP blocks Generate overview and recommendations. Each block will have its own prototyping milestones | |

# Participation matrix

| Institute | WG1 Radiation | WG2 Top level | WG3 Sim./Ver | WG4 I/O | WG5 Analog | WG6 IPs |
|---|---|---|---|---|---|---|
| Bari | C | | A | | | A |
| Bergamo-Pavia | A | | | C | A | B |
| Bonn | C | A | A | B | B | A |
| CERN | B(*) | (*) | A | C(*) | A | B(*) |
| CPPM | A | B | C | C | B | A |
| Fermilab | A | B | | | A | |
| LBNL | B | A | B | B | A | A |
| LPNHE Paris | A | B | A | | | A |
| NIKHEF | | A | A | | | A |
| New Mexico | A | | | | | |
| Padova | A | | | | A | |
| Perugia | B | | A | | | B |
| Pisa | | B | A | A | | A |
| PSI | B | A | | C | A | A |
| RAL | | B | B | | A | C |
| Torino | C | B | C | B | A | A |
| UCSC | C | B | C | | | A |

A: Core competency, B: High interest, C: Ability to help

(*): General CERN support for 65nm

# Summary

- Highly focused ATLAS - CMS RD collaboration to develop/qualify technology, tools, architecture and building blocks required to develop phase 2 pixel readout chips
- Synergy with other pixel projects: CLIC, ?
- Centered on well defined working groups
- Baseline technology: 65nm
- 17 Institutes, 100 Collaborators
- Initial work program of 3 years