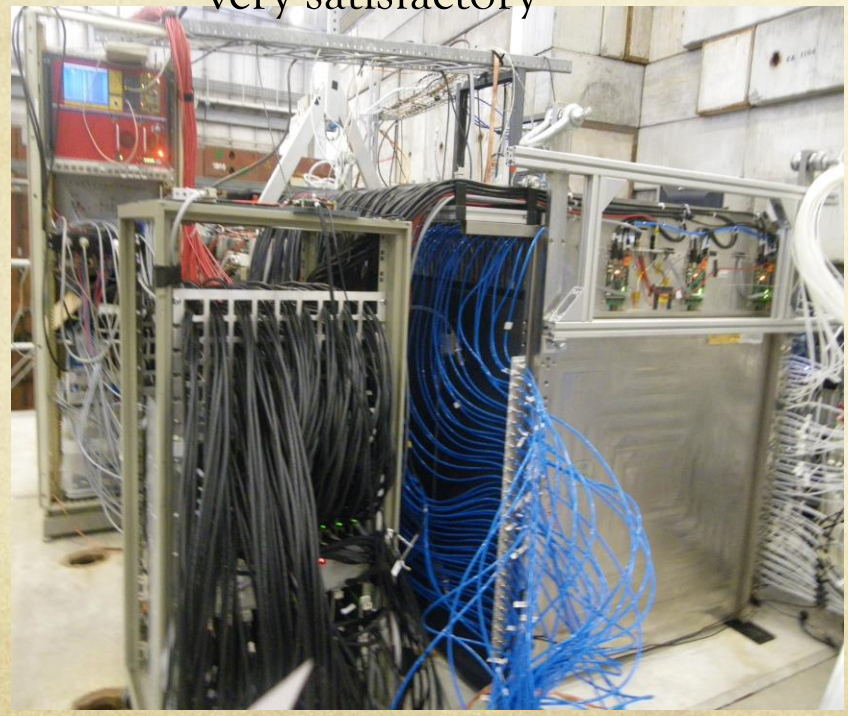
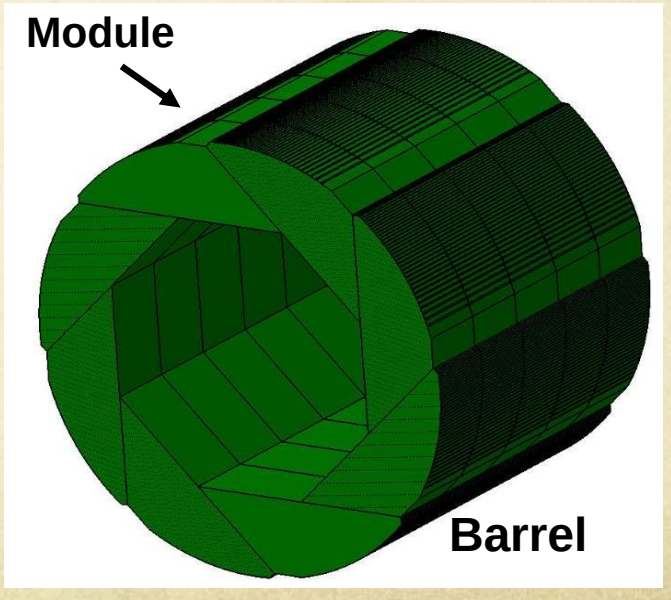
SDHCAL Status

- $1m^3$ prototype with 48 GRPC layers realised as technological demonstrator:
  - electronics integrated in active layers
  - power-pulsed
  - data analysis ongoing, first results very satisfactory



- needed to demonstrate scalability to full ILD layout:
  - large GRPC detectors
  - mechanical structure for Videau geometry
  - optimised PFA



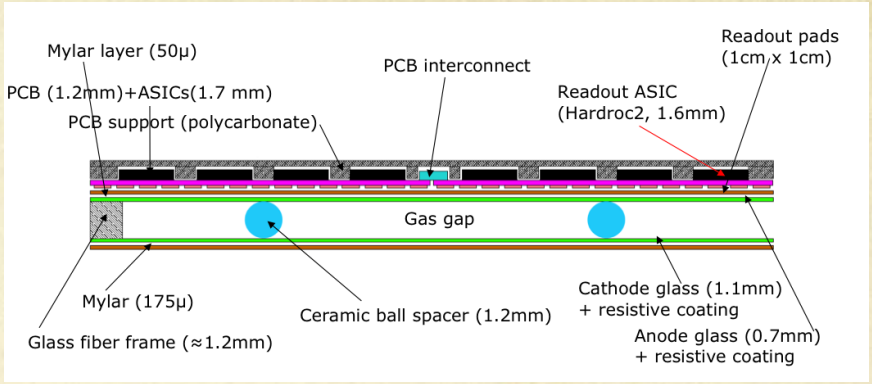
SDHCAL: Current Layer Layout and Plans

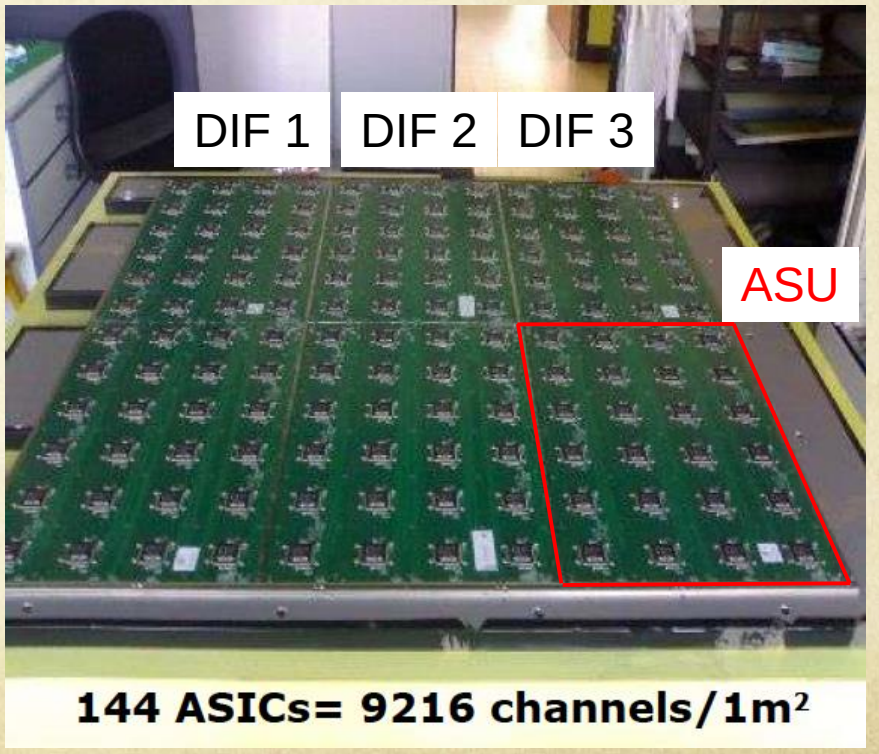
- have demonstrated layers withintegrated electronics of 1 m^2
- next steps:
  - build few very large GRPC

detectors (2-3 m^2): gas circulation system, thickness…

  - improve on the readout electronics (3rd generation ASICs)
  - design a new ASU capable to read the large GRPC
  - develop a new DIF (low power consumption, reduced size, new functionalities)
  - build a small mechanical prototype

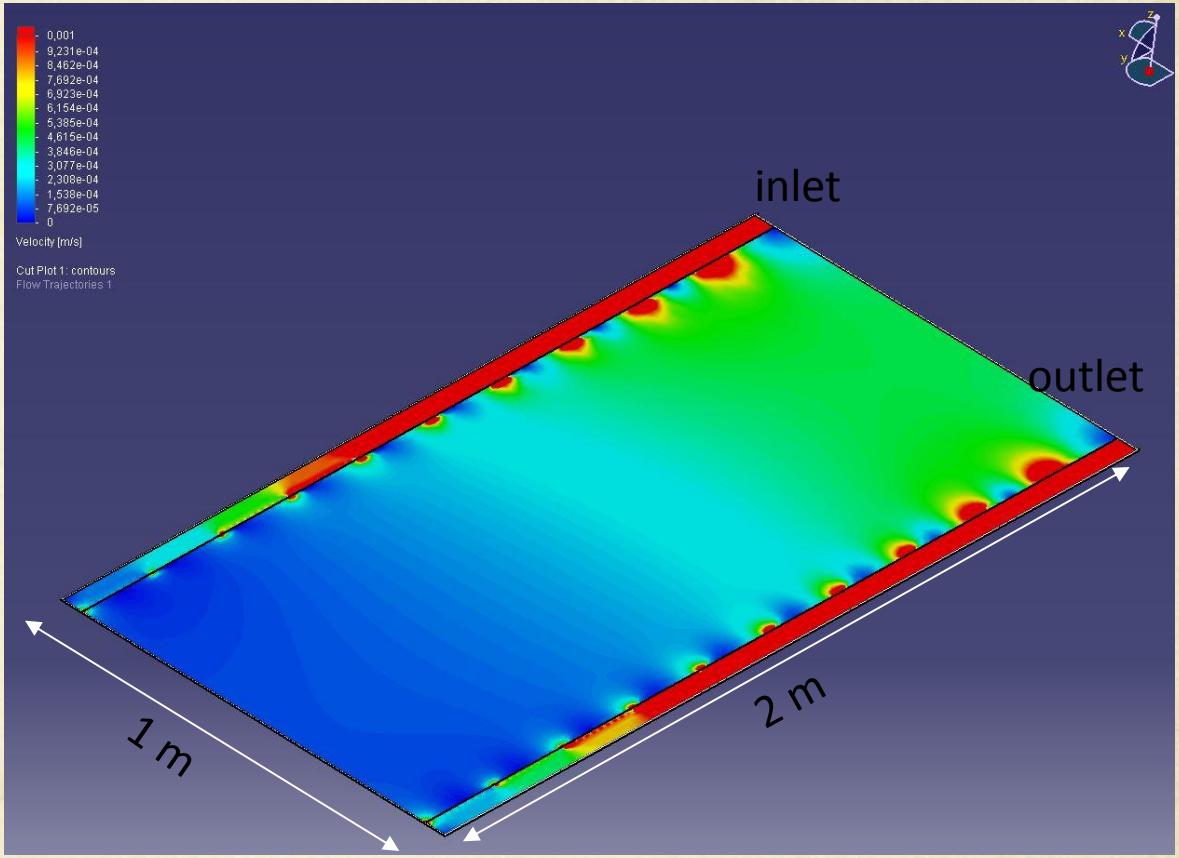
to host the few large chambers



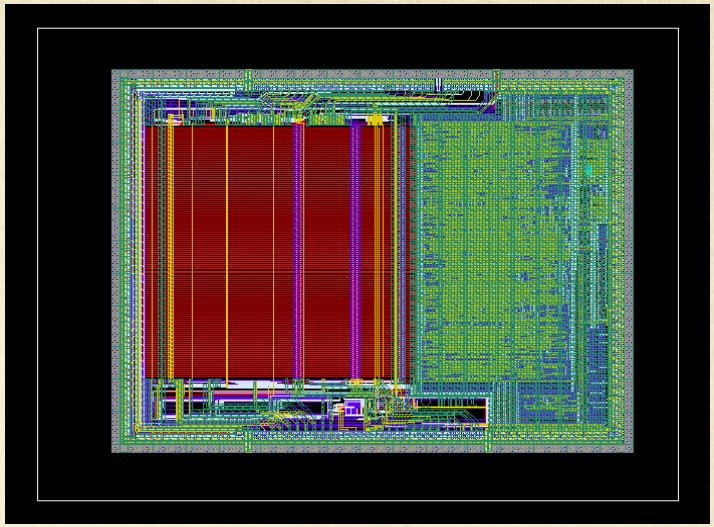


SDHCAL: Large GRPC for ILD

- for ILD, GRPC with a surface of up to 3 m^2 are needed
- intend to build a 2 m^2 GRPC (glass are already there)
- currently studying the gas distribution system to ensure a good gas renewal
  - scaling from 1 m^2 to larger surface needs more study to ensure fast gas renewal



SDHCAL Readout Electronics: 3rd Gen. ASIC HARDROC3



2nd generation ROC ASICs:

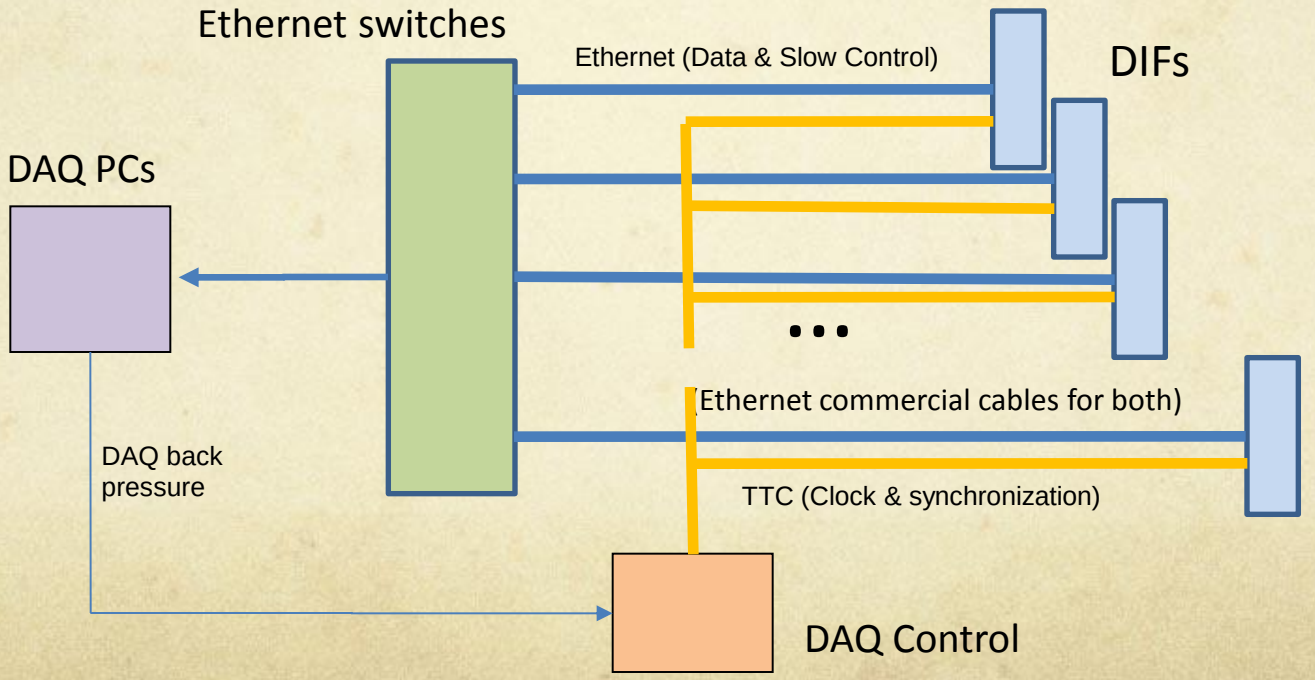
- auto-trigger, power pulsing

3rd generation ROC ASICs:

- independent channels (= zero suppression)
- digital part much more complicated
- new slow control (triple voting) using I2C link
- new PLL:
  - input frequency 2.5 MHz → output frequency: 10, 20, 40, and 80 MHz
  - need to distribute only slow clock to ASUs
- HARDROC3 is the demonstrator for all 3rd gen. ROC chips (SKIROC, SPIROC, …), same digital part for all
- HARDROC3 received in June 2013
- Tests have started

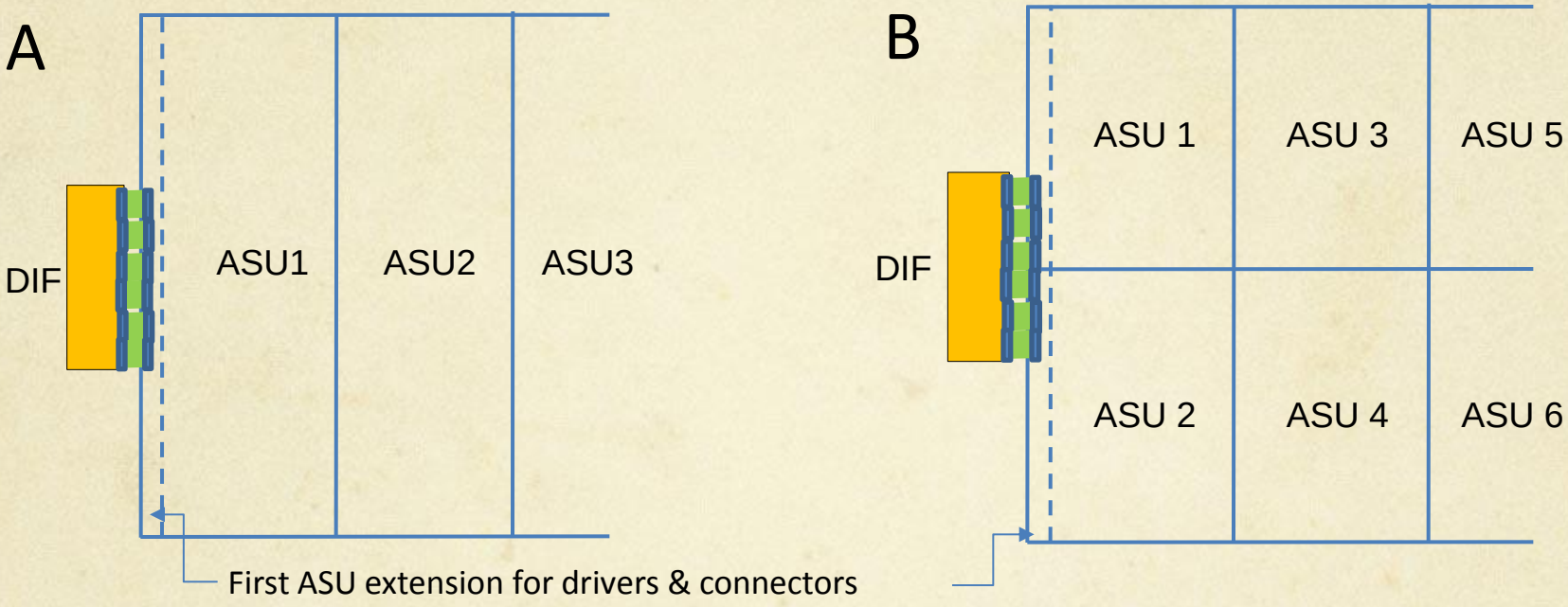
New SDHCAL DAQ architecture

- only one DIF per plane (up to 432 HARDROC3 chips)
- slow control through the new I2C bus
- data transmission to DAQ by Ethernet using commercial switches
- clock and synchronization by TTC (LHC Timing, Trigger and Control chips)
- USB 2.0 for debugging



SDHCAL: New ASU Layout Options

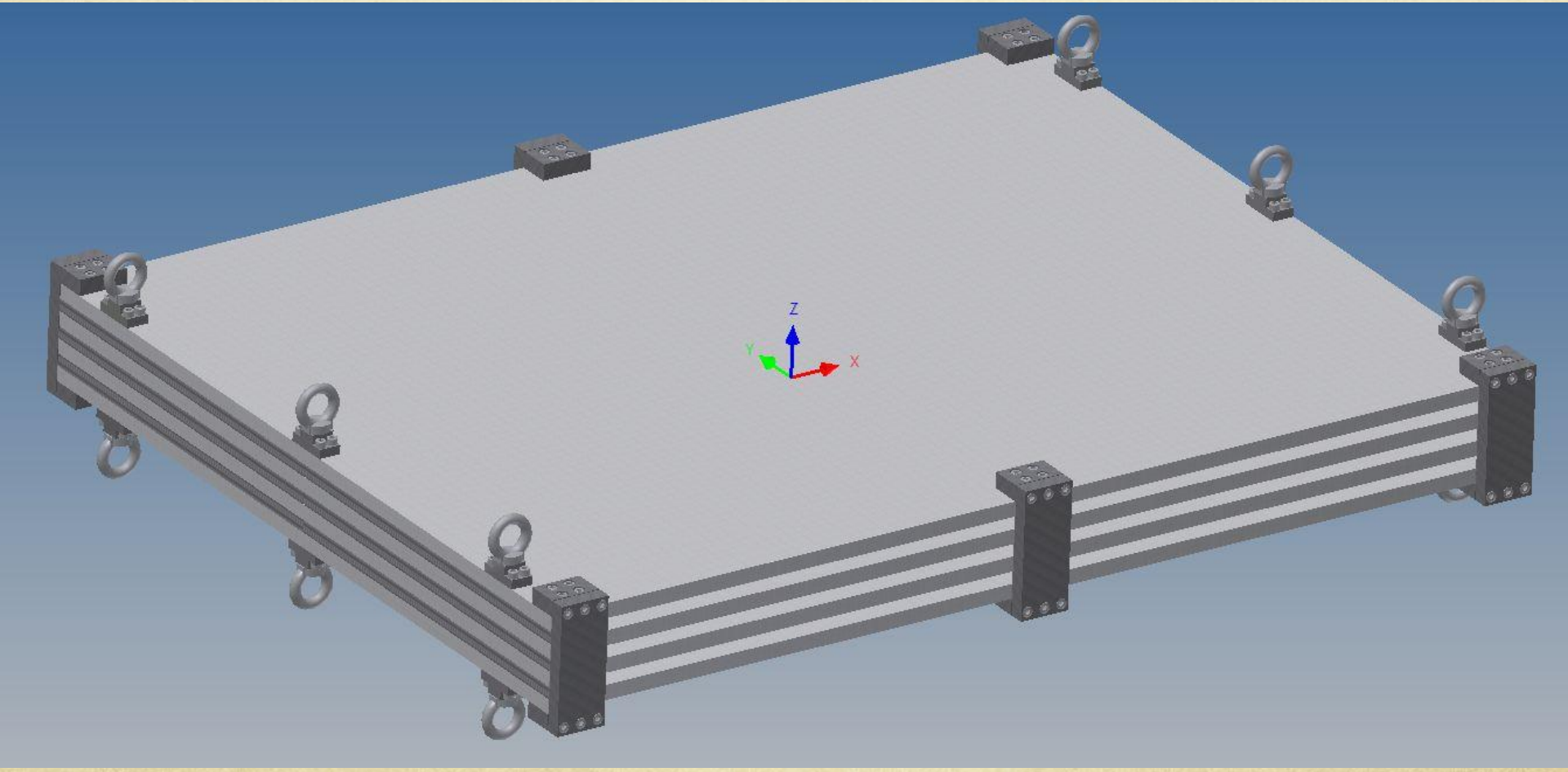
only one DIF per plane → rearrange ASU boards in the plane to reduce the number of connections between the DIF and the plane



- option A: looks more risky because of 1m long ASU boards
- option B: need to send common signals twice (one per slab)
- both options: first ASUs will have extension to host the connectors and the buffers for driving the long lines

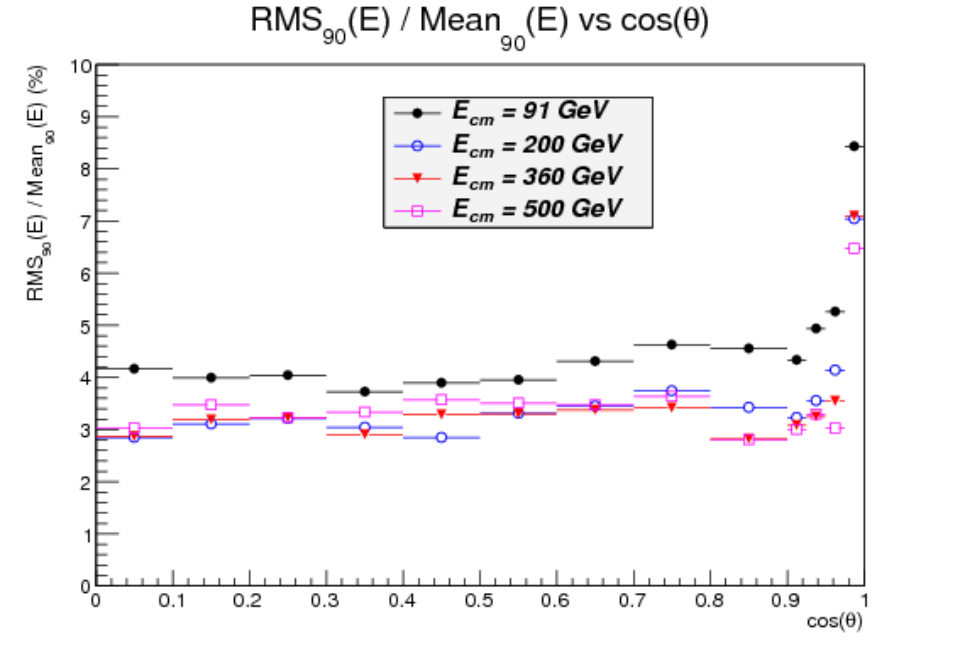
SDHCAL: Large Self-supporting Mechanical Structure

- design of large self-supporting structure for 3 layers



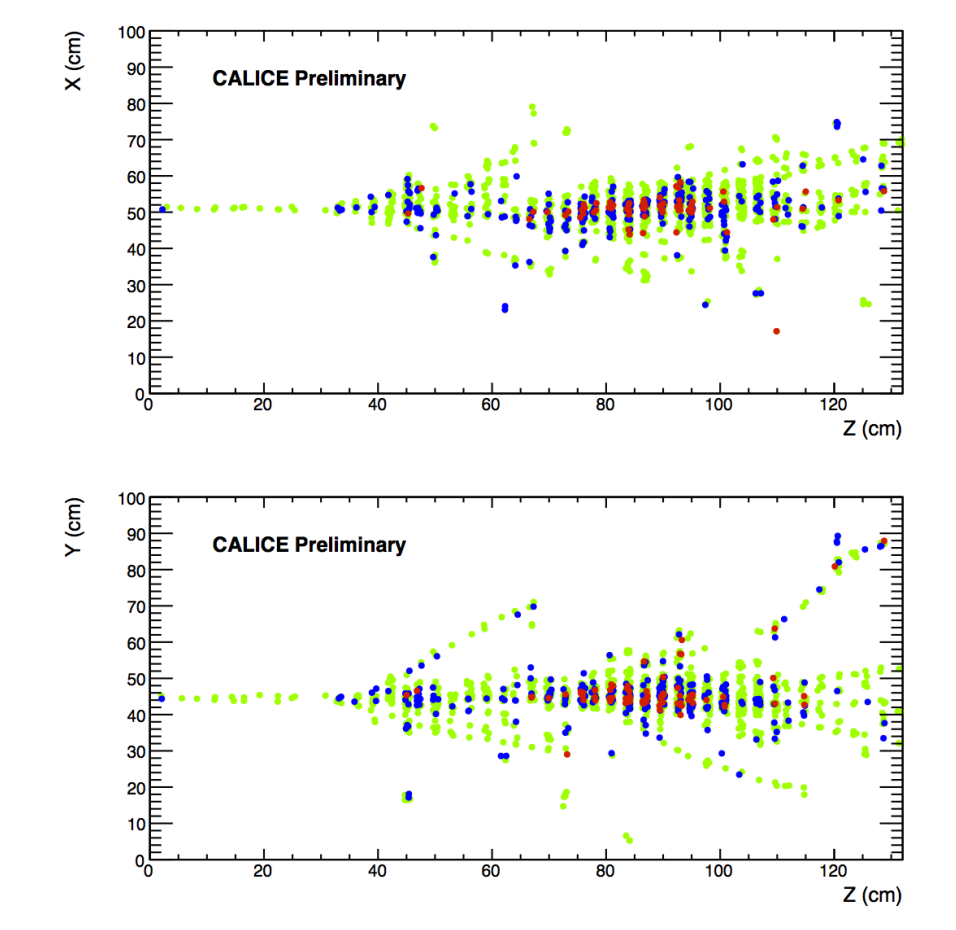
SDHCAL: Optimisation of Particle Flow

reasonable jet reconstruction with non-optimized Pandora PFA

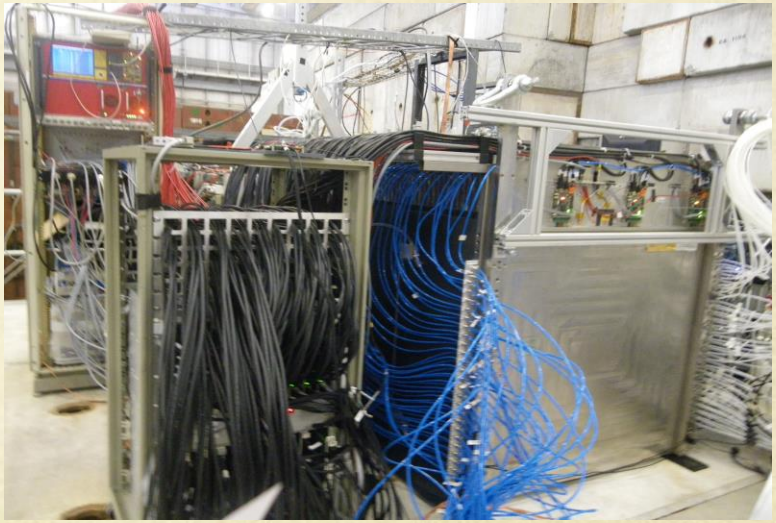


- Energy reconstruction:
  - $E_{old} = \alpha N_1 + \beta N_2 + \gamma N_3$
  - $E_{new} = \alpha(N_{shower})\, N_1 + \beta(N_{shower})\, N_2 + \gamma(N_{shower})\, N_3$
- Neural Network
  - use the hadronic shower shape
- SDHCAL radius:
  - collaborate with ECAL people
- cell size (?), more bits (3?)

Semi-Digital HCAL

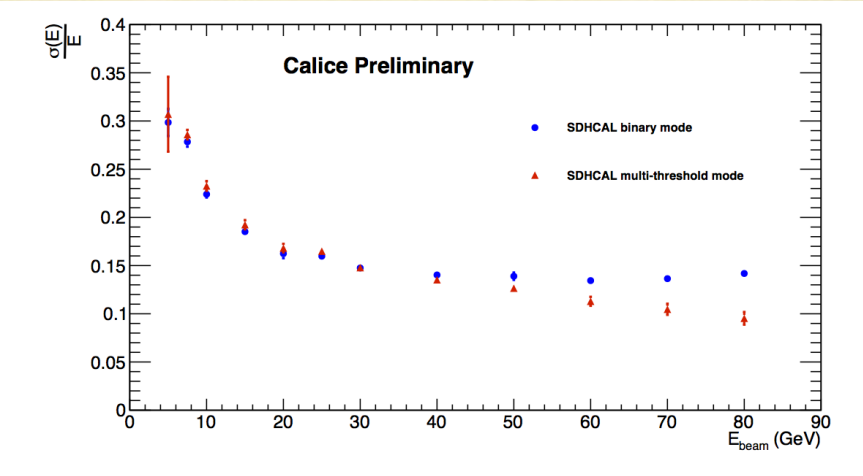


- Glass Resistive Plate Chambers
- 1×1 cm^2 pads
- read-out: 2 bit (semi-digital)



Energy Resolution for Hadrons

SDHCAL

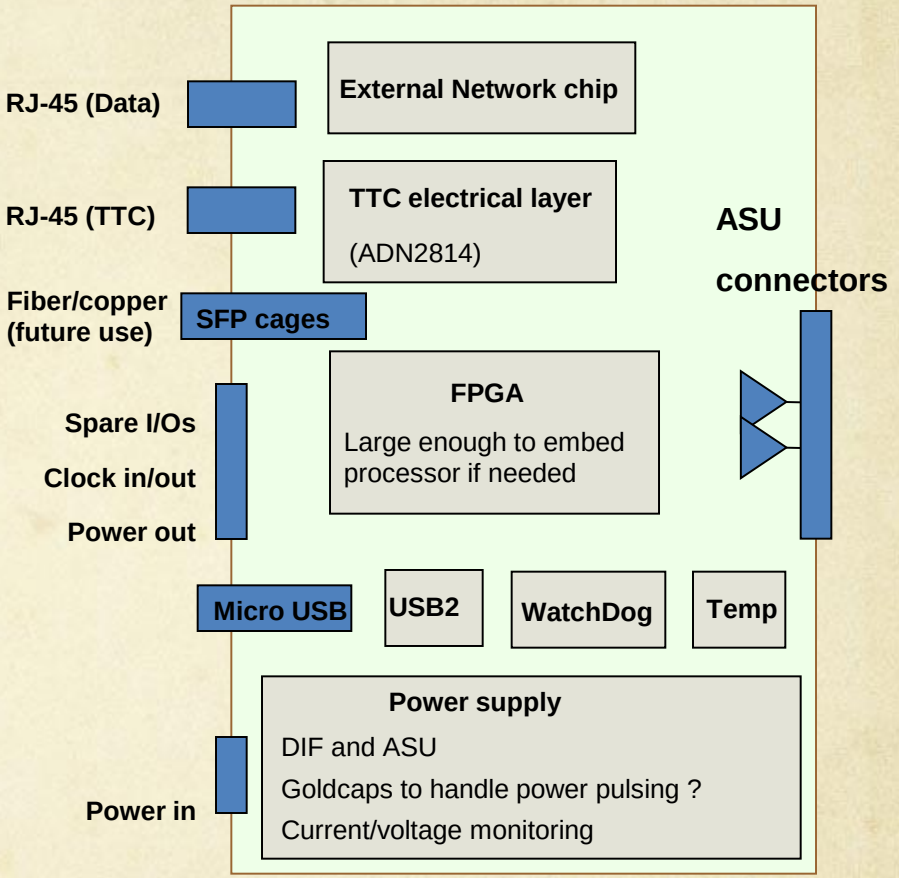


Resolution with **1** or **3** thresholds

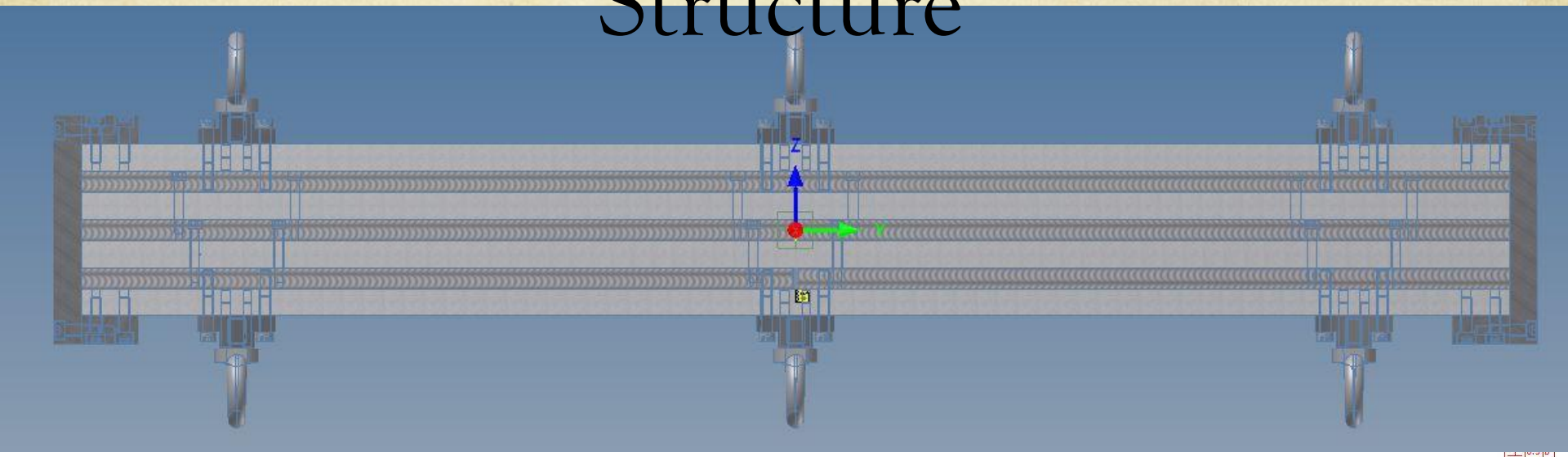
3 thresholds improve resolution at large energies

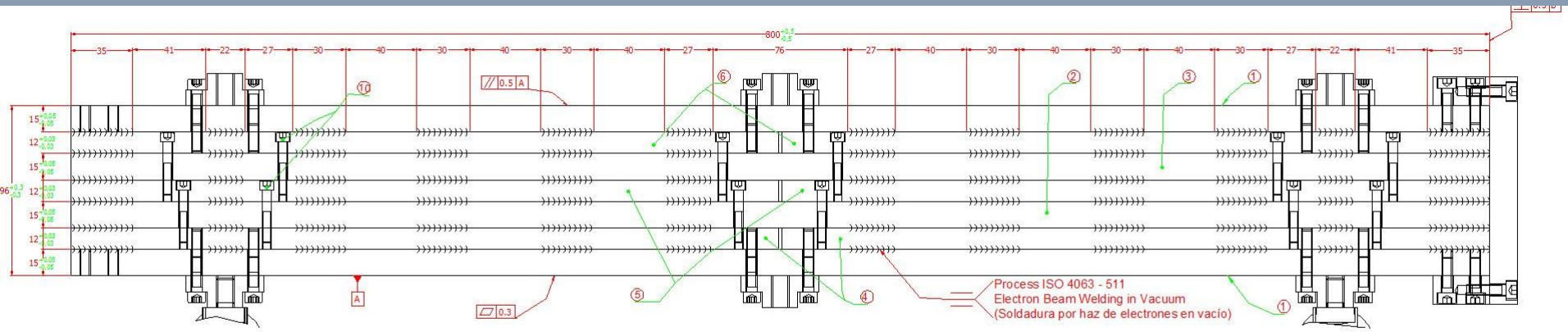
DIF: Designed for ILD SDHCAL

- Only one DIF per plane. For the maximun lenght plane (1x3m) the DIF will handle 432 HR3 chips
- Slow control through the new HR3 I2C bus
- Data transmision to DAQ by Ethernet using comercial switches for concentration
- Clock and syncronization by TTC
- USB 2.0 for debugging



Self-supporting Mechanical Structure





Made by Electron Beam Welding proccess in Vacuum.
Welding deep of 5 mm.