AMICSA 2014

Sunday 29th June 2014 - Wednesday 1st July 2014

Geneva, Switzerland

Proceedings

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Need and Requirements for Radiation Hardened Analogue and Mixed-Signal ICs

Strategy for Radiation Tolerance Assurance of the A&T electronic Equipment

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Abstract

This paper present an overview of the criteria for choosing radiation test facilities, the test strategy and procedures, adopted considering the type of the Accelerator Sector Equipment, its individual list of required components, as well as the radiation levels of the area where it will be installed.

I. INTRODUCTION

The radiation environment encountered at high-energy accelerators differs from the environment relevant for space applications. The mixed field expected at modern accelerators is composed of charged and neutral hadrons (protons, pions, kaons and neutrons), photons, electrons and muons, ranging from very low (thermal) energies up to the TeV range [1].

This complex field is due to particles generated by primary particle collisions in the experimental areas, distributed beam losses around the machine, and the circulating beam interacting with the residual gas inside the beam pipe. Electronic components and systems exposed to a mixed radiation field will experience at once all three different types of radiation damages: Single Event Effects (SEEs), damage from Total Ionizing Dose (TID) and Displacement Damage (DD), where in all cases, not only the particle type, but also the respective energy distribution are to be considered. One important example of the latter are latch-up errors (possibly destructive) where in the context of accelerator environments their cross section can still increase until energies in the GeV range, especially if high-Z materials are present near the device's sensitive region [2]. In addition, for some devices the impact of thermal neutrons is not to be neglected; and when it comes to dose, pure gamma test measurements are partly not fully representative.

For the CERN accelerator sector, the control and the functioning of the Large Hadron Collider (LHC) requires many systems and equipment partly to be installed in radiation areas, such as power converters providing up to 13 kA current to the super conducting magnets, safety and monitoring electronics, actuators for discharging the superconducting coils, pumps for creating the required vacuum conditions in the beam pipe, in the magnets, and in the helium distribution line, cryogenic systems to reach the temperatures down to a few Kelvin, and many others. Moreover, depending on the functionality, each system is replicated 10, 100 or 1000 times along the LHC and its injections lines, thus amplifying even low failure rates in terms of their possible impact to the accelerator operation.

Within these constraints, the conception of full custom solutions down to the component level is often not possible and must be adopted according to each individual design limitations, defined by the electrical specifications on the one side and the harsh radiation environment on the other. Depending on the latter, in the context of accelerators, equipment can thus be either a fully commercial system, or a custom development, based on hardened or qualified electronic components, or a mix of the two solutions.

Therefore, all exposed electronic systems have to be qualified for their radiation tolerance. The latter has to include a failure analysis and an estimation of the respective impact on accelerator operation. In this context, the device degradation due to cumulative effects, or its functional limitations due to single event failures, is not a limitation by itself, but must be quantified. In terms of respective design acceptance criteria, the performance degradation must not prevent the proper use of the component or the system up to its defined (and qualified) TID and DD targets, as well as the rate of SEE must remain sufficiently low in order to cause only a limited (and acceptable) number of stops of the accelerator, while also keeping as short as possible the consequent machine downtime.

Combining all accelerator operation, control and monitoring systems, the R2E project [3] aims for an accelerator operation with an overall radiation induced 'Mean-Time Between Failures' (MTBF) greater than or equal to one week for nominal, ultimate and later high-luminosity operation conditions, therefore finally assuming a peak luminosity of $\sim 5\times10^{34}$ $cm^{-2}s^{-1}$ allowing for an annual integrated luminosity of more than 200 fb^{-1}.

In order to keep the overall failure rate under control and to reach the goal defined by the MTBF target, one requires a long-term radiation test and qualification strategy trimmed to the needs of the accelerator radiation environment and its applications.

After presenting the structure of the R2E project and the mandate of the RADiation Working Group (RADWG), this paper will describe the radiation levels in the accelerator sector, the criteria for choosing radiation test facilities, both standard facilities as well as a new CERN-based one (CHARM), the test strategy and procedure, with flow charts of the radiation tests to be performed, taking into account the type of the equipment, its individual list of required components, as well as the radiation levels of the area where it will be installed. A generic architecture of the electronic systems used in the accelerator is described highlighting the critical parts which could be developed as radiation hard ASICs (Application-specific integrated circuit) for future applications.

II. R2E PROJECT ORGANIZATION

Figure 1 reports the organization of the R2E project which was set in 2007. In order to reduce the radiation failures, the equipment, which is or will be installed in areas where radiation levels are critical, must be radiation tolerant. The designers of that equipment participate to the RADWG meetings [4]. The R2E project advices that at least one member of each accelerator group has to attend the meeting. The RadWG provides support to the accelerator sector equipment groups for the assessment of radiation tolerance of electronic equipment to be installed in radiation exposed areas. The RADWG is as a forum for electronic engineers to discuss common design practices and appropriate radiation tests, as well as observed radiation induced failures in the accelerators and their follow-up. The group also coordinates radiation test campaigns within CERN and at external facilities. The RADWG assists the R2E Project leader for the evaluation of the technical aspects of the proposed mitigation actions with the representatives of the equipment groups, and is used by the R2E project leader to inform the equipment groups of the action proposed. The relocation of the equipment and the shielding of exposed areas are also among the possible countermeasures to protect electronics against radiation but are not discussed in this document. The RadWG furthermore informs about simulated and measured radiation levels in the various underground areas, delivered by the Monitoring and Calculations Working Group (MCWG). The MCWG studies the radiation levels of the LHC and its injection lines with FLUKA Montecarlo calculations and collects the on-field data of the monitoring devices (Beam Loss Monitor, Radiation Monitors, passive dosimeters) to weekly provide the evolution of the radiation levels during the operation.

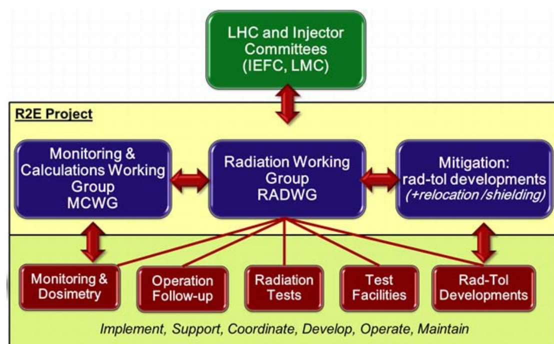

Figure 1. Organization of the R2E project.

III. Environment and Radiation Levels

The variety of radiation source terms present in a particle accelerator results in a unique radiation field composed of different particles at various energies which will provoke the three different types of radiation damage [1]. High Energy Hadron (HEH, >20 MeV) radiation levels range from a few 10^7 cm^{-2} (protected, shielded areas) to 10^{12} cm^{-2} (tunnel areas) per year, corresponding to an annual TID range of 1 rad-100 krad(Si) [1]. In the CERN injection lines, several smaller particle accelerators which feed the main LHC ring, where radiation levels up to 100-1000 krad (Si) (with hadron fluence to 10^{13} cm^{-2}) are to be expected at the location of the electronic equipment. Electronic systems containing only COTS components, installed in the shielded areas, can already fail at hadron fluences as low as 10^7 cm^{-2}; damage to COTS components, used in custom designed boards, is not negligible starting from doses of 1-10 krad (Si). Therefore, the LHC tunnel and its injection lines present radiation levels induced by a hadron fluence ranging from a few 10^7 to 10^{13} cm^{-2}. Figure 2 reports the range values in terms of HEH fluences, TID, and 1MeV neutron equivalent, considering the ratio among those quantities provided by means of the FLUKA Monte-Carlo calculations.

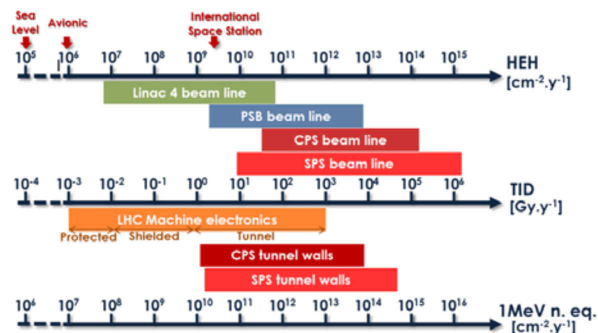

Figure 2. LHC and injection lines radiation levels. The typical values of radiation levels at sea level (New York), avionic altitudes and international space station are also indicated.

IV. Test Facilities choice

Several areas close to the accelerator tunnel and partly not sufficiently shielded, are equipped with commercial or COTS based systems which are mostly affected by the risk of SEEs, whereas electronics installed in the accelerator tunnel, based on custom design, will in the long-term also suffer from additional cumulated damage (TID and DD, Figure 2). On this basis, all three types of radiation effects must be considered for testing although they will not impact in the same way the electronic systems. The radiation tolerance of electronic devices can be estimated by using different particle types. Protons are able to trigger all three types of radiation effects but create synergistic effects among SEE induced failures and total dose and displacement damage. Neutrons at ~1 MeV are used to test the robustness to displacement damage; neutrons at high-energy are exploited to study the SEE without creating total dose effect. Gamma irradiations are conceived to characterize the TID of the DUT (Device Under Test) without creating any displacement damage. Two, partly parallel, strategies can be pursued:

- The first one consists in selecting and using external facilities which are recognized by the radiation community: e.g., a) the Paul Scherrer Institute (PSI) providing a monochromatic proton beam, b) the Centre Energie Atomique (CEA) providing a neutron environment at ~1 MeV, c) Fraunhofer INT institute offering a ^{60}Co or neutron source, d) the European Space Agency (ESA) offering a ^{60}Co source and several others. In addition, specific facilities, such as the PTB (Physikalisch-Technische Bundensanstalt), the Nuclear Research Institute (NRI in Rez), and the nuclear reactor in Kijeller can be exploited for calibration purposes. (e.g., for the Radiation Monitor project).
- The second strategy aims at building a mixed radiation facility capable of reproducing the representative

accelerator environments (e.g., of both the shielded and tunnel areas). In the past, two test areas, CNRAD and H4IRRAD, have been used for this purpose, although their operation was not fully optimized for radiation testing (limited availability, intensity, etc.). On the basis of this experience, a dedicated new radiation facility (CHARM) has been built [5].

A collection of the available test facilities is available on the RADWG website [4].

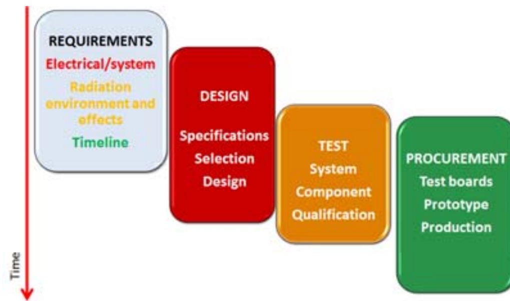

Figure 3: Timeline of a new electronic accelerator system development where radiation test is a dedicated phase of this process.

V. Test and Qualification Strategy

The test of the components and/or the system is part of a process with defined phases which starts with the definition of the requirements of a given project (Figure 3). Once the designers will specify the type of systems to be used and its components, the radiation effects to be considered are analysed by knowing the environment, which depends on the installation area. The test strategy will then strongly depend on the radiation environment and the complexity of the electronic system to be qualified. The LHC equipment and its subsystems can be classified in two main categories:

- fully commercial system, here referred to as COTS system;
- custom electronic systems based on COTS components.

In order to define the test strategy and the requirements, first the location of the equipment is to be considered. We can distinguish the following areas where one usually can find electronic systems:

- Accelerator tunnel areas
  - LHC areas close to experiments (*e.g.,* inner triplets) or areas with high losses (*e.g.,* collimation areas): very high radiation levels generally excluding the installation of electronic systems
  - LHC Dispressor/suppressor (DS): tunnel area with higher radiation doses
  - LHC ARC: tunnel area with lower doses
  - Injectors: usually higher radiation doses, partly excluding the installation of electronic devices
- Shielded areas
  - Critical zones (areas with annual fluences above 10^6 n/cm^2)
  - Safe zones.

Radiation hardened devices as used in space or military applications are evidently advisable for custom solution, but are used only in a limited amount due to component costs and the additional limitation that they do not always offer the electrical performance required for an individual application. Therefore, keeping in mind the target radiation levels and the fact that repair interventions are not impossible but only have to be limited in terms of time and number, the use of radiation hardened parts is limited for the actual designs. In terms of radiation tolerance required for individual applications, starting from the radiation levels, one obtains for each application a list of locations and corresponding radiation levels for TID, DD and HEH. To this, depending on the location and the component or equipment type, one must take certain safety margins into account:

i. the uncertainty of the radiation levels (if not known by measurements: x2),
ii. the low dose rate effects (x3, to be considered only for bipolar devices),
iii. the traceability of the components (x3, absence of lot codes or respective characterization).

The last two parameters only apply for the calculation of the TID levels in the tunnel for the test of COTS components, whose traceability and quality assurance strategy will be described later.

In order to obtain an estimate for the expected global failure rate, the equipment group needs also to specify the number of exposed systems/components. This collected information can then either be used to estimate the failure rate and life-time based on radiation test results, or determines the target levels required for radiation tests.

Based on the radiation levels already present at CERN accelerators and those expected for future operation, it can be concluded that:

- commercial systems: are ideally tested in order to allow for an estimate of the global failure rate and can only be installed in shielded and relatively low radiation areas, provided that mitigation measures (e.g., remote reset) reduce the impact on accelerator operation and that they are not linked to safety systems
- COTS based systems can be installed in tunnel areas but require a respective radiation tolerant design and dedicated radiation test program. Depending on the details taken into account during the qualification process (e.g., lot testing) more or less safety factors have to be applied
- systems based on hardened electronic components shall be considered for the most exposed location (in case these cannot be avoided).

Based upon this general framework, we describe the CERN test strategy and requirements per installation area and per type of equipment by indicating the goal of the test, the modality, the suggested facilities, and the consequent follow-up actions to be taken on the basis of the collected fault scenarios.

VI. Shielded and Low-Radiation Areas (<10^9 HEH/cm^2/y)

TID and the DD are not a concern for the equipment installed in the shielded areas where the SEEs remain the

unique source of radiation effects. The difference between safe and critical areas depends on the level of cumulated high-energy hadrons. We recall that radiation tests are not required for areas where the annual cumulated high-energy hadrons fluence is lower than 10^6 n/cm^2.

A. COTS system

COTS systems are fully commercial devices. Among others, we can find an Uninterruptable Power Supply (UPS), a commercial solution to monitor the voltage distribution of the area, fire detectors with its central unit, PLC stations of different branches, and so far so forth. The traceability of this equipment is difficult. The products are purchased from external companies and there is no control of the single components whose reference can even change from one system to another. The main phases of the project development and the respective radiation test period are shown in Figure 4. It is important to note that depending on the annual radiation levels, as well as the failure impact of the system, each installation case must be evaluated individually prior installation.

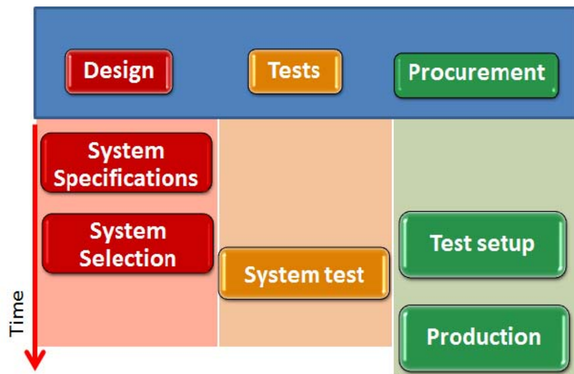

Figure 4: Design, Test and Procurement phases for a COTS system used in low radiation areas.

In this case it is required to qualify the entire system for their overall SEE vulnerability only. The test aims at finding an indicative cross section for soft SEEs and verifying if destructive events can occur. Those types of systems can only be tested in CERN test areas where big volumes can be placed. Although the system is almost a black box for the equipment owner, the survey of the total current consumption and the monitoring and logging of accessible analogue test points or digital data are required during the radiation test. The evaluation of the cross section for the different types of soft SEEs and the knowledge of the expected radiation levels provide a good indication if the system failure rate is acceptable in terms of MTBF. Should the failure rate not be acceptable, mitigation techniques at the system level, such as the implementation of automatic resets, software fault diagnostics, use of redundant subsystems, are to be put in place.

As far as hard single events are concerned, the evaluation of the cross section is usually not possible for such partly large and complex systems, especially if only one or two units were tested. If observed, the study of a mitigation technique is performed to verify if the destructive event can be intercepted and controlled. If this study does not provide a robust solution, either an overall equipment redundancy is to be considered, or the failure can be accepted in case the equipment responsible prepares a strategy to promptly replace the defective unit in case of a destructive SEE (without major impact on accelerator operation).

B. Custom systems based on COTS components

Custom systems are electronic boards, devoted to control actuators, acquire signals, manage power converters, which have been designed by CERN engineers based on COTS components. Those systems are not black boxes for the equipment responsible who masters both the design and the component choice. Conversely to the case of COTS system, individual electronic boards are to be considered for the testing. Whenever it is possible, the designer uses components, which have already been tested or qualified. However, in this case the test of the single parts and the lot traceability against SEEs is not required because the radiation levels are sufficiently low. Thus, we do not apply the corresponding safety margin on the lot to calculate the required radiation tolerance criteria. The R2E strategy recommends at least a SEE test of the boards to investigate on SETs and quantify soft and hard SEE cross sections at the defined radiation tolerant levels (see Figure 5). The radiation test can be performed either at a CERN test area or at PSI. For the latter case, if the board is larger than a circle of 5 cm diameter, a scan, and thus multiple runs are required to irradiate all the components. The current consumption of the board and other analogue test points, which can suffer SETs potentially harmful for the board, are to be monitored and all numeric data of digital components are to be checked.

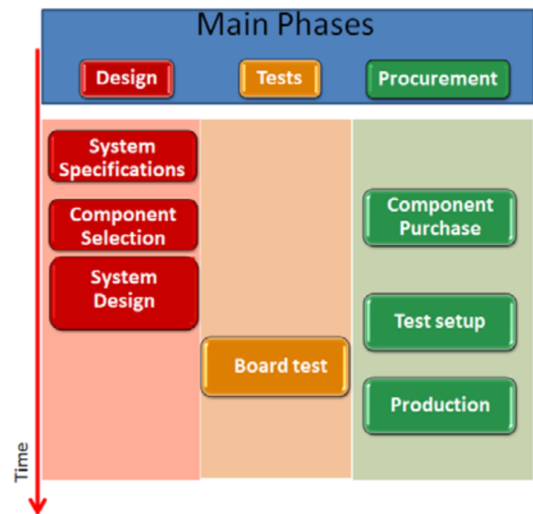

Figure 5: Design, test and procurement phases for custom board with COTS components used in low radiation areas.

The respective evaluation of the cross section for the different types of SEEs and the knowledge of the expected radiation levels indicate if the system failure rate is acceptable in terms of MTBF. Should the failure rate not be acceptable, mitigation techniques can be applied at design level for individual components, such as replacement of sensitive parts, the use of filters for SETs, or at system level, such as the implementation of automatic resets, software fault diagnostics, or the use of redundant subsystems. As far as hard single events are concerned, the evaluation of the cross

section can be done if an active current consumption monitor is put in place during the test. The mitigation techniques can be applied at component level if the sensitive part is individuated or at board level by using an anti-latchup system. The latter anti-latchup circuit can then be also considered as final mean of mitigation, depending on the eventual application case. As an ultimate option the redundancy of the board can be considered. Table 1 summarizes the radiation test facilities, test modalities, and the possible mitigation actions for systems installed in shielded areas.

VII. Tunnel and High-Radiation Areas (>10^9 HEH/cm^2/y)

In this case all three types of radiation effects are to be considered for the installed equipment. The CERN injector areas, as well as the LHC DS zones impose a more severe limit on the TID and DD radiation tolerant criterions. In those areas, the installation of the equipment is allowed only when electrical and functional constraints make it necessary, i.e. no other reasonable installation solution can be found in more protected areas. The use of fully commercial system is not anymore allowed because of their possible high sensitivity and their traceability and qualification constraints; moreover their internal design is often not known.

Table 1: Summary of the test type, facilities, test modality and mitigation actions for systems of the shielded areas.

Location	System type	Test type	Facility	How	Mitigation actions
Shielded area	COTS system	SEE	CERN test area	Test points for SET Current consumption SEE on numeric data	System Software Redundancy
	Custom on COTS	SEE	CERN test area PSI	Test points for SET Current consumption SEE on numeric data	Component Board design Firmware Software Redundancy

All custom developed systems must be radiation tested; moreover, the traceability and the qualification of the lots of the critical components are required, or respective safety margins are to be taken. The process of design, test and procurement is depicted in Figure 6. The ideal test process foresees a component screening test, the lot qualification after the component purchase and then an additional verification of the entire board/system with the chosen components. The component selection is a phase of the system design and depends on the project specifications. Apart a few exceptions, the design of a system can go in parallel with the screening tests, the purchase of the components lots and their qualification. Finally a prototype board is produced, populated with the qualified components, and tested for production acceptance, to be followed by the verification of the latter.

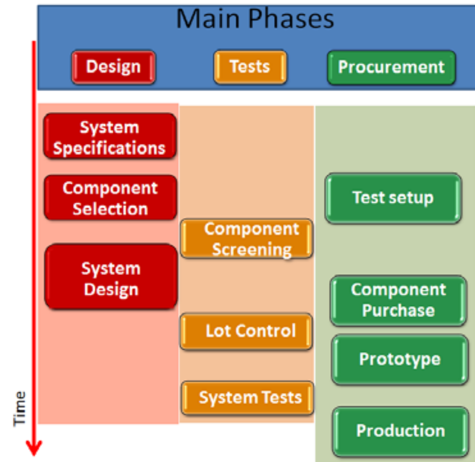

Figure 6: Flow chart of the test strategy for custom boards based on COTS components.

The lot qualification demands a significant amount of work and requires a defined time schedule, which might sometimes not fit within the overall available time planning of a new installation (often driven by accelerator requirements and available shut-down periods). In such cases, the management can decide to proceed with the production and installation of the boards whose components were selected on the basis of radiation screening tests but do not belong to a qualified lot. Since this is a scenario which CERN faced and might also face in the future, two general strategies (discussed in the following sub-sections) are defined to assure the radiation tolerance of custom equipment. Only the first one foresees the lot qualification of the critical components.

The definition of a “lot” for COTS components is not trivial. The components are often bought through vendors who collect the components from different foundries or assembly factories. Among the accelerator electronic groups, it was agreed to try as much as possible contacting vendors in order to get the samples from the same foundry (e.g., through combined purchases). However, that is not always feasible since the number of parts required for the accelerator projects is often not sufficiently high to justify a dedicated production follow-up. However, to a certain extend one can rely on the assumption that COTS samples belong to the same lot when they have the same imprinting on the chip as well as the same production date. That definition is often used for accelerator applications although there is no absolute guarantee that all the samples will have the same internal design; that risk can be accepted depending on the component importance and failure consequence in the design.

Saying this, it is useful to clarify also the definition of a “critical component”. A component is critical if:

- the main functionalities of the board depend on it
- it can potentially suffer or trigger destructive events
- the performance degradation due to radiation cumulative effects makes it useless for the application.

Those definitions are generic and the list of components of a custom board to be considered as 'critical' needs to be decided upon a dedicated analysis.
In the following we briefly describe the two general test strategies and, then, guidelines will be given on the radiation test methods of the components against TID, DD, and soft and hard SEE, high-lightening the facilities which can be exploited for each type of the test.

A. Test strategy with lot validation

The first strategy to select a COTS component for a custom developed board is sketched in Figure 7.

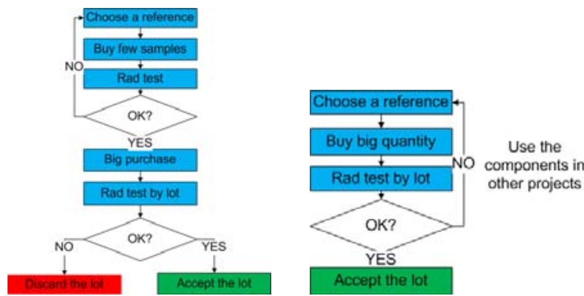

Figure 7: COTS components (to be used in high-radiation areas) selection process with (left) and without (right) the screening phase.

This method is applied when there is the necessity to evaluate different candidates for the same type of the required component (ADC, DAC, differential amplifier, or voltage regulator). The candidates fulfilling the electrical and functional requirements of the application, which they are chosen for, are tested against radiation to determine the best choice. In this case, the best radiation test facility is the one which allows the test of all three types of radiation effects (in a representative way), thus

- PSI, where the test can be done in short time, although ELDRS, which can be an issue for bipolar devices, is then not taken into account and also safety margins for the maximum beam energy have to be taken into account for destructive effects.
- CERN mixed-beam test facility is usually a very good and efficient alternative.

If only TID is a concern for the device under test, then a ^{60}Co source can be used. The DD test is used as a screening test only if the device under test has to work until relatively high fluences (>1x10^{13} n/cm^{2}) or is known to be very sensitive to non-ionizing damage (e.g., optical components). Concerning destructive single events, Section VIII will give the details of the applied strategy. The final facility and test choice is then to be confirmed by the CERN radiation test expert on a case-by-case study depending also on the contingency plan of each individual project (Table 2). Once a component candidate has been chosen, a quantity of parts is bought to fulfil the requirement of the project at long term (including spare parts). If possible, the manufacturer will be asked to provide the samples from the same lot, according to the definition we have provided. The number of samples to be tested for each lot has to be between 5 and 10. The lot should ideally be tested in the same facility where the screening test was performed. If the SEE test is not possible because of time-line constraints, the lot must be qualified against TID.

Table 2: Screening tests and facility option summary.

	Facility	Features	Comments
Proton	PSI	TID, DD, SEE	Fast test No ELDRS (bipolar)
Mixed field	CERN	TID, DD, SEE	Individual components, Batch screening, System tests
^{60}Co source	ESA, Fraunhofer, CERN (>=2015)	TID	ELDRS option
1 MeV neutron	CEA	DD	Recommended if Φ >1x10^{13} n/cm^{2}

The respective risk is acceptable since the literature shows that SEE vulnerability does not change that much from lot to lot. If a TID test at low dose rate (100-400 rad/h) is to be performed, then a dedicated ^{60}Co source at Fraunhofer INT or at ESA (and in the near future also at CERN) can be used.

For urgent projects, the above strategy can be simplified, without any impact on the final quality, but still allowing to avoiding the screening test (Figure 7 right). However, the required component is then purchased immediately for the full required quantity, thus ideally only when (i) a good component candidate already exists and was already tested for, or (ii) the component is not that expensive and also used in other projects of the groups at CERN. Then, the same test criteria as for the previous case are applied.

B. Test strategy without lot validation

Tight time schedules or emergency upgrades sometimes do not allow for a proper selection of the COTS components followed by a detailed lot qualification. In these cases, the designer tries to use components which have been already tested for and whose behaviour under radiation is known. Whenever that is not possible and a new unknown component is used, a radiation test is to be foreseen for each of the most critical components and/or for the entire board. The flow chart of the process is the same as in Figure 5. As far as the test of the single component is concerned, the same criteria described in the previous subsection (A) apply. This then has to be validated by a verification of the entire board once produced (see test criteria of Section VI-B), however including TID and DD effects, as well as ideally a larger random sample in order to compensate for possible lot variations, if not traced during the production process. The CERN R2E strategy foresees as such a series of tests of individual random boards to qualify for SETs and determine soft and hard SEE cross section at the defined radiation tolerant levels, as well as the TID and DD limits, either by including a larger random sample or by applying required safety margins. In this case radiation tests can be done preferably in a CERN test facility (allowing to test a larger set of boards at the same time) or also at PSI. For the latter, if the board is larger than a circle of 5 cm diameter, a scan, and thus multiple runs, is required to irradiate all the components. The current consumption of the board and other analogue test points are to be monitored in detail. The numeric data of digital components are to be checked in a continuous way. The evaluation of the TID and DD limits will indicate if the board can stand the radiation levels at which it

will be exposed; the calculation of the cross section for the different types of soft SEE and the knowledge of the expected radiation levels will determine if the system failure rate is acceptable in terms of MTBF. Should the failure rate not be acceptable, or the TID, DD limits be lower than the radiation acceptance criteria, then the critical components must be replaced with better candidates. In addition, mitigation techniques can be applied at design level, such as filters for SET, drift correction; or at system levels, such as the implementation of automatic resets, software fault diagnostics and correction, or the use of redundant subsystems. As far as hard single events are concerned, the evaluation of the cross section can be done if an active current consumption monitor is put in place during the test. A respective mitigation technique can then be applied at component level if the sensitive part is individuated or at board level by using an anti-latchup system. As an ultimate option the redundancy of the board can be considered.

VIII. Basic Guidelines

In the following sub-sections, more details are given on the guidelines for the component test, which can also be adopted for the test of custom boards. In particular, specific considerations will be added for the test of the destructive single events.

A. TID and DD testing

Total ionizing dose affects almost all types of components and must be carefully considered for the qualification of components that will be used in accelerator tunnels. The TID test requires following the main parameters of a component during the test in an on-line mode, by means of a continuous acquisition during the run, or in off-line mode by performing the measurements at intermediated dose steps (with shortest possible annealing times). It is advised to power the component and to bias it as it will be used in the real application. Measurements in a different bias mode can be done to better understand the behaviour of the DUT at intermediate dose steps. If the real application case is not known, the test must aim at figuring out the DUT characteristics as a function of the dose. The main parameters indicated in the datasheet are to be checked. In this case, the test can get longer and more complicated as more setups are to be foreseen. Only as a last option the DUT can be tested in passive mode without the powering and the bias; however this test mode is not advised for most applications and component types. For comparison purposes, the parallel test of a chip which is not irradiated and checked as a reference is strongly recommended. In addition, often a careful temperature logging is required as it can provide valuable input for the final data analysis. An available test standard [6] requires checking the components after irradiation to verify if the observed effects are stable in time or if annealing effects occur. This is especially important as the average dose rate in accelerator tunnels is usually relatively low and unpractical to be tested for. Therefore, a dose rate range 100-360 rad/h (ESCC22900 [7]) is usually chosen for bipolar components as a trade-off for testing of low dose rate effects in a reasonable time. CMOS components can be tested at higher dose rate which is considered a worst case condition for this technology. TID test for CERN equipment are usually performed at:

- the ^{60}Co source at Fraunhofer INT or ESA/ESTEC and in the future also at CERN: this allows for lot validation of components which are known to be immune to destructive events and displacement damage, as well as optional low dose rate tests.
- Proton beam at PSI: DUTs will also suffer DD and any destructive single event can stop the test. Synergetic effects can thus occur, but often also provide a more global picture of the device under test. However, low dose rate tests are not possible and available beam dimensions do not allow for testing many DUTs at the same time.
- CERN mixed-beam test areas: here tests can be carried out in representative environments and – if required– also at sufficiently low dose rates in order to account for ELDRS. Synergetic effects of DD and destructive SEE have to be accounted for.

For most of the CERN accelerator radiation environments and applications, displacement damage can be considered as a second order problem when compared to the TID effects for two main reasons: the DD only affects a specific category of components (optical components, Zener and integrated bipolar circuits); in addition, in many accelerator areas of concern the expected levels of 1-MeV-equivalent neutron fluence are not that high (<$5\text{x}10^{11}$ n/cm^2/y) to induce significant damage to the components. In addition, 1 MeV conversion tables for proton tests and also the mixed-beam environment are available and are often sufficient to characterize the DD behaviour alongside the TID tests when performed in proton or mixed-field facilities. It is important to note that the equivalence also depends on the material and is given for Si generally. DD tests can be conducted with bias or in passive mode. As for the TID case, it is advised either to test the device at intermediated fluence levels in bias conditions close to the real application or to verify all generic parameters of the DUT. The flux at which the irradiation is carried out does not play a significant role as DD effects are generally stable along time. The test facilities usually used in the CERN accelerator context are:

- CEA, nuclear reactor: allowing for an almost pure DD test since only very low TID levels will be accumulated along the test. The facility is usually used either (i) to specifically check for DD effects on optical and other sensitive devices, or (ii) to reach relatively high fluences (~$1\text{x}10^{14}$ n/cm2) in the order of one day
- The neutron gun of the Fraunhofer institute, especially indicated for small components and intermediate fluence range (<10^{13} cm^{-2})
- Proton beam at PSI: It is important to note that synergetic effects of TID can occur. In this sense, the test is more representative for the final accelerator application where also both effects are present at the same time. The equivalence of the proton fluence in 1 MeV-equivalent neutron fluence depends on the used proton energy and on the material substrate of the DUT. As previously noted for SEE and TID testing, beam dimension limitations do not allow for testing many DUTs at the same time.

- CERN mixed beam test area: as for the PSI case, synergetic effects of TID can occur. However, as representative fields of the final application are used, test results are fully appropriate for the final installation.

B. SEE testing

SEE is a common name to refer to a large category of stochastic radiation effects on electronics due to single-particle interactions. Here we focus on the distinction between soft and hard or permanent single events.

Soft single events can happen on digital devices (upset of a memory or register bit) or analogue devices (transients on an amplifier output) or mixed signal devices such as ADCs or DACs. SEFIs, single functional interrupts possibly freezing the component operation, form a border case of the category of the soft single events. All those effects are non-destructive and respective SEE testing requires reading the numeric data of the DUT, checking for data coherence, eventually rewriting the data after a failure is observed or making a power cycle after a SEFI, finally counting the number of failures. Respective radiation tests can be either static (e.g., fixed register data until an upset occurs) or dynamic (e.g., continuous read/write operation on numeric registers). In many cases a tester board, based on a FPGA or microcontroller is used to control the test. Concerning the SET, which is an analogue transient, it can be either detected via a dedicated hardware circuit and then counted for, or transmitted along a cable to acquire its shape on a scope. These few general lines are intended to illustrate that the setup for SEE tests can easily get complicated also imposing cable length constraints, as the maximum distance between the DUT and the tester or the scope often has to be limited in order to conserve the signal integrity and assure the correctness of the test. For direct monitoring during accelerator operation, or tests in large mixed-beam facilities, this has to be correctly accounted for. Since soft SEUs are due to the flux of high-energy hadronic particles, the actual radiation flux is a very important parameter to set in order to have an error rate which can be monitored and allow to correctly counting the events. In addition, also the representativeness of the radiation environment (e.g. the energy of the hadrons) has to be considered (for SEUs in a limited amount, but possibly important for calibration applications which have to consider also the contribution of hadrons at energies between few MeV and tens of MeV). Soft SEU tests for accelerator applications are usually performed at:

- PSI (proton beam): monochromatic beam from 30 to 230 MeV; generally the beam energy of 230 MeV is used; the irradiation flux can be accurately regulated, however not lower than ~10^7 $cm^{-2}s^{-1}$; synergetic effects of TID and DD have to be considered, but are often of advantage as also representative for accelerator applications. Specific tester boards can be installed close to the DUT and scanning can allow compensating for limited beam dimension which do not permit testing of many DUTs at the same time.
- CERN mixed-beam test area: the radiation field is not monochromatic but representative of the accelerator areas; the radiation field and flux can be regulated by choosing the installation position; synergetic effects of TID and DD have to be considered, but are often of advantage as also representative for accelerator applications; specific tester boards have to be used in the facility, considering that not only DUTs but also the directly surrounding components are exposed to radiation.
- Neutron beam facilities (e.g., at Uppsala): this test avoids having synergetic TID effects. The flux can be regulated but the beam is not monochromatic (distributed or white spectrum with lower high energy tail as applicable to accelerator applications).

Special care must be taken when analysing hard or permanent single events radiation failures as they can lead to device damage if the cause which provoked them, is not removed in due time (e.g., a power switch can be affected by a Single Event Burnout, or a mixed signal device as an ADC can suffer a Single Event Latchup). Without going into the details of the mechanism, in both cases, a current higher than in normal condition, passes through the device and can lead to a possible damage. Therefore, protection methods are required to limit the current and save the device in order to continue the test and cumulate the necessary statistics. Moreover, during the test all critical parameters of the DUT must be checked to verify if the occurrence of a hard single event did not compromise its overall and representative functionality. In addition, if there is no protection method applied or possible, then a significant quantity of DUTs has to be tested. As for soft SEEs, the hadron flux must be regulated in order to be able to count the events in a significant way (i.e. reset cycles and downtime have to be short as compared to failure periods). The setup might also require a scope to acquire the current shape when the event occurs in order to carefully analyse the impact on the system level (e.g., accelerator control). The choice of the facility for testing hard single events is not easy as accelerator environments are characterized by the presence of high-energy hadrons up to several GeVs and there is no mono-energetic test facility easily and sufficiently available providing such high energies. In a mixed beam and high-energetic hadron environment, destructive events are caused by the secondary recoil products created by the impinging particle on the material used within the DUT. The production probability and the LET of the recoil depend on the energy of the impinging particle and on the atomic number of the DUT material. As a rule of thumb, the higher the atomic number of the material, the higher the maximum recoil LET can be with the production probability largely increasing for heavy elements as a function of the impinging beam energy. E.g., if one considers Tungsten of the metallization layer and the vias of the integrated circuit, which is the material with the highest atomic number among the ones used, the recoil can have an LET of up to 40 $MeV.cm^2/mg$. In case mono-energetic facilities (e.g., PSI) are to be used, a safety margin on the target fluence has to be taken into account, in order not to under-test the device, ranging from a few up to more than 10 (depending on the radiation hardness of the application location) [2], [8]. This consideration and the respective safety margin are also to be considered for the characterization of soft single event cross section of critical devices. The criteria to apply the safety factor are reported in [8] for three cases:

I. a low LET onset case (for which the tungsten volume is irrelevant)
II. a high LET onset example with 0.5 mm3 of tungsten per cell, using a simulated cross section of a COTS SRAM
III. a simulated, worst-case, tungsten-dominated response, taking the geometry of the SRAM of case (II) while considering 10 times more tungsten per cell and a step-function heavy ion cross section with a threshold value of 20 MeV.cm2/mg and therefore above what can be produced in silicon

In order to evaluate the impact of the specific energy dependence on the estimated SEL rate value for a given operation environment, we fold the response functions of the above three cases with the HEH energy spectra of different environments. The respective failure rates per unit HEH fluence are presented in Table 3 for the different environments, normalized to the 100 MeV proton value.

Table 3. Expected failure rate for different responses and environments normalized to the 100 MeV case. Marked in bold are environments for which the respective cross sections are at least 3 times larger that at 100 MeV. For these cases, the increase with respect to the 230 MeV case is also shown in brackets [8].

Environment	Case I	Case II	Case III
230 MeV	1.8	2.8	**3.4** (1.0)
LHC- high Shielding	0.7	0.8	0.9
Polar Orbit	0.9	1.6	2.5
Atm 375m	1.0	2.1	**3.3** (1.0)
LHC Low Shielding	1.3	**5.2** (1.9)	**9.7** (2.8)
LHC tunnel	1.5	**9.6 (3.4)**	**20 (5.8)**
Atm 20 km	1.2	**10 (3.6)**	**23 (6.7)**
LHC Exp	1.6	**18 (6.3)**	**40 (12)**

As can be seen in Table 3, for Case I (low LET onset, saturated proton cross section example) the failure rate for all environments is within a factor 2 of the 100 MeV value, which can therefore be considered as representative for them. However, for Cases II and III (tungsten driven, saturating at ↑ 3 GeV), the dependence of the SEL rate with the environment is very strong. For cases with tungsten present near the SV and high LET onset values, the differences are significant (e.g. the LHC tunnel cross section for the Case II model is a factor 3-4 larger than that at 230 MeV). The failure rate is underestimated by a factor ~20 if one considers the 100 MeV cross section for a component with a response of the type of Case III used in an LHC tunnel or atmospheric 20 km altitude environment. Even considering the 230 MeV mono-energetic response, the operational SEL rate could be 6-7 times larger than the one extracted experimentally, which depending on the application can lead to crucial limitations. Therefore, the representativeness and corresponding safety margins to be applied for each case need to be carefully considered.

However, radiation tests can be carried out without taking these important (and possibly costly) safety margins if performed in a CERN test area where the detailed accelerator environment is correctly reproduced. Alternatively, an optional or additional heavy ion test can be performed in order to analyse the threshold LET. This allows for a partial answer; if the DUT shows a threshold larger than 40 MeV.cm^2/mg, then it can be safely used for accelerator applications. Conversely, if the threshold LET turns to be lower than 40 MeV.cm^2/mg, it means that destructive failures can happen with a rate which is difficult to evaluate as it is not trivial to translate a heavy ion cross section into a hadron cross section without applying again significant safety margins.

In summary, the radiation test facilities that can be used in these cases are:

- CERN mixed beam test facility: as it reproduces exactly the accelerator radiation spectra
- Proton beam at PSI: one possibly underestimates the risk of destructive events unless a proper safety margin is applied on the target proton fluence (Table 3).
- Optional or additional heavy-ion tests in order to decide on a possible usability of a component candidate.

Table 4 provides a brief overview of the radiation effects, test facilities and methodologies for COTS components and COTS based boards used for accelerator applications in relatively high radiation areas. Furthermore guidelines and standards from the space community can be consulted: a list is provided in Figure 8 and the on-line links are available at [9].

Standard	TID	DDE	SEE
ESCC 22900-4	X		
ESCC 25100-1			X
MIL-STD 883J Method 1019.9	X		
MIL-STD 883J Method 1017.3		Neutrons	
EIA JESD57			Heavy ions
EIA JESD59			Neutrons
MIL-STD 750-1 Method 1080.1			MOSFETS Heavy ions

ESCC European Space Component Coordination
MIL-STD US Military Standard
EIA-JESD Electronic industries Association / JEDEC Standard
JEDEC Joint Electron Device Engineering Council

Figure 8. List of test standards used by the space community.

IX. Typical Architecture of the Accelerator Equipment

Figure 9 reports the list of the accelerator groups which develop radiation tolerant equipment. The column *System* indicates if the equipment is entirely designed at CERN (*Custom*) or partially uses commercial solutions (*Semi-Custom*). Most of the applications are based on COTS components and only a few groups use in their designs radiation hard devices, developed by the Microelectronic group of the Physics (PH) department at CERN. Medium and high power components are especially used for the power converters and the kicker magnets applications. The other groups use analogue, digital or mixed devices to have equipment which is able to read external sensors and inputs, threat the signals, and execute commands by means of actuators.

Table 4: Summary of the test type, facilities, test modality and mitigation actions for COTS components and COTS based boards used in high-radiation accelerator areas.

Test	Facility	How	Mitigation actions
SEE	CERN test area PSI Heavy Ion	Test points for SET Current consumption SEE on numeric data	Filter TMR De-Rating (Power switches) Anti-latchup Redundancy
TID	Fraunhofer ESTEC CERN Co-60 PSI	Test points for drift checking and parameter degradation	Foresee the drift effect at design stage
DD	CEA, Fraunhofer	Test points for drift and parameter degradation	Foresee the drift effect at design stage

Team	Activity	Devices components			System	Type
		Analog	Digital Mixed	Power		
TE/MPE	QPS	x	x		Custom	COTS
TE/EPC	Power Converter	x	x	x	Custom	COTS
TE/CRG	Cryogenics	x	x		Custom	COTS/Rad hard
BE/ABT	Interlock and Kicker	x	x	x	Semi-Custom	COTS
EN/STI	Radiation Monitor	x	x		Custom	COTS
BE/BI	Beam instrumentation	x	x		Custom	COTS/Rad hard
BE/RF	RF Cavities	x		x	Custom	COTS
BE/CO	Control equipment	x	x		Custom	COTS
EN/MEF	Survey	x	x		Custom	COTS
TE/VSC	Vacuum equipment	x	x		Semi-Custom	COTS
IT	IT tools		x		Semi-Custom	COTS
EN/EL	Light, LED	x			Semi-Custom	COTS
GS/ASE	Safety, Alarms	x	x		Semi-Custom	COTS
EN/STI	Radiation test activities	x	x	x	-	-

Figure 9. List of the Accelerator groups developing radiation tolerant equipment.

A typical board of a radiation tolerant equipment installed in the LHC tunnel (e.g. power converter controller, Quench Protection System cards, beam screen heaters, RadMon), is based on the architecture depicted in Figure 10. The block diagram, extremely simplified with respect to the real implementation, aims at showing the parts which are common to several designs. The FPGA is the core unit which manages the analogue and digital inputs, the other peripherals, the outputs, the signal processing and the communication with the high level front-end via a field bus. Analog to Digital (AD) and/or Digital-to-Analog (DA) converters are used to acquire signals from sensors and send analogue waveforms to actuators. In many cases, multiple inputs and outputs signals are to be managed, requiring the use of multiplexer and analogue switches. Depending on the dynamic range of the input/output signals, amplifiers are integrated. Each system uses about 50-200 number of digital I/O. For a few applications, optical transceivers are used to treat high rate data from optical fibres. Furthermore Flash and RAM memories are used to store fix configurations and buffer data, respectively.

Making this typical board radiation tolerant requires a significant amount of testing if COTS components are used. As explained above, several candidates are to be tested in order to choose a good candidate; then a batch of component is acquired and qualified.

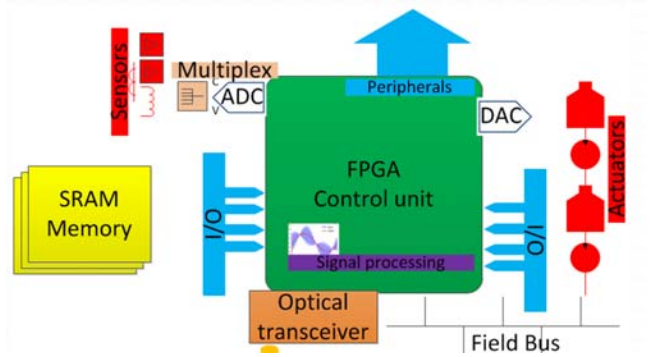

Figure 10. Architecture of typical accelerator equipment.

Although each application has its own peculiarities and requires specific electrical performance for a given component, there are several parts which are common to different projects and are reported in Figure 11. The Intellectual Property (IP) of functionalities very similar to those in Figure 11 exist and can be implemented with radiation hard library of semiconductor fabrication facilities. Although the rad-hard single ASIC is more expensive than an equivalent COTS part, proposed by the manufacturers for large markets, the price can still be competitive if an ASIC is used by several groups and a volume of 1000-5000 units is required. Furthermore, the accelerator applications require neither special packaging, nor the qualification of the part over large temperature range and against mechanical vibrations, as it happens for the space projects. On this basis, implementing the required commune functionalities with radiation hard ASICs could be an option to be considered for future developments and design.

X. Conclusions

This paper described the test strategy and procedures to be applied for the radiation qualification of the equipment installed in the LHC and its injectors. The type of equipment, its location, the actual impact of radiation induced failures on the overall accelerator operation are considered to drive the most convenient and appropriate radiation assurance. The radiation environment encountered at CERN accelerators, the large number of electronic systems and components, as well as the actual impact of radiation induced failures on the overall accelerator operation, strongly differ from the environment and systems usually relevant for space applications. Additional constraints, but in some cases also simplifications, which have to and can be considered with respect to the test and monitoring standards, have been respectively summarized. To date, most of the accelerator applications rely on COTS devices; however, there are a few functionalities, needed and critical for the single application, such as AD converters, optical transceivers, or analogue switches, which are very demanding in terms of electrical performance. Thus only a few (and in some cases just one) candidates can be chosen from the COTS market; furthermore this selected device must be radiation tolerant. Up to now it was always possible to find a good solution but in the future it can be considered to implement the critical functionalities,

which are in common to several applications, in order to have a significant volume of unit, in radiation hard ASIC.

ASIC	Requirements
ADC	• 18-24 bit resolution, Sampling rate 10-50 kSps • 16-18 bit resolution, Sampling rate 50-200 kSps • 14-16 bit, Sampling rate 60 MSps
DAC	• 12-16 bit resolution • 10 V range
Signal process	• FIR filter • Median filter
MUX	• Multiple channels for AD/DA
Peripheral Management	• ADC, DAC (if not embedded) • Field bus • Optical transceivers • Serial ports
ULA	• Programmable logic
I/O	• 100 to 200 • LVDS drivers • SERDES input for optical transceivers (2.4 Gb/s-5 Gb/s)
SRAM	• No SEL (> 40 MeV.cm²/mg) • No SEFI on the reading/writing circuitry • Limited TID effect • Sensitive to SEU to measure hadron fluence

Figure 11. List of ASICs of interest for the accelerator groups.

XI. ACKNOWLEDGMENT

The authors would like to thank the members of the R2E project and accelerator Radiation Working Group (RADWG) and the equipment groups for their collaboration.

XII. REFERENCES

[1] K. Roed, M. Brugger, and G. Spiezia, "An overview of the radiation environment at the LHC in light of the R2E irradiation test activities," CERN ATS Note 2011-077, 2011.

[2] R. Garcia Alia et al., “Energy dependence of tungsten-dominated SEL cross sections”, submitted to IEEE TNS.

[3] Radiation to Electronics (R2E) Taskforce at CERN. Available: r2e.web.cern.ch R2E project

[4] RADiation Working Group (RADWG) list of facilities. Available: radwg.web.cern.ch

[5] CHARM website, www.cern.ch/charm

[6] ESA Standard, F. Sturesson, "Total Ionizing Dose (TID) testing," 9 June 2009. http://space.epfl.ch/webdav/site/space/shared/industry_media/04%20TID%20Testing%20F.Sturesson.pdf.

[7] Total Dose Steady State Irradiation test, European Space Standard. Available: https://escies.org/download/specdraftapppub?id=29

[8] R. Garcia Alia et Al., “SEL Cross Section Energy Dependence Impact on the High Energy Accelerator Failure Rate”, submitted to IEEE TNS.

[9] http://radwg.web.cern.ch/RadWG/Pages/links.aspx

Assessment of Mixed Signal Technology

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Abstract

In 2013, within the ECI (European Component Initiative) program of the European Space Agency, the activity “Assessment and characterisation of Mixed Signal Technology” has been initiated. In this paper the activities performed for the assessment of an European mixed signal technology for the development of ASICs for space applications will be described. The assessment has been conducted through different surveys and the results obtained from them will be presented and analysed. Finally a brief description of the test vehicle for the technology characterization will be provided.

I. INTRODUCTION

The “Assessment and characterisation of Mixed Signal Technology” activity has been funded by European Space Agency in order to collect information of mixed signal ASIC processes with particular focus on their capability for space applications. The information on requirements to be supported by mixed signal technologies have been collected from [1], [2] and [3] and through a survey with the collaboration of space community. The tentative was addressed to look for information about similar on-going activities and on existing analogue, digital and mixed signal libraries or ASICs for space applications already manufactured or designed to avoid to duplicate the efforts.

The collected data on the user need has been compared against the processes capabilities available in Europe for mixed signal ASIC manufacturing. At the end of this review one particular process has been choosen for a further reliability and radiation characterization.

The paper is organized as follows: in the Section II the surveys carried out will be described. The results will be shown and discussed in Section III. In Section IV, a description of the test vehicle will be reported together to the test procedure and the list of the parameters to be measured; finally the conclusion will be reported in Section V.

II. DESCRIPTION OF SURVEYS

The assessment of an European mixed signal technology for ASIC design and manufacturing has been driven by 3 different surveys. In the first survey a comparative assessment and verification about the availability of several existing European mixed signal technologies has been performed. In the second survey, inputs covering the needs for mixed-signal ASICs from the space community and the Agency's planned missions have been collected. In last survey, information about the existing rad hard libraries and design kits in terms of primitive devices, SEEs, TID and reliability performances have been collected.

In the next paragraphs each survey will be described and detailed.

A. First Survey: Mixed Signal Technologies Availability

This survey has been addressed to European foundries accessible to the Agency's member states. Twelve (12) European and Non-European manufacturers have been contacted obtaining reply from six (6) of them: Atmel, Austria Micro Systems (AMS), IHP Microelectronics, ON Semiconductor, Telefunken Semiconductor and XFAB. In total, data from 18 technology processes have been collected and analyzed.

The survey was split into 2 sections.The first part focused on general items related to the foundry availability, in particular addressing following questions:

- Licensing and conditions for use
- Foundry expected lifetime
- Foundry loading and product range
- Foundry process options
- Manufacturing turnaround time
- Manufacturing options (Full mask, MPW, MLM; Runs per year; longer availability) and their cost
- Cost of the supported tool chain (external and custom)
- Cost of the digital and analogue design-kit (front- and back-end)
- Supported batch manufacturing
- Supported Digital and Analogue development flows and constraints
- Foundry macro libraries cost
- Third party macro libraries access, conditions, cost and license
- Design kit for usage within space user community and the right for modifications
- Eventual technical support and maintenance of space-DK/libraries for European Space community

In the second part of the survey, specific information about environment, quality, digital performances and

analogue performances of different processes have been collected.

i. Environment

The questions related to environment features have been:

- Temperature range (operational and storage)
- Voltage range
- Radiation tolerance (TID, SEE: SEL, SEU, SET, SEGR, ...)
- ESD and EMC levels supported

ii. Quality

The questions related to quality features have been:

- Intrinsic reliability data/performance
- Wafer thickness
- Process lifetime
- Mean time to failure (FIT)
- Manufacturing yield
- Manufacturing quality systems
- Inspectibility of the manufacturing quality system and PID
- Cost associated with quality inspection
- Reporting and inspectibility of the process control monitors
- Process stability reporting the manufacturing process changes
- Failure analysis support
- Manufactured high-reliability and space qualified flows/components

iii. Digital Performances

The questions related to digital performances features have been:

- Gate density
- Power consumption
- Clock frequency
- Supply voltage range
- Number of metal layers
- Leakage
- Cell library (combinational and sequential; commercial and radiation hardened variants)
- Foundry and/or Third party digital macro libraries (commercial or radiation-hardened; development/qualification state)
- IO Pads (Voltage levels, ESD, EMC, ...)
- Manufacturing spread (power consumption, clock frequency, leakage)
- Accuracy of the models
- Development tool flow supported
- Sign-off tool chain

iv. Analogue Performances

The questions related to analogue performances features have been:

- Analogue IO Pads (Voltage levels; ESD; EMC; ...)
- Number of poly layers
- Sub-threshold conducting model
- Accuracy of the models
- MOS transistors availability
- Bipolar transistors availability
- Diodes availability
- Passives availability
- Development tool flow supported
- Sign-off tool chain
- Foundry or Third-Party analogue macro libraries (commercial or radiation-hardened; development/qualification state) and their support

Table 1 summarizes the list of contacted foundries and the corresponding 18 processes analyzed (processes which require manufacturing steps in USA have been excluded from the analysis due to the resulting ITAR export restriction which may be implied for space applications):

Table 1: Foundry processes analysed.

Foundry	Process	Process Features
Austria Micro System	C35B4C3	0.35um
	H35B4D3	High Volt. 0.35um
	C18	0.18um
	H18	High Volt. 0.18um
ATMEL	AT77.9K	High Volt. 0.15um
	AT58K85	High Volt. 0.15um
IHP Microelectronics	SGB25RH	0.25um
	SG13RH	0.13um
ON-Semi	C3/D3	0.35um
	C05	0.5um
	I3T25	High Volt. 0.35um
	I3T50	High Volt. 0.35um
	I3T80	High Volt. 0.35um
Telefunken	TFSMART1-HV	High Volt. 0.8um
	TFSMART2	High Volt. 0.35um
XFAB	XH035	High Volt. 0.35um
	XH018	High Volt. 0.18um
	XT018	High Volt. 0.18um

B. Second Survey: Agency and Space Community Needs

The survey has been addressed to the space community in order to collect feedbacks covering the needs of mixed-signal ASICs for the planned missions.

Twenty-eight (28) companies have been contacted, collecting eighteen (18) compiled surveys.

C. *Third Survey: Investigation about Comparable Activities*

To avoid to duplicate the effort and in order to harmonize and coordinate with on-going existing activities, a third survey addressed to the space community has been prepared to collect information about the existing rad hard libraries and design kits in terms of primitive

devices, SEEs, TID and reliability performances. The questions have been grouped in the four (4) sections: Primitive Devices, Single Event Effects Test, Total Dose Ionization Test and Reliability Test

i. Primitive Devices

- Funding mechanism used for rad hard libraries development (self-funding, public funding, private funding, etc.)
- Availability free of charge of the results (libraries, design-kits,…) for scientific research
- List of scientific papers published about the performances of Rad Hard libraries
- Technology process used to develop the Rad Hard libraries
- List of primitive devices with increased radiation tolerance
- For each primitive device, list of updated parametric cells (symbol and layout view)
- List of the violated design rules, accepted by the foundry
- List of modification on the fabrication process
- List of the modification on the design and layout-versus-schematic rules taking into account the modifications on primitive devices
- List of the modified primitive devices model
- List of analog simulators supported by these new models
- List of digital libraries developed based on this library
- Type of characterization performed on digital libraries

ii. Single Event Effects

- List of test(s) to evaluate the Single Event Effects
- Description of manufactured test vehicle/custom ASIC for SEE characterization/modeling
- Parts or devices included in the test vehicle
- Parts or devices not included in the test vehicle
- Parts or devices tested
- Heavy ions or protons source has been used
- Description of heavy ions/protons cocktail and LET used
- List of primitive devices tested against SEE
- Measured performances in terms of SEL, SEU, SET, SEB, SEGR, SEFI
- Test procedure used (i.e. ECSS 25100)
- Description of the SEE test by laser
- SEE performances obtained with laser test
- Description of simulation model to take into account the SEE effects
- List of analog simulators supported by these new models

iii. Total Dose Ionization Test

- List of test to evaluate the performances in terms of Total Ionization Dose (TID)
- Description of manufactured test vehicle/custom ASIC for TID characterization/modeling
- Parts or devices included in the test vehicle
- Parts or devices not included in the test vehicle
- Parts or devices tested
- Description of the source used
- Final TID accumulated
- What was the dose rate?
- List of primitive devices tested against TID
- Test procedure used (i.e. ECSS 22900)
- Description of simulation model to take into account the TID effects
- List of analog simulators supported by these new models

iv. Reliability Test

- Description of reliability test performed on the library
- Description of the obtained results

III. Analysis of Surveys

In the next figure haves been summarized the main results extracted from the three (3) surveys.

Figure 1 summarizes the preferred mixed-signal foundries expected to be used for future ASIC manufacturing;. Figure 2 -Figure **7** summarizes the users preference with respect to The process gate length, the technology lifetime, the operational temperature range, the TID and the SEE performances expected from technologies for development of mixed signal ASIC for space applications.

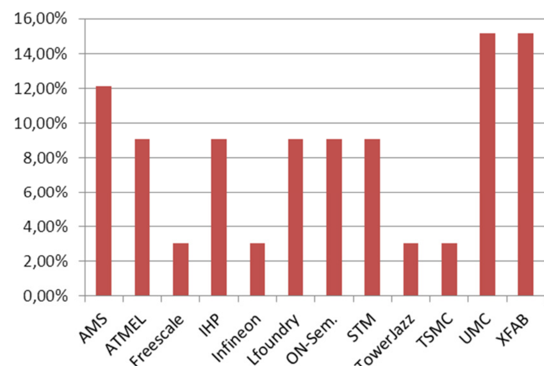

Figure 1: Preferred mixed-signal ASIC foundries.

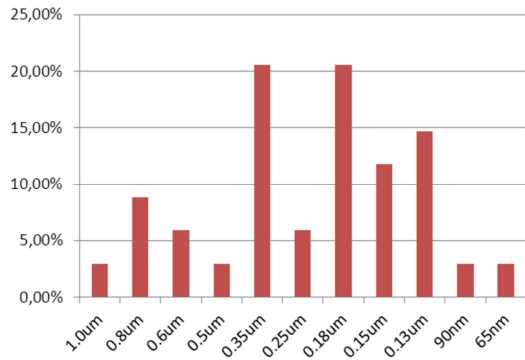

Figure 2: Preferred mixed-signal ASIC process gate length.

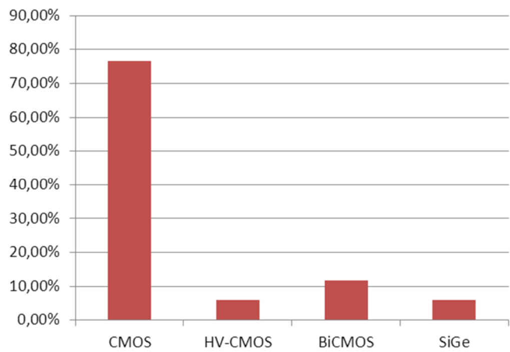

Figure 3: Preferred mixed-signal ASIC technologies.

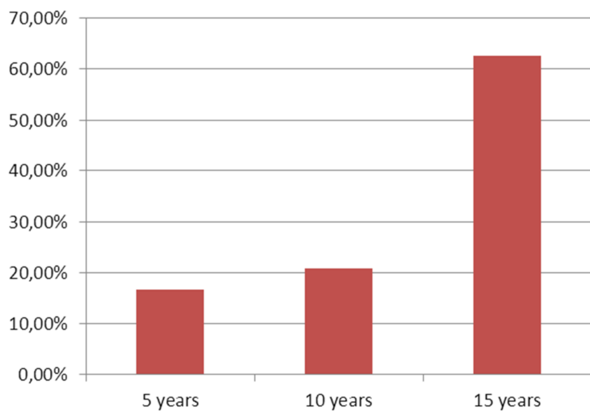

Figure 4: Expected technology's lifetime.

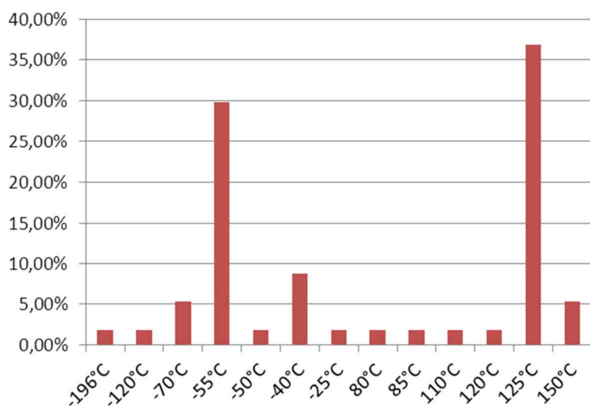

Figure 5: Expected operational temperature range.

Figure 6: Expected TID performances.

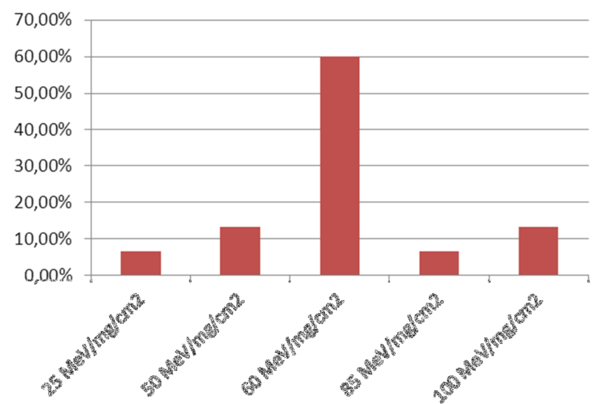

Figure 7: Expected SEE performances.

From Figure 8 to Figure 12 the expected performances and requested features to the preferred mixed signal technologies for the digital devices is shown, such as the I/O and digital core power supply, the number of metal layers, the digital output pad current capability, the toggle rate and the memories type needs.

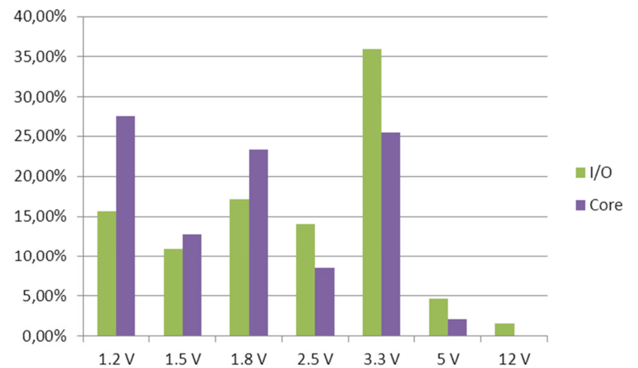

Figure 8: Expected I/O and digital core power supply.

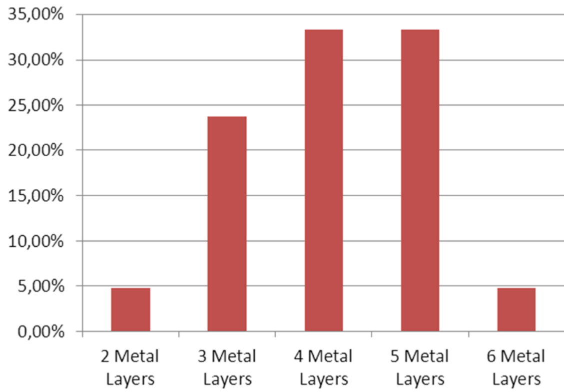

Figure 9: Expected number of metal layers.

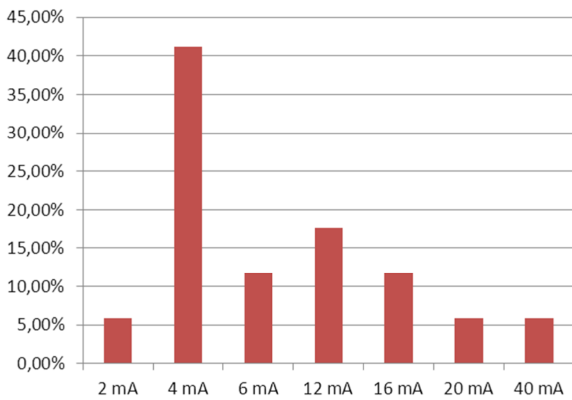

Figure 10: Expected digital pad output current capability.

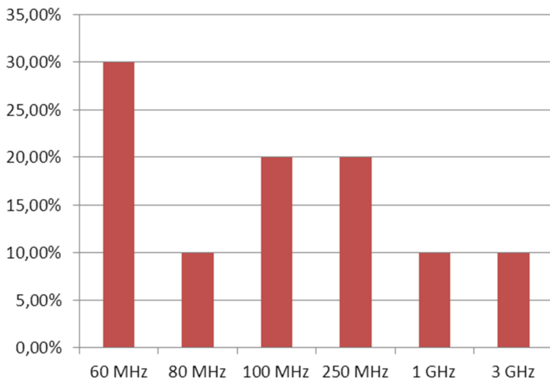

Figure 11: Expected toggle rate.

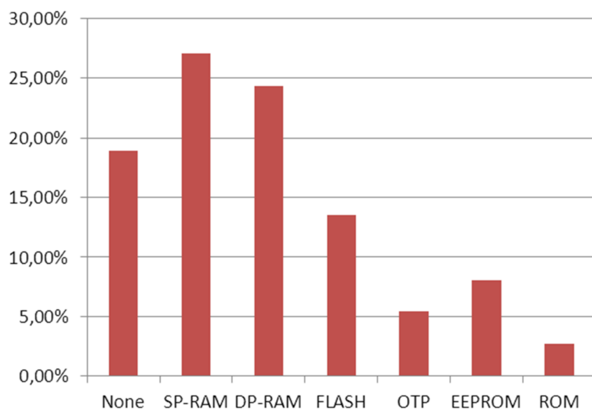

Figure 12: Expected memories type need.

From Figure 13 to Figure 18 the expected performances and features requested to the preferred mixed signal technologies for the analogue devices is shown, such as the analogue core power supply, high voltage needs, the primitive devices availability, the F_{MAX}, F_T and beta (for bipolar primitives) expected and the preferred analogue IP cores availability.

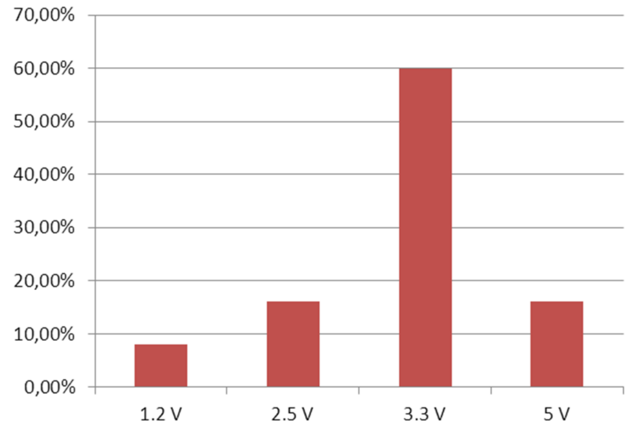

Figure 13: Expected analogue core power supply.

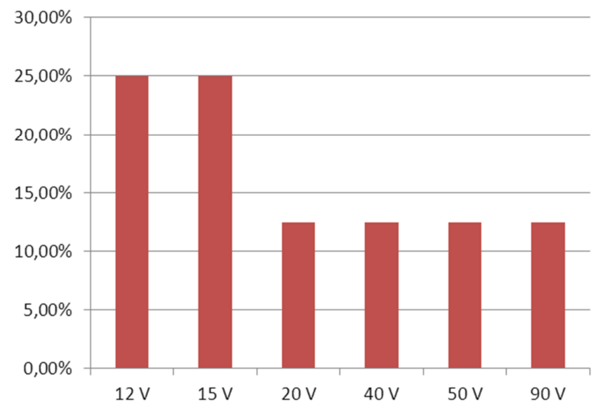

Figure 14: Expected High Voltage capability.

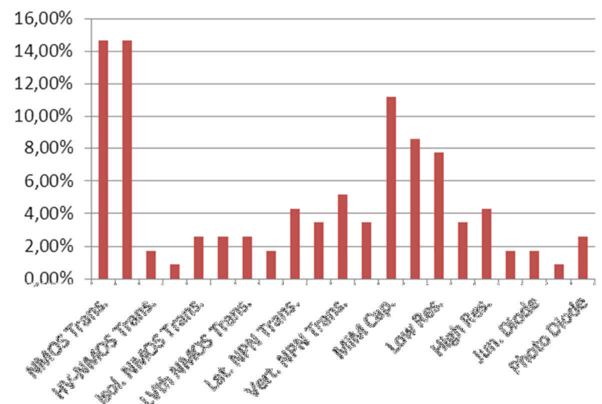

Figure 15: Expected primitives availability.

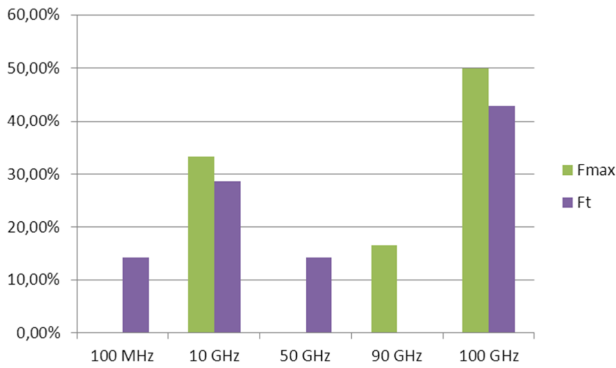

Figure 16: Expected FMAX and FT.

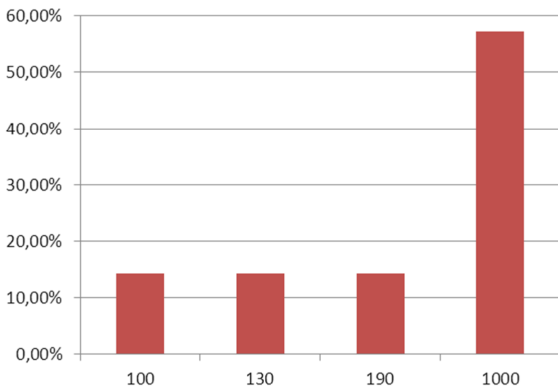

Figure 17: Expected beta values for bipolar transistor.

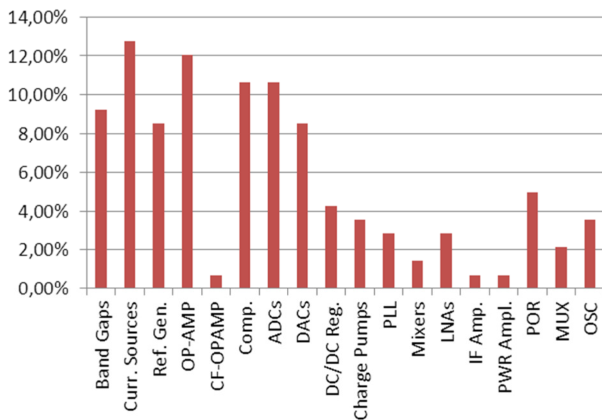

Figure 18: Expected analogue IP cores availability.

Analysing the data shown in the previous figures has been deduced that the features requested are mainly:

- Gate length of 0.35um or 0.18um (they can cover almost the 50% of need)
- CMOS technology with bipolar and high voltage option and with 15 year of lifetime
- Operational temperature range from -55°C to +125°C
- A 100Krad of TID limit can cover more than 50% of needs as well as a LET of 60MeV/mg/cm^2 it is enough for 60% of applications
- The 1.2 V, 1.8 V and 3.3 V of digital core power supply cover the most applications whereas the 3.3 V is the most requested for the I/O pads
- Technologies with up to 5 metal layers, with output pad with 4 mA of current capability and toggle rate below 250 MHz can cover the main applications
- Beside the static RAM (single or dual port) considerable importance is the availability of nonvolatile memory availability such as Flash.
- For analogue domain a technology with a 3.3 V of core power supply and up to 50 V of high voltage capability appears to cover the needs of most applications

The figures below summarize the conclusions reported above giving a grade of coverage of the needs against the features of technologies process analyzed; the values have been calculated by a weight average, taking into account the requirements, the grade of needs and the process features. Parameters like cost, qualification, MPW runs per year, … have not been taken into account.

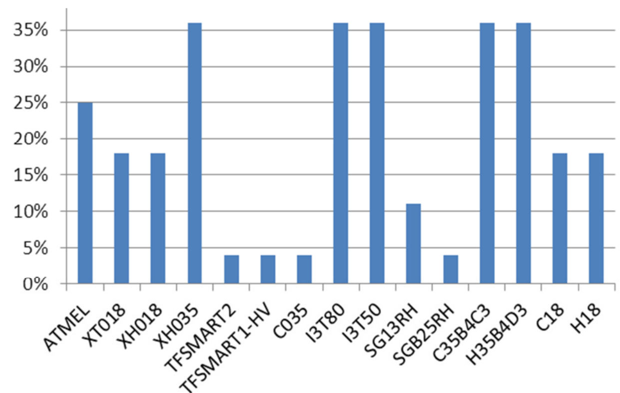

Figure 19: Coverage of the required process gate lengths.

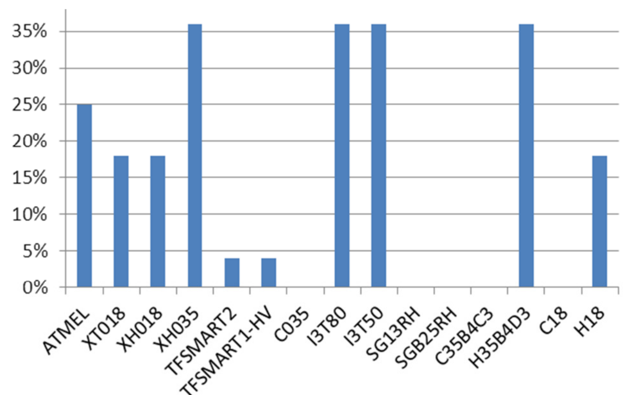

Figure 20: Coverage of gate lengths and HV requirements.

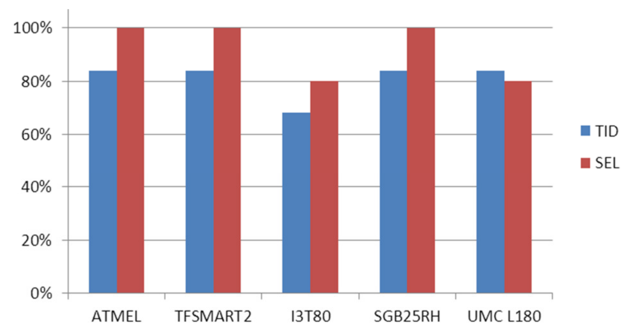

Figure 21: Coverage of the TID and SEL performances (the UMC L180 process has been introduced as reference).

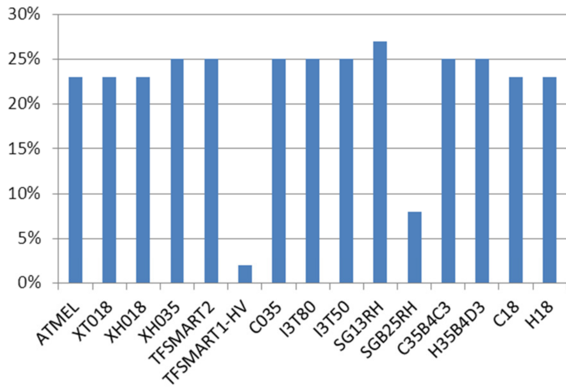

Figure 22: Coverage of the required core digital power supply.

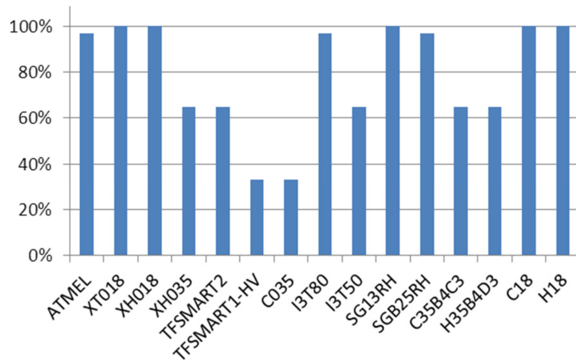

Figure 23: Coverage of the number of requested metal layers.

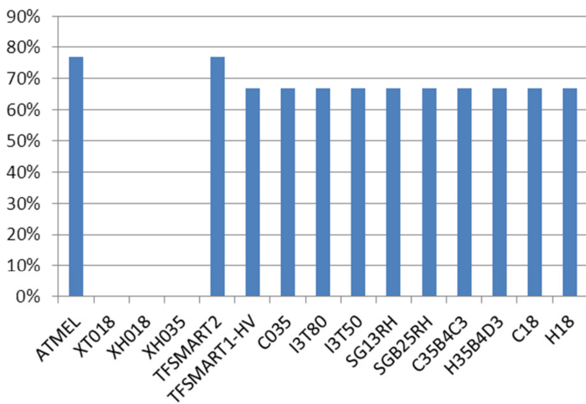

Figure 24: Coverage of required speeds.

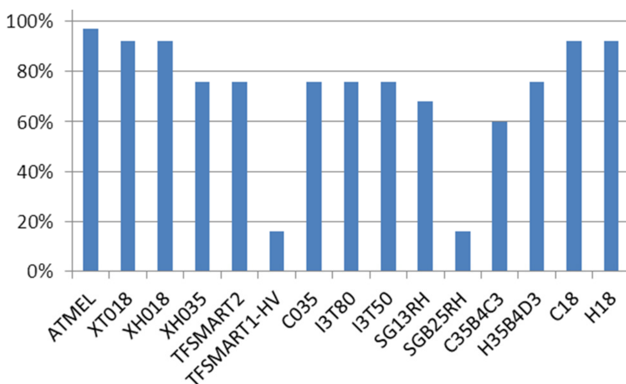

Figure 25: Coverage of the required analogue core low-range power supplies.

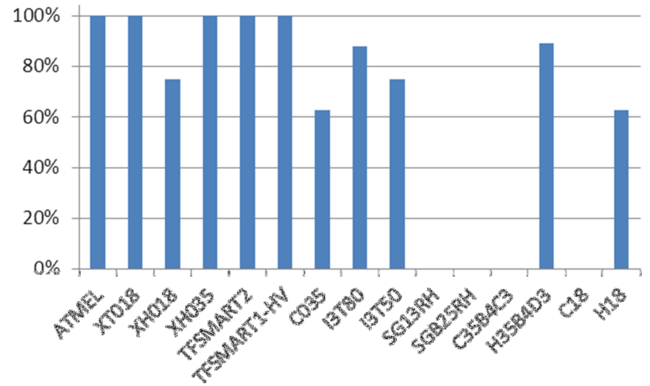

Figure 26: Coverage of the required analogue high voltage-range power supplies.

The availability of a process with High Voltage (HV) capability was a key requirement in order to meet the growing demand for HV power devices. Up to now no HV process has been submitted to a complete space qualification campaign, even if, for some technologies, this activity is planned for future or it is in development status.

Another important aspect to take into account for the process technology selection is the availability of Non Volatile Memory (mainly FLASH memories but also EEPROM). The status of NVM availability for mixed signal technology selected is reported in Table 2:

Table 2: NVM availability status.

Foundry	Process	NVM
Austria Micro System	C35B4C3	EEPROM FLASH
	H35B4D3	EEPROM
	C18	N/A
	H18	N/A
ATMEL	AT77.9K	EEPROM
	AT58K85	EEPROM
ON-Semi	C05	EEPROM
	I3T50	EEPROM
	I3T80	EEPROM
Telefunken	TFSMART1-HV	N/A
	TFSMART2	N/A
XFAB	XH035	EEPROM
	XH018	EEPROM FLASH
	XT018	N/A

By taking the conclusions from above, following main technology requirements for a mixed signal ASIC technology has been concluded:

- HV analog core capability
- NVM capability
- RH digital libraries, or analog/mixed signal RH IP, or analog PDK already developed or in development status or planned for future work

Based on the review of the data collected by the questionnaires and by consideration that several ESA and national Space Agencies activities are currently on-going or

have been completed on various technologies (e.g. ATMEL mixed signal processes are being characterised in the frame of a different project) the following candidate short list for the execution of the characterisation work planned in the phase 2 of this ECI activity has been concluded.

Table 3: Foundry process short list for phase 2

Foundry	Process	NVM
Austria Micro System	H35B4D3	EEPROM
ON-Semi	I3T80	EEPROM
XFAB	XH018	EEPROM FLASH

As mentioned above, due to the higher digital density capability, a 0.18µm process is expected to cover more application needs as compared to a 0.35µm process, XH018 has been chosen for the characterization activities planned in the second phase of this ECI contract.

IV. Description of Test Vehicle

As mentioned above, the second phase of this activity will focus on the characterisation of the selected process. The technology characterization test vehicle is currently being designed and will contain primitive devices and simple analogue circuits. For each devices type, the evaluation will focus on I-V and C-V curves extraction, noise characterization, end of life (EOL) test and Total Ionization Dose (TID) test. The Single Event Transient (SET) will be characterized in term of pulse width and charge injected by a test session based on pulsed laser. At the end of test campaign analogue models for simulations will be extracted in different condition (EOL, TID, SET,….) and they will be incorporated into the design-kit to allowing to designer a more accurate design and verification under critical conditions.

Since it is difficult to correlate the laser energy with the equivalent LET, heavy ion beam test for the selected technology devices are foreseen and are in preparation.

Currently heavy ion beam test for the selected technology devices are foreseen and are in preparation and it will be useful because the laser tests do not give indication whether the HV transistors survive the heavy ions. Moreover the heavy ion beam test will allow to know what charge injection is to be expected with LET because this information is not easily achievable with laser test.

V. Conclusions

In this paper foundry process appropriate for the manufacturing of mixed signal ASICs for space applications have been assessed.

The investigation has been driven by three (3) different surveys addresses respectively to European foundries, space community and companies and design centre involved in similar activities.

A candidate short list for the execution of the characterisation work planned in the phase 2 of this ECI activity has been concluded based on the results and analysis that was performed. Finally a brief description of the test vehicle for the technology characterization has been presented.

Of course different requirements and emphasis might affect the outcome.

VI. Acknowledgements

The authors wish to thank the companies and research laboratories for their precious contribution on the data collection.

VII. References

[1] Proceeding of 4th International Workshop on Analogue and Mixed-Signal Integrated Circuits for Space Applications (AMICSA) August 26 – 28 ESTEC - Noordwijk - The Netherlands

[2] Analogue & Mixed-signal ASIC Technology Requirements and Priorities of Space Industry Users: round table of 4th International Workshop on Analogue and Mixed-Signal Integrated Circuits for Space Applications (AMICSA) August 26 – 28 ESTEC - Noordwijk - The Netherlands

[3] Proceeding of European Space Components Conference ESCCON 2013 March 12 – 14 ESTEC - Noordwijk - The Netherlands

Applications for Radiation Hardened Analogue and Mixed-Signal ASICs: Instrumentation Front-End

High performance analog Front End ASIC for interfacing with a Si Drift Detector and the control electronics – AMICSA 2014

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Abstract

In the frame of the LOFT (Large Observatory For x-ray Timing) program, a high performance analog Front End ASIC has been developed for interfacing with a Si Drift Detector and the control electronics.

The collaboration among IRAP, CNES and Dolphin Integration targeted an ASIC embedding 16 Analog Front Ends (AFEs,) a 12-bit ADC for digitization, DACs for the generation of the threshold for the minimum detectable event, low noise comparators, multipliers and the full digital interface used to control the AFEs and to read the measures. The ASIC was developed using the 180nm mixed technology of TSMC.

Keywords: ASIC, SDD, Xray, low power, low noise, CPA, shaper, LOFT, Analog Front End, mix signal, high performance.

I. Introduction

A. Context of the development of the ASIC

In the frame of the LOFT (Large Observatory For x-ray Timing) program, IRAP, CNES and Dolphin Integration have collaborated to develop a high performance ASIC (SIRIUS2) for interfacing Silicon Drift Detectors (SDDs, [13]) with the digital back-end

LOFT was candidate X-ray mission for the M3 slot of the Cosmic Vision program of the European Space Agency [10], [14]. It will be proposed again for the M4 mission. The LOFT objectives are to study the neutron star structure and equation of state of ultra-dense matter and to explore the conditions of strong-field gravity.

The primary enabling technology for the Large Area Detector (LAD) is the SDDs developed for the Inner Tracking System in the ALICE experiment of the Large Hadron Collider at CERN, by scientific institute INFN Trieste, Italy.

The project targets a 10 m² detector array for 2 to 80 keV Xrays detection at high sensitivity (50 – 200 eV) and good energy resolution (limited by electronic noise, itself limited by EOL detector leakage current) with a dead time << 1% at 1 Crab.

Such system will require 500 k to 600 k SDD detectors managed by 35 k to 40 k ASICs.

In Figure 1, the LAD and WFM (Wide Field Monitor) instruments are shown (The instrument design is described in detail in reference [10] and [11]).

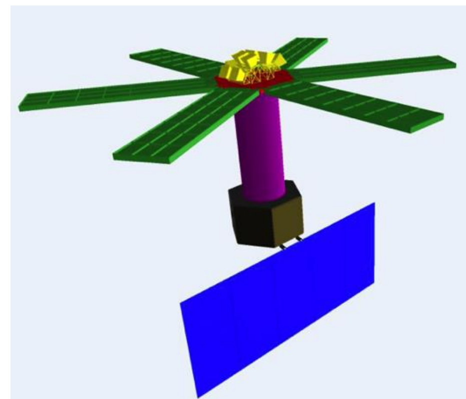

Figure 1: Loft payload in its original M3 proposal configuration. At the top the 6 panels of LAD (10 m2 effective area) and in the center the 6 cameras of WFM: green = LAD, yellow = WFM, red = Optical bench, purple = Structural Tower.

B. Interfaces with SDD and Module Back End Electronics

A LAD detector has 112 anodes on each side. 16 detection chains are implemented in each ASIC to fit with the size and the number of anodes of the detector

14 ASICs are glued on the rear side of a panel (seven per detector side). The Figure 2 shows the rear of a panel detector.

The ASIC control/test pads are bonded to the PCB, and the sixteen inputs directly to the SDD anodes, to reduce as much as possible the capacitance of the bonding's and so minimize the induced noise.

Each ASIC communicates through SPI like interface with a Module Back End Electronics (MBEE). A trigger line is provided to indicate that an event has occurred. An internal register (trigger map) indicates which anode is hit. This trigger is provided to the adjacent ASICs in order to hold and then read the 16 ASICs for noise measurements and common mode correction.

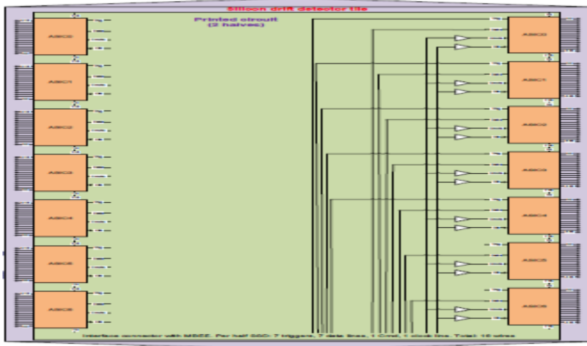

Figure 2: One panel of SDD and the 14 ASICs.

C. *Performance requirements*

The project started in 2012 targets the development of a first testchip (SIRIUS1) for the validation of the analog performances in a first phase and the development of the ASIC embedding all required functionalities (SIRIUS2) in a second phase.

SIRIUS1 embedding 8 Analog Front Ends (AFEs) was developed using the 180nm mixed technology of TSMC.
SIRIUS2 content has been extended for ASIC version with 16 Analog Front Ends (AFEs,) a 12-bit ADC for digitization, DACs for the generation of the threshold for the minimum detectable event, low noise comparators, multipliers and the full digital interface used to control the AFEs and to read the measures. The ASIC was developed using the 180nm mixed-signal technology of TSMC.
The challenging performances of SIRIUS1/SIRIUS2 are the energy resolution of 200eV @ 6keV (requiring a very high performance in term of noise corresponding to an ENC of 17 electrons end of life of the SDD), the very low power consumption (lower than 650 µW/channel) and a full scale higher than 22200 electrons.

The electrical requirements of SIRIUS1/SIRISU2 are summarized in the Table 1.

Main requirements impacting the design of the analog Front End of SIRIUS1/SIRIUS2

Item	State-of-the-art 2012	SIRIUS requirements
Input charge range	500 eV – 50 keV	200 eV – 80 keV
ENC (at -30°C)	< 30 electrons rms	< 20 electrons rms
EOF leakage current of the SDD	< 2 pA	< 10 pA
Shaping peak time	1-10 µs programmable	2-8 µs programmable
ADC resolution	9-10 bits	13 bits
Dead-time	Not available	0.7 %
Baseline restoration	Not available	50 µs

In term of radiation challenges, the total radiation dose expected on the LOFT orbit is low (1 krad), so a standard technology was used with design precautions. Indeed, the ASIC was designed using layout mitigation techniques to reduce the SEU effects and to increase the LET (the LOFT requirement is LET > 60 MeV):

- guard ring around the various functions
- ring of the opposite polarity around transistors when NMOS and PMOS transistors are close
- increased distance of active zone from the pads when they are connected to a pad
- maximized the number of contacts and vias
- differential design and differential routing
- optimized the matching (by reducing the size of the basic elements if necessary)
- avoided using the polysilicon for routing

The Figure 3 shows the detail of the layout mitigation techniques.

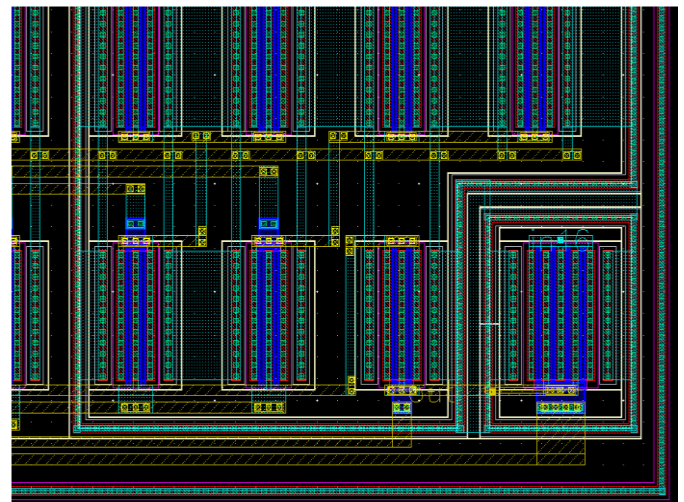

Figure 3: Detail of the layout showing the rules (rings) used to reduce the susceptibility to latch-up.

II. SIRIUS1/2: AFE ARCHITECTURE

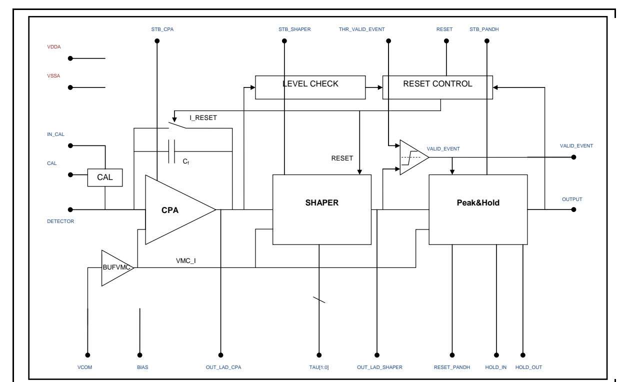

Figure 4: Detection Analog Front End (AFE) diagram

In terms of analog design, since the SDD delivers current pulses of low intensity and short duration, the AFE uses an integrator to accumulate the corresponding charge in a capacitor to deliver the resulting voltage output. This structure

is called a charge preamplifier, and will be noted CPA here below.

In order to add gain and improve signal to noise ratio, the CPA is usually followed by a pulse shaper, working as a matched filter.

The output of the CPA plus the shaper is a voltage pulse. Depending on the application, this pulse is either compared to a threshold and sent to an event counter, or sampled and digitized. In order to capture the energy of the Xray events, it is required to detect the pulse maximum and hold the voltage by a Peak and Hold, or P&H here below.

The Figure 4 provides an overview of the AFE architecture.

D. CPA design

The choice of the architecture of the CPA was driven by the noise performance which had to be lower than 20 e^-.

The Figure 5 describes a resistor based CPA. The effects of the resistance on noise and recovery time have been analyzed. As expected from theoretical analysis, noise is inversely proportional to feedback resistance (curves at 1 to 100 GΩ).

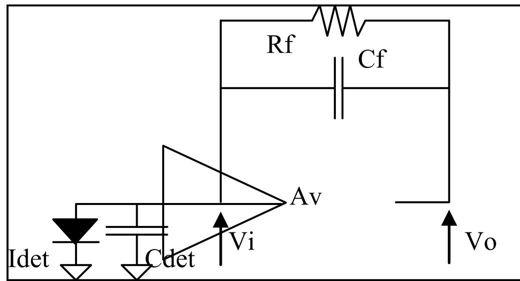

Figure 5: Resistor based CPA

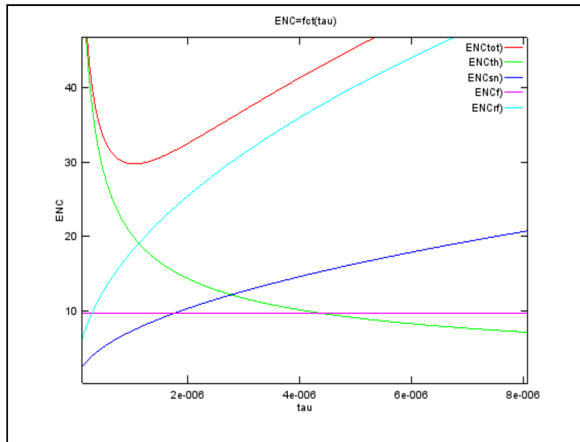

Figure 6: Simulation showing the noise performance as a function of τ with a resistor of 1.5 GΩ (10pA SDD leakage, τ in s). ENC_{tot} (red) is the square root of the sum of the square of the various ENC (ENC_{th}: CPA thermal noise, green; ENC_{sn}: shot noise due to detector, blue; ENC_f: 1/f noise, violet).

The Figure 6 represents total noise (red), thermal noise of CPA (green), 1/f flicker noise from preamplifier (blue-green), Rf thermal noise (light blue) and detector noise -at end of life worst case leakage current of 10 pA- (dark blue).

$$ENC_{tot} = \sqrt{\left(ENC_{th}{}^2 + ENC_{C_f}{}^2\, ENC_{sn}{}^2\, ENC_{R_f}{}^2\right)}$$

As shown in Figure 6, simulations and computations prove that a 1.5 GΩ resistor is not sufficient to keep noise within the specifications: it is mandatory to select a CPA structure without a feedback resistor. The Figure 7 provides the noise performances for a reset-based CPA: the noise performances are achievable!

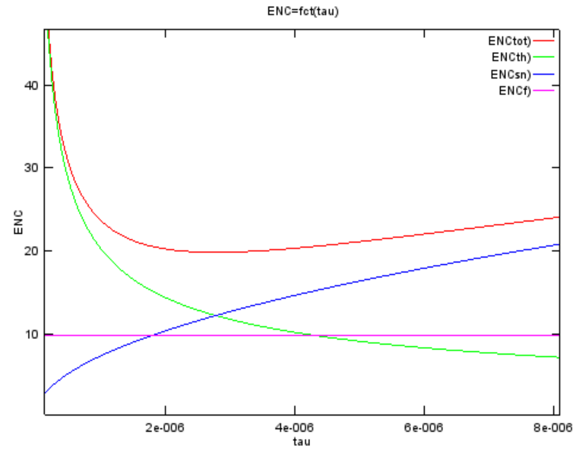

Figure 7: Simulation showing the noise performance as a function of τ without resistor (switched reset, 10pA SDD leakage, τ in s).

A reset circuit has been used to restore the base line after each event and when the baseline drift is such that a threshold is reached. A capacitor is used to inject charges for calibration purpose (see Figure 8).

Minimal gain Av is 60 dB worst case.

Power consumption target is 250 µW worst case.

Gain feedback capacitor is 75 fF: this is the best trade-off between signal gain and fast recovery (which requires low capacitance) and reset rate (which claims for larger capacitance).

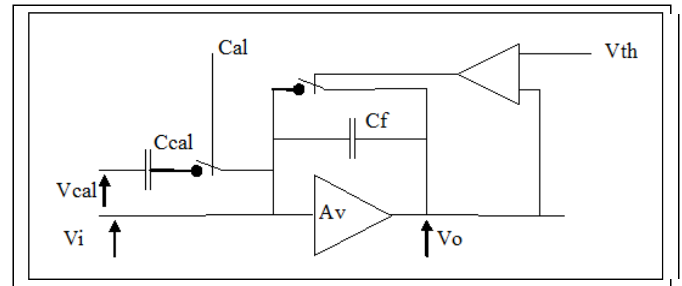

Figure 8: CPA architecture.

A. Shaper design

Pulse shaper is a single ended simple RC-CR^2 semi Gaussian filter (see Figure 9). Inverting configuration allows for a simple common mode voltage buffer with low drive requirements. The time constant is set by a switched network capacitors and selection logic. This allows maintaining the input impedance (at high frequency) identical regardless of time constant τ.

Gain settings: n1 = 8 and n2 = 5.

This is achieved with R = 125 k W and C = 8pF at t = 1 µs (C1 = 64 pF).

Offset is less than 5 mV per amplifier.

Time constant is programmable between 1µs and 4 µs.

Power consumption target is 200 µW worst case.

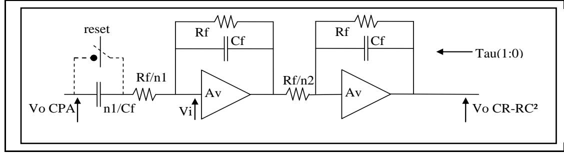

Figure 9: SHAPER architecture.

E. Peak&Hold design

The P&H is based on a peak detector and switched capacitor based hold amplifier (see Figure 10). Peak detection is performed by voltage derivation and zero detection, and for best performance, separate Peak and Hold functions are used. The feedback capacitor is selected according to Tau value to optimize the detection.

A 5 pF hold capacitance Ch provides good noise and retention performances at reasonable power consumption (target: 150 µW worst case).

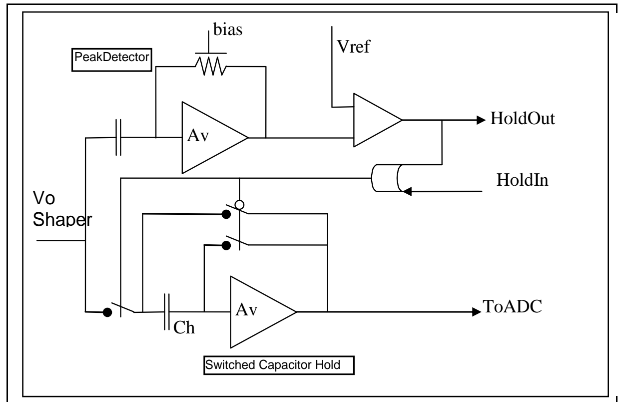

Figure 10: Peak&Hold architecture.

A. SIRIUS2: ASIC architecture

The ASIC version (SIRIUS2, Figure 11), jointly developed by IRAP and Dolphin Integration, is a fully functional version implementing all the functionalities required for LAD-LOFT: various controls capabilities and serial interface with the Front End Electronics, size and pitch for LAD, 16 channels, PGA and 10/12/14 bit ADC, threshold control (16 x 8 bit DACs), calibration DAC (5 bit), reference band gap and internal test feature. The topology of the ASIC was also changed with all detector inputs placed at one side of the chip and the control on the opposite side to comply with size of the SDD and to reduce the coupling between digital section and low level signal sections.

No improvement of the analog section (analog chains) has been added due to the short time before the ESA M3 selection.

The ASIC prototype will be used to perform radiation tests, aimed at qualifying the ASIC design and technology for TID and Latch-up.

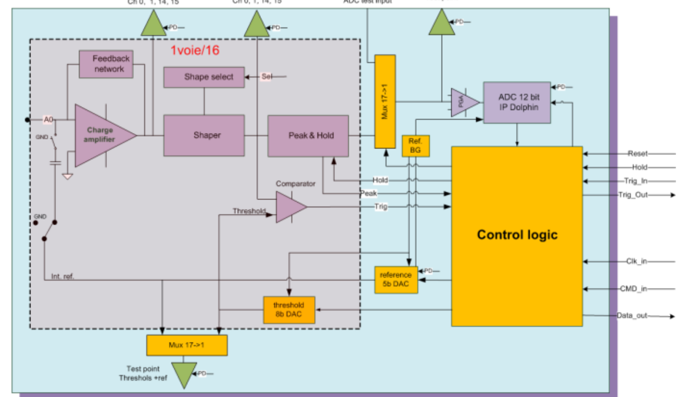

Figure 11: Functional block diagram of the SIRIUS 2 ASIC designed by IRAP and Dolphin. Orange colour indicates the functions designed by IRAP

B. SIRIUS1: Measurements

The SIRIUS1 testchip was tested alone at IRAP, Toulouse and with the SDD detector at INAF/IASF, Bologna, Italy. The test tools use modules installed in a PXI Express Chassis: controller with 16 bit Digitizers, Virtex 5 FPGA and Multi bank multiplexer (Figure 12 and Figure 13)

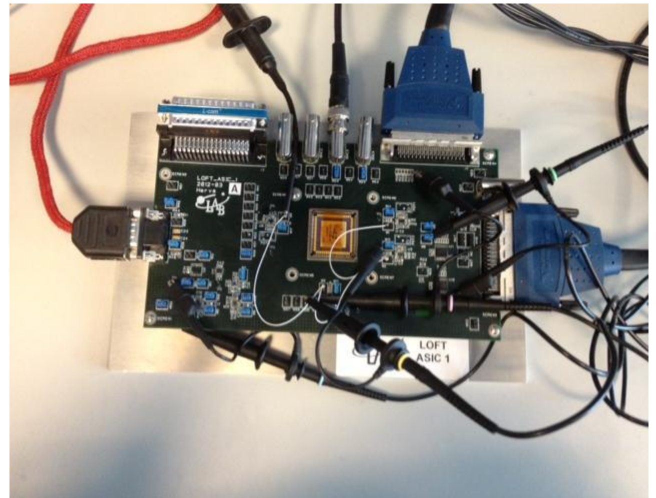

Figure 12: Test board for SIRIUS1

Figure 13: Test bench for SIRIUS1

The testchip was powered by an external power supply that provides +5V for the test board electronics. Linear regulators provide the 3.3V to the digital I/0's of the testchip. A low noise power supply provides the 1.8V to the internal analog and core digital electronics of the ASIC. It is possible to power or switch off independently the bias circuits, the 8 CPA's, the 8 Sampler's, the 8 Sample & Hold's and the 12 buffers. We measured (Figure 14) at each temperature, the power consumed by the 8 analog chains (buffers off). The power is lower than the expected from simulations and within specifications.

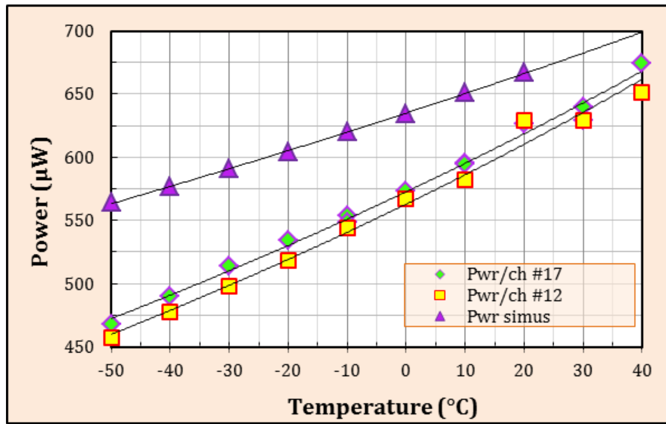

Figure 14: Measured power consumption of 2 ASIC versus temperature (green lozenge and yellow square) compared to post layout simulations (purple triangle)

We used the testchip built-in capacitor to inject a charge at the input of the CPA. For each injection 1000 measurements are made of the hold voltage using a 24-bit ADC. The mean value is calculated to minimize the noise due to the test equipment. One thousand identical charges are injected for each injection level. The mean value of the output voltage is computed and the sigma of the distribution of the 1000 measurements. The value of noise is computed from this sigma value. It is not varying much according to the injected level. We repeated the same measures at various temperatures (see Figure 15). The ENC is decreasing with the temperature to reach 16.5 e- below -30°C.

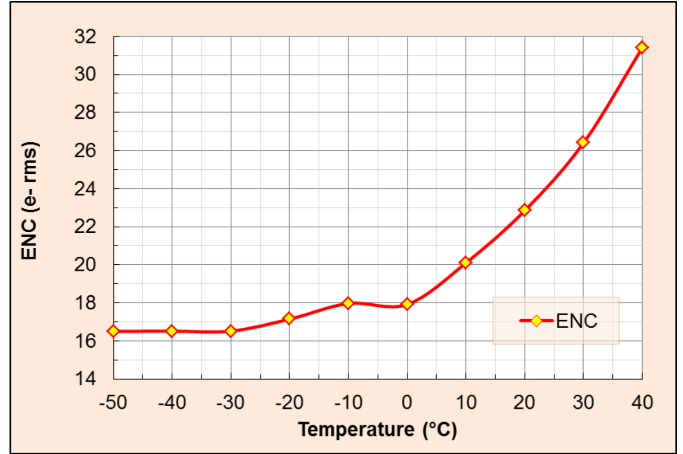

Figure 15: Variation of the noise of the ASIC alone, versus temperature the post-layout simulations provides the following performances: 27.3 e- @ +25°C and 13 e- @ -30°C

The performances in term of noise, power consumption and linearity meet the specification (see Table 2) and the excellent correlation with the simulations permit to have a good predictability of the performances of the 40 k ASICs

Measurement at room temperature

Item	Specification	Simulations	Measurements
Power consumption (in µA)	360	325	317
AFE noise (in e-)	< 30 e-	23 e-	22 e-
Linearity (in %)	< 1 %	< 1 %	< 0.5 %

C. Test with the SDD

Figure 16: Test board

Figure 16: the SDD Detector is in the middle. On the bottom of the detector (LAD side of the SDD), 4 SIRIUS1 testchip are bonded directly to the pads of the SDD, and on the top of the detector (WFM side), 2 other SIRIUS1.

Figure 17 and Figure 18: the resolution of the peaks, (see Fe-55 spectra) suffers for the charge sharing effect between two or three adjacent anodes that cannot be taken into account with this simple setup. The raw spectrum of a single channel acquired with the shaper signal includes not only the complete charge collection for one event, by the connected anode (single-anode events), but also the partial charge due to events impinging near the adjacent anodes. This is reflected in the tail on the left side of the peaks.

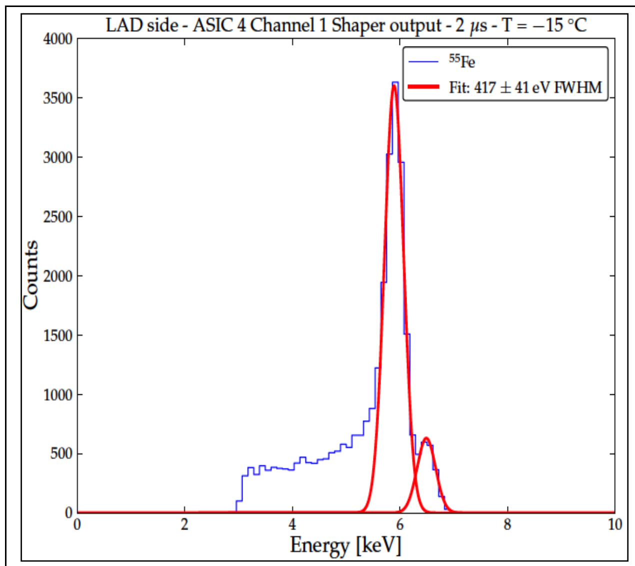

Figure 17: Spectrum measurement (^{55}Fe)

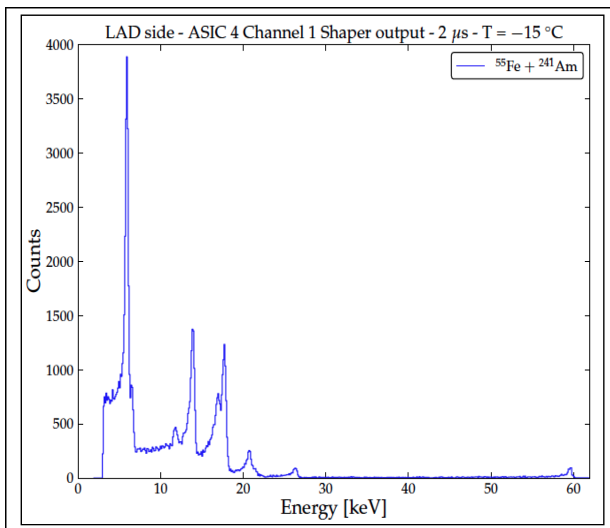

Figure 18: Spectrum measurement (^{55}Fe+^{241}Am)

D. SIRIUS2: Measurements

A High Density PCB (Figure 19 and Figure 20) has been developed to support the test of SIRIUS2: more than 50 bondings are necessary to feed the inputs/outputs; the 16 CPA input pads are not bonded and left unconnected. Low noise power supply regulators for the ASIC and the associated decoupling capacitors are installed on this board. A temperature sensor placed close to the ASIC is used to measure the temperature of the ASIC. It is readable through a SPI like protocol. The interface with the control PC is made through an Opal Kelly board plugged directly on the test board.

The characterization is in progress.

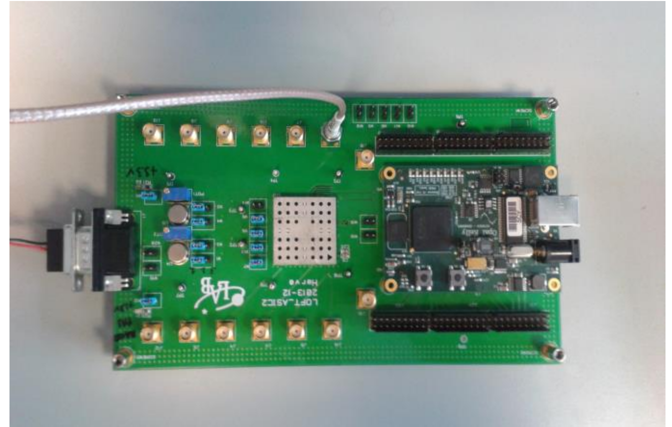

Figure 19: ASIC board

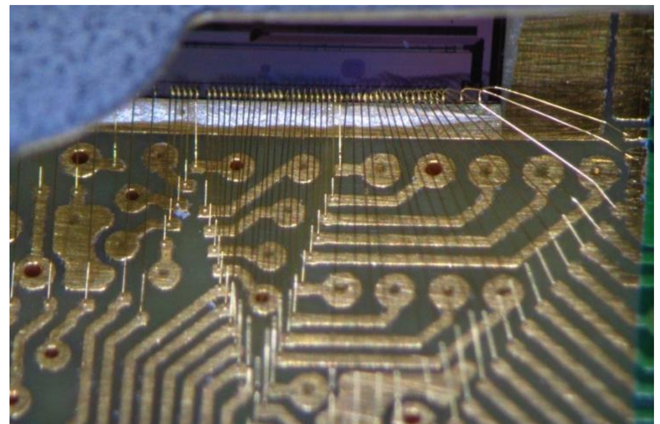

Figure 20: ASIC bonding

E. Conclusions

Two circuits (testchip + ASIC prototype) have been developed in 2 years demonstrating:

- State-of-the-art electrical performances in terms of noise of the Analog Front End
- Good team work between Dolphin Integration and IRAP to cope with the design, the characterization of the logic and mixed-signal blocks
- Mastery in controlling high performance analog blocks in terms of functionality and noise sensitivity to get compliance to the specifications
- Performances verified on silicon

REFERENCES

[1] Willy M.C. Sansen, Zhong Yuan Chang, "Limits of Low Noise Performance of Detector Readout Front Ends in CMOS Technology," IEEE transactions on circuits and systems, vol. 37, N°11, November 1990.

[2] Caccia, S., Bertuccio, G., Maiocchi, D., Malcovati, P., Ratti, N., Martin, D., "A Mixed-Signal Spectroscopic-Grade and High-Functionality CMOS Readout Cell for Semiconductor X-gammaRay Pixel Detectors," IEEE Transactions on Nuclear Science, Vol. 55, N°. 5, October 2008, p. 2721.

[3] Bastia, P., Bertuccio, G., Caccia, S., Cappelluti, I., Grassi, M., Malcovati, P., Martin, D., Ratti, N., "STARX32: A Complete On-Chip X-Ray Spectroscopy Readout System with Imaging Capability," AMICSA 2010, 5-7 September (2010).

[4] Singh, H., Dr. Sarin, R.K., Dr. Singh, S., "Analysis and Modeling of 1/f noise in MOSFETs for circuit Applications: The Joint Effect of Channel Length and Conducting Slab Resistance," Canadian Journal on Electrical and Electronics Engineering, Vol. 1, N°6, October (2010).

[5] Izadpanah, S., Gollmakani, A., "Three Stage Low Noise Operational Amplifier in 0.18m CMOS Process," ICSES proceedings (International Conference on Signals and Electronic Systems), 2012.

[6] Habid Muhammad Nazir Ahmad, Mohammad Shafquatul Islam, Arman Riaz Ochi, "Analysis of Ultra Wide Band Four stage Distributed Low Noise Amplifier in TSMC 0.18um Process," International Journal of Research in Computer Engineering and Electronics, vol. 2, issue 6, (Dec. 2013).

[7] Tsividis, Y., "Operation and modeling of the MOS transistor," McGraw-Hill, pp. 440-512, (1999).

[8] Bouyjou, F., "Nouvelles chaînes d'instrumentations intégrées multivoies pour l'astrophysique," These of Toulouse University, December 2011.

[9] Goulding, F. S., Landis, D. A., "Signal processing for semiconductor detectors," IEEE Transactions on Nuclear Science, Vol. NS-29, No. 3, June 1982.

[10] Feroci, M, et al., "The Large Observatory for X-ray Timing (LOFT)," Experimental Astronomy 34, issue 2 (2012) 415.

[11] Zane, S., et al., "The Large Area Detector of LOFT: the Large Observatory for X-ray Timing," SPIE proceedings, Montreal, 2014.

[12] Miller, J., "Dependence of the input impedance of a three-electrode vacuum tube upon the load in the plate circuit," Scientific Papers of the Bureau of Standards, Volume 15, 1919-1920, 330-368.

[13] Rachevski et al. 2014, SPIE proceedings, Montreal 2014.

[14] Feroci, M., et al. 2014, SPIE proceedings, Montreal 2014.

Radiation Hardness Tests of the CLARO-CMOS Chip: a Fast and Low Power Front-end ASIC for Single-Photon Counting in 0.35 μm AMS CMOS Technology

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Abstract

The CLARO-CMOS is a prototype ASIC primarily designed for single-photon counting with multi-anode photomultipliers tubes (Ma-PMTs). The chip features 5 ns peaking time, a recovery time to baseline smaller than 25 ns, and a power consumption at the order of 1 mW per channel. It was developed in the framework of the LHCb RICH detectors upgrade at CERN, but also found application in the readout of Silicon Photo-Multipliers (SiPMs) and microchannel plates. The prototype, realized in AMS 0.35 µm CMOS technology, has four channels, each made of a charge amplifier with settable gain (3 bits) and a comparator with settable threshold (5 bits) that allow tuning the response of the chip to the gain spread of the Ma-PMT pixels. The threshold can be set just above noise to allow an efficient single-photon counting with vacuum photomultipliers. In the readout of SiPMs, the threshold can be set above the single photon signals, allowing to count events with two or more photoelectrons with high efficiency and good separation of the photoelectron peaks. The CLARO-CMOS chip was fully characterized on the test bench. The chip was coupled to a Hamamatsu R11265 Ma-PMT, the baseline photon detector for the LHCb RICH upgrade, and was found able to read-out single-photon signals up to the maximum average rate expected in the LHCb RICH (~10 MHz) with a low power consumption (~1 mW) and a negligible crosstalk between pixels. In the LHCb RICH environment, over ten years of operation at the nominal luminosity expected after the upgrade in Long Shutdown 2, the ASIC must withstand a total fluence of about $6 \cdot 10^{12}$ 1 MeV n_{eq}/cm^2 and a total ionizing dose of 400 krad. A systematic evaluation of the radiation effects on the CLARO-CMOS performance is therefore crucial to ensure long-term stability of the electronics front-end. We present results of multi-step irradiation tests with neutrons up to the fluence of 10^{14} 1 MeV n_{eq}/cm^2, with protons up to the dose of 8 Mrad and with X-rays up to the dose of 8 Mrad. During irradiation, cumulative effects on the performance of the analog parts of the chip and single event effects (SEE) were evaluated. The chips were biased continuously and the chip threshold voltages were measured regularly, in order to detect possible single event upsets (SEUs) affecting the threshold DAC settings. Power consumption was also monitored online, and an additional circuit provided protection against Single Event Latchup (SEL). S-curves were measured before and after each irradiation step, to follow the evolution of counting efficiency, threshold shifts and noise during the irradiation.

I. Introduction

The capability to detect single photon signals is a requirement shared between several different applications. For instance, the Ring Imagining Cherenkov (RICH) detectors exploit the light emitted by relativistic charge particles crossing a suitable medium to provide their identification over a wide momentum range. Such detectors are extensively used in high energy physics experiments and, particularly, in the LHCb experiment at CERN.

An update of the whole LHCb detector is foreseen in 2018 in order to make it able to run at higher luminosity and sustain a proton-proton collision rate of 40 MHz [1]. Also the RICH detector will be updated and the currently used Hybrid Photon Detectors (HPDs) will be replaced by Multi-anode PhotoMultiplier Tubes (Ma-PMTs) coupled with an external wide-bandwidth read-out electronics [2]. The baseline photon sensor for the LHCb RICH Upgrade is the R11265 Ma-PMT, produced by Hamamatsu, which ensures an adequate spatial resolution thanks to the small pixel size (3×3 mm^2) [3][4]. The photon detector planes will consists of several thousands R11265 Ma-PMTs located side-by-side to minimize the dead area. This results in a high channel density which forces the read-out electronics to operate at very low power consumption. Indeed, the front-end electronics must be placed as near as possible to the photon sensors in order to minimize the stray capacitance between neighbouring channels or from the input node to ground which can lead to an increase of the cross-talk and noise, respectively.

The CLARO chip [5] is a custom designed ASIC realized in the 0.35 µm CMOS technology from Austria Micro Systems (AMS). The CLARO is able to read-out the R11265 Ma-PMTs fulfilling the LHCb RICH Upgrade requirements. Although a new improved 8-channels version of the chip has recently been designed (not described in this proceeding), the first versions of the chip are equipped with 4 channels with a 8-bits digital register each. The good chip performance led the LHCb collaboration to choose it as the baseline front-end device for the Ma-PMT read-out [2]. As the CLARO is supposed to be used in the LHCb environment, radiation hardness tests are needed to verify the radiation tolerance of the technology. Thus, some chips were irradiated with

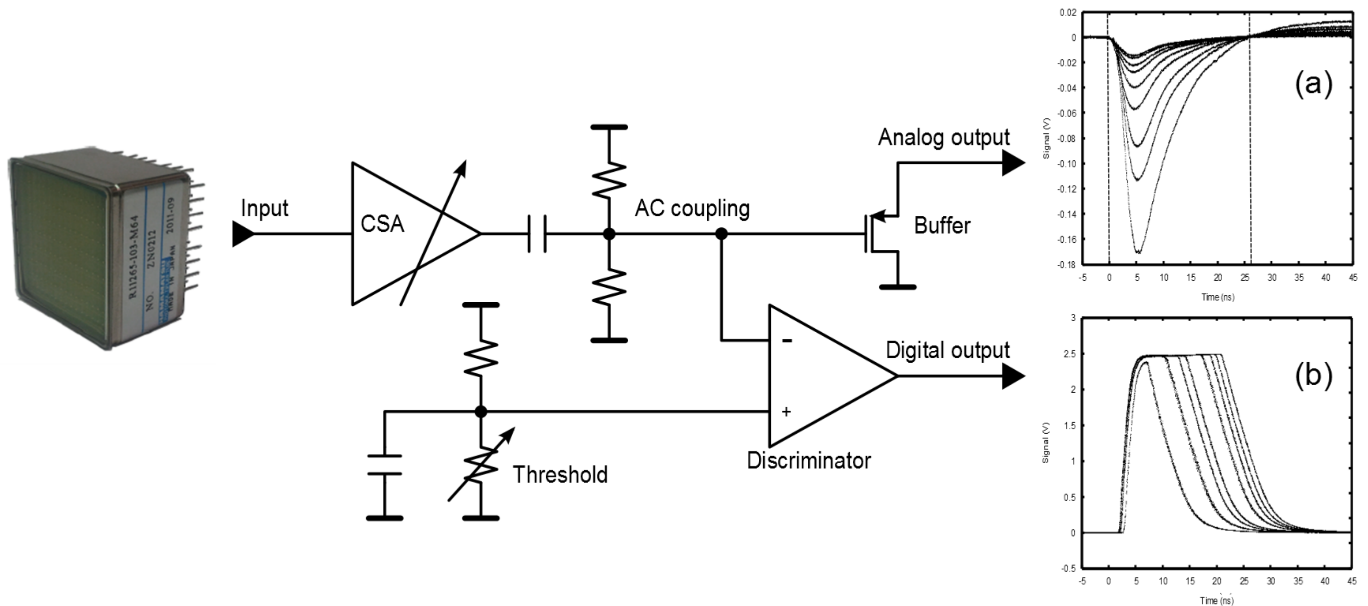

Figure 1: The block diagram of a CLARO CMOS channel. The typical analog and digital output signals are shown in figure 1.a and 1.b respectively.

neutrons, X-rays and protons so that the radiation hardness properties of several CLAROs could be studied in terms of both total ionizing dose (TID) and single event effects (SEE) [6].

A brief overview of the main chip features and of its performance is provided in Section II. The results of the radiation hardness tests are described in Section III.

II. The CLARO chip

As shown in the block schematic (Fig. 1), the CLARO chip is essentially composed of an input Charge Sensitive Amplifier (CSA) and a Discriminator.

When a photon hits the Ma-PMT surface, a photoelectron is emitted from the photocathode starting the charge multiplication over the 12 dynodes. The collection time of the photon detector is very small, of the order of 1 ns. Thus, the typical signal at the anode consists of a $\sim 1\ \mathrm{Me^-}$ current pulse which is injected at the input node of the CLARO.

The CSA provides the amplification and the shaping of the input current giving a proportional exponential shaped voltage signal at its output. The rise time constant (τ_R) of the CSA is of the order of 1 ns and is proportional to the input capacitance, while the fall time constant (τ_F) amounts to ~ 5 ns, large enough for an effective integration of the fast pulses but short enough to sustain high rates without pile-up. The CSA is AC-coupled with a PMOS follower buffer and with a discriminator stage which provide the auxiliary analog output and the main digital output respectively.

Fig. 1.a shows the superposition of the signals read from the auxiliary analog output (input charge ranging from $330\ \mathrm{ke^-}$ to $3.3\ \mathrm{Me^-}$). The PMOS follower buffer, which allows to read the CSA output signal without adding capacitance at this node, was externally biased with a 1 kΩ resistance. Note that this output is not meant to be used for single photon counting but only for debugging purposes. As observable, the baseline is not well restored since an undershoot occurs after the pulses. Such behaviour is due to the AC coupling between the CSA and the buffer (~ 55 ns) and can lead to a threshold shift at photon counting rate higher than ~ 10 MHz. This is the main reason why in the new version of the chip the AC capacitance was removed and a DC-coupled approach was chosen.

The analog signal coming from the CSA is also read by a discriminator stage which provides a digital pulse in case it crosses a programmable threshold level (32 values available). Fig. 1.b shows the superposition of the signals acquired from the main digital output with a threshold level of $800\ \mathrm{ke^-}$ and for an input charge ranging from $810\ \mathrm{ke^-}$ to $5.6\ \mathrm{Me^-}$. As observable, the width of the pulses is proportional to the input charge, a feature which allows to adopt the technique based on the time-over-threshold to compensate the time walk in case the CLARO is used for precise time measurements. However, even for input signals ten times larger than the threshold the FWHM of the digital output signals is lower than 25 ns so that rates of 40 MHz can be sustained avoiding pile-up. As mentioned, each channel is equipped with a 8-bit register, similar to a SPI interface, which permits to select the CSA gain (3 bits, 8 values available) and the threshold level (5 bits, threshold step $150\ \mathrm{ke^-}$).

Another requirement that the CLARO CMOS has to fulfill is the low power consumption. Despite its wide bandwidth, the power consumption in idle mode amounts to about 1 mW per channel and it stays below 2 mW per channel even at a photon counting rate of 10 MHz. This ensures a low heat injection in the most illuminated areas of the RICH detector, avoiding the need for front-end cooling.

As mentioned, in order to ensure a suitable rise time (few ns), the input capacitance should not exceed few pF. Moreover, the series noise of the preamplifier is proportional to the input to ground capacitance, as shown in fig. 2, where the equivalent noise charge is plotted as a function of the input capacitance. With the CLARO CMOS mounted in a small QFN48 package, the total input capacitance was measured to be ~3.3 pF, mainly due to the input bonding pad, the bonding wire, the package and the interconnects (the contribution of the photon sensor is not included). In this best case condition, the ENC turns out to be $\sim 7.7\ \mathrm{ke^-}$. Note that also the stray capacitance between the input nodes of neighbouring pixels has to be minimized since it would result in an increase of cross-talk. In particular, the stray capacitance between the input nodes of neighbouring channels has to be negligible with respect to that due to the Ma-PMT alone (~ 0.5 pF). The minimization of the input capacitance guides the design of the CLARO PCBs and it is one of the main reasons to keep low the number of channels per chip, so that

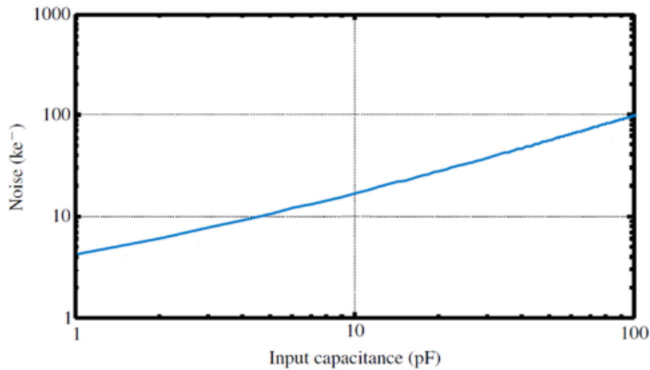

Figure 2: the input referred noise as a function of the input capacitance

the length of the traces connecting the pixels to the CLARO can be minimized.

In agreement with the LHCb Technical Design Review [2], the CLARO CMOS was chosen as the baseline front-end device for the read-out of the R11265 Ma-PMT for the LHCb RICH Upgrade. In addition to a deep characterization on the test benches, the CLARO CMOS performance was studied while reading the current signal coming from a R11265 Ma-PMT operating in single photon regime. Fig. 3 shows the superposition of single photon spectra acquired at different Ma-PMT biasing voltages. They are measured by illuminating the Ma-PMT with a LED and by counting the signal rates during a CLARO threshold scan. As it can be seen, the spectra look good and the signal to noise ratio is more than adequate since the single photon peak is clearly resolved. Moreover, the gain adjustment behaves as expected. Indeed, for analogous threshold step, setting a gain of 0.5 (points with a circular marker) the spectra are sampled with a double resolution with respect to the ones acquired using a gain of 0.25 (points with a x-cross marker). Anyway, in the last improved version of the CLARO CMOS, a finer threshold step is available in order to reach even higher resolution.

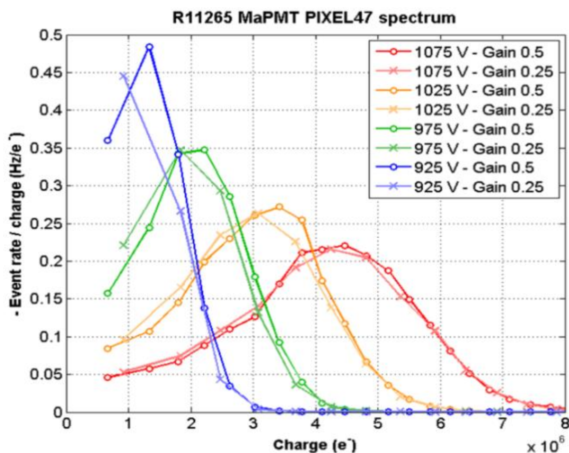

Figure 3: single photon spectra acquired by a R11265 Ma-PMT coupled with a CLARO CMOS chip.

III. Radiation Hardness Tests

All the electronic components which are supposed to be used in the LHCb environment have to pass the radiation hardness tests. Indeed, the radiation levels reached in the LHCb experiment could deteriorate the component performance in terms of Total Ionizing Dose (TID) and Single Event Effects (SEE). In order to ensure stable operation of the upgraded RICH detector over 10 years in the LHCb upgrade environment, a dedicated test of the CLARO performance under high radiation fields has been done.

Table 1 summarizes the radiation level expected in the LHCb Upgrade environment. The estimates are based on the worst case radiation level for a single proton-proton collision provided by M. Karacson [7] and assuming one year of LHCb operation (10^7 s), at a luminosity of $L=2\cdot10^{33}\,s^{-1}cm^{-2}$, with a proton-proton collision cross section of σ=84 mbarn. Note that the values shown in Table 1 do not include any safety factor and they could be affected by statistical fluctuations by a factor ~10-30 %. Furthermore, neither the final geometrical configuration nor the materials to be adopted are still completely defined and so they are not implemented in the current estimates.

Table 1: Radiation level expected per year in the LHCb RICH-1 and RICH-2 detectors

	Neutrons 1 MeV n_{eq}/cm^2	Hadrons E_H>20 MeV [cm^{-2}]	TID [krad]
RICH-1	$6.1\cdot10^{11}$	$2.3\cdot10^{11}$	39.6
RICH-2	$3.1\cdot10^{11}$	$1\cdot10^{11}$	15.9

In a very conservative approach, several CLAROs were irradiated up to a factor 10 times larger than the radiation level expected in 10 years of LHCb. The radiation hardness tests were performed irradiating the chip with neutrons, X-rays and protons.

A. Neutron irradiation

The neutron irradiation measurements were performed at the Université Catholique de Louvain-la-Neuve (Belgium) in May 2013. A cyclotron (T2 Hall) accelerates a deuteron beam on a beryllium target producing a high flux neutron beam (average energy ~23 MeV) with a very low gamma (2 %), proton and electron (0.02 %) contamination. Three CLARO PCBs were placed in a cascade configuration, powered and irradiated in three steps that correspond to 4, 40 and 160 equivalent years in LHCb (final cumulative fluence of ~ 10^{14} 1 MeV n_{eq}/cm^2). During the irradiation process the threshold level and the supply current were continuously monitored so that Single Event Upset or variation in the supply could be detected. Before and after each irradiation step bursts of 1000 identical test pulses was sent to all the CLARO inputs simultaneously and the number of discriminated output signals was measured for different input signal amplitudes. This process permits to acquire the "S-curves", such as the one shown in Fig. 4. The position of the edge of the curve allows to evaluate any variation in the threshold level, while an increase of the noise would result in a smoother transition. As it can be seen, no significant increase of the noise was observed and also the variation of the threshold level turned out to be of the order of few percentage points. Furthermore, neither Single Event Upset nor Single Event Latch-up occurred.

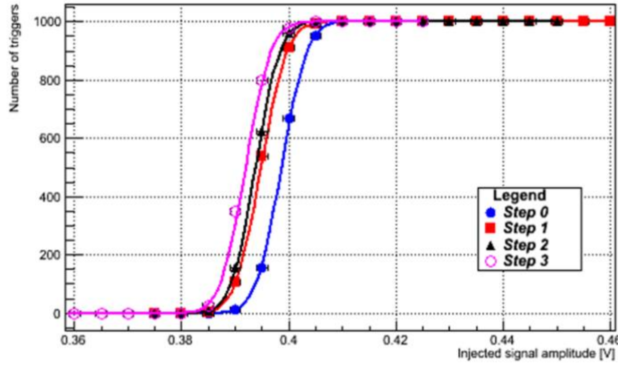

Figure 4: S-curve acquired during the neutron irradiation.

B. X-rays irradiation

In order to test the CLARO CMOS chip tolerance to the total ionizing dose (TID), a X-rays irradiation measurement was performed at the INFN National Laboratory in Legnaro (Italy) in September 2013. The X-rays were produced using tube with a tungsten anode biased at 50 kV. Two bare CLAROs (the lid which covered the ASIC was removed) were biased and irradiated in three steps that correspond to about 1, 10 and 110 years of LHCb operation (the final cumulative dose amounts to 4 Mrad).

The measurements performed are similar to those described in the previous section. Again, no Single Event Upset nor Single Event Latch-up occurred, while the supply current decreased by a factor 10-15 %. From the S-curves (see Fig. 5) a variation in the threshold level by a factor 10-15 % can be evaluated, while the noise did not change significantly.

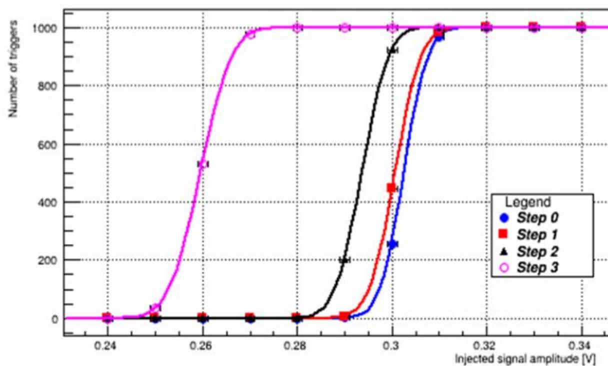

Figure 5: S-curve acquired during the X-rays irradiation.

C. Proton irradiation

Finally, the proton irradiation tests were performed at the Institute of Nuclear Physics, Polish Academy of Sciences in Krakow (Poland) in February 2014. The proton beam had an average energy of about 60 MeV and ensured a good uniformity over the CLARO CMOS area (beam diameter ~ 1 cm). Three bare CLARO were biased and irradiated in four steps that are equivalent to 1, 10, 100 and 190 years in the LHCb environment (final cumulative dose of 7.6 Mrad). Performing the usual measurements, no Single Event Latch-up was observed, a decrease by a factor 10-15 % in the supply current was recorded, while the threshold level reduced by a factor 15-20 %. Furthermore, a Single Event Upset occurred (see Fig. 6) which made the DAC output move abruptly from ~ 1.13 V to ~ 1.1 V. This event suggests to equip the new version of the CLARO with a register protected with triple modular redundancy and a SEU internal counter in order to monitor and correct such events.

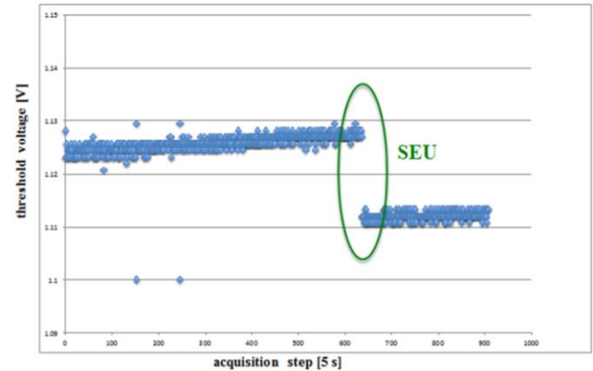

Figure 6: Single Event Upset observed during the proton irradiation.

IV. Conclusions

The CLARO CMOS chip has been described. It is an ASIC designed in 0.35 µm AMS CMOS technology for the readout of Ma-PMTs. The CLARO was chosen as the baseline front-end device to be used in the upgraded RICH detectors in the LHCb experiment. The main features of the chip are the capability to sustain high photon counting rate (up to 40 MHz) with a low power consumption (~ 1 mW per channel). The relative old technology also meets the requirements of minimizing the costs, enhancing the yield. The performance of the chip have been briefly described also when coupled with the R11265 Ma-PMT, produced by Hamamatsu. The results of the radiation hardness tests have been presented. The CLARO turned out to be tolerant to neutrons, X-rays or proton irradiation up to levels 10 times larger than those expected in 10 years of LHCb operation.

V. Acknowledgments

We would like to thank Nancy Postiau, Eduardo Cortina and the Université Catholique de Louvain Cyclotron staff for their support during neutron irradiation. We would like to thank Andrea Candelori, Devis Pantano and Serena Mattiazzo for their support at the X-ray irradiation facility at the INFN Laboratori Nazionali di Legnaro. We would like to thank Mariusz Witek, Tadeusz Lesiak, Jan Swakon and the Cyclotron/Therapy staff for their support during proton irradiation at the Institute of Nuclear Physics in Krakow.

VI. References

[1] LHCb Collaboration (2011), Letter of Intent for the LHCb Upgrade, CERN-LHCC-2011-001, LHCC-I-018.

[2] LHCb Collaboration (2013), LHCb PID Upgrade Technical Design Report, CERN-LHCC-2013-022, LHCB-TDR-014.

[3] L. Cadamuro et al (2014), Characterization of the Hamamatsu R11265-103-M64 multi-anode photomultiplier tube, JINST 9, P06021, doi: 10.1088/1748-0221/9/06/P06021.

[4] M. Calvi et al. (2014), First Characterization of the Hamamatsu R11265 multi-anode photomultiplier tube, Nuclear Instruments & Methods in Physics Research A, doi: 10.1016/j.nima.2014.05.123.

[5] P. Carniti et al. (2012), CLARO-CMOS a very low power ASIC for fast photon counting with pixelated detectors, JINST 7, P11026, doi: 10.1088/1748-0221/7/11/P11026.

[6] M. Fiorini et al. (2014), Radiation hardness tests and characterization of the CLARO-CMOS, a low power and fast single-photon counting ASIC in 0.35 micron CMOS technology, Nuclear Instruments & Methods in Physics Research A, doi: 10.1016/j.nima.2014.04.072.
[7] M. Karacson (2013), Radiation levels in the LHCb cavern, presentation during the LHCb Upgrade Electronics meeting on February, 14th.

CMOS Analog Front End Design for Particle Energy Measurement in Space Environment

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Abstract

In situ studies of the geospace environment, including space weather monitoring, is mainly based on the measurements of particles and fields. The particle content of the Earth's magnetosphere is studied with electron and ion detectors in various energy ranges, from the cold and dense eV solar wind to the MeV radiation belts. Here, the in situ high-energy (50 keV to 725keV) electron measurement is targeted. The design and development of space embedded electronic equipment require a specific approach. An Analog-Front-End (AFE) design methodology is proposed to optimize noise, bandwidth, consumption, crosstalk and radiation hardness performances of such AFEs for Si semiconductor detectors. The conception of an Analog-Front-End optimized in noise, bandwidth, consumption, crosstalk and radiation hardness, dedicated to a silicon (SiA) detector. Each channel includes an 8 bits successive approximation register (SAR) ADC in order to digitize

the incident electron energy. The chip was designed in a 0.35 µm HV CMOS process. The ASIC measurements have shown that for a charge range of 0.6 fC to 32 fC , the charge-to-voltage conversion gain is approximately 60 mV/fC. The equivalent noise charge (ENC) is 3119 e- for 40pF input parasitic capacitance while consuming 2.5 mW. The circuit can perform measurements up to a 650 kHz rate. The next step is to characterize the ASIC associated with the SC detector in a vacuum chamber. Furthermore, the total ionisation dose (TID) and the single event effect (SEE) tolerances must also be evaluated.

I. INTRODUCTION

Particle instruments incorporate sensors that are used to convert particle energy into quantifiable electrical charges. These sensors with their corresponding analog electronics circuits, also called Analog-Front-End (AFE), form detection channels called "sensor heads" [1-3]. The necessity to improve both spatial and spectral resolutions requires the design of multichannel integrated electronics. Thus, space-borne detectors with Application Specific Integrated Circuits (ASICs) should be developed. These integrated circuits allow not only to perfectly adapt the readout circuits to each sensor in order to optimize performances but also to benefit from the various advantages inherent to the use of monolithic technologies: reduced power consumption, smaller size, shorter transit time signals [4] and higher integration [5].

However, specific design methodology should be employed in order to withstand constraints due to space applications. The radiation environments can especially damage electronic systems on spacecraft and orbital satellite [6-7;16]. Nowadays, instead of using CMOS technologies dedicated to space (such as specific BiCMOS or SOI) in order to improve the radiation hardness of integrated circuits, it seems appropriate to use specific design techniques (radiation hardening by design (RHBD)) [7-8] applied on standard CMOS technologies which are less expensive [9], provide higher performances and for which parasitic effects are studied and well known [10-11]. Knowing the duration of the mission as well as its corresponding radiative environments, an 0.35 µm CMOS technology was chosen because it can naturally withstand more than 50 krad [8] and provide high enough dynamic ranges as its standard operating supply voltage is 3.3V. Note that a previously designed AFE allowed us to assess the TID behaviour of this technology [17]. The tests showed that the ASIC tolerates doses up to 360 krad without any relevant impact on the performance (degradation of the amplifier by the increase of leakage currents). In addition, to protect circuits from latchup, the extensive use of guard rings is required. Furthermore, in order to minimize crosstalk which can cause faulty detections, reduce the ASIC sensitivity, and improve power supply rejection, isolated-well technology process option was used. This feature is usually provided by High Voltage (HV) technologies where the transistors have almost the same characteristics as the ones used in the standard technology. Therefore, a 0,35 µm CMOS HV technology has finally been chosen.

Once the technology is chosen, it is necessary to perfectly understand the detector and propose an equivalent electrical model of the detector before design the ASIC. With this aim, the GEANT4 simulator is used to model the various physical effects associated with particles interacting within semiconductor detectors. The number of generated electron-hole pairs can thus be estimated as a function of the incident particle energy. Further, the main electrical characteristics of the sensor such as its charge collection time, its parasitic capacitance as well as its leakage current, can also be retrieved to correctly create an equivalent electrical model of the detector. With this aim, a sensor based on semiconductors (SCs) is presented in section 2.

Then, a description of the designed AFE that should linearly quantify the amount of detected charges in order to reconstruct the electron energy spectrum is given in section 3.

Finally, in section 4, ASIC experimental results are presented.

II. THE DETECTOR MODEL

The detector is an electron energy spectrometer based on semiconductors. This instrument is intended to analyze the atmosphere-ionosphere-magnetosphere interactions during Transient Luminous Events (TLE) that can occur during atmospheric storms, in order to understand the physical mechanisms responsible for vertical impulsive coupling between the atmosphere and the ionosphere. The final aim is to assess the impact of these phenomena on the earth environment [12]. The purpose of the instrument is to provide a high resolution electron energy spectrum with its corresponding angle distribution. It is designed to measure electron energy in a wide range of fluxes. For instance, these fluxes can range from ~1 to 106 $cm^{-2}.s^{-1}$ for the 70-100 keV energy level inside the low altitude radiation belt, including the South Atlantic Anomaly, and from 1 to 5.10^2 $cm^{-2}.s^{-1}$ for the 4 MeV energy level which are reached during terrestrial gamma flashes (runaway electron beams). The instrument consists of two spectrometers, each having a maximum view angle of 30°x150°. The instrument is covered with an aluminium foil of 6 µm thickness to stop any incoming stray photons (~ 100% and 70% mitigation of respectively 1 keV and 5 keV soft x-rays). This foil also stops the protons with energies below 600 keV.

In order to detect the particle energy within this range, the use of semiconductors (SCs) of different kinds is necessary. By using different ionization energy SCs as well as different semiconductor thicknesses, each particle within the required energy range can be stopped while providing a linear charge amount. Therefore, stacking different kind of SCs allows not only to analyze a larger energy spectrum but also to use the method of coincidence in order to determine the direction of arrival of the particle. Here, the detection heads are made of two superposed plates of SCs to measure both the energy and the trajectory direction of electrons. The top plate is made of silicon (Si) and the bottom one of Cadmium Telluride (CdTe) with ionization energy per e/h pair of 3.6 and 5 eV respectively. The use of these two SCs allows to characterize the electrons over the whole energy range (from 60 keV to 4 MeV). Si can detect energies from 10 keV to 500 keV and CdTe starts stopping energetic particles beyond 500 keV up to 4 MeV.

The Si detector is divided in five cells: four large cells called Si A (10 mm × 10 mm) and one smaller cell called Si B (0.4 mm × 10 mm) placed in the centre. This SiB cell is required to avoid saturating the instrument in the South Atlantic Anomaly and to improve the determination of the electron trajectory when the detector is working in coincidence mode between Si and CdTe. The CdTe detector consists of 64 CdTe cells of 10 mm x 10 mm. This CdTe matrix is used to detect the electrons that completely traverse the Si plate.

The complete response of a given semiconductor to an energetic electron beam is difficult to predict because many physical effects occur (probabilistic domain). However, GEANT4 software (for GEometry ANd Tracking) [13-14], developed by CERN, can be used to predict all these interactions. Both the SCs geometry and thickness are key input parameters for GEANT 4. The amount of electron-hole pairs produced by incident electrons can be obtained using Monte Carlo simulations over the whole electron energy range. The GEANT4 results are presented in the following paragraph.

A. *Simulation results*

The 3D and cross sectional views of the detector are represented in figure 1.

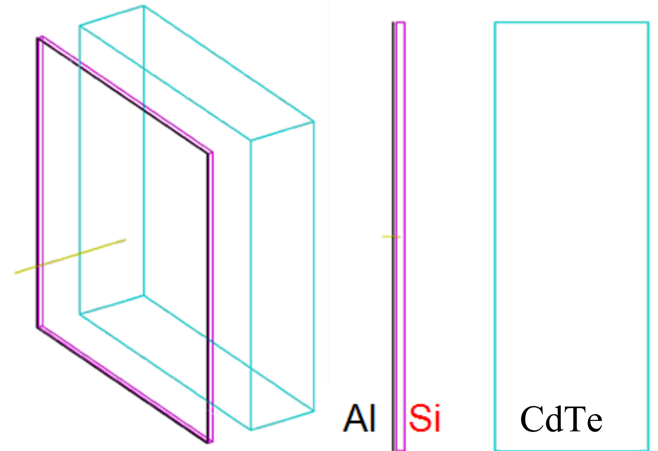


Figure 1: 3D (left) and sectional (right) diagrams of both cells forming the SCs detector and covered by aluminium foil.

Once the design of the detector is completed, Monte Carlo simulations are run to assess its performances for different incident electron trajectory angle and energy. These simulations allow to take into account all the physical phenomena that can occur along the particle path through detector. The thicknesses of both kinds of SCs can thus be tuned in order to obtain the required energy detection ranges [6]. The Si and CdTe thicknesses are d=0.3 mm and d=5 mm respectively. Note that electrons with an energy level lower than 10 keV cannot cross the aluminium foil. From energy higher than 500 keV, electrons traverse the Si and start to lose their remaining energy in the CdTe. Up to 4 MeV, the CdTe captures completely the electrons. For energy levels higher than 4 MeV, the bremsstrahlung effect starts to be significant [15]. For the most energetic electrons > 6 MeV, the emission of bremsstrahlung is dominant and as a result, the electrons can pass through the CdTe. Note also that the simulations take into account the effects of the photons generated by electrons (Compton scattering, photoelectric effect...). However, such events are too rare at these energy levels to noticeably influence the detector response. The number of electron-hole pairs, n_{e-h} generated in the semiconductors by an incoming electron that transmits an energy E_{lost} to the semiconductor, is given by:

$$n_{e-h} = \frac{E_{lost}}{E_I} \quad (1)$$

with E_I the ionization energy (energy per pair) of the absorbent material.

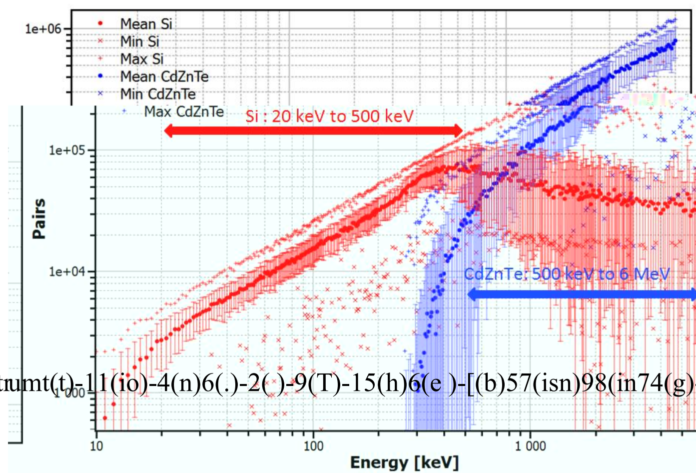
B. *Output response*

Using GEANT4, the energy loss along the incoming electron path can be computed for each SC. Consequently, using eq.(1), the total n_{e-h} generated within each SC can be deduced. As GEANT4 uses physics probabilistic models, Monte Carlo simulations need to be run in order to statistically characterize n_{e-h} as a function of the incident electron energy ranging from 10 keV to 6 MeV. In Fig. 2, the mean, standard deviation, maximum and minimum number of pairs generated in each SC are represented with Si and CdTe thicknesses of d=0.3 mm and d=5 mm respectively. It can be observed that the semiconductor response to incoming electrons is sufficiently linear to retrieve the electrons incident energy from the number of pairs generated in the detector in specific ranges. The linear energy range of the Si is [20 keV - 500 keV] (Fig. 2). Within this range for d=0.3 mm, the average number of pairs n_{pairs_Si} generated is defined as:

$$n_{pairs_Si} = 166\, E_{in} - 683 \quad (2)$$

where E_{in} is the energy of the incident electron in keV.

To define the charge input range of the AFE, the minimum and maximum values observed for each SC are taken into account to avoid any loss of information. Si can generate 1.10^4 to 2.10^5 electron-hole pairs.



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the holes at the cathode and the electrons at the anode. Table 1 summarizes the estimated characteristics of the SiA detectors found.

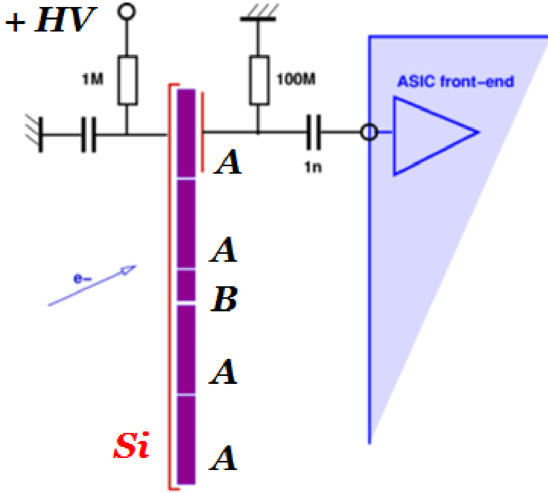

Figure 3: Biasing circuit of the Si cell (type A) and connection to the electronic "front-end".

Based on the previous detector analysis, Si cells can be modelled by a pulse current source I_{det} to simulate a charge injection Q_{in} in parallel with the equivalent capacitor C_{det} of the cell. Also, leakage current I_0 estimated is included in this model by a constant current source at this value.

Table 1 : Characteristics of the Si detectors used in the instrument

Characteristic	Symbol	Si A
Size (mm)	$L \times l \times d$	10x10x0.3
Pairs range (e^- ou e^+)	-	1,4x10^4 to 2x10^5
Equivalent charge (fC)	Q_{in}	2.2 to 32
Collection time (ns)	t_c	50
Equivalent capacitor (pF)	C_{det}	34.8
Leakage current (nA)	I_0	2
Anodes number	-	4

III. ANALOG FRONT END DESIGN

The first step is to convert charge into a voltage using a charge preamplifier (CPA). The CPA consists of a transconductance amplifier (OTA) with a feedback capacitance C_f to perform the charge integration. Then, in order to improve the Signal-to-Noise Ratio (SNR), the CPA output voltage is filtered by a circuit called pulse shaper (PS). These two blocks are widely used in the type of application [1-3; 18]. Therefore, the analog-to-digital converter (ADC) input signal noise is reduced, which thus decreases the detection threshold level and increases the AFE achievable precision. To save power as well as reduce the influence of any external parasitic signals, analog-to-digital conversions of the CPA+PS output should be performed within the same chip. Thus, each channel has the following architecture: a CPA+PS, a comparator with an adjustable threshold voltage level, a peak detector (PD) and an 8 bits Successive Approximations Register (SAR) ADC. To summarize, the CPA+PS converts the incident charge into a proportional voltage and the comparator detects if the incoming charge is higher or lower than the desired threshold level. Note that the minimum detection threshold level can be obtained by setting the threshold voltage of the comparator just above the noise floor. The PD is used to store the maximal peak value of the PS output voltage, which is proportional to the electron energy. This stored voltage is then digitized by the SAR ADC. A control logic block of the system is also designed to manage the communications between the blocks. The AFE schematic is represented in Fig.4 and the design of the SiA AFE has been detailed in [19].

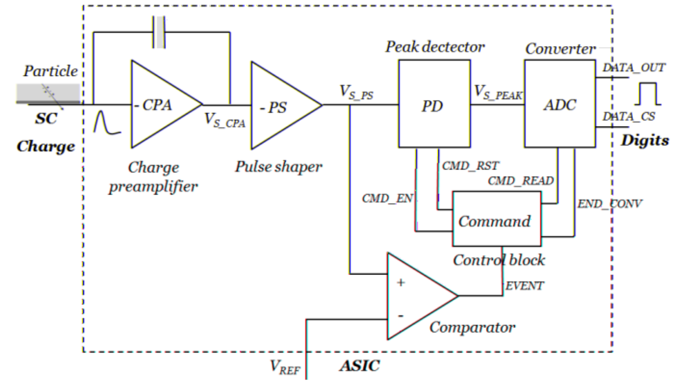

Figure 4: AFE conversion system to measure the transmitted energy by an incident electron in a SC detector.

IV. MEASUREMENTS AND PERFORMANCES

The AFE have been implemented in a CMOS HV 0.35 µm technology. Fig. 5 shows the layout view of the SiA channel (CPA+PS (1), discriminator (2) and ADC (3)). Each channel occupies a surface area of approximately 0.21 mm². To reduce crosstalk, analog and digital circuit wells are separated from each other and the corresponding circuits have their own power supplies VDD and GND (implementation of insulated wells, only available in BiCMOS or HV technologies).

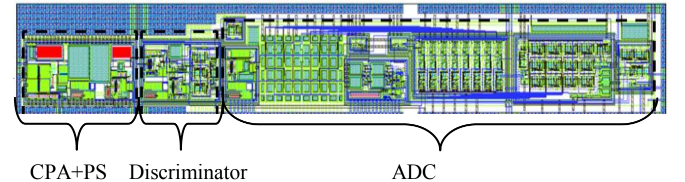

Figure 5: Die layout of the SiA channel implemented in a CMOS HV 0.35 µm technology.

On the analog test blocks, the measured value of the shaping time is 105 ns. Also the measured power consumption for one Si channel is 2.5 mW including static and dynamic power consumption of CPA+PS, discriminator and ADC.

The linearity of the system can be evaluated by analyzing the ADC output. Its dynamic range is 44 dB with a linearity

error of less than 0.32 %. Then the particle detection delay, which corresponds to the time between the arrival of the charge and the start of its conversion at the output of the ADC (DATA_CS = '1'), can be estimated by observing the outputs of the SiA channel (DATA_OUT and DATA_CS) for a 50 ns (T_(C_MAX)) input charge of 22.35 fC (see Fig. 6)corresponding to the digital output '10101001'. The measured detection delay is equal to 320 ns. The ADC conversion time is 1 µs and the reset time of the digital blocks is 200 ns. So, the final effective operating frequency of the chains is approximately equal to 650 kHz.

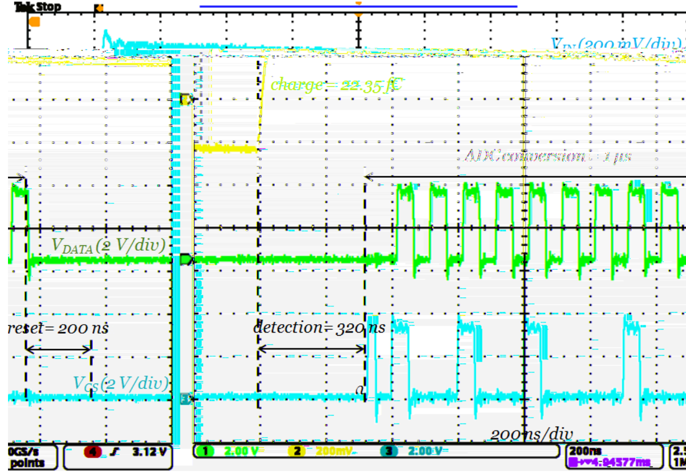

Figure 6: ADC outputs measurement (DATA_OUT and DATA_CS) of the Si A channel conversion for a 50 ns input charge of 22.35 fC and C_{det} = 40pF.

The linearity is plotted in Fig. 7 obtained for 50 acquisitions for each charge step and averaged over three different ASICs. The conversion gain is 57.7 mV.fC^{-1} with an ENC of 3119 e^{-} (or 0.5 fC) in the linear region and the saturation value is approximately 32 fC for linearity errors less than 0.81%. The minimum detectable value is approximately 0.6 fC which is different from the measured ENC values. That is explained by the fact that the detection thresholds are affected by the noise mass supply of the PCB.

Crosstalk measurements similar to those made in [17] have shown that crosstalk is non-existent. So using an isolated-well technology (HV) and a differential pair in the CPA bring a major interest in the integration on a multichannel same chip.

In Table 2, the specifications, the simulated and measured data are summarized for the SiA channel. Measurements are very close to simulations which validate our design methodology.

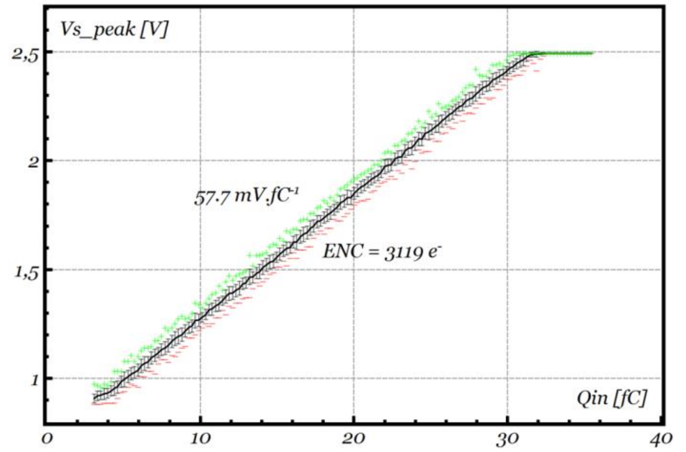

Figure 7: Linearity of the SiA channel deduced from the output of the 8-bit ADC, for 50 acquisitions, 3 ASICs and Q_{in} varying between 0.6 fC and 35 fC (C_{det} = 40pF). Averages (line), standard deviations (error bars), maximum (green +) and minimum (red -) values of 50 measures by step.

Table 2 : Summarize of SiA instrumentation channels performances

	Specifications		Measurem ents
Input charge range (fC)	0,6 to 32	0.53 to >32	0.6 to 32
Detector capacitance (pF)	40		

VII. References

[1] Bonvicini, V., et al., "A Double-Gain, Large Dynamic Range Front-end ASIC With A/D Conversion for Silicon Detectors Read-Out." Nuclear Science, IEEE Transactions. vol.57, no.5, pp.2963-2970, 2010.

[2] Kaplon, J. and Dabrowski, W., "Fast CMOS binary front end for silicon strip detectors at LHC experiments." Nuclear Science, IEEE Transactions. vol.52, no.6, pp.2713-2720, 2005.

[3] Kishishita, T., et al., "Low-Noise Analog ASIC for Silicon and CdTe Sensors." Nuclear Science, IEEE Transactions. vol.57, no.5, pp.2971-2977, 2010.

[4] Orton, D.E., "Small, smart, intelligent and interactive handheld devices." VLSI Design, 2006. Held jointly with 5th International Conference on Embedded Systems and Design., 19th International Conference on. pp1, 2006.

[5] Baltes, H., et al., "CMOS MEMS - present and future." Micro Electro Mechanical Systems, 2002. The Fifteenth IEEE International Conference on. pp 459 – 466, 2002.

[6] Leroy, C. and Rancoita, P.G., Principles of Radiation Interaction in Matter and Detection. Hackensack, N. J. : World Sci., 2004.

[7] Lacoe, R.C., "Improving integrated circuit performance through the application of hardness-by-design methodology." IEEE Trans. Nucl. Sci. vol. 55, no. 4, pp. 1903–1925, 2008.

[8] Dodd, P.E., et al., "Current and Future Challenges in Radiation Effects on CMOS Electronics." Nuclear Science, IEEE Transactions. vol.57, no.4, pp.1747-1763, 2010.

[9] Qu, H. and Xie, H., "Process Development for CMOS-MEMS Sensors With Robust Electrically Isolated Bulk Silicon Microstructures." Microelectromechanical Systems, Journal of. vol 16, Issue 5, pp 1152 – 1161, 2007.

[10] Caignet, F., Delmas-Bendhia, S. and Sicard, E., "The challenge of signal integrity in deep-submicrometer CMOS technology." Proceedings of the IEEE. Volume 89, Issue 4, pp 556 - 573, 2001.

[11] Ando, B., et al., "Characterization of parasitic behaviors in CMOS microsensors." Instrumentation and Measurement Technology Conference, 2001. IMTC 2001. Proceedings of the 18th IEEE. Volume 3, pp 1459 - 1462, 2001.

[12] Lefeuvre, F., Elisabeth Blanc, Jean-Louis Pinçon, Robert Roussel-Dupré, David Lawrence, Jean-André Sauvaud, Jean-Louis Rauch, Hervé de Feraudy and Dominique Lagoutte., "TARANIS—A Satellite Project Dedicated to the Physics of TLEs and TGFs." Space Science Reviews. Volume 137, Numbers 1-4, 301-315, 2008.

[13] Agostinelli, S., Allison, J. and all., "GImage 4—a simulation toolkit." Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment. Volume 506, Issue 3, Pages 250-303, 2003.

[14] Allison, J. and all., "Geant4 developments and applications." Nuclear Science. IEEE Transactions vol.53, no.1, pp.270-278, 2006.

[15] Berger, M.J., Coursey, J.S., Zucker, M.A. and Chang, J., Databases ESTAR, PSTAR, and ASTAR : Stopping-Power and Range Tables for Electrons, Protons, and Helium Ions. http://www.nist.gov/pml/data/star/index.cfm. [Online] The National Institute of Standards and Technology (NIST) is an agency of the U.S. Department of Commerce, Date created: October 7, 2009.

[16] Schwank, J.R., et al., "Radiation Effects in MOS Oxides." Science, IEEE Transactions. vol.55, no.4, pp.1833-1853, 2008.

[17] Bouyjou, F., Bernal, O., Tap, H., Picaut, G. and Sauvaud, J-A., "Qualifying a CMOS Instrumentation Chain for Charged Particles Detection in the Space Environment." Analogue and Mixed-Signal Integrated Circuits for Space Applications. ESTEC - Noordwijk - The Netherlands, 2012, Vol. 4th International Workshop.

[18] Sansen, W.M.C. and Chang, Z.Y., "Limits of low noise performance of detector readout front ends in CMOS technology." Circuits and Systems, IEEE Transactions. vol.37, no.11, pp.1375-1382, 1990.

[19] Bouyjou, F. ; Bernal, O.D. ; Tap, H. ; Sauvaud, J.-A. ; Jean, P., Low Noise CMOS Analog Front-End Circuit With an 8-bit 1-MS/s ADC for Silicon Sensors for Space Applications, Sensors Journal, IEEE, Vol. 14, Issue: 5, 2014 , Page(s): 1617- 1624

An ASIC for Spaceborne Radiation Monitors

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Abstract

The IDE 3465 is an application specific integrated circuit (ASIC) that has been designed for the readout of silicon detectors for charged particles. The chip has 20 inputs of charge sensitive pre-amplifiers (CSA), a total of 37 digital logic trigger outputs, and one analogue multiplexer output for pulse heights. Out of the 20 channels, 16 have a high gain with saturation at 2.6 pC, and 4 have a low gain with saturation at 26 pC. In the high-gain channels, the charge sensitive pre-amplifier is connected to one slow shaper of 1-µs shaping time and two fast shapers of 250-ns shaping time, while the low-gain channels have only one slow shaper and one fast shaper of 1-µs and 250-ns shaping time. Each fast shaper output is connected to a comparator, which triggers when the pulse shape exceeds the reference level that can be programmed by 8-bit DACs. The two fast shapers and comparators of the high-gain channels are used for charges in the range from 1 fC to 100 fC and from 100 fC to 2.6 pC, respectively. The fast shapers and comparators of the low-gain channels are designed for charges in the range from 1 pC to 26 pC. Each comparator feeds a mono-stable output, which can be connected directly to an FPGA. The chip requires negative and positive voltage supplies (-2 V, +1.5 V and +3.3 V) and one reference bias current to generate its internal biases. The total power consumption is less than 65 mW, depending on the input event rate and options enabled. The chip has a 356 bit register, programmable via serial interface, which allows one to set various functions, to program digital-to-analogue converters (DACs), and to tune parameters. All amplifier inputs are protected by diodes against over-voltage and electro-static discharge (ESD). The chip is SEU/SEL radiation hardened by design and manufacture.

I. Introduction

A. *Objectives*

The IDE3465 is a full custom-application specific integrated circuit (ASIC) for the readout of space based charged particle detectors that use silicon sensors for charged particle tracking and/or counting. Such instrumentation can help providing answers to scientific questions and support space weather data acquisition. The ASIC is developed from the IDEAS TAP-family of trigger ASICs and have been designed in two versions, the IDE3464 engineering model (EM) and the radiation hardened IDE3465 flight model (FM). The IDE3465 is integrated into the Next Generation Radiation Monitor (NGRM) [1] and the ASIC development has reached an ESA technology readiness level (TRL) > 6. The NGRM shall be used for example in the EDRS-C. The development is also relevant for other applications, and will be the baseline ASIC for the upcoming RADEM radiation monitor for the JUICE mission [2].

B. *Radiation Detector Readout Principle*

Figure 1 shows the detector readout principle. A charged particle interacts in the silicon sensor and generates an electric charge that is proportional to the energy deposited in the interaction. The electrodes of the sensor are biased to generate an electric field inside the sensor, which moves the free charges and thereby generates a current. The electrodes are connected to the inputs of the charge sensitive amplifiers (CSA) in the ASIC. The CSAs integrate the induced currents over time and deliver a pulse height that is proportional to the energy dissipated in the particle interaction. The ASIC delivers individual trigger signals for every channel when a pulse height exceeds the programmed threshold. In addition, the system can read out the pulse height from all channels.

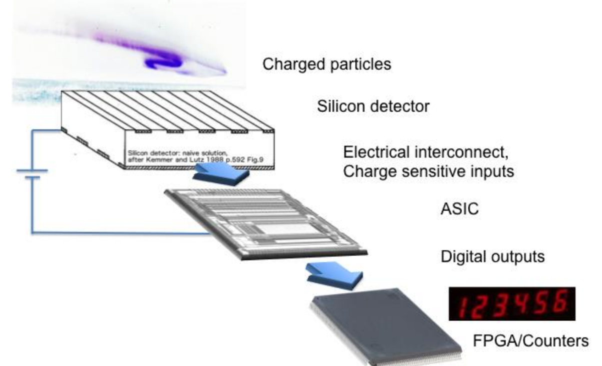

Figure 1: Radiation detector readout principle.

A. *Specific Goals*

The ASIC has charge sensitive amplifiers with two different fixed gains to accommodate different charged particles (*e, p,* ions) in the silicon sensor. There are up to two comparators per channel and their reference voltages can be programmed independently using 8-bit DACs. Each comparator result can be a direct input a field-programmable gate array (FPGA), which provides coincidence logic and digital counting. Important goals of this development were the low power dissipation and the relatively high radiation tolerance against single event effects, *i.e.,* 50 MeVcm^2/mg linear energy transfer threshold (LET_{th}).

A. *Design Heritage for Space Instrumentation*

Our group has designed similar ASICs in previous years. For this type of ASIC, our space heritage includes the analogue

front-end for the silicon charged particle trackers in AGILE [3], Stereo/Plastic [4], PAMELA [5], AMS1 and AMS2 [6], MEGA [7], BepiColombo [8], FOXSI [9], and ASTRO-H [10]. Other space heritage is described in [11].

II. Experimental technique

A. Architectural Overview

Figure 2 shows the block diagram of the ASIC. The chip has 20 inputs of charge sensitive pre-amplifiers (CSA), a total of 37 digital logic trigger outputs, and one analogue multiplexer output for pulse heights. Out of the 20 channels, 16 have a high gain with saturation at 2.6 pC, and 4 have a low gain with saturation at 26 pC. The chip contains a bias network that generates all bias needed for the operation. The chip has a programmable configuration register that allows one to control internal bias values and other settings.

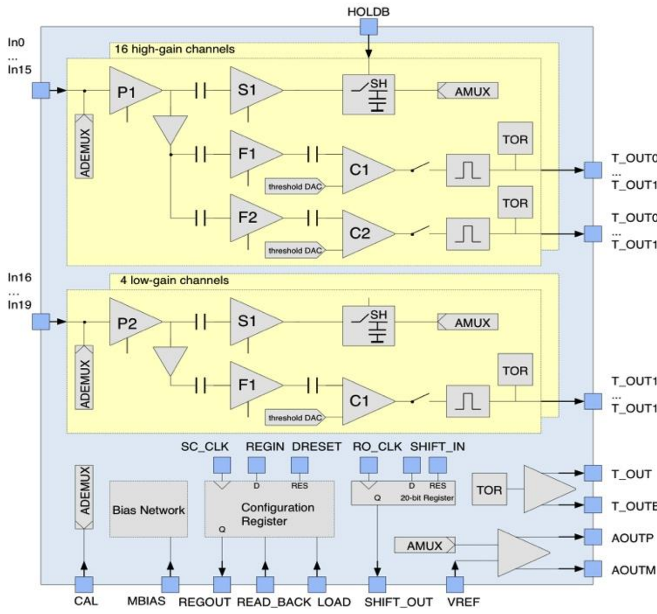

Figure 2: Block diagram of the chip.

B. Channel Architecture

Figure 3 shows a block diagram of a high-gain channel. The pre-amplifier (P1) integrates over time the electrical current and outputs a voltage step. The pre-amplifiers are designed for a capacitive load of 30 pF. The shaping amplifier (S1) has 1-µs shaping time and provides pulse height for sample-and-hold (SH) to the analogue multiplexer (AMUX). The other two shaping amplifiers (F1, F2) have 250-ns shaping time and provide pulse heights to the comparators (C1, C2), which trigger a mono-stable. The outputs from the mono-stables can be used by the system to count triggers from each channel individually or in coincidence.

A. Signal Timing

Figure 4 shows a timing diagram of the most important signals. The current in the pre-amplifier of channel N (2) generates a trigger at **T_OUT*N*** and a trigger at **T_OUT** (3). These signals can be used for external coincidence and counting. The system can sample the pulse heights from all channels by activating **HOLDB** at the peaking time T_p (4). The system acquires the pulse heights at the differential current at **AOUT** by applying **SHIFT_IN_B** and **RO_CLKB**.

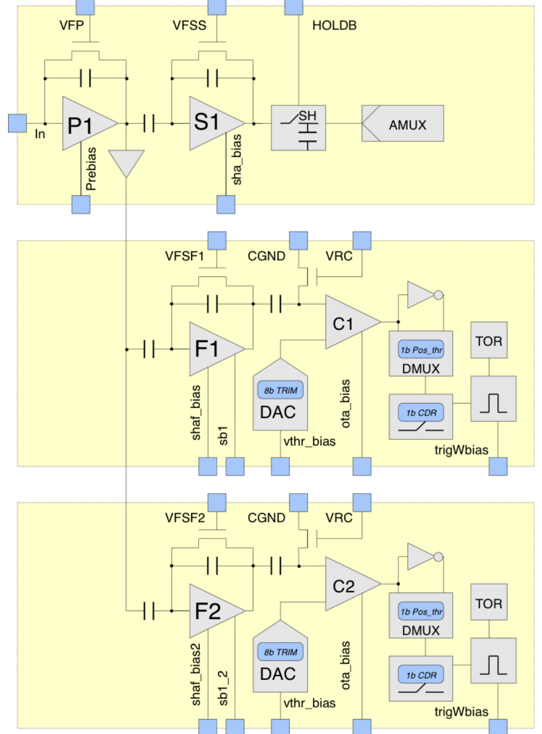

Figure 3: Block diagram of a high-gain channel.

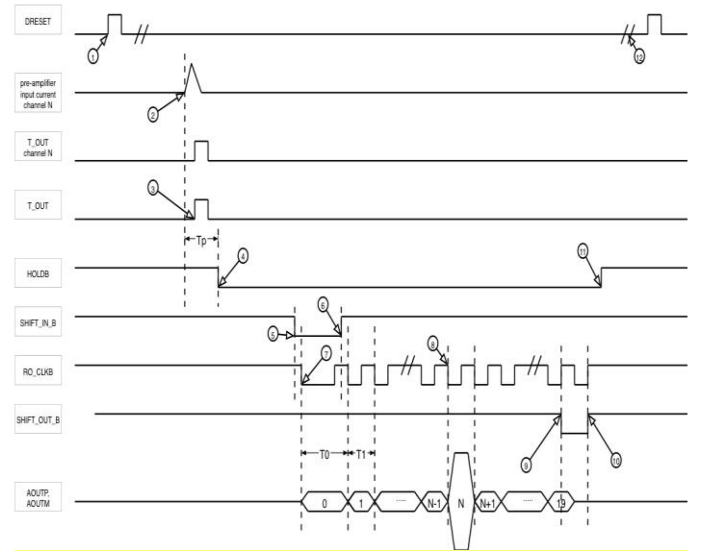

Figure 4: Signal timing.

B. Specifications

Table 1 summarizes the ASIC specifications. The values were experimentally validated on a few samples of the flight model ASIC.

A. Radiation Tolerance

The flight model ASIC was designed to meet the radiation requirements set for the NGRM [1]. The digital circuits have been designed using guard rings to prevent single event latch-up (SEL). Tests with heavy ion beams show a SEL threshold

higher than 116 MeVcm^2/mg. The programmable configuration register has been designed to correct for single-event upset (SEU), *i.e.*, each register cell has triple redundancy with a self-correcting circuit and a SEU output signal. The 0.35 µm CMOS process meets the 100-krad total-ionizing dose requirements (TID).

Table 1: Specifications.

20 charge sensitive inputs	< 2.6 pC in 16 high-gain channels < 26 pC in 4 low-gain channels
37 digital logic trigger outputs	32 outputs from the 2 comparators in the high-gain channels 4 outputs from the comparator in the low-gain channels 1 OR from all comparators
1 analogue output	Pulse height spectroscopy from all channels
Noise	0.45 fC ENC in high-gain channels 5 fC ENC in low-gain channels
Trigger threshold, minimum	1.5 fC and 71 fC in high-gain channels 150 fC in low-gain channels
Power	62.5 mW maximum, typical consumption 50 mW
Rate, maximum	> 1 Mcps/channel capability at the trigger outputs > 2.5 kcps/channel with analogue readout of all channels
Radiation tolerance	The chip is SEL immune (SEL LET_{th}>100 MeV/mg/cm2) The chip is radiation tolerant by design and manufacture, with respect to single event upsets

B. *Layout*

Figure 5 shows a photograph of the chip. The pre-amplifier inputs are located on the top and trigger outputs are on the bottom. The chip has many pads on the left and right side for power supplies and pads to monitor or apply internal bias settings. Except for the main bias, the bias pads do not need to be used during normal operation, because these are generated internally. The chip is designed for wire bonding.

C. *Manufacture*

The chip was designed and manufactured in AMS 0.35-µm CMOS technology [13] using our radiation tolerant full-custom ASIC design library. Table 2 summarizes the manufacturing information.

Table 2: Manufacture.

Supplier	IDEAS
Wafer fab	AMS
Technology	0.35 µm CMOS
Epitaxial layer	Yes
Metal Layers	4
Capacitor option	Double poly
Chip dimensions	6045 µm × 7140 µm

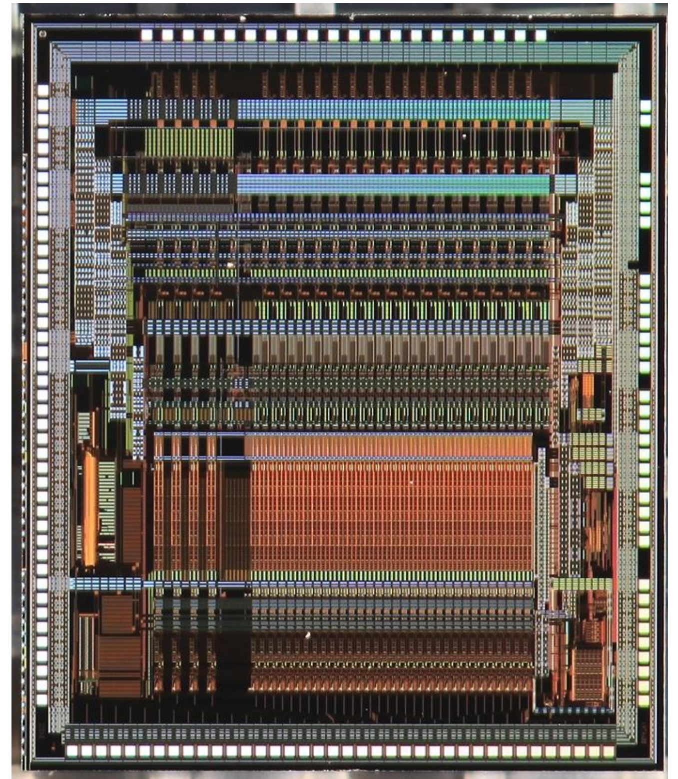

Figure 5: Photograph of the flight model ASIC.

III. RESULTS

A. *Input Charge Range*

Figure 6 shows the pulse height measured versus the input charge in a high-gain channel (top) and a low-gain channel (bottom) at different temperatures. The pulse height was measured at **AOUTM** and **AOUTP** using a test system with differential current-to-voltage converter and analogue-to-digital converter. At room temperature, the high-gain channel has a linear gain of about 330 µA/pC up to 2.6 pC; the low-gain channel has a linear gain of about 32 µA/pC up to 26 pC.

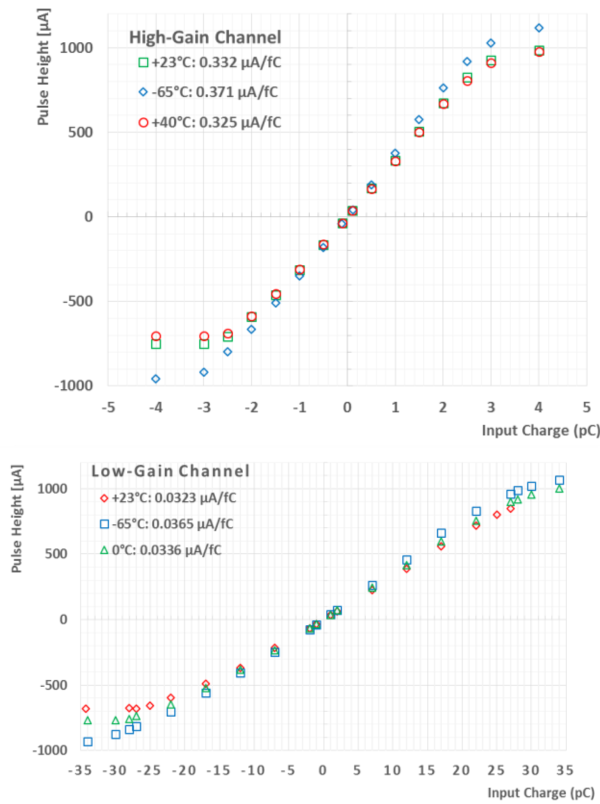

Figure 6: Measurement of the pulse height versus injected charge in a high-gain channel (top) and a low-gain channel (bottom) at different temperatures.

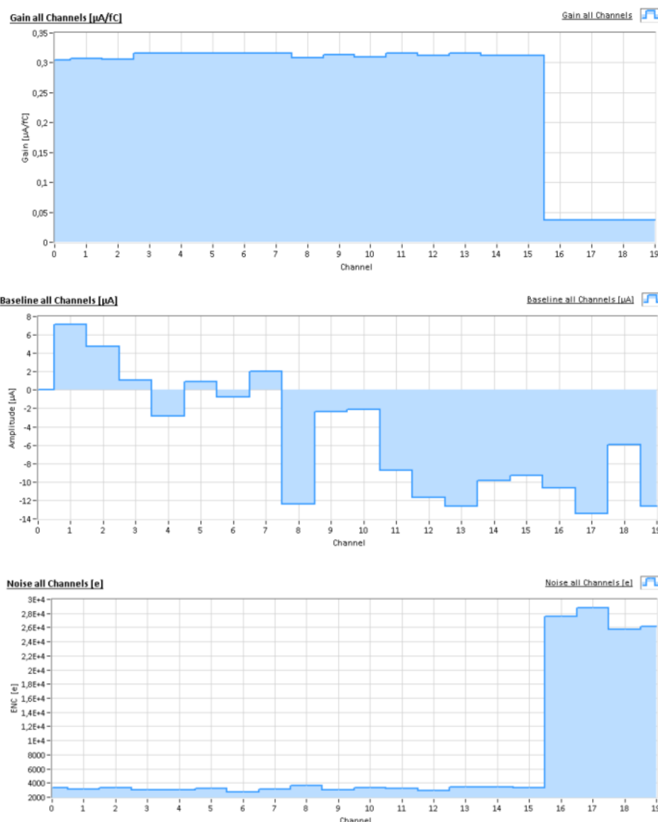

Figure 7: Gain, baseline, and equivalent noise charge (ENC) in all channels of the chip under test.

A. *Noise*

Figure 7 shows the baseline, the equivalent noise charge (ENC) and the gain from all 20 channels in the chip under test. We measure ENC of 0.45 fC in high-gain channels and 5 fC in low-gain channels. The noise does scale as expected with the saturation charge.

B. *Trigger Threshold Characteristics*

To verify rate capability, we injected test pulses at a constant rate of 1 MHz into one channel, and at that rate, we observe zero loss counts in the channel. Figure 8 show the rate capability of the high-gain channel high threshold and low threshold discriminator as a response to a 1 MHz, 200 fC input ramp signal. The ASIC is capable of trigger rates beyond 1 MHz.

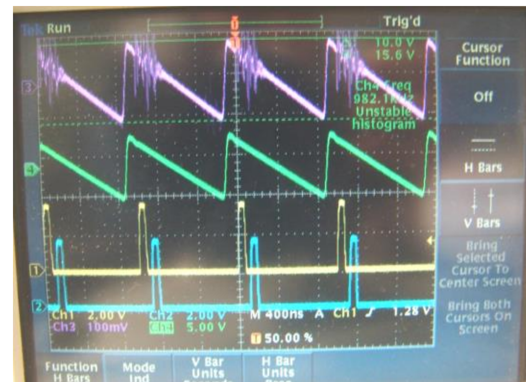

Figure 8 Measurement of the trigger output rate capability.

C. *Performance with Temperature*

Figure 9 and Figure 10 show the gain and noise measured versus temperature in the range from -65 °C to +40 °C. The gain decreases by about 0.1 %/°C with increasing temperature relative to the gain at the lowest temperature. The noise is about constant within the measurement error.

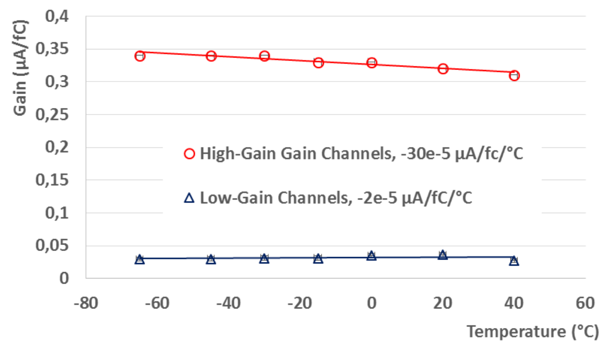

Figure 9: Mean value of the gain from high-gain channels and low-gain channels measured versus temperature.

D. *Radiation Testing*

The IDE3465 has been tested for radiation tolerance with respect to Single Event Effects (SEE) at Université Catholique de Louvain using the Heavy Ion Irradiation Facility (HIF).

The ASIC was tested using the M/Q ion cocktail with 40 µm penetration depth in Si. The ions with highest energy

available at UCL were 459 MeV $^{132}Xe^{26+}$ ions resulting in a linear energy transfer in silicon (LET (Si)) of 67.7 MeV/mg/cm^2. To induce SEL, the ASIC was mounted on a test card with heaters to increase the ASIC temperature to 80°C. The test card was mounted on a 3-axis movable test-frame. The ASIC was tilted in respect to the ion beam to produce a slanted ionization track. The resulting LET_{eff} was thus increased to 116 MeV/mg/cm^2. The results of the irradiation tests show that the IDE3465 does not latch-up at 116 Mev/mg/cm$^{2.}$

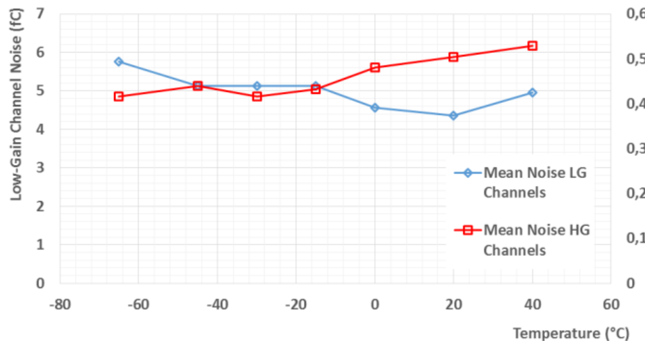

Figure 10: Mean equivalent noise charge (fC) from high-gain and low-gain channels measured versus temperature.

IV. Summary

We have developed an ASIC that can be used for charged particle counting with silicon detectors in space. The ASIC was designed to meet the requirements of the ESA Next Generation Radiation Monitor (NGRM) [1]. The main characteristics are the two types of channels with saturation charge of 2.6 pC and 26 pC, respectively. Each channel provides trigger outputs that can be directly connected to an FPGA for additional logic and counting. Single event effect tests show that the ASIC has a latch-up threshold of more than 116 MeVcm^2/mg. The work on a successor for the ASIC is ongoing as a part of the ESA RADEM project.

Acknowledgements

We like to thank the Norwegian Space Center for support. We also thank Willy Dang for wire bonding and assembly.

References

[1] L. Desorgher, *et al.,* ESA Next Generation Radiation Monitor, Proc. IEEE Nuclear Sci. Symp. 2013.
[2] P. Goncalves, Towards a Radiation Monitor for the Jovian System, XXIII Encontro Nacional de Astronomia e Astrofisica (ENAA) conference, Lisbon, July 2013.
[3] M. Prest, *et al.,* The AGILE silicon tracker: an innovative gamma-ray instrument for space, Nuclear Instruments and Methods in Physics Research A 501 (2003) 280–287.
[4] A.B. Galvin, *et al.,* The Plasma and Suprathermal Ion Composition (PLASTIC) Investigation on the STEREO Observatories, Space Science Rev., 136, 437–486, doi:10.1007/s11214-007-9296-x, 2008.
[5] L. Bonechi, *et al.,* Status of the PAMELA silicon tracker, Nuclear Instruments and Methods in Physics Research A 570 (2007) 281-285.
[6] J. Alcaraz, *et al.,* The alpha magnetic spectrometer silicon tracker: Performance results with proton and helium nuclei, Nuclear Instruments and Methods in Physics Research A 593 (2008) 376-398.
[7] G. Kanbach, Development and Calibration of the tracking Compton/Pair telescope MEGA, Nuclear Instruments and Methods in Physics Research A 541 (2005) 310-322.
[8] S. Takeda, et al., Development of Double-Sided Silicon Strip Detectors (DSSD) for a Compton Telescope, Nucl. Instr. Meth. A 579 (2007) 859–865.
[9] S. Ishikawa, et al., Fine-Pitch Semiconductor Detector for the FOXSI Mission, IEEE Trans. Nucl. Sci. 58, 4, 2011.
[10] H. Tajima, *et al.,* Design and Performance of the Soft Gamma-Ray Detector for the NeXT Mission, IEEE Trans. Nucl. Sci. 52, 6, (2005), 2749.
[11] D. Meier, et al., Development of an ASIC for the Readout of CZT/CdTe Radiation Detectors in Space, Proceedings of the IEEE Nuclear Science Symposium, 2013.
[12] S. Mikkelsen, *et al.,* An ASIC for Multi-Energy X-ray Counting", IEEE Nucl. Sci. Symp. 2008.
[13] AMS AG, Foundry Support, Headquarter: Tobelbader Strasse 30, 8141 Unterpremstaetten, Austria, http://aisc.ams.com

Applications for Radiation Hardened Analogue and Mixed-Signal ASICs: Read-Out-IC

FAIR, a front-end ASIC for infrared detector readout

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Abstract

In the FAIR project (Front-end ASIC for Infrared detector Readout), an IC is developed for the readout of state-of-the-art NIR/SWIR detectors for future Earth observation missions and astrophysics. The chip consists of a high-resolution ADC with integrated offset correction and adjustable gain, and voltage regulators to generate bias/reference voltages for the detector.

The ADC has a 16-bit resolution and offers a sampling rate of 1 Megasample per second. It is designed for an ultra-low power consumption of 16mW. The ADC analog circuitry area is 2mm^2 in 0.18μm CMOS.

The chip is designed to operate in a large temperature range from -218 degrees Celcius up to 50 degrees Celsius, because the original mission goal was for the Exoplanet Characterization Observatory (EChO). The close proximity to the cooled detector requires the read-out electronics to operate at an equally reduced temperature. Considering that the target atmospheric gases addressed by EChO - CH_4, CO, CO_2 and H_2O - are the same as addressed by current and future in Earth-observation missions in the SWIR-IR spectral range (e.g. ESA CarbonSat, CNES MicroCarb), it is clear that the FAIR chip also offers interesting opportunities for application in future Earth observation missions.

The FAIR chip can be placed naturally into the existing electronic readout environment for application to other future IR detectors, replacing and significantly miniaturizing the analog electronics, fitting in the on-going trend of integration in detector electronics for space instrumentation in general: obvious advantages are the reduction of power consumption, volume and weight.

Special analog layout techniques were used to ensure radiation hardness, and all digital circuitry was place&routed using the rad-hard IMEC DARE library.

I. Introduction

There are several upcoming Earth-observation missions that have cooled IR detectors as their baseline, e.g. ESA's Carbonsat, and the French MicroCarb instrument. An ASIC based design for the front-end significantly reduces the budgets on mass, volume, and power, and allows for more flexibility in the board design and integration. Furthermore, it allows the front-end electronics to be placed as close to the (cooled) detector as possible. The analog signals from the detector need only travel a short distance to the ASIC, where they are amplified and digitized. The signal integrity and immunity to electromagnetic interference (EMI) is thus improved. Furthermore the entire front-end IC can be qualified for low temperature operation in one single test campaign.

A typical IR detector front-end readout circuit consists of the following blocks:

1. low-noise high-stability pre-amplifiers with gain and offset compensation
2. analog-to-digital converters (ADCs)
3. power regulators, bias, reference voltage generators
4. housekeeping (voltage / current monitoring)
5. digital clocking and pixel addressing.

As a first step toward a fully integrated front-end chip, we started by integrating the parts most critical for signal integrity: the amplification and digitization of the detector signals. The chip block diagram is shown in Fig. 1. This 'heart' is formed by four independent signal processing chains (to match the four analog pixel outputs of the detector). The chip comprises of a low-noise pre-amplifier functionality with gain and offset compensation and of analog-to-digital converters (ADCs). Furthermore, voltage regulators are included for controlling the IR detector bias & reference voltages.

Pixel clocking, addressing, and configuration functionality is vendor specific. We chose to leave this out of the ASIC. It can be placed in an external FPGA to offer the greatest flexibility and widest applicability to detector chips from different vendors.

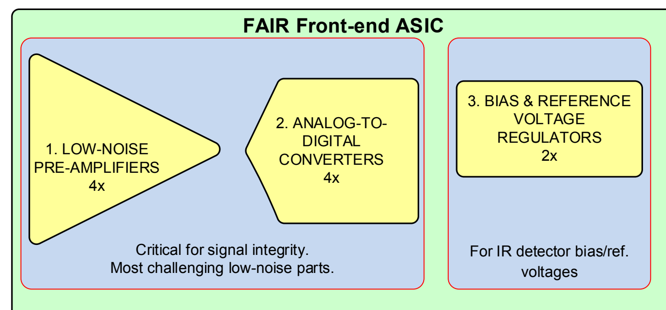

Fig. 1. Block diagram of FAIR front-end ASIC

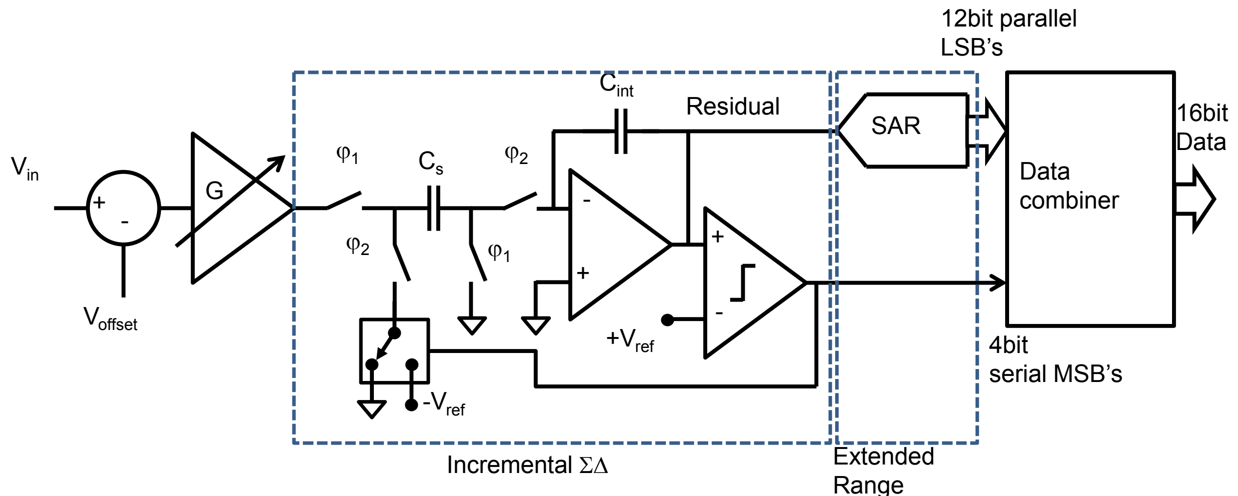

Fig. 2. Architecture of analog signal processing chain.

II. Chip Specifications

The FAIR chip specifications are given in Table 1.

Technology	UMC 0.18um CMOS
Supply voltage	3.3V (analog) 1.8V (digital)
Operating temperature range	40K - 328K
Analog front-end	
No. of independent front-end chains	4
Gain settings	1x, 2x, 4x 8x
Offset compensation range	0.5..3V
Offset DAC resolution	24 bits
Analog input voltage range	0V..3V
Analog input capacitance	12-16pF
Analog-to-digital converters (ADC)	
ADC sampling frequency	1.0 MHz
Analog bandwidth	500kHz
Resolution	16 bits
Effective number of bits (target)	15 ENOBs
Bias and reference voltage generators	
No. of independent regulators	2
Output bias/ref voltage range	0 .. 2.8V
DAC resolution	24 bits
Max current	2mA

III. ADC Architecture

The analog front-end is the heart of the ASIC and its quality is critical to the signal integrity. Our prime focus was therefore on the pre-amplifier and the analog to digital conversion (ADC) for the pixel signals.

The requirements for the ADC are quite stringent. The low noise and low distortion requirements in combination with the sample-rate require a very high-performance ADC. Normally, one would use sigma-delta type of ADC for this purpose, as sigma-deltas can combine high resolution with high sample-rates. (Classical algorithms to obtain high resolution, such as dual-slope converters, operate at much lower sample-rates.) However, a normal sigma-delta converter works under the assumption that the sampled signal is a single band-limited signal and not a multiplexed signal. For a normal sigma-delta to work with a multiplexed signal, the states have to be stored between every signal switch which is not very practical.

To circumvent this problem, a special type of sigma-delta converter has emerged in recent history, which is suitable to convert multiplexed signals, the so-called 'incremental ADC'. For more background information on this type of ADC, see e.g. [1]. A drawback is that incremental sigma-delta ADCs require quite many clock-cycles to reach a high resolution. For example about 400 clock cycles are required per sample when a second-order sigma delta would be used to reach the required 16-bits of resolution [1]. This is much more than the 16 cycles that are required for a classical binary search algorithm. However, converters that typically use search algorithms such as successive approximation (SAR), pipeline or algorithmic ADCs, are not natively suitable to obtain high resolutions (unless very complex calibration algorithms are used).

The architecture of the analog front-end is shown in Fig. 2. To obtain the best of both worlds and combine high resolution with a low number of clock-cycles per sample, a hybrid converters is used. An example of such a converter is given in [2], were an incremental ADC is combined with a successive approximation ADC, with the latter extending the range of the former. In this publication a resolution of almost 16bits (90.1dB) is achieved over a bandwidth of 1MSample/s, with a clock-frequency of only 45MHz (45 cycles per sample).

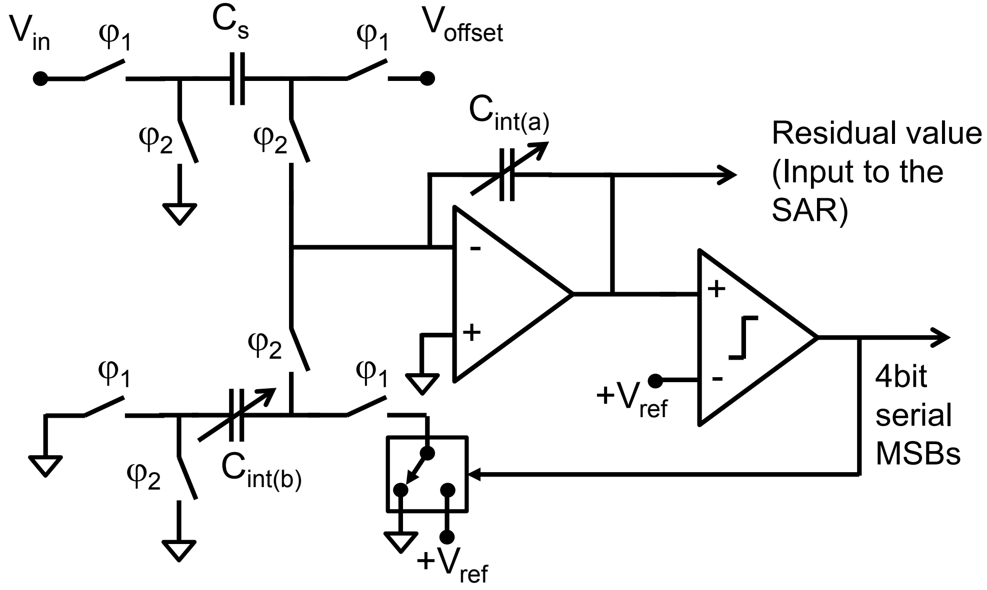

Fig. 3. Incremental sigma-delta front-end circuit with gain and offset cancellation

Such a hybrid converter is also best suitable for this application. The remaining challenge in this project was to further reduce the noise-floor to more than 16 bits and create a system that is radiation hard and can operate at low temperature.

A. ADC front-end with offset compensation and adjustable gain

Implementation of the offset cancellation circuit and the variable gain preamplifier for the ADC in a traditional way would require extra active circuits. An offset compensation mechanism is required because the base level of the IR detector output is around 1.0V (no light). An adjustable gain is needed to be able to use the full ADC resolution under any light conditions. Two extra opamps (beside the opamp used for implementing the integration function) would be needed for the mentioned purposes. The existence of these circuits at the front of the ADC would add extra noise and nonlinearity to the input signal. Therefore they would need to be designed quite linearly and would need to consume enough power to satisfy the low noise requirements of the 16bit conversion. The power consumption limitations required a new circuit topology to satisfy all functions with the lowest possible number of active circuits. Therefore, a new circuit topology has been introduced which merges offset cancellation, gain and integration functions into a single circuit.

In Fig. 3, the front-end circuit is shown. During phase φ_1, V_{in}-V_{offset} is sampled at capacitor C_s and during phase φ_2, the sampled value is integrated on $C_{int(a)}$. At each period the output voltage of the integrator (residual value) is compared to a fixed reference voltage ($+V_{ref}$), and in case of exceeding a fixed amount of charge is subtracted from C_{int}(a). The subtraction action is done via charging $C_{int(b)}$ to the ($+V_{ref}$) voltage. The tunable capacitors $C_{int(a)}$ and $C_{int(b)}$ are equal to each other. The pre-amplification factor for the total circuit is controlled by changing the ratio between C_s and $C_{int(a)}$. A 0-20dB controllable gain with a 3dB step size was implemented by this technique. After 16 cycles of integration in the incremental sigma delta converter, 4 serial bits come out and also a residual value comes out. The residual value is fed to the SAR to produce the rest of the 12 bits. The total operation is called "Extended range incremental sigma delta converter" and results in a 16 bit resolution. No ADC range is lost due to the offset voltage compensation mechanism.

B. Low-temperature operation

The low temperature operation at 55 Kelvin gives two effects on the CMOS transistors:

1) higher threshold voltages for the CMOS transistors

2) higher carrier motilities (low scattering).

At 55 Kelvin, compared to operation at the room temperature (27°C), transistor transconductance will be higher for the same current consumption. The g_m of each single transistor changes with 1dB in this range. Therefore in this large operating temperature range, gain of the opamps can vary and cause instability. Therefore large phase and gain margins for the integrators were taken to satisfy the operation of the system both at room temperature and 55 Kelvin temperature.

IV. BIAS / REFERENCE VOLTAGE REGULATORS

The bias / reference voltage regulators have a PMOSt common source output stage, and the feedback resistors are used as a load (therefore an NMOSt current source is not

needed). The opamps in the regulators have a PMOSt input pair. In Fix 4, the circuit diagram is shown.

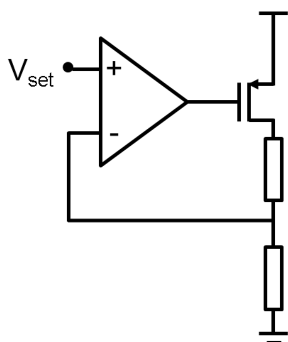

Fig.4. Bias / reference voltage regulator circuit

V. Chip Design

The GDS of the complete design is shown in figure 5. This is the end version as submitted to the fab. On top, there are 4 ADCs. On the bottom, from left to right: the bias/ref. voltage regulators (small block), and 3x the DACs (large blocks). One DAC generates the offset voltage as an input to the ADCs, and the other two are for the bias/ref. regulator control. The dark blue space between the blocks is filled with rad-hard cells from the DARE library (sea-of-gates).

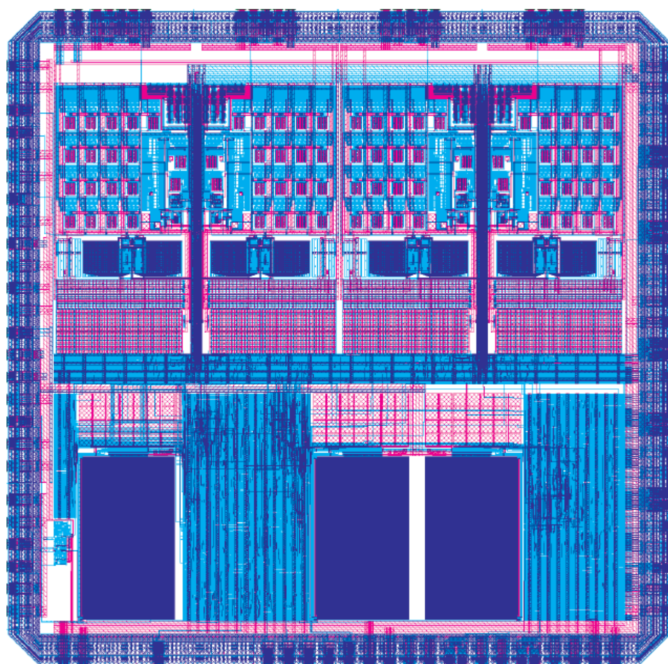

Fig. 5. GDS view of the complete design

VI. Planning

The packaged chip will be back from processing in July, and then we will start measurements.

VII. Conclusion

An IC for the readout of state-of-the-art NIR/SWIR detectors for future Earth observation missions and astrophysics was presented. The 16 bit, 1 Megasample/s, 16mW ADC with hybrid sigma-delta/SAR architecture offers integrated offset correction and adjustable gain. The ADC analog circuitry area is $2mm^2$ in 0.18μm CMOS. Voltage regulators are included on the chip to generate bias/reference voltages for the detector. The chip is designed to operate in a large temperature range from -218 degrees Celcius up to 50 degrees Celsius. Testing will start in July 2014.

VIII. References

[1] Markus, J.; Silva, J.; Temes, G.C., "Theory and applications of incremental ΔΣ converters," Circuits and Systems I: Regular Papers, IEEE Transactions on , vol.51, no.4, pp. 678- 690, April 2004.

[2] Agah, A.; Vleugels, K.; Griffin, P.B.; Ronaghi, M.; Plummer, J.D.; Wooley, B.A. , "A High-Resolution Low-Power Incremental ΣΔ ADC With Extended Range for Biosensor Arrays," Solid-State Circuits, IEEE Journal of , vol.45, no.6, pp.1099-1110, June 2010.

Analog Front End Integrated Circuits for Mixed Signal Spacecraft Applications

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Abstract

By definition mixed signal systems include a digital processing function and an analog or power function. When complex circuits are integrated to reduce parts count, it is typically not optimal to combine the analog and digital portions in one device. Application targeted Analog Front End (AFE) ICs tend to be a more efficient combination of circuitry than a random programmable analog array. By partitioning the majority of the digital circuitry in a programmable device such as an FPGA, control functionality can be readily programmed using an intuitive hardware definition language such as VHDL or Verilog. An AFE reduces the number and complexity of the analog to digital communication links.

I. Introduction

Digital electronics are designed to function at low voltages to minimize power dissipation due to logic transitions. The digital sensor interfaces that are present in the spacecraft environment typically must be buffered to be compatible with I/O thresholds of the digital circuits. [1] Provision must be made for ground references within the spacecraft which introduce common mode voltage differences between the sensor and monitoring equipment. Linearly varying signals are not compatible with logic and must therefore be sampled and converted to digital format. Power delivery is not possible with the limited current sourcing ability of the digital I/O. Redundant control interfaces require cold sparing which is typically not supported by digital I/O. Table 1 summarizes typical signal conditioning provided by the AFE.

Table 1: Typical AFE signal conditioning functions

- Differential Receiver
- Level Shifting
- ADC or DAC Converters
- Power Driver
- Cold Sparing
- Bi-level logic buffer

II. Discussion

The best approach for implementing an AFE is to target a specific range of applications and combine the commonly used functions for those applications. A more flexible approach is to implement the design using single function ICs, but this has the drawback of requiring a large number of components and circuit board area. A more integrated solution is to design a fully custom AFE for a particular application; this is the least flexible solution if the requirements change. The development of custom ICs also presents a schedule risk and requires the investment of NRE costs. Another approach is configurable general purpose analog circuitry; the popularity for these parts comes from the metaphor they represent AFEs with configurable higher level functions. [2] Table 2 summaries the pros and cons of the first three approaches.

Table 2: AFE implementation approach comparison

	Single Function ICs	AFE	Custom
NRE	Low	Low	High
Development Time	Months	Months	Years
Qualification	Fast	Fast	Long
Risk	Small	Small	High
Flexibility	High	High	None
Power	Worst	Good	Best
Reliability	Average	Excellent	Excellent
Size and Weight	Poor	Good	Best

The development time and schedule risk are reduced when the AFE solution is available as a prequalified standard part. Reducing the part count through integration helps reduce size and weight and improves reliability at the system level.

FPGA processes optimized for spacecraft SEE immunity have specific provisions such as Triple Modular Redundancy with voting logic help mitigate single event upsets due to radiation. [3] Anti-fuse programming offers better retention

than other forms of reconfigurable logic. The FPGA utilizes a smaller geometry process than can be used to implement radiation tolerant mixed signal designs; this results in denser more highly integrated solutions than are possible with a mixed signal process. AFE processes can utilize higher voltage devices that tolerate a wide range of input voltages. Processes with dielectric isolation (DI) allow for fault tolerance between sections of circuitry such that a failure in one place on the die does not impact adjacent circuits.[4] Bipolar CMOS DMOS (BCD) processes provide a combination of bipolar devices for developing precision bandgaps and linear circuits, CMOS devices for logic and switches and DMOS devices for high current capability. The separation of the digital functions from the analog and power functions allows for process optimization of both resulting in smaller size, increased reliability and improved performance.

Table 3: Specialized digital and analog process advantages

Process	Attribute	Advanatage
Digital	Small geometry	High density
	Anti-fuse	High retention
	Triple redundancy	SEU immunity
Analog	Higher voltage	Wide range I/O
	DI process	Fault containment
	BCD process	High power and Precision linear

Using an FPGA to implement the data processing function has several advantages. If there are multiple data paths, it is possible to provide parallel processing of each path allowing multiple data pipelines. If the FPGA is equipped with math blocks that efficiently implement multipliers, these data processors can quickly perform complex arithmetic. The FPGA can also be sized to the application providing only the needed number of logic cells for high utilization.

Table 4: Some FPGA advantages over microprocessor

- Parallel processing
- Complex math using predefined math blocks.
- Number of gates per device scalable to application

Several areas of spacecraft design are well suited for AFE integration. Telemetry is an application where a large number of sensors are monitored for health monitoring or attitude adjustment. The sample rate required can be relatively slow since the changes are gradual; the sensors can be monitored sequentially rather than continuously. A multichannel multiplexer is a common circuit to integrate into an IC. For motor driving applications, typically a power driver is required and position sensing is often used for feedback to control the speed, torque and position. For power control applications, power is switched, sequenced, supervised and adjusted.

Table 5: Applications benefiting from AFE

- Telemetry management
- Motor Control
- Power Control

Sensors can typically be passive or active. Passive sensors require an applied stimulus such as a current to provide a measurable voltage. A four wire technique is typically used for this type of measurement where a current is directed into the sensor to develop a voltage and a voltage measurement is taken across the terminals of the sensor to reduce errors that can occur due to line drops in the higher current path; this is particularly useful when measuring low impedance sensor voltages such as RTDs (resistor temperature detectors). A higher impedance sensor such as a thermistor might tolerate a two wire measurement and still provide sufficient accuracy.

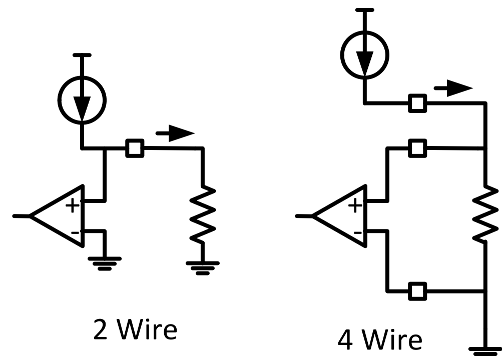

Figure 1: Two and four wire measurements

One method of configuring an AFE is through control registers. Typically a register map defines which bit codes must be written to the control registers to initiate certain commands. Similarly data can be extracted from the AFE using status register reads. For space applications and AFE can be provided with a redundant control interface. In the case of the LX7730, two SPI interfaces are provided.[5]

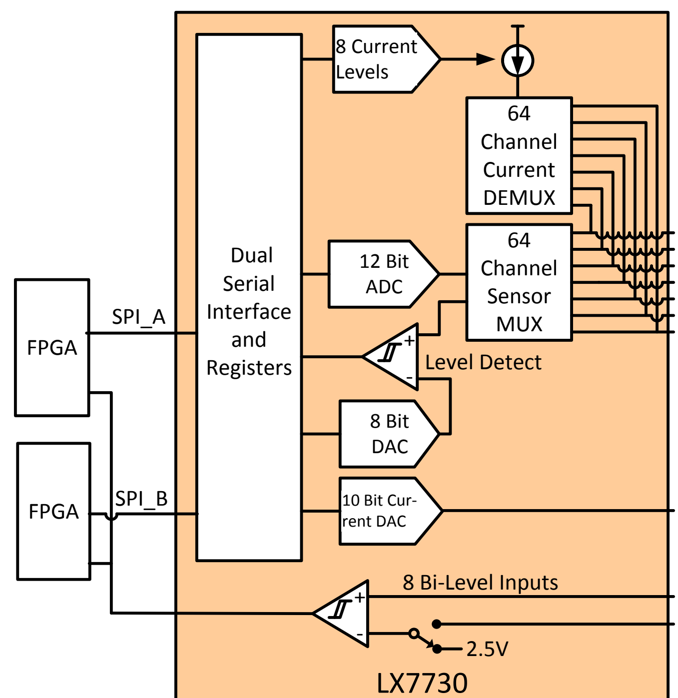

Figure 2: Block diagram of Telemetry AFE

An AFE optimized for telemetry measurements would contain inputs that were configurable for single ended or differential inputs and a current de-multiplexer that can be used to stimulate passive sensors. With the 64 channel multiplexer in Figure 3, the inputs of this device can be configured as any combination of single ended or differential inputs. When using single ended inputs, 8 of the channels can be simultaneously routed to a level detector comparator bank.

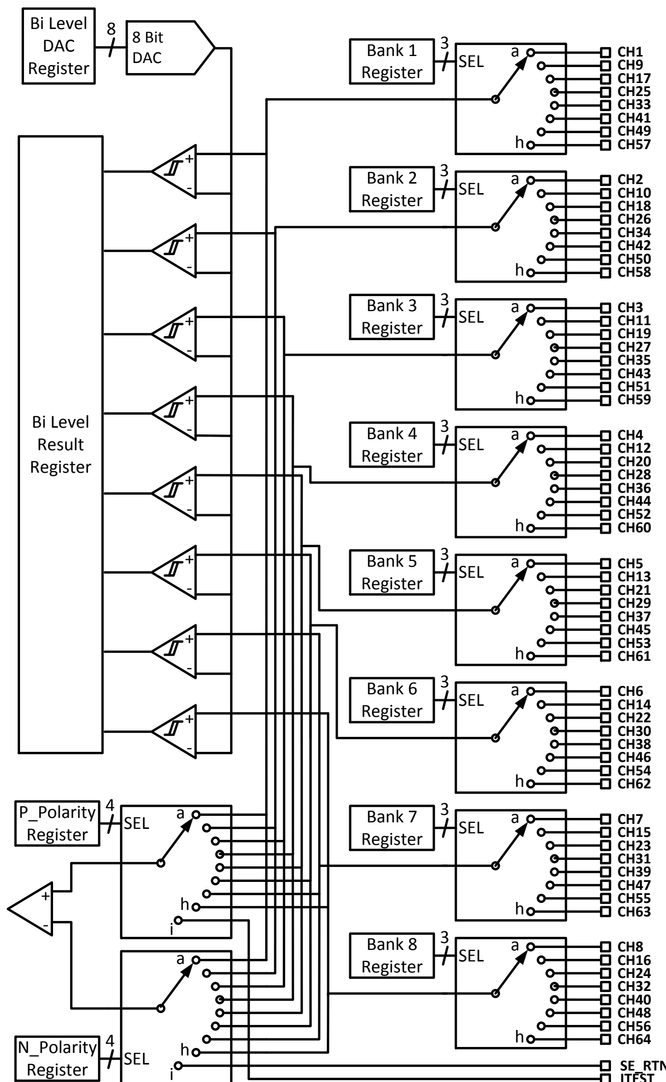

Figure 3: Multifunctional Sensor Multiplexer

The HDL modules being developed to support the LX7730 AFE include:

Table 6: HDL modules for support of telemetry management

- SPI interface
- Parallel interface
- Single register reads and writes
- Data logging routine
- Calibration

An AFE used for motor driving applications requires a high power half bridge configured driver; using external transistor switches allows the driver to be sized to the voltage and current required for the application. An N channel switch typically has a lower resistance than a P channel; an upper N channel transistor driver is floating and receives power via a charge pump or boot strap. Motor coil currents are typically sensed and used as part of the control loop for the motor torque. Sensing motor currents directly at the output of the half bridge on the switch pin gives the most accurate reading for the motor coil current. Unfortunately, since the switch pin moves between the upper rail and ground with the PWM switching action, there is a large common mode signal present at the current sensor resistor terminals. Using several stages of amplifiers and level shifters it is possible to accurately extract this current with integrated circuit techniques. The diagram in figure 4 shows one of four half bridge drivers in the LX7720. [6]

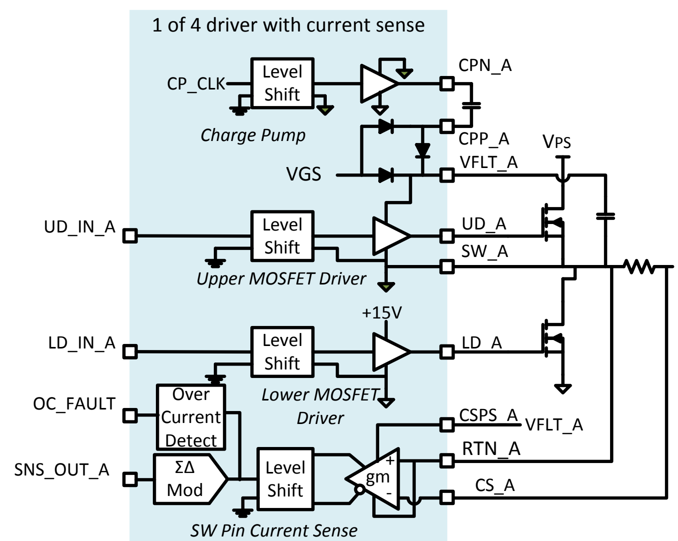

Figure 4: Half bridge power driver with current sense

The output of the current sensor is a ΣΔ modulated ones density data stream that feeds directly into the FPGA. This data has its own dedicated processing pipeline in the FPGA where the sin3 filter and decimator reside. The application can determine the tradeoff between number of bits and the latency limit required by adjusting the decimation rate.

Motor driver applications that use field oriented control require feedback on the position of the motor rotor relative to the stator fields. Resolver transformers coupled to a tracking speed and position algorithm (Resolver-to-Digital) can be used for this. Where motors drive a precision actuator, a linear variable differential transformer (LVDT) is used to sense linear speed and position. These transformer systems require a reference carrier to drive the transformer and a demodulator to extract the sine and cosine angle data from the transformer outputs. A digital processor can implement the tracking conversion but requires a precision ADC input with typically 15 to 16 bit accuracy.

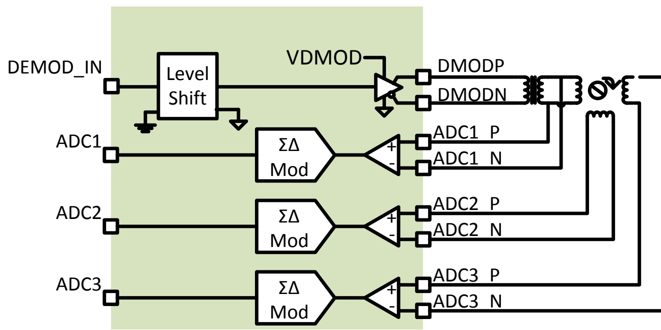

Figure 5: Resolver or LVDT AFE interface

The DEMOD_IN is a pulse stream that is continuously loop read from a lookup table and represents the ΣΔ modulated carrier; the transformer magnetizing inductance provides the filtering to remove the modulation leaving the carrier fundamental. ADC1 monitors the carrier amplitude and ADC2 and ADC3 provide the modulated sine and cosine inputs. These are sigma delta modulated inputs that feed directly into dedicated FPGA processing pipelines.

In some cases an optical encoder or hall sensors are used to provide motor position feedback and the AFE should provide bi-level inputs with adjustable thresholds to sense these inputs and level shift them to FPGA compatible levels.

The complete motor driving system for a brushless DC motor is diagrammed in Figure 6.[7] The blocks that are colored blue are implemented in the FPGA and the blocks that are colored green are implemented in the AFE.

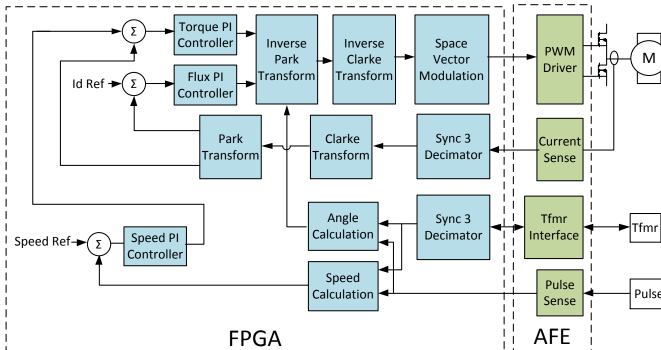

Figure 6: Motor control partitioning

The motor driver AFE is designed to be universal and can also be configured to drive permanent magnet synchronous motors, bipolar stepper motors or unipolar stepper motors. Several VHDL modules are in development to support these applications:

Table 7: HDL modules to support a motor driver system

- 2 phase bipolar drive with microstepping
- Stepper average current regulation
- Sinc 3 filter and decimator w adjustable accuracy
- Pulse exciter for Resolver or LVDT
- Tracking Resolver to digital converter
- BLDC motor with trapezoid drive
- PMSM with sinusoidal drive
- Field oriented transformations
- Space vector modulation
- Fault management

III. Summary

The use of a standard integrated circuit AFE paired with a configurable FPGA takes advantage of high levels of integration. Separation of the analog and digital functions allows IC process optimization for both the implementation of the digital and the analog functions. The application targeted AFE provides a higher level of integration over an implementation of basic single function ICs but avoids the development expense and time associated with developing a fully custom IC. Higher integration reduces parts count which improves reliability and reduces size and weight of the spacecraft electronic modules.

IV. References

All bibliographical references should be numbered and listed at the end of the paper in a section called "REFERENCES". When referring to a reference in the text, place the corresponding reference number in square brackets [1], [2], [3], etc...

Example:

[1] Vincent Piscane. (2005). Fundamentals of Space Systems 2nd Edition. Text Book: Pages 616-622

[2] Ron Wilson. (2009). Programmable Chips: Piecing Together an Analog Solution. Magazine Article: EDN Network

[3] Sana Rezgui, et al. (2010). SEE Characterization of the New RTAX-DSP Antifuse-Based FPGA, IEEE Transactions on Nuclear Science

[4] NAVSEA SD-18. (2006). Radiation Tolerant Isolation Technology

[5] LX7730, 64 Analog Input Rad Tolerant Telemetry Controller, Datasheet, Microsemi (available on request)

[6] LX7720, Rad Hard Spacecraft Power Driver with Rotation and Position Sensing, Datasheet, Microsemi (available on request)

[7] Microsemi Users Guide (2012). Smart Fusion Field Oriented Control of Permanent Magnet Synchronous Motors Using Hall and Encoder

[8]

A Complete Space Based CCD Biasing Solution in a 0.35µm High Voltage CMOS ASIC

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Abstract

An ASIC designed to fulfil the role of a general purpose bias voltage generator for CCDs in space based camera systems is presented. The STAR (Space Telemetry And Reference) chip has been developed to reduce both the size and power consumption of the circuitry required to bias a science grade CCD. Implemented in a 0.35µm 50V tolerant CMOS process, STAR provides 24 independent voltage outputs with a 32V range and noise of <100µV. Each output channel features a 10-bit DAC and a high voltage output buffer to provide current drive of up to 20mA. The output buffer can drive loads of 1KΩ / 10µF, and also includes output current limiting for short circuit protection.

An on-board telemetry system featuring a 12-bit ADC and programmable gain buffer allows measurement of the output voltages from the chip as well as up to 32 single ended and 4 differential external voltages. Control of the ASIC is via an SPI interface and all required voltages and currents are generated from internal bandgap circuits. Layout of the circuits uses established radiation hardening techniques with the intent that the circuit be SEL (Single Event Latchup) immune by design. Designed for encapsulation in a 144 pin package the STAR ASIC replaces an entire PCB of discrete electronics in current camera electronic systems.

Details of the chip architecture and circuit design will be presented, along with simulated performance and test results.

I. INTRODUCTION

At present the vast majority of space based optical wavelength camera systems use CCDs at their focal plane, particularly for scientific instruments requiring high quality images with minimal noise. These devices often operate at higher voltages falling outside the range of standard ASICs or FPGAs. Discrete drive circuits are therefore needed to reach the required signal levels. However these circuits bring with them associated issues of increased power consumption, PCB area and instrument mass. Finding suitable space qualified parts for these circuits is also an ever-present problem for the designer. Figure 1 shows the camera electronics box supplied by STFC Rutherford Appleton Laboratory for the HMI and AIA instruments on NASA's Solar Dynamics Observatory [1]. In this already compact system one of four PCBs used for operating the attached CCD (the second card from the top in figure 1) is entirely devoted to discrete circuits generating bias voltages.

In this paper a high voltage mixed signal ASIC is described which has been developed to address this problem. The STAR (Space Telemetry And Reference) ASIC integrates all the circuitry required for generating programmable biases of up to 32V with on-chip references and a housekeeping telemetry system in a single die. The device requires only appropriate power supplies with decoupling, a single noise filtering capacitor, and a digital serial interface to operate, making it a simple and highly compact alternative to traditional discrete biasing solutions. The device is designed to replace the entire biasing PCB required for systems such as the electronics box in figure 1.

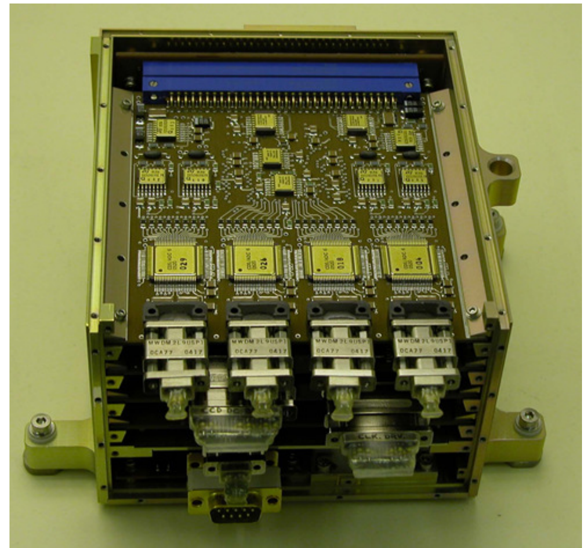

Figure 1: Camera electronics box from the HMI & AIA instruments on NASA Solar Dynamics Observatory. The CCD biasing circuitry occupies one of the lower circuit boards.

The paper will be arranged as follows: section II will describe the architecture of the STAR ASIC and provide details of its sub-blocks, section III contains test results from the prototype devices, and section IV discusses conclusions and future work.

II. ASIC ARCHITECTURE

The STAR ASIC provides 24 independently controllable, low noise bias voltages with an output range of 0-32.736V and a current drive capability of +/-20mA, plus a short circuit current limit of +/-25mA. Each output can drive resistive loads as low as 1kΩ and provide stable operation with load capacitances from 10pF up to 10µF to allow for loading from the CCD and cable harness plus noise filtering. The telemetry system allows monitoring of the generated voltages, plus point-of-load external connections, differential temperature monitors, and general purpose uncommitted inputs. Control of the system is via a simple digital SPI interface operating at standard 3.3V CMOS logic levels. All required bias voltages and currents are generated on-chip, and no additional active

circuitry should be required to operate the chip. The low voltage portions of the chip operate on a 3.3V supply while the output buffers in each channel require high voltage supplies, nominally 35V and -2.5V. The device is designed to operate across a military temperature range (-40°C to 125°C) and be resistant to radiation Total Ionising Dose (TID) up to at least 100kRad and Single Event Effects (SEE) such as upset or latchup. A functional block diagram of the circuit is shown in figure 2.

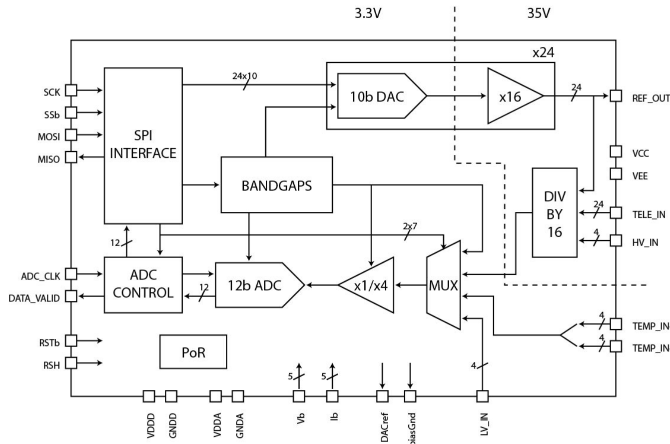

Figure 2: Functional block diagram of the STAR ASIC.

A. *High voltage output channels*

Control of the output bias voltages is achieved using 10 bit segmented resistor string DACs [2] in each channel. Each DAC is provided with an individually buffered 2.048V reference voltage taken from a master DAC reference produced by the voltage bandgap circuit. This gives an output range of 0-2.046V in 2mV steps. The structure of the DAC using two 5-bit stages is shown in figure 3.

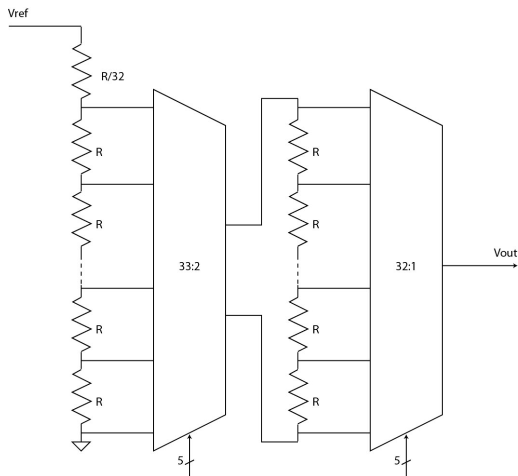

Figure 3: Schematic showing the segmented resistor string DAC.

An amplifier with a gain of 16, realised with a high voltage class AB differential input op-amp, is then used to boost the output voltage to the required 32V output level. The amplifier (shown in figure 4) is constructed using a PMOS input folded cascade first stage and a class AB second stage with cascoded compensation and floating control cell [3]. To save power the input tail current source is run on the low voltage 3.3V power supplies, while the rest of the circuit runs on the high voltage supplies. The amplifier power consumption is 22.7mW running on 35V and -2.5V supplies and can source or sink up to 20mA into a 1kΩ while maintaining amplifier accuracy to 10b. Current mirrors inserted in series with the op-amp output stage (not shown in figure 4) limit the output current to +/-25mA, to prevent damage to the chip in case of a short circuit in one of the load components. Since the amplifier is designed to provide DC bias voltages it is compensated to provide a low small signal bandwidth of approximately 60kHz for noise reduction. The amplifier has an output slew rate of 0.55V/µs giving a full power bandwidth of 5.3kHz.

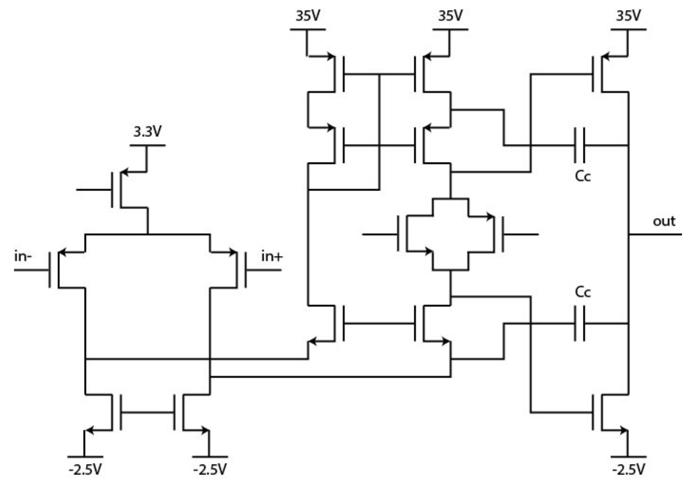

Figure 4: Schematic of the high voltage buffer amplifier.

The op-amp is used in a resistive feedback non-inverting configuration as shown in figure 5, with a gain set to 16 (Rg = 4kΩ, Rf = 60kΩ). A signal dependant current of up to 512µA therefore flows through Rf and Rg. The resulting circuit in conjunction with the DAC has an output range of 0 - 32.736V with a resolution of 32mV. To help ensure amplifier stability across the full 10pF – 10µF range of capacitive loads a series output resistor (Rs) of 25Ω is included to enhance the amplifier phase margin.

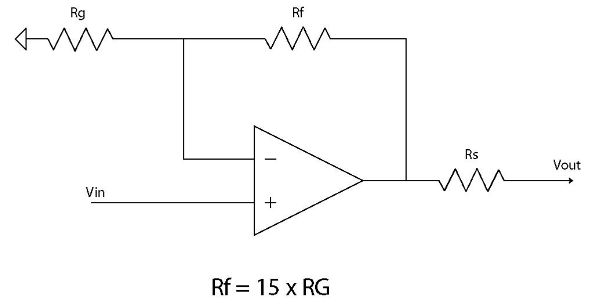

Figure 5: Feedback arrangement of the high voltage output buffer.

B. *Telemetry system*

The telemetry system incorporated into STAR is designed to allow monitoring of the 24 output bias voltages plus all voltages generated on-chip. External inputs for point-of-load monitoring of the biases are provided, or for measurement of other system voltages. An additional 8 uncommitted inputs

are also available for this purpose (four low voltage inputs and 4 high voltage inputs). Finally four pairs of differential inputs allow PRT bridge circuits to be connected for temperature monitoring.

The system is constructed from a twin channel analogue multiplexer, a differential input variable gain amplifier, and a 12 bit Successive Approximation Register (SAR) ADC. The multiplexer includes 16:1 resistive dividers on its inputs where appropriate for scaling high voltage signals to match the 2.048V input range of the ADC. The two independently controllable paths through the multiplexer facilitate either differential inputs, or measurement of an input against a selectable internal or externally provided reference.

The variable gain amplifier is used to buffer the multiplexer signals and drive the ADC input capacitance. It is implemented as a switched capacitor amplifier circuit with a selectable gain of 1 or 4 to allow amplification of smaller signals, and also performs the necessary level shifting to match the single ended output to the input range of the ADC. The architecture is shown in figure 6. Operation of the buffer is tied to that of the ADC, with switches phi1 being closed while the ADC is idle or converting, and switches phi2 only being closed when the ADC samples an input. This means the inputs are sampled during the reset phase of the amplifier and allows the voltages on Cin a longer period settle, reducing the bandwidth requirements through the multiplexer.

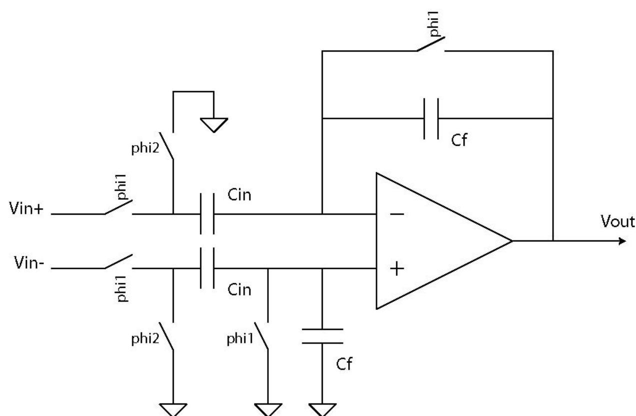

Figure 6: Variable gain multiplexer buffer architecture

The ADC itself uses a single ended 4 bit resistor string / 8 bit capacitor array architecture with a 2.048V input range between 0.512V and 2.560V, operating at up to 667kSPS with a 10MHz clock. Control of the ADC is via dedicated clock and sample signals taken from external inputs, with an external data valid signal indicating when data is available for retrieval via the SPI interface.

C. *Digital interface*

Control of all the ASICs remaining functions and setting is via a 3 or 4 wire SPI serial interface operating on standard 3.3V CMOS logic levels. This is used to access an internal register bank controlling chip functions, which is implemented with Triple Module Redundancy (TMR) to provide protection from Single Event Upsets (SEU). A dedicated 'refresh' signal is included in the design to update any registers affected by a Single Event Upset (SEU) with corrected data from its TMR voting circuit when the SPI clock is not running. ADC conversion data is also accessed from a read only location in the memory map of the SPI interface. The SPI interface uses a 16 bit word length and supports burst mode read and write operations.

D. *Reference voltages and currents*

The required reference voltage and currents on the STAR ASIC are generated from a pair of on-chip bandgap reference circuits based on the low voltage architecture detailed in [4]. Each bandgap includes a 5 bit current mirror DAC at its output to allow for trimming out of errors due to process variations. The voltage bandgap circuit provides a range of voltages used in the telemetry system and the master DAC reference voltage. The current bandgap produces a single reference used to set bias currents in all the circuit amplifiers and output current limiters. A power-on reset circuit is also included to ensure correct known operating conditions after power-up.

E. *Process and layout*

Due to its intended application the STAR ASIC will be exposed to the radiation environment of space. For this reason the H35 2 poly 4 metal 50V 0.35µm CMOS process from AMS was chosen for the fabrication of the STAR ASIC due to the availability of 50V tolerant transistors and the suitability of the process for use in radiation environments with relevant layout techniques [5, 6]. Guard banding was applied to all elements of the layout to provide enhanced protection from SEL. The completed STAR die size is 15.125mm x 13.955mm, the layout is shown in figure 7.

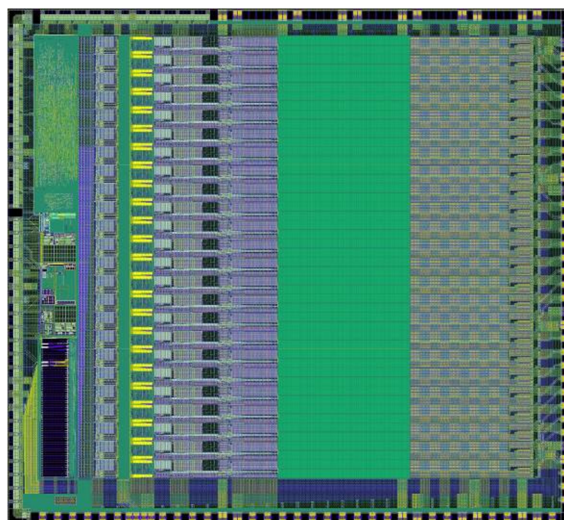
Figure 7: Layout of the STAR ASIC

F. *Power dissipation*

Each circuit on the ASIC (with the exception of the bandgaps, some biasing circuits, and the power on reset) has a power down mode to enable unused circuits and channels to be disabled if not required and save power. The ASIC powers up in the minimum power state with only the bandgaps and basic biasing circuitry active. The telemetry circuits and ADC, channel DACs, and HV output buffers can then be enabled individually. The minimum power dissipation of the circuit at power on is 36.57mW, and maximum with all circuits activate and outputs driving 32.736V is 1.17W. A

breakdown of current and power consumption by power supply and circuit element is shown in table 1.

Table 1: Current and power consumption by circuit element and power supply.

Circuit	Current by supply (A)			Power (W)
	3.3V	35V	-2.5V	
Biasing	2.9m	0.72m	0.72m	36.57m
ADC	6.6m			21.78m
DAC (each)	0.61m			2.01m
HV output (each)	0.21m	0.67m	0.83m	26.22m
HV feedback resistors (each)		15.63µ/V		546.9 µ/V
Full 24 channels driving 32.736V, no load current	29.18m	29.08m	20.64m	1.17

III. Results

A. *Test system*

The completed design of the STAR ASIC has been fabricated and the unpackaged die mounted on a carrier PCB for evaluation (shown in figure 8). Testing was carried out using a National Instruments PXI crate to provide analogue and digital stimulus and measure the analogue outputs from the ASIC. An interface PCB was used for signal multiplexing, cable connections, and to implement load circuits for the bias outputs. Each output was connected to selectable load resistors of 680Ω, 1.5kΩ or 15kΩ connected to the positive or negative high voltage supplies to control load current. A 4MΩ resistive divider to ground, feeding the output to the NI ADC card, was present on all outputs. All but five of the outputs were connected to a fixed 1nF capacitor. The five remaining channels (0, 5, 11, 17, and 23) had selectable capacitive loads of 10pF, 1nF, 100nF, 1µF or 10µF to investigate output stability and noise filtering. A high pass RC filter on these channels was used to remove the DC component of the outputs before high resolution noise measurement. Tests were carried at 22°C with a low voltage supply at 3.3V and high voltage supplies of +35V and either -2.5V or -5V.

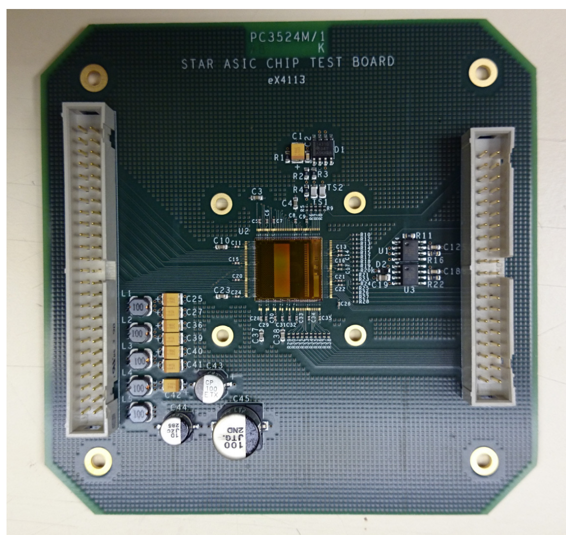

Figure 8: Prototype STAR ASIC bonded to a carrier PCB.

B. *HV outputs*

Testing of the high voltage bias outputs was conducted for the full range of resistive and capacitive loads on each output, representing the range of likely operating conditions for the device. The outputs were found to be stable for all capacitive loads up to 10µF. Gain and offset measurements were taken for all channels in an unloaded state (only the 4MΩ resistive divider to ground connected), the results being shown in figures 9 and 10. In all cases it can be seen that the gain is accurate to <0.3% and the zero offset measured is less than 1LSB (32mV). All channels were demonstrated to be monotonic with the worst case channel DNL and INL measurements shown in figure 11 and figure 12 respectively. The transitions between sub-ranges in the DACs give rise to the saw-tooth pattern in the INL plot and spikes in the DNL plot.

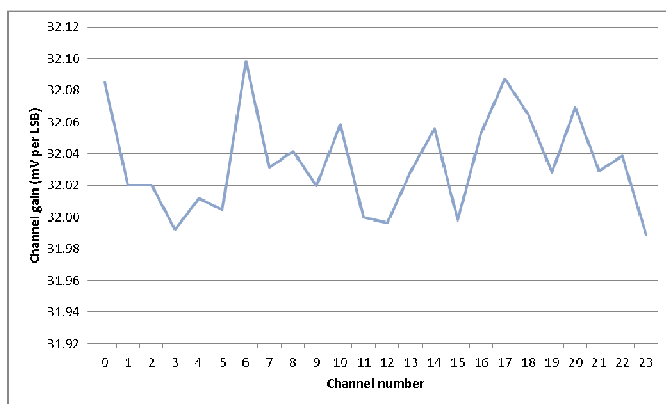

Figure 9: High voltage output gain by channel calculated from least-square straight line fit, nominally 32mV/LSB (4MΩ load to ground).

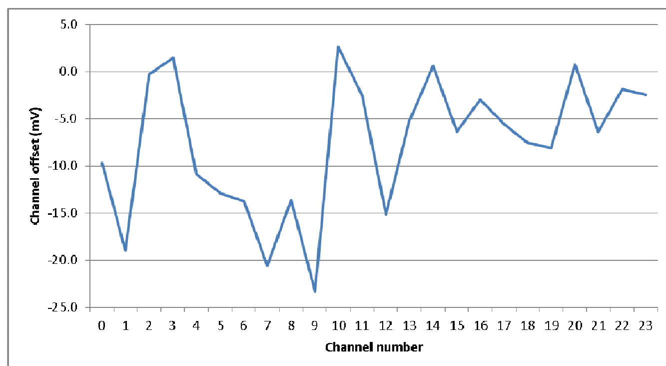

Figure 10: High voltage output offset by channel, calculated from least-square straight line fit (4MΩ load to ground).

Measurements of noise were carried out as a function of output voltage and load capacitance for each of the 5 channels with selectable capacitors. The results from a representative channel are shown in figure 13. At low load capacitances the noise is dominated by thermal noise from the output amplifier and feedback resistors. At higher loads noise from the DAC reference buffer and DAC resistance become significant giving a slope proportional to DAC code. The ripple seen in the plots is the result of the changing equivalent resistance of the channel DAC as it moves through sub-ranges.

Short circuit current limits for all channels were tested and confirmed to be 25mA +/- 5% in all cases.

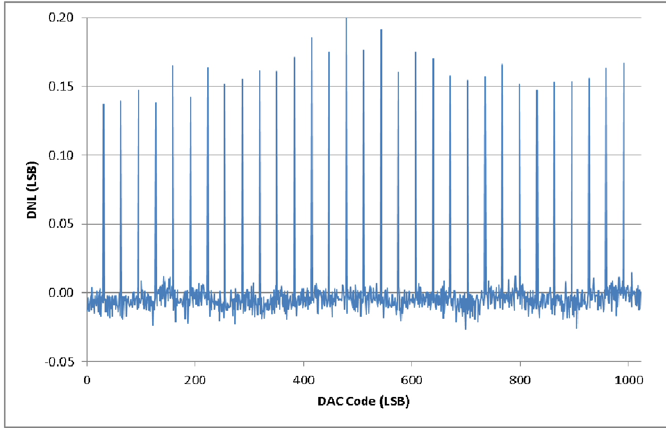

Figure 11: High voltage output DNL measurement of worst case high voltage channel output (channel 9, 4MΩ load to ground).

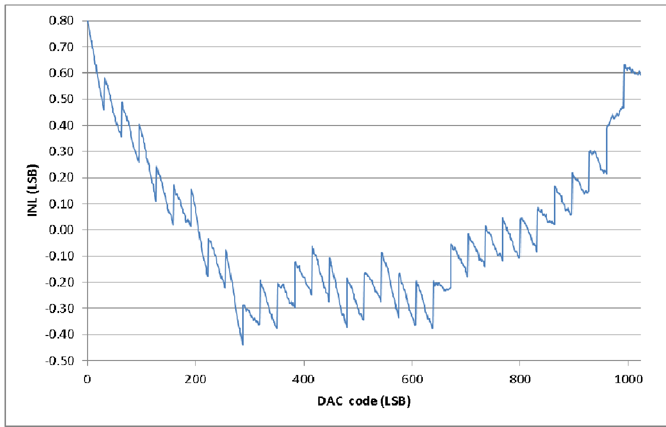

Figure 12: High voltage output INL measurement of worst case high voltage channel output (channel 8, 15kΩ load to -2.5V).

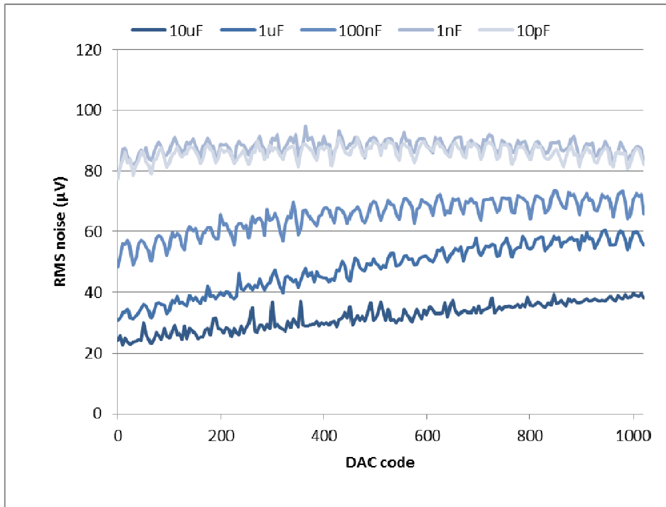

Figure 13: High voltage output noise as a function of DAC setting for a variety of load capacitances, (channel 11, 15kΩ load to +35V).

C. ADC & Telemetry system

The telemetry system and ADC were tested using a DAC outputs from the NI crate via one of the uncommitted inputs to the telemetry system. The test signal was then swept across the native 0.512V – 2.560V range of the ADC against the internal ADC mid-range reference voltage of 1.536V. The multiplexer gain buffer was set to 1 for these tests. The DNL and INL of the telemetry ADC are shown in figures 14 and 15 respectively. The telemetry system as a whole showed an INL of -1.26 LSB and a DNL of -0.43 LSB. The measured noise of the telemetry system as a function of input voltage is shown in figure 16. The mean measured noise was 0.73 LSB.

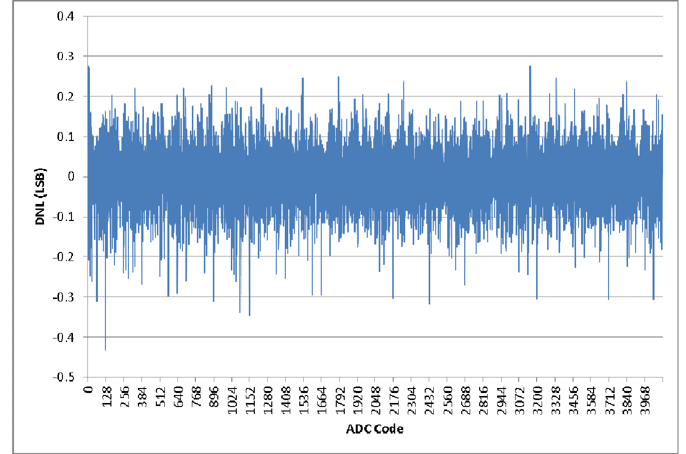

Figure 14: Telemetry ADC DNL measurement for a mux buffer gain of 1.

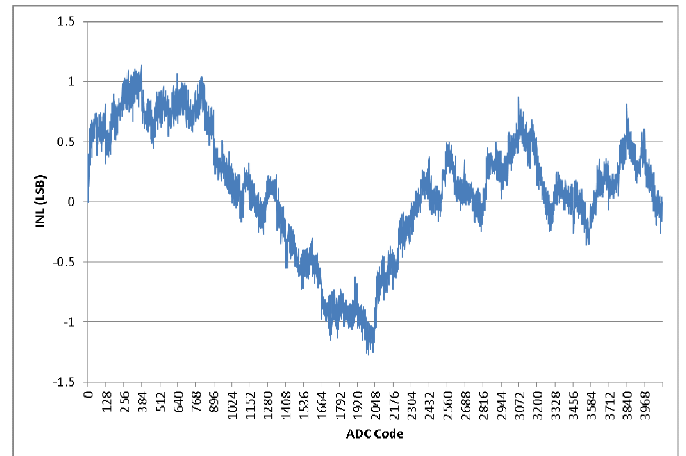

Figure 15: Telemetry ADC INL measurement for a mux buffer gain of 1.

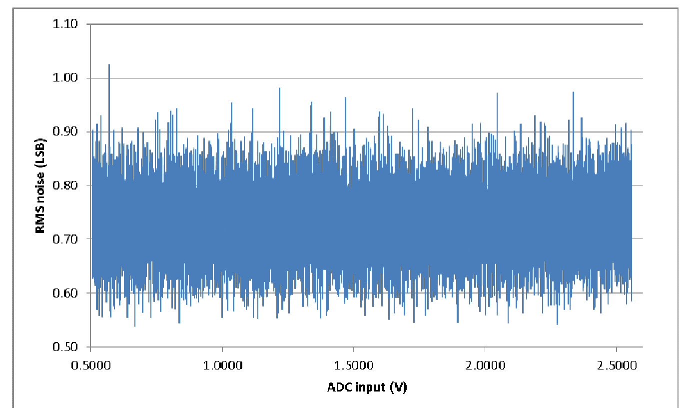

Figure 16: Telemetry ADC noise as a function of input voltage for a mux buffer gain of 1.

D. Reference voltage and current

The bandgap circuit output voltages and currents were measured at a fixed temperature of 22°C. The current and voltage references were tested across the range of possible trim settings for each, the results being shown in figure 17. For both circuits the range of trimming adjustment was found to be sufficient to reach the nominal outputs for each circuit, being 2.048V and 300µA.

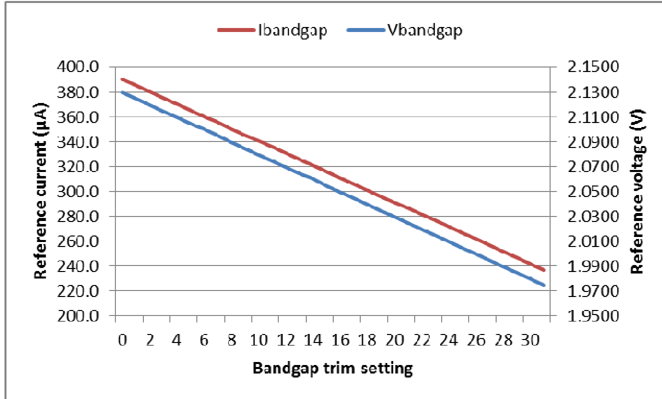

Figure 17: Bandgap outputs as a function of trim settings, showing the nominal settings of 300µA and 2.048V are within the trim range of both circuits.

E. SPI Interface

The SPI serial interface and register bank were tested at a range of speeds and were found to be error free up to bit rates of 50MHz, the maximum speed of the digital I/O card being used.

F. Power

Power dissipation for the main circuits was measured from the power supplies as the individual elements were enabled. Due to other test circuitry sharing the supplies it was not possible to accurately determine the current drawn by the ASIC at power up. However the current draw from other circuit elements was measured and the results are shown in table 2. These can be seen to be in broad agreement with the predicted values listed in table 1.

Table 2: Measured current and power consumption by circuit element and power supply.

Circuit	Current by supply (A)			Power (W)
	3.3V	35V	-2.5V	
ADC	7m			21.78m
DAC (each)	0.6m			2.01m
HV output (each)	0.2m	0.7m	0.8m	26.22m

IV. Conclusions

A high voltage mixed signal ASIC for the generation of CCD bias voltages has been presented. The device has been fabricated in a commercial 50V 0.35µm CMOS technology and prototype die tested. Results show the device performs well, providing low bandwidth output biases on a 0 – 32.736V range with less than 100µV of noise which can be reduced further through the use of filtering capacitors. The controlling DACs are monotonic showing good INL and DNL performance. The telemetry function was also assessed and found to have good characteristics with monotonic behaviour and DNL, INL and noise measurements of 0.43LSB, 1.26 LSB and 0.73LSB respectively. Testing across the full temperature range of -40°C to 125°C will now proceed, followed by TID and SEL radiation testing in the future.

V. References

[1] N. Waltham et al., “Systems Approach to the Design of the CCD Sensors and Camera Electronics for the AIA and HMI Instruments on Solar Dynamics Observatory”, Int. Conf. on Space Optics, Rhodes, Greece, Oct 2010.

[2] *Analog Devices Data Converter Seminar*, Analog Devices Inc., Norwood, MA, 2004.

[3] R. Hogervorst and J. H. Huijsing, “Design of Low-Volage, Low-Power Operational Amplifier Cells”, Kluwer Academic Publishers, Dordrecht, The Netherlands, 1996.

[4] J. Chen and B. Shi., “1 V CMOS current reference with 50 ppm/"C temperature coefficient,” *IEE Electronics Letters.*, vol. 39, no. 2, pp. 209–210, Jan. 2003.

[5] J. Ramos-Martos. “ Evaluation of the AMS 0.35 µm CMOS Technology for Use in Space Applications”. Presented at 4th AMICSA Workshop, Noordwijk, The Netherlands, Aug 2012. Available: http://amicsa.esa.int/2012/pdf/S5_07_Ramos%20Martos.pdf

[6] F. Faccio et al., “TID and Displacement Damage Effects in Vertical and Lateral Power MOSFETs for Integrated DC-DC Converters”, *IEEE Trans. Nucl. Sci.*, vol. 57, no. 4, pp. 1790–1797, Aug. 2010.

Applications for Radiation Hardened Analogue and Mixed-Signal ASICs: Wired and Wireless Communication

Digital Step Attenuators for Microwave Applications in Space – AMICSA 2014

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Abstract

Digital Step Attenuators (DSA) are broadly used within Satellite Payloads to adjust signal levels either as standalone blocks or as a key part of complex systems. Wherever a DSA is employed its critical function is delivering accurate, consistent, repeatable level control in a difficult space environment. The environment in space creates additional challenges due to the wide range of temperature and radiation effects.

Commercial 7 bit/31.75dB DSA have been reported with attenuation errors in the range of (+/-0.1dB + 3% of setting) to (+/-0.15dB + 1.5% of setting) for 8GHz devices. When we investigate these numbers further we find the best attenuation accuracy is typically only achieved over the lower frequency range.

Above these frequencies there are fewer vendors and attenuation accuracy degrades significantly. A 0-13 GHz DSA has been reported with attenuation error of (+/-0.5dB +5% of setting). The attenuation error is highest for the higher attenuation values, to get around this some vendors reduce the maximum attenuation of their DSAs from 31-32dB to approximately 16dB.

The author will review the building blocks of a DSA and describe circuit solutions to improve attenuation accuracy as frequency increases.

Measured results for a 6GHz DSA and an 11 GHz DSA will be compared along with the differences in circuit topology and packaging approach. These results will demonstrate how to achieve improved high frequency attenuation error for microwave DSAs.

I. Introduction

The Satellite Market is experiencing a number of trends; in the commercial communications satellite market we see a move towards higher frequency bands, coupled with a requirement to make Satellite reconfigurable and capable of higher data rates (e.g. high throughput satellites). At the same time we see increased activity in earth observation imagery, using a range of different sensor techniques to collect high resolution images of the earth. Although these applications are very different the technical solutions result in significant overlap in the circuit blocks required to meet the market needs.

For example earth observation agencies continue to launch new, finer resolution synthetic aperture radar (SAR) while communications satellites are increasing being launched with phased arrays to create movable spot beams. Both of these applications require the phase and amplitude of signals to be accurately adjusted to many parallel paths. A typical block to adjust amplitude and phase for one antenna element is shown in Figure 1 below.

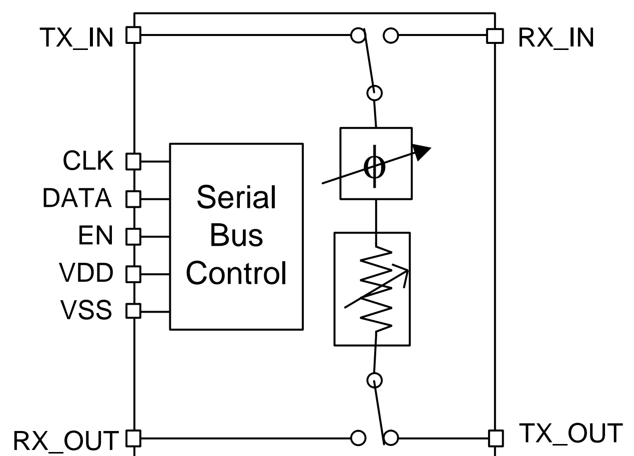


Figure 1: "Core Chip" Phased Array Building Block

The amplitude adjustment with the Core Chip is achieved with a DSA, shown as a tuneable resistor block in Figure 1.

Similarly the requirement for larger, higher data rate Communications satellites is putting pressure on the power bus of the satellite. One way to alleviate the problem is to improve the efficiency of the power amplifier, using advanced linearizers. A possible approach is a Doherty power amplifier, although this technology is not new, recent advances in asymmetric Doherty amplifiers has seen renewed interest in this approach. The Doherty PA relies on accurate adjustment of signal amplitude and phase in two independent paths. A typical Doherty PA circuit is shown below in Figure 2, with the DSA (tuneable resistor) controlling the amplitude.

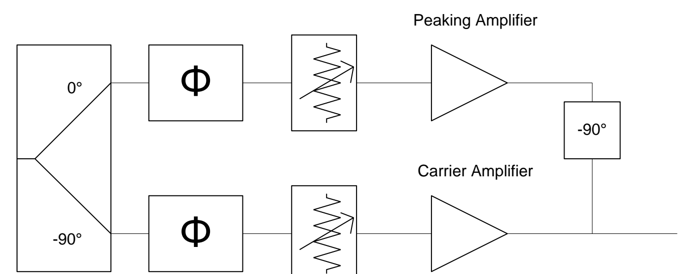


Figure 2: Doherty PA

A third application requiring accurate amplitude adjustment is navigation satellites, for example Galileo. As the system consists of a constellation of satellites, with end users receiving signals from multiple satellites it is important to radiate equivalent power from all satellites in the constellation. Failure to accurately control and balance signal levels could result in the signal exceeding the allowable maximum radiated power. A simplified Galileo RF path block diagram is shown below in Figure 3.

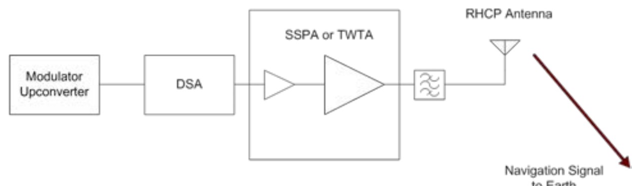


Figure 3: Galileo Navigation Satellite Simplified RF Path

II. Important characteristics for DSAs

As reported by previous authors [1] there are several key parameters for a DSA, including power handling capability, switching speed, insertion loss, phase error and amplitude error. Generally all of these have to be balanced in the design of the DSA. For the purposes of this article we focus on Amplitude Error as there are specific challenges to achieving the required amplitude accuracy as frequency increases.

The commercial DSA market has a large number of product offerings, many reporting high attenuation accuracy. However when we review the data carefully this performance is achieved for the lower frequency of operation and rolls off quickly at higher frequency.

Attenuation error	0 dB – 15.75 dB Attenuation settings	50 MHz – 2.2 GHz			+ (0.15 + 1.5% of attenuation setting) - (0.1 + 1% of attenuation setting)	dB dB
		>2.2 GHz – 4 GHz			+ (0.15 + 3% of attenuation setting) - (0.1 + 1% of attenuation setting)	dB dB
		>4 GHz – 6 GHz			+ (0.2 + 6% of attenuation setting) - (0.15 + 1% of attenuation setting)	dB dB
	16 dB – 31.75 dB Attenuation settings	50 MHz – 2.2 GHz			+ (0.15 + 1.5% attenuation Setting) - (0.1 + 1.5% of attenuation setting)	dB dB
		>2.2 GHz – 4 GHz			+ (0.15 + 4% attenuation Setting) - (0.1 + 0.75% of attenuation setting)	dB dB
		>4 GHz – 6 GHz			+ (0.25 + 7.5% of attenuation setting) - (0.2 + 0% of attenuation setting)	dB dB

Figure 4: PE43705 Digital Step Attenuator Attenuation Accuracy

Figure 4 shows the published [2] attenuation accuracy for a commercially available 8 GHz DSA, packaged in a 32 lead 5x5mm plastic QFN package. This product offers class leading performance for a commercial part at this frequency range. However we can see that the best accuracy is achieved below 2.2GHz, particularly for the higher attenuation settings. For the maximum attenuation setting above 4GHz the attenuation accuracy, although still very good, has approximately doubled the error observed below 2.2GHz.

Attenuation Accuracy: (Referenced to Insertion Loss) 0.5 - 16.5 dB States 17 - 31.5 dB States	DC - 13.0 GHz DC - 13.0 GHz	± 0.4 + 4% of Atten. Setting Max ± 0.5 + 5% of Atten. Setting Max	dB dB

Figure 5: HMC424LH5 DSA Attenuation Accuracy

Figure 5 shows the published [3] attenuation accuracy for a commercially available 13.5GHz DSA, packaged in a leadless 5x5 ceramic package. Although this product does not specify attenuation over frequency sub-bands, we can see from Figure 6 that similar behaviour occurs versus frequency, as the 8 GHz DSA. The trend is attenuation accuracy degrades with frequency, particularly above 9GHz, and the effect is more pronounced for larger attenuation values.

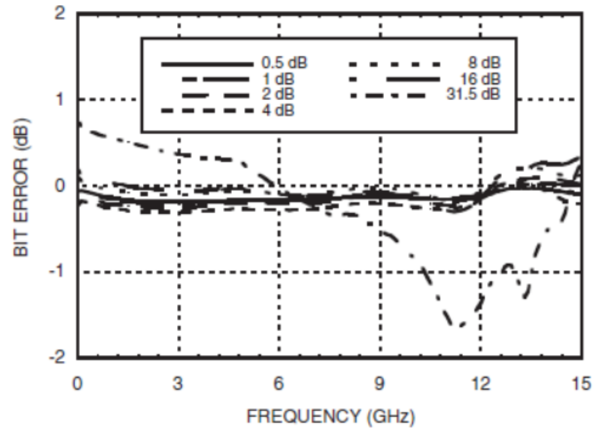
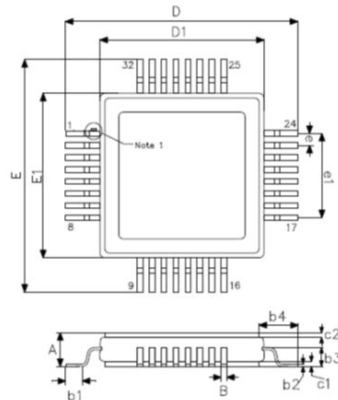


Figure 6: HMC424LH5 Bit Error

III. Peregrine Space Qualified DSA Example

Peregrine have developed a 7 bit, 0.25 dB step DSA in its proprietary 0.5um Silicon on Sapphire (SOS) process for an ESA funded project. The product is the PE43751. The aim of the project was to create a European developed, radiation hard DSA for space applications. The product was packaged in a 32 Lead CQFP package; the package can be seen in Figure 7.



Symbol	Dimension (mm)		Notes
	Min	Max	
A		1.82	2
B	0.25	0.35	2
b1	0.88		2
B2	0.10	0.16	2
B3	0.76 typical		2
B4	2.25 typical		2
C1	0.20	0.30	2
C2	0.25 typical		2
D / E	12.93 typical		
D1 / E1		8.89	
e	0.65 typical		2

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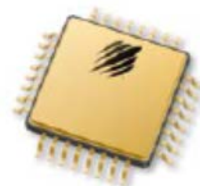


Figure 7: 32 Lead CQFP Package

CQFP packages are preferred by many Space customers for several reasons: the package can be hermetically sealed, allowing parts to be placed outside of modules/hybrids; the device can be visually inspected after soldering, ensuring solder joints have formed correctly. However leaded packages introduce undesirable lead inductance, resulting in reduced performance, as will be shown later.

A. PE43751 Attenuation Accuracy

The PE43751 DSA is intended for applications ranging in frequency from 30 kHz to 6 GHz, although as with previous examples optimum performance is achieved at lower frequencies. Figure 8 shows the devices attenuation accuracy at 4GHz for all attenuation steps. The x-axis is the unit-less attenuation setting, as a decimal value from 0-127. Each decimal increment corresponds to a 0.25dB attenuation step. The response shows several large steps, these steps correspond to the switching of larger attenuators in the DSA. The following section will discuss the basics of how a DSA is constructed and how this influences the accuracy.

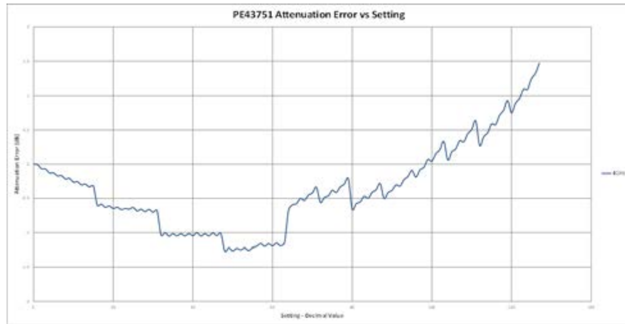


Figure 8: PE43751 4GHz Attenuation Accuracy

B. Basic Step Attenuator Building Blocks and Construction

A simplified block diagram of a 31.75dB DSA is shown below in Figure 9. A simplified block diagram is presented to allow the architecture to be studied without the complexity of the switches. For this discussion the switches will be considered ideal. In reality the switches will have an on resistance, a finite off isolation (off capacitance) and various parasitics. These non-ideal features will not be discussed here.

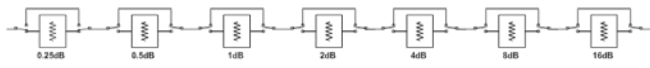


Figure 9: Simplified Digital Step Attenuator Block Diagram

The Step attenuator in Figure 9 consists of a series of resistive Pi or T pads, interconnected with a series of single pole, double throw (SPDT) RF switches. Each attenuator can be included in the overall attenuation or bypassed by the SPDT switches. In the ideal case we are able to add the attenuation of each individual attenuator to get a combined attenuation, in increments of 0.25dB, up to a maximum of 31.75dB.

In the example in Figure 9 we have shown the individual attenuators arbitrarily ordered from smallest attenuation to largest attenuation. As will be shown later this may not provide the best overall result.

Considering the DSA as the sum of individual attenuators allows us to better understand the limitations of a combined device. Reviewing the PE43751 European DSA and considering the larger attenuators in the device (4dB, 8dB, 16dB), we can see some interesting behaviour versus frequency.

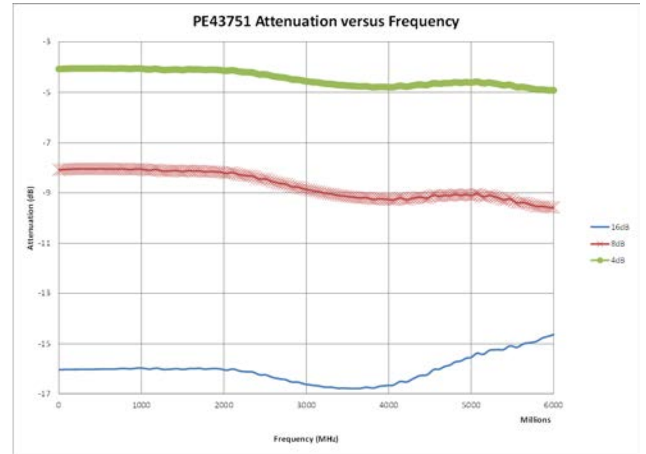


Figure 10: PE43751 Major Attenuators versus Frequency

Figure 10 shows the attenuation of the 4dB, 8dB and 16dB attenuators versus frequency. This data has been corrected for the insertion loss of the DSA, by subtracting the 0 setting insertion loss from the raw data. Considering first the 4dB and 8dB attenuators we see a general trend of the correct attenuation at low frequency, and increased attenuation as frequency increases. The responses aren't linear and don't follow a simple curve, suggesting more than one effect or root cause; this will be discussed further later.

The 16dB exhibits a different behaviour versus frequency; up to approximately 3GHz the response is similar to the smaller attenuators. Above 3 GHz the 16dB attenuators attenuation begins to reduce, leading to a large error at 6GHz. This characteristic is a well understood phenomena and is attributable to finite isolation or coupling within the device. As frequency increases a combination of ground bond coupling and limited isolation on die result in reduced attenuation. As will be discussed in the improved architecture section this effect can be reduced.

IV. Improving DSA Performance

The two frequency dependent effects on attenuation accuracy identified in the previous section were: increased attenuation versus frequency and reducing attenuation with frequency for 16dB attenuators above 3 GHz. This section will investigate these effects further and propose ways to reduce the devices sensitivity to these effects.

A. Large Attenuator Isolation and Coupling

The simplest and most effective way to reduce isolation and coupling effects is to physically separate the large attenuators from each other. An additional technique is to divide the large attenuator into two smaller attenuators, and to physically separate these. Dividing the large attenuator in to two with half the attenuation each reduces the isolation required per attenuator and physically separating increases the isolation. For example a 16dB attenuator can be divided in to two 8dB attenuators, which can in turn be separated from each other by the smaller attenuators. An example of this approach can be seen below in Figure 11.

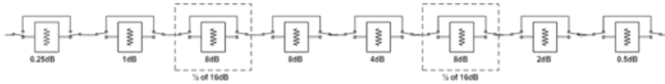


Figure 11: Improved Isolation Attenuator Architecture

In this example the 16dB attenuator is made up of two 8dB attenuators and these are in turn separated by the 4dB attenuator and the 8dB attenuator. This approach requires slightly more die area, but virtually eliminates the isolation effect. The resulting die layout can be seen below in Figure 12.

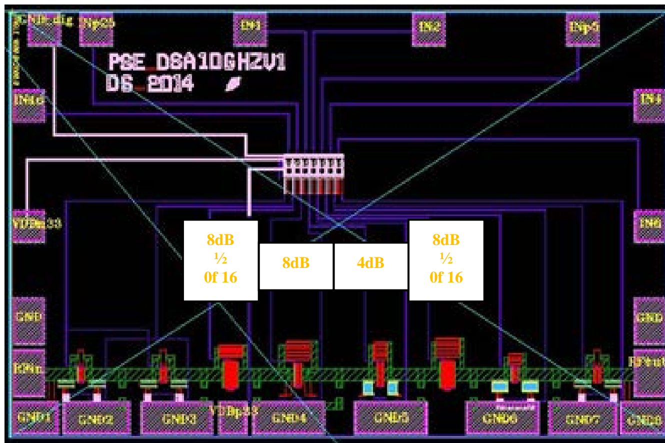


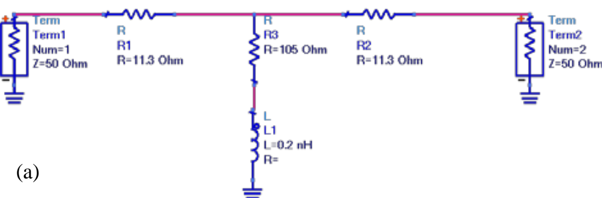
Figure 12: Die Layout for improved isolation, high attenuation accuracy

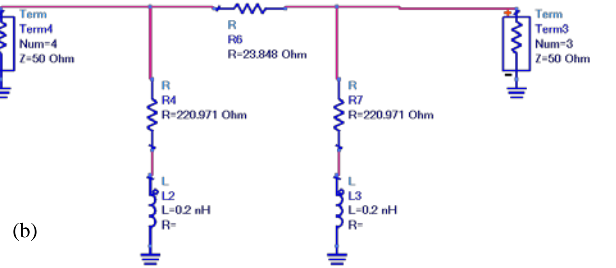
B. *Minimising the Attenuation Increase with Frequency*

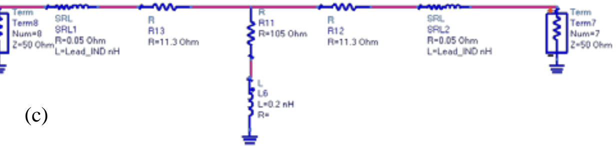
The increased attenuation with Frequency is primarily due to lead inductance and ground bond inductance. To demonstrate the sensitivity to inductance in the series and shunt path of a high frequency attenuator a series of simple simulations were completed.

1) Pi versus T Attenuator

To optimize the Step Attenuator for high frequency operation we must consider which configuration (Pi or T) is least sensitive to package and bond wire inductances. A simulation was constructed using a 4dB Pi and 4dB T pad, with realistic inductances added to represent package and bond wire inductances. Figure 13 shows the schematics of the Attenuators.







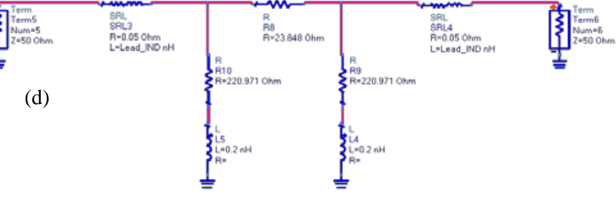


Figure 13. (a) T-pad with ground inductance. (b) Pi-pad with ground inductance. (c) T-pad with ground inductance and lead inductance. (d) Pi-pad with ground and lead inductance.

The series inductance values used in the simulation was Lead_IND=0.2nH. 0.2nH is a typical value for a short bond wire or down bond.

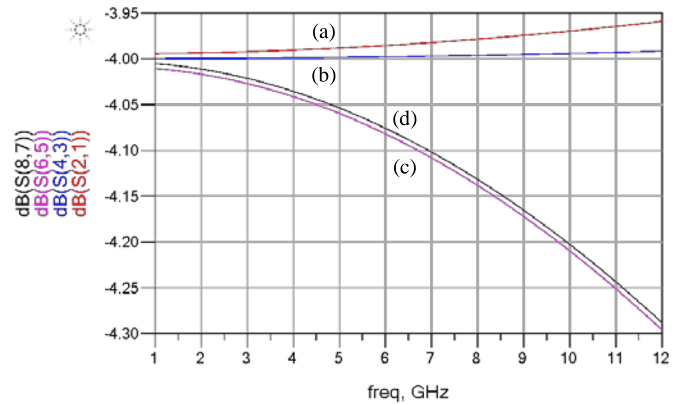


Figure 14: (a) 4dB T-pad with shunt inductance, (b) 4dB Pi-pad with shunt inductance, (c) 4dB T-pad with series and shunt inductance, (d) 4dB Pi-pad with series and shunt inductance

Figure 14 shows the results of the simulation, from these results we can see the T-pad is generally more sensitive to inductance in either the series or shunt leg of the attenuator. In both cases the series inductance has more impact than a shunt inductor.

C. *Improving the 4dB Attenuator*

In this section we discuss improvements Peregrine are implementing in their Space DSA for applications in X-band (8-12GHz). The improvements are contrasted with the results previous results for the PE43751 (6GHz Space DSA) and a simulation is constructed to show the impact of the package lead inductance.

Figure 15 below shows a comparison plot for the 4dB attenuator measured in the PE43751 versus a new 4dB attenuator as part of a new X-Band DSA. Both measurements are normalized by subtracting the loss of the 0dB state.

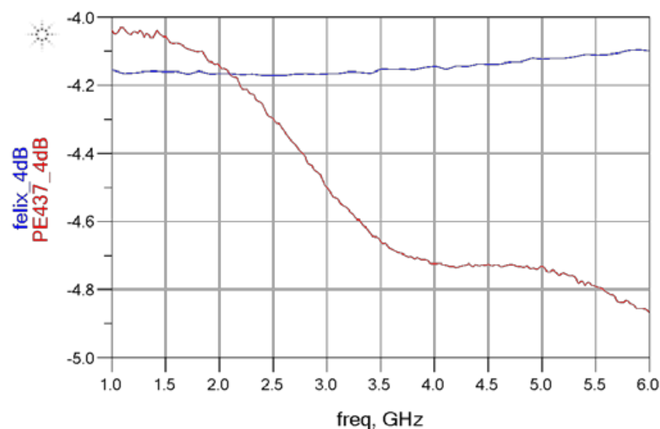


Figure 15: Comparison of 4dB attenuator accuracy versus frequency

The red curve is for the PE43751 DSA 4dB attenuator and the "felix_4dB" is the new X Band DSA 4dB attenuator. The new attenuator is tested as a bare die, probed on a carrier. The die has ground down bonds, equivalent to being bonded in a package. The "felix_4dB" results show a similar characteristic to the simulations with a small ground inductance i.e. the attenuation reduces with increasing frequency due to the inductor. The PE43751 attenuator exhibits an increase in attenuation with increasing frequency, consistent with series inductance due to a package.

A simulation was constructed using the s-parameters from the new 4dB attenuator, with the addition of a pair of series inductors and a shunt inductor. The aim of this simulation is to demonstrate addition of these inductance results in a similar response to the PE43751, and by extension these inductances are due to the choice of package.

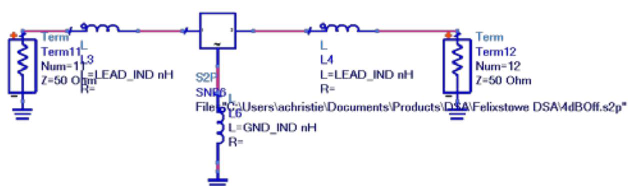


Figure 16. Schematic of New DSA with Lead and Ground Bond Inductance

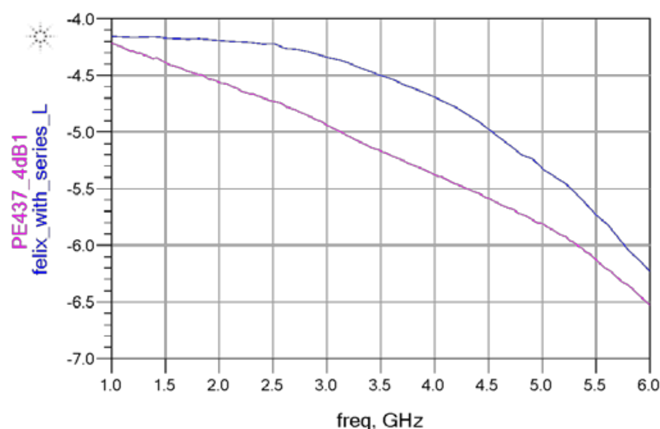
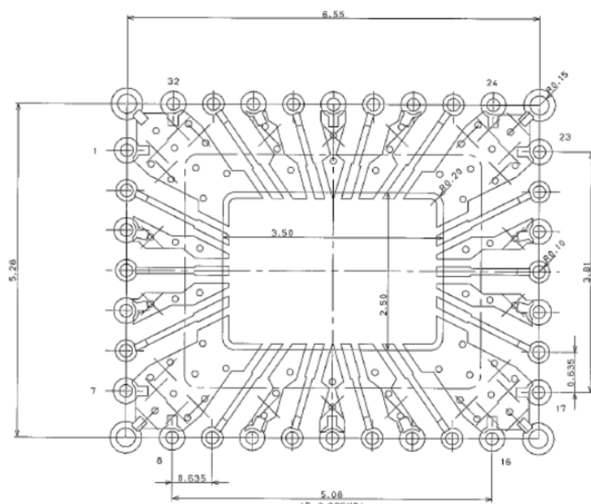


Figure 17 Impact of adding Series and Shunt Inductance

Figure 17 shows the impact of adding series inductance and shunt inductance to the improved "Felix_4dB" DSA. The new DSA response looks similar to the response of the PE43751. The inductor values used to achieve this result were 1.7nH series and 1nH shunt. The lead inductance of a CQFP package is approximately 0.9nH, while the input and output bonds for the PE43751 are relatively long (due to the package choice). The device has 2 parallel input and output bond wires, each pair approximately 1.4mm long. Assuming 1nH/mm per bond wire would introduce approximately 0.7nH of additional inductance. This would result in a total series inductance of approximately 1.6nH.

These results highlight the limitations of using a CQFP package for higher frequency applications. A better alternative for applications at 10GHz is the use of a leadless package, for example a leadless ceramic package. An example of a leadless ceramic package suitable for 10GHz is shown below in Figure 18.



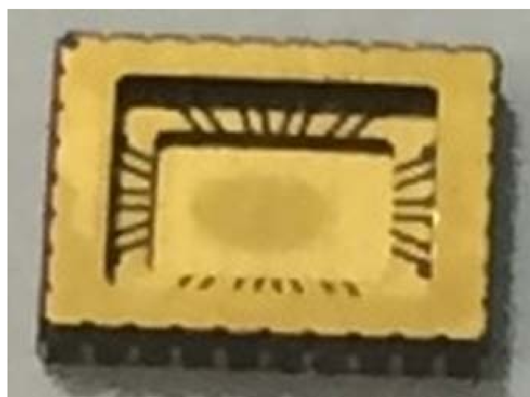


Figure 18: Leadless Ceramic Package

This package has been specifically designed for high frequency operation and uses alternate ground and signal pins, allowing Co-planar wave (CPW) techniques to be used. This coplanar wave approach minimizes the lead inductance and simplifies the transition to a circuit board. Additionally laying out the die to position the input and output bond pads to have the shortest possible bond wire lengths will further improve performance.

D. 4dB Attenuator in leadless ceramic package

The leadless ceramic package in Figure 18 minimises the inductance of the packaged device and allows us to improve DSA performance at higher frequencies. In addition to eliminating the lead inductance associated with a CQFP package the leadless package contains a shelf to reduce bond wire inductance. A partial cross section of the package is shown in Figure 19

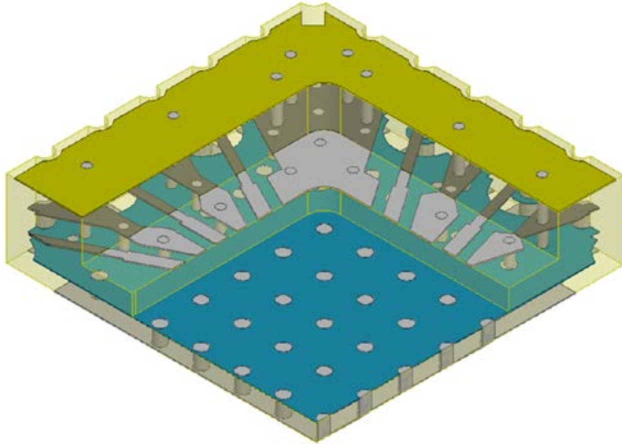


Figure 19: Leadless package cross section

The shelf allows the top of the die to be co-planar to the package bonding area. A simplified cross section comparison between the leadless package and a CQFP can be seen in Figure 20

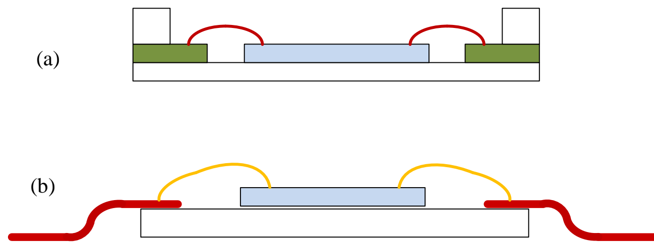


Figure 20: Bonding benefits of leadless package (a) leadless package bonding, (b) CFQP package bonding

Figure 20 (a) shows the bond wire length and shape for the leadless package; Figure 20(b) is the equivalent bond for the CQFP package. The co-planar die and package bond pad significantly reduces the bond loop height and overall length compared to the CQFP package. This results in a significant reduction in the series inductance for the attenuator and DSA.

1) Results for 4dB attenuator in leadless package

To demonstrate the performance improvement of the leadless package compared to the CQFP package the “felix_4dB” (new 4dB attenuator RF probe measurements) was combined with the vendor provided package model in the simulator. The package vendor model consists of a 28 port S-parameter file to model every package I/O from the outside of the package to the bonding area.

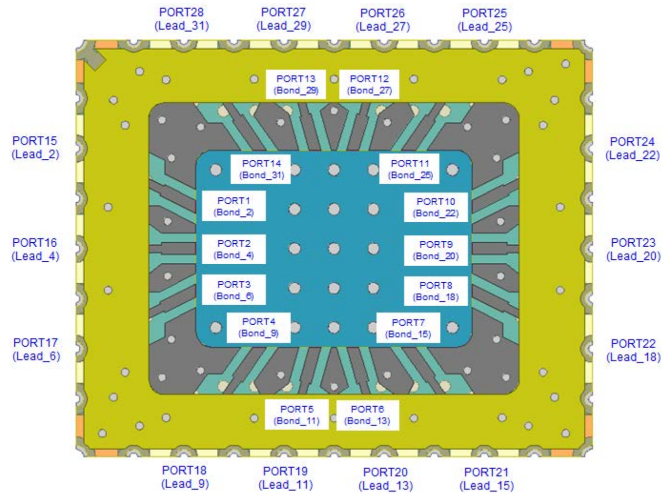


Figure 21: Leadless package 28 port model ports

Figure 21 shows the port numbers for the leadless package. The model can be understood in the following way: alternate pins on the package are ground and RF to create a CPW transition; leads 2, 4, 6, 9, 11, 13, 15, 18, 20, 22, 25, 27, 29 and 31 are the RF connections; all other leads are ground. The S-parameter S(16,2) provides a model for Lead 4 and S(9, 23) provides the model for Lead 9.

Combining the leadless package model and the probed data for the 4dB attenuator we created the following model for the packaged attenuator.

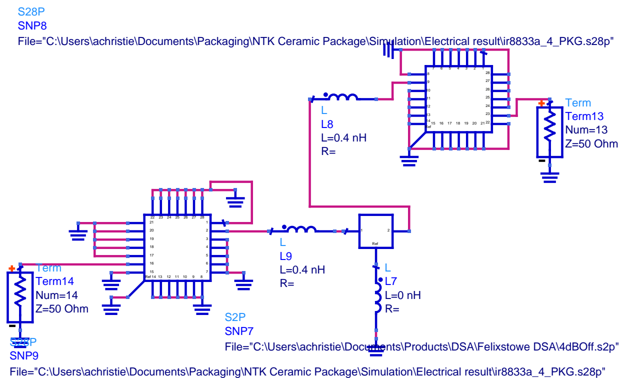


Figure 22: Model for 4dB attenuator and leadless package

The combined model in Figure 22 consists of the package model (S28P file) followed by 0.4nH for the input bond wire, the probe data (S2P file), 0.4nH for output bond wire and the package model. The ground inductance for the probe data (L7) was set to zero as the probe data already includes down bonds. The input and output bond wire lengths are <0.6mm and each consist of a pair of bond wires. 0.4nH is a worst case estimate for the bond wire inductance.

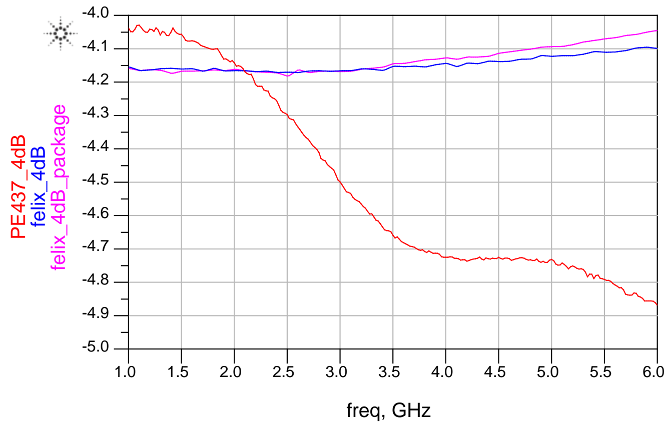


Figure 23: Improved 4dB Attenuator response in leadless package

Figure 23 shows the attenuation of the 4dB attenuator (felix_4dB_package) in the leadless package compared to the improved attenuator probe data (felix_4dB) and the existing PE43751 DSA. The leadless package creates a slight increase in attenuation variation versus frequency compared to the probe data, but the effect is small. When compared to the CQFP packaged PE43751 the leadless package shows a significant improvement in attenuation accuracy and consistency versus frequency.

V. Conclusion

This paper presented a 6 GHz Space qualified DSA fabricated in 0.5um SOS CMOS technology. The performance of this DSA was reviewed and used to highlight the challenges of developing high frequency DSAs. DSA architectures were reviewed and a series of simple simulations were constructed to demonstrate how to improve high frequency performance. A method of improving attenuation accuracy was demonstrated using a combination of an improved 4dB attenuator and a new ceramic leadless package. The paper shows that by minimising inductance outside of the die performance significantly improves. This resulted in a 1.8dB improvement in attenuation accuracy for the 4dB attenuator at 6GHz.

VI. Acknowledgements

The author would like to thank the following people: Vikas Sharma for technical inputs and suggestions regarding content of this article; Daoud Salameh for developing the improved DSA and sharing measured probe data; John Dench for collecting and post-processing data for the PE43751 DSA and Mark Moffat for editorial comments.

VII. References

[1] M K Cho, J G Kim, and D Baek, " A Broadband Digital Step Attenuator with Low Phase Error and Low Insertion Loss in 0.18-µm SOI CMOS Technology," ETRI Journal, Volume 35, Number 4, August 2013, pp638-643

[2] PE43705 Data Sheet. http://www.psemi.com/pdf/datasheets/pe43705ds.pdf

[3] HMC424LH5 Data Sheet. http://www.hittite.com/content/documents/data_sheet/hmc424lh5.pdf

Low-Power Analogue Receiver ASIC for Space Telecommand Applications

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Abstract

In this paper an ASIC implementation of an analogue receiver chain for telecommand applications for Category A missions (Return-to-Earth, lunar and even Lagrangian missions) will be presented. More specifically, in addition to the Low-Density Parity Check (LDPC) 128 bit analogue decoder component, the ASIC receiver will also include other important blocks of the telecommand reception chain normally accomplished inside an FPGA device, such as IF coherent demodulation stage front end, carrier recovery, baseband clock recovery, data conversion from input SP-L signal to NRZ codify, Start Frame pattern recognition, analogue memory for input codeword storing. The ASIC is now in detail design phase and it will be manufactured in XFAB 0.18um technology.

I. INTRODUCTION

Nowadays, on-board telecommand receivers for space applications consume an important percentage of the overall offered power of the satellite, especially due to their always ON need of operations.

Decoders, in charge of elaborating received data and of providing error correction according to redundancy introduced by related encoding protocol are one of the fundamental components of a satellite receiver. They currently follow a digital development approach based on a large FPGA. Even though, initially, the power consumption of digital decoders was not a factor of concern, the increasing communication and data storage complexity and capacity makes the applicability of error correction codes in a digital domain more and more expensive in terms of hardware resources and power consumption.

Therefore, in the last ten years, being analogue decoding recognised for its potential to efficiently decrease the overall power consumption of a receiver, an important growth in analogue decoding research programs is registered, although only a few VLSI integrated circuits have been developed satisfying a given communication standard. Analogue domain implementation of error correction codes, despite its lower power consumption potential with respect to its digital counterpart, seems to also provide some additional advantages: it takes benefit from the similarity between the mathematical operations required by the algorithms and the physical laws governing the circuit; it improves the total system efficiency, because the analogue decoder is much smaller than its digital counterpart and consumes about one order of magnitude less power at the same frequency; it offers high modularity design more immune to noise, by means of differential operation; it offers the capability of providing a finer estimation of the logic state of a single information unit with respect to digital implementations (no quantization); it needs a lower signal to noise ratio to properly correct a wrong input sequence of information unit.

Thus, the proposed paper will address such benefits of an on-board analogue receiver chain implementation for telecommand applications for Category A missions (Return-to-Earth, lunar and even Lagrangian missions.

In particular, Low-Density Parity Check (LDPC) 128 bit analogue decoder have been chosen as the design basis of the analogue decoder, since it showed in preliminary investigations a big potential for increased power saving when short length codes are concerned as of telecommand communication for Category A missions. Moreover, the analogue receiver will be compliant with the communication protocol described in ECSS-E-ST-50-04C “Telecommand protocols synchronization and channel coding”.

The paper is organized as follow: in the Section II the ASIC architecture description has been reported whereas details about the receiver, symbol synchronization, codify block and start frame recognizer have been reported respectively in sections III, IV, V and VI. The decoder core organization has been described in section VII and, finally, the conclusion has been reported on Section VIII.

SITAEL S.p.A. has produced all relevant work in the frame of “RLP_AD: Receiver Low-Power Analogue Decoder” activity (ESA TRP), developed in the context of ESA ITT AO/1-6722/11/NL/GLC with the aim of investigating feasibility of analogue decoding for space applications.

II. ARCHITECTURE DESCRIPTION

The ASIC Block Diagram is reported in Figure 11.

The Serial Programming Interface (SPI) accepts external customized commands for proper internal bias and for test modes configuration.

The analogue input to the ASIC is the intermediate frequency DC component and the sidelobes of the modulated signal: the in-phase and the in-quadrature components of baseband signal are produced internally to the ASIC, after the final down conversion step, and they are filtered and amplified inside the AFE (Analog Front End) block.

The CR (Carrier Recovery) section provides to the local mixer a suitable frequency (same as carrier frequency) and phase (such that maximizes the In-Phase baseband demodulated component) for down conversion purposes: carrier tracking proceeds by extracting the carrier frequency to be tracked by the PLL from the received signal, and by

aligning the tracking-carrier phase according to a signal-energy-maximization principle.

In details, carrier phase tracking is achieved by correcting the PLL phase based on the measured amplitude inside the demodulated channels: the aim of phase correction is to re-phase the oscillation output by the PLL and used for local mixing (demodulation) in order to maximize the in-phase signal energy with respect to the in-quadrature signal energy. Downstream circuitry accepting the demodulated signal operates only on the in-phase demodulated baseband signal.

The SSU unit (Symbol Synchronization Unit) operates the clock extraction from the baseband PCM/PM/BI-PHASE signal: a local PLL tracks the data transition synchronism (since SP-L codify guarantees always at least one transition per clock cycle). Clock recovery is operated in the digital domain, that simplifies the PLL configuration. Due to the digital configuration adopted for clock recovery, ad hoc matched filtering must necessarily be provided inside the Codify Conversion block.

The CC (Codify Conversion) section converts the data codify from PCM/PM/BI-PHASE to NRZ codify. The PCM/PM/BI-PHASE to NRZ conversion task is performed by differentiating the left and right symbol half integrations with respect to the useful clock edge of data transition. Integration provides matched filtering and noise averaging.

Finally, the decoder block presides to data decoding and provides output NRZ digital decoded data and clock for sampling: it is able to trigger when a Start Frame pattern is recognized and it is able to stop decoding once an End Frame command is detected, waiting for next Start Frame pattern.

Being the signal processing chain of ASIC a fully concatenated-cascaded chain, several test modes are foreseen in order to allow verification of single functional sections.

III. Receiver Section Description

The Receiver Section is composed by AFE and CR block. The block diagram is reported in Figure 1.

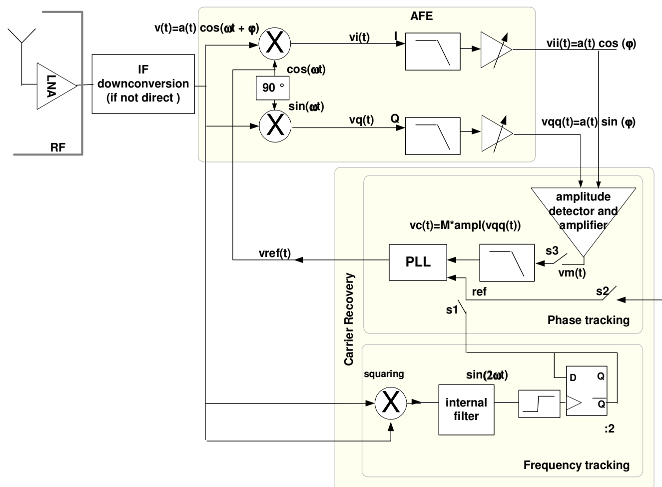

Figure 1: Receiver Section Block Diagram.

The carrier frequency recovery (which mixer works at 8MHz of IF) can be operated in two (2) different ways:

a. by a squaring and frequency divider by two, which sends a reference reconstructed frequency to the PLL (with switches s1 closed, s2 and s3 open). This configuration is a standard frequency recovery approach for BPSK suppressed-carrier signals;

b. by using the carrier-only transmission phase CMM1 of PLOP2 procedure [1] to drive the PLL output frequency in the neighbours of carrier frequency (s1 initially closed, s3 open, s2 open), and, once the PLL is in lock, by leaving the internal VCO being controlled by the amplitude detector and amplifier block (s3 closed, s1 and s2 open). The training frequency during CMM1 phase can be optionally provided by a local oscillator (s2 closed, s1 and s3 open). s3 and s1/s2 switch activity is mutually exclusive in time, and it is governed by the PLL lock signal. A dedicated internal configuration selects between s1 and s2 training options.

Carrier phase tracking is achieved by correcting the PLL phase based on the measured amplitude inside the demodulation channels: the aim of phase correction is to re-phase the oscillation output by the PLL and used for local mixing (demodulation) in order to maximize the in-phase signal energy with respect to the in-quadrature signal energy. Downstream circuitry accepting the demodulated signal operates only on the in-phase demodulated baseband signal.

The amplifier and filter inside the AFE chain condition the down-converted signal and filter the out-of-band signal components.

The AFE block has twofold functionality: to produce the final signal down-conversion for demodulation purposes on both I and Q signal components by using properly re-phased local reconstructed carrier and to amplify and filter the baseband demodulated I and Q signals. For this purpose, continuous time bi-quad filters are used in order to reject the image frequency components. The DC-rejecting amplifiers are used in order to reject the DC component at amplifier input.

IV. Symbol Synchronization Unit Description

The Symbol Synchronization Unit is composed by a Data Transition Detector and a Clock Recovery Unit.

The Data Transition Detector Unit is a simple comparator whereas the Clock Recovery Unit is a PLL like the one shown in Figure 2 which receives the 1-bit quantized data information and locks its oscillating frequency to the data transition frequency.

The clock recovery function extracts the clock information from the demodulated symbol data stream in order to allow correct signal sampling inside the matched filter and decoder downstream sections.

The main drawback of employing linear phase detectors in the PLL loop is that the phase detector response strongly depends on transition density, that has an heavy impact on clock phase jitter.

In PCM/PM/BI-PHASE signals (Figure 3), transitions are allowed to happen or synchronously with the data clock (in a string of all “0” or in a string of all “1” logic signal) or every

clock rising edge (in a string of alternating “0” and “1” logic signal).

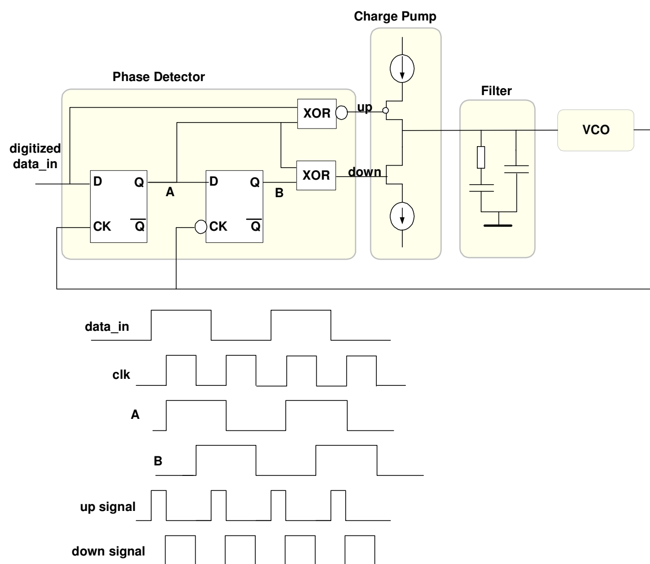

Figure 2: signal activity and timings for the Hogge’s phase detector. Retimed data are present at the output of lower flip flop.

Since there is a factor two between the transition frequency corresponding to the two above different cases, the transition density dis-uniformity is important: as an effect, the equivalent phase detector gain walking causes an important dispersion in the reconstructed clock phase.

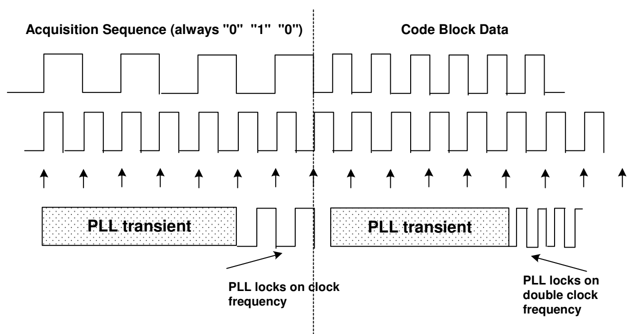

Figure 3: PLL acquisition sequence.

To overcome this issue, a principle has been applied, which equalizes the transition density and takes benefit of the property of PCM/PM/BI-PHASE signals of presenting always a data transition at the significant lock edge.

In practice, a PLL employing a standard linear phase detector is adopted using a certain (programmable) frequency divider in the feedback chain: the high-frequency clock at the input of frequency divider (VCO output) is used as a synchronism in order to mask the undesired transitions from the input data sequence, and to equalize data transition density over time.

After the PLL locks during the data Acquisition Sequence, the introduced synchronism allows to keep the transition density constant over time after the Acquisition Sequence ends and code block reception starts (with related data transition density discontinuities).

This mechanism allows the phase detector to operate with a fixed gain, greatly improving the performances of the PLL itself and reducing clock frequency/phase jitter.

The synchronism signal used to equalize the data transition density practically masks the extra-transitions not synchronous with the clock rising edge in the data stream, according to the principle reported in Figure 4.

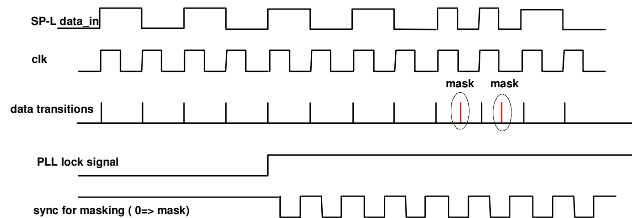

Figure 4: Masking data transitions operation to equalize data transition density over time.

As a result of masking operation, the data transitions are only the useful data transitions at symbol middle point individuated during the Acquisition Sequence, and any other data transition (used in PCM/PM/BI-PHASE codify for properly set upping data level before the symbol middle transition) is discarded and not used for PLL phasing.

In details, the symbol duration is divided into 4 equally spaced quadrants during the Acquisition Sequence: once the PLL locks and after Acquisition Sequence ends, this quadrant-spacing is kept for each symbol and data transitions happening within the second and the third quadrant are systematically masked.

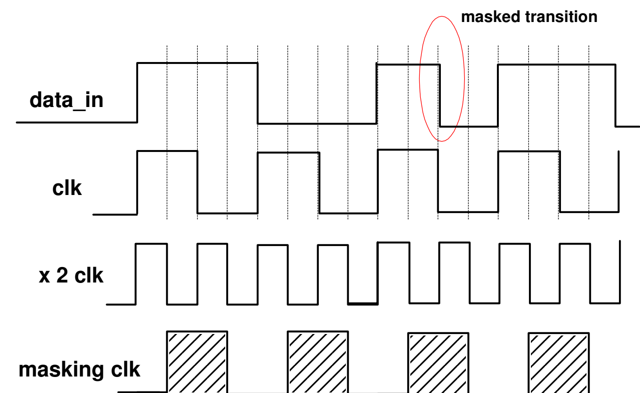

Figure 5: Clock multiplying internal to PLL allows an easy data transition masking principle.

Masking operation is enabled only if the PLL is locked during the Acquisition Sequence and the locking status is detected during the Acquisition Sequence when the transitions passible of masking are not detected for a certain number of clock cycles.

The masking mechanism provides a systematic solution to the transition density uncertainty proper of PCM/PM/BI-PHASE signals. Another mechanism is part of the PLL design to improve the PLL noise tolerance. This different mechanism detects the missing data transitions and inserts transitions into the data stream fed to the PLL in order to maintain the PLL in lock condition.

By summarizing, the strategy for the clock recovery is:

a. during the Acquisition Sequence to achieve the lock starting from the first data transition, a timeout corresponding to the expected symbol rate inserts artificial transitions when missing transitions are detected by the timeout in the data stream;

b. once the lock is achieved, the masking mechanism is enabled: in this way, data transition corresponding to the clock edge not representing the SP-L are systematically masked to the PLL, in order to avoid PLL frequency walking according to the data transition density.

Both mechanisms are aimed to provide to the PLL a constant data transition density in order to maintain the lock.

The lock status of clock recovery PLL is used to enable downstream signal processing chain, in details the Start Frame Recognizer

The data rate change is achieved internally to the clock recovery circuit by properly programming (through SPI) the frequency divider that is used inside the PLL loop. This frequency divider allows obtaining six (6) binary progressively increasing data rates from 8Kbit/s to 256Kbit/s.

V. Codify Conversion Description

Once the data clock is extracted, correct data sampling is possible. However, soft values are required to be passed to the analogue decoder by avoiding any squaring operation on analogue levels before decoding: on the contrary, an analogue level has to be stored inside the decoder memory representative of the log-likelihood probability of corresponding bit. Hence, this representative level has to be constructed and sampled. Sampling analogue could be affected by superimposed noise; in fact considering at the moment NRZ signals, if at sampling instant a large noise spike is superimposed to the signal, the resulting sampling is affected by that noisy sample. If, instead, the symbol level is subjected to a continuous integration operation during the symbol period, the sampling of the result at symbol end will take advantage from the integration, allowing an effective noise filtering and a signal-to-noise ratio maximization.

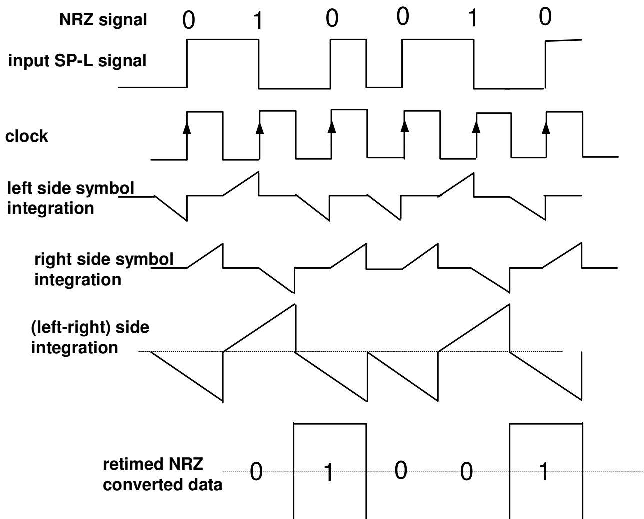

Figure 6: Conversion of PCM/PM/BI-PHASE signal into NRZ signal by averaging noise on half symbol periods and by measuring the level jump related to received logic state at clock edge.

In PCM/PM/BI-PHASE signals, the logic state information resides in the sign of level jump experienced at clock rising edge: if the data stream presents a positive jump, it is associated with the reception of a logic “0” whereas if the data stream presents a negative jump, this is associated with the reception of a logic “1”.

As a conclusion, averaging noise on logic states when codified according to the PCM/PM/BI-PHASE convention means producing the differentiation between the integration results of right-symbol side and left-symbol side (Figure 6): the differentiation result is sampled on the opposite clock edge with respect to data transition in order to provide the NRZ data conversion.

VI. Start Frame Recognizer and Data Memory

The input data stream pattern, to be recognized in order to allow decoding operation starts, is composed by 16-bit logic pattern 1110101110010000; however the programmability of the target pattern can easily be achieved through SPI interface. For pattern recognize a sliding window approach has been used. The incoming level is stored bit-by-bit into a 16-bit analogue First-In First-Out chain and each value is compared with the 16 values corresponding to the pattern to be recognized; the 16-bit correlations between received and expected bit are summed too (Figure 7).

If the correlation result exceeds a certain (externally programmable) correlation threshold, the Start Frame pattern is recognized, and the START flag is asserted for decoding operation and it will remain asserted until an End Sequence will be recognized. Multiple triggers caused by possible recognition of a Start Frame sequence during normal decoding operation has been carefully avoided.

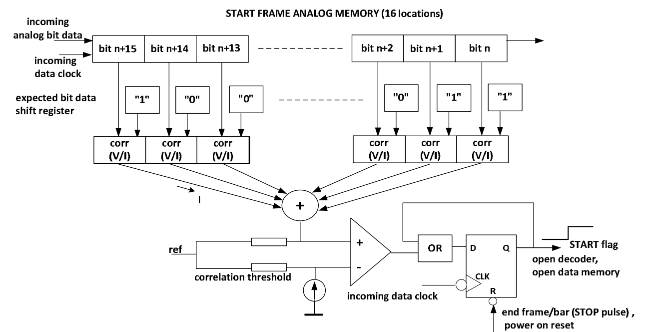

Figure 7: Acquisition Sequence Recognizer functional description.

The input memory is in charge of storing the incoming serial input analogue values upon each clock cycle into a corresponding memory cell, before parallel feeding the values to the decoder core for elaboration.

In principle, after the input values are stored inside the memory, they are fed all simultaneously to the decoder core for parallel decoding operation. With this approach, a “dead time” in input data throughput should be observed between the reception of two consecutive words caused by the decoding time. This constraint, although tolerated by a demonstrator, becomes unacceptable in real applications, where data throughput is in general continuous and a double buffer strategy seems better responding to the requirements.

Double buffering allows to fill one memory with incoming analogue values while the second memory is being redirected in parallel to the decoder inputs: in front of the cost of an additional memory, data throughput is allowed to be continuous, and the period available for the decoder core to converge into the decoded sequence is the whole period needed for receiving a single (next) encoded word, with a single word latency. This last property of double buffering relaxes the decoder speed requirements and hence the power consumption requirements.

The memory organization is reported in Figure 8.

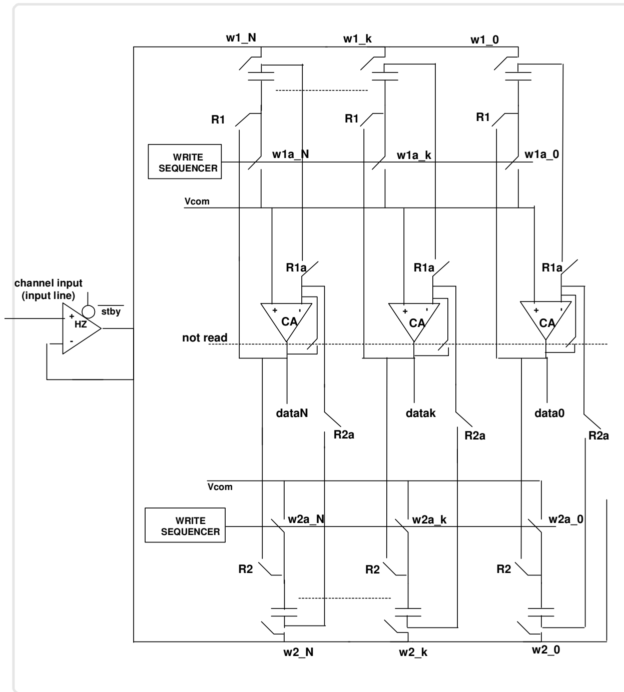

Figure 8: Double buffer memory structure.

Two arrays of capacitors, building the memory storing elements, are alternatively charged to store the incoming word values. A single input buffer provides the current capability for charging the quite high-capacitive writing line (due to the long tracks stray capacitances): the capacitors are charged in sequence, according to the switches *"w1_k/w1a_k"*, whose timings are synchronous with the input signal sampling operation.

While one of the memories is written sequentially with the incoming analogue values, the other one is read-out in a block and its values are fed in parallel to the analogue decoder core; during the read operation, each memory capacitor is connected as the feedback element of the column amplifier (CA), which provides an unitary replica of the input voltage stored in the capacitor element, referred to the common mode voltage. It is noticed that a single column amplifier is used which serves two different memory cells, read and written in different times: while one of the two memory cells connected to the unique amplifier is written (by storing a charge into the capacitor actually connected between the input line and the common mode reference), the column amplifier is in closed loop connection because it serves the other memory cell, so that its negative input terminal is never floating.

Finally, and for correctly resetting the decoder after each decoding operation, each column amplifier is connected as a buffer to produce an output level corresponding to the same common mode voltage for memory and decoder when no memory read operation occurs that is when a decoding operation is just finished and a new decoding operation is not yet started. It is noticed that, thanks to switches *"R1a"* and *"R2a"* in Figure 8, the resetting operation does not affect memory cells write operation.

With the purpose of using the above described reset phase also to discharge the memory capacitors before next memory bank write operation, the deactivation of read switches *"R"* and *"Ra"* of Figure 8 is delayed of half clock cycle with respect to the logic signals read. During this half clock cycle, the memory bank is still in its read phase, but the reset switch is closed, allowing the memory capacitor discharges (Figure 9).

In the following, some details about the optimum timing sequence for switches closing/opening are discussed with respect to charge injection issues.

The charge in steady state condition for each capacitance when the writing switches are both closed is determined basically by the signal-to-common-mode level, and both the input channel buffers and the common mode buffer driving the line *"Vcom"* in Figure 8 are low impedance nodes.

When the write operation ends for a single capacitor, the switch *"wa"* are open, whereas switch *"w"* remain in the low impedance state. Since the switch *"wa"* has a null voltage at its terminals, the charge injection expected by its turning OFF is a constant amount, not signal depending and this means that a systematic offset is added to the useful signals but no signal distortion is introduced by charge injection phenomena. Selecting a common mode voltage close to half the power supply rail and by implementing the switch as a carefully-sized complementary-transistors pass gate, the positive charge injection related with the pass-gate PMOS opening (which causes the bottom plate voltage of memory capacitor raises) is compensated by the equivalent negative pass-gate NMOS opening charge injection, thus leading in compensating effects.

During the read operation, still the closing sequence of switches *"R"* and *"Ra"* has poor relevance, because, until both switches are closed, no charge injection can occur: on the other hand, in steady state conditions, the memory capacitor terminals are respectively the CA (virtually to ground forced to *"Vcom"* level by the amplifier gain) and the CA low-impedance output node. When the read operation ends, first *"Ra"* switches open and as previously noticed for the write operation, the charge injection related with *"Ra"* switches opening is a constant amount of charge, not signal depending, which can be compensated for by adopting careful pass-gate design for the switches; of course, once *"Ra"* switches are open, no charging of capacitor can happen by the subsequent opening of switches *"R"*.

The most expensive power consumption inside the memory block is imputed to the line buffers because they have to provide the memory-capacitors charging/discharging currents within a single clock period, whereas the column

amplifiers settling time is drowned in the longer decoding time.

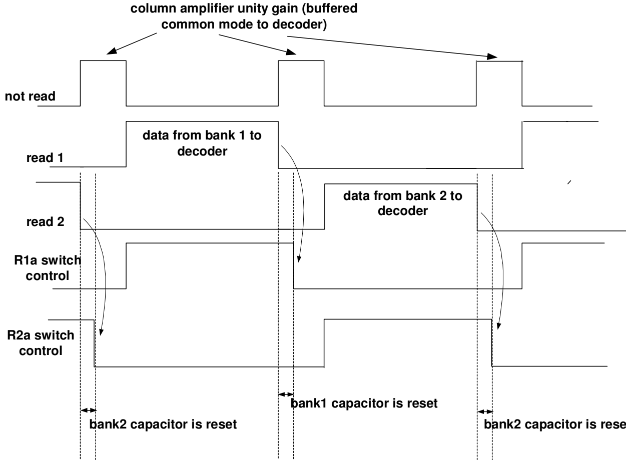

Figure 9: Timings diagram for decoder reset and memory bank capacitors reset on delayed read phase end.

VII. DECODER CORE ORGANIZATION

The last element of the receiver chain is the Decoder. According to ESA interest in LDPC short length code block codes for telecommand applications ([1] and [2]), the decoder implements the min-sum algorithm on the code LDPC (128, 64) referred in [2], which uses 64 check nodes, 8-bit-complexity each.

The mathematical steps of min-sum approximation approach to LDPC decoding and the main architectural results have been summarized in the general schema of Figure 12 and Figure 13.

The whole decoder configures as an asynchronous analogue network, built basically by two types of macro-cells (variable and check nodes), in which the decoding law is established by the interconnections between the cells at routing level, virtually programmable by metal mask option.

The iteration principle of digital implementation for solving the check law equations by progressively converging estimations is substituted by a continuous back-connection of each estimation-process-output at the estimation-process-input that forces the network to find its equilibrium "final" point estimations that satisfy the decoding law. Iterations and related overclocking with respect to input data throughput are hence suppressed, together with the need of checking the parity check matrix at each step in order to verify convergence.

By referring Figure 13, each variable node ("*qij*" level in the picture) calculates its own estimation, based on input log-likelihood data and based on data provided by all check nodes which are providing an estimation for that variable node, except the check node to which the variable node is just sending its own estimation.

Each parity check node ("*rji*" level in the picture) provides an estimation of each variable nodes afferent to it, by applying the parity check law (min-sum) to all other variable nodes (other than the one under estimation) afferent to it.

Both message forming processes (from the variable nodes to the check nodes and in the contrary direction) take place by adopting an *extrinsic information principle*: the information produced by a node (at its output) is never looped at its input to confirm itself but on the contrary, the information building process inside each node (variable or check node) always happens on the base of the information passed by different nodes.

The above observation is at the base of correct decoding principle: it may be noticed that each estimation of a single log-likelihood variable $\hat{ci}$ passed to check node *j* in Figure 13 is built by summing all estimations available for that variable (included the input log-likelihood level) except its estimation produced just by node *j*.

In the log min-sum approximation of the sum-product algorithm, the functionality of each variable node is log-likelihood probabilities summing (current sum), whereas the functionality of each check node is to select the minimum confidence (absolute value) of input log-likelihood probabilities and to assign it the expected sign for the check node output message.

Consequently, the basic processing analogue cells required for implementation are as follows:

- at variable node level, a voltage-to-current conversion must be operated to convert the input log-likelihood voltage levels into currents (the current sum can be easily performed afterwards by wiring currents together)
- at check node level, the minimum absolute value of input currents (disregarding their sign) has to be produced. To this purpose, each input variable to the check node is treated and de-composed in amplitude and sign (Figure 10): a looser takes all circuit coupled with a multiplexer (block "*select min (|u|)*") and it is used to select the minimum amplitude and the sign computation is performed by propagating the sign through XOR digital gates; finally, a reconstruction block is used to assign the proper sign to the minimum individuated for the output amplitude.

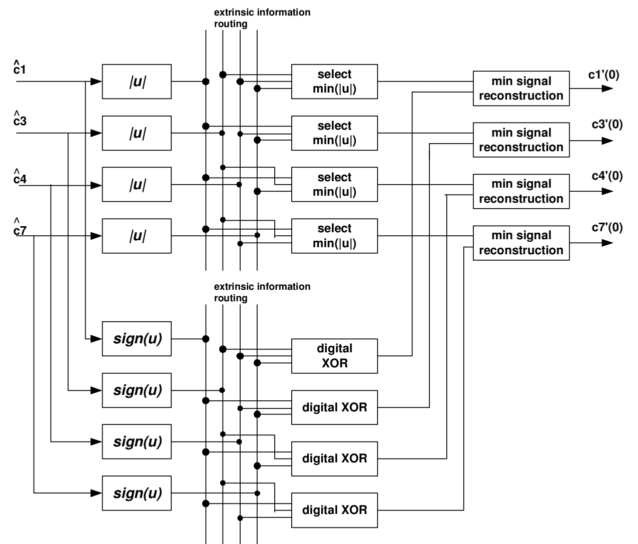

Figure 10: Details of the min-sum check node functionality.

The above operation performed by the check node finds its implementation in Figure 14, which reports the organization

of the basic 8-bit check node. The sub-block VN implements the functionalities of absolute value extraction and sign extraction of Figure 10, but it presides also to extract the a priori information and to combine this information with check nodes messages ($\sum$ operator of Figure 13). The LTA sub-block implements the minimum absolute value extraction and selection and the XOR sub-block implements the sign attribution to the check node estimation. Hence, for each input variable *i*, the schematic of Figure 12 selects minimum confidence and assigns logic sign to force parity-check law. In performing this operation, it applies an *extrinsic information principle*, basing its estimation about variable node *i* by relying only on other variable nodes (other than *i*) afferent to it.

Figure 15 shows the LDPC 128 bit decoder hardware organization.

VIII. CONCLUSIONS

In this paper have been presented a complete analogue receiver chain ASIC for telecommand applications for Category A missions (Return-to-Earth, lunar and even Lagrangian missions). Advantage and disadvantage of the analogue implementation respect to the traditional digital implementation based on FPGA have been presented. The blocks component the receiver have been described in detail and their functionalities have been analysed.

The receiver is now in detail design phase and it will be manufactured in XFAB 0.18um CMOS process.

IX. REFERENCES

[1] "European Cooperation for Space Standardization – Engineering – Space data links - Telecommand protocols, synchronization and channel coding", ECSS-E-ST-50-04C, Revision 2, 31/07/2008

[2] "Short Blocklength LDPC Codes For TC Synchronization and Channel Coding - Draft Recommendation for Space Data System Standards", (ref. CCSDS 231.0-O-x.x, Orange Book, April 2012)

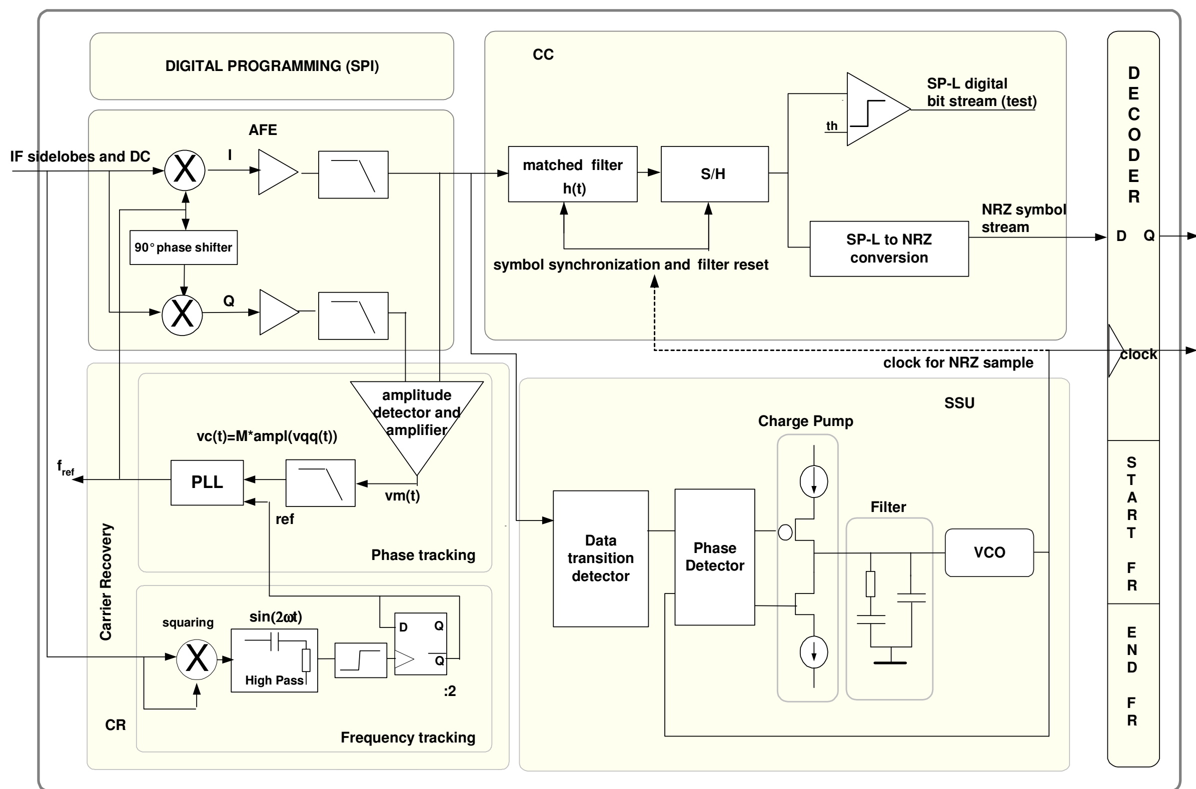

Figure 11: ASIC Block Diagram.

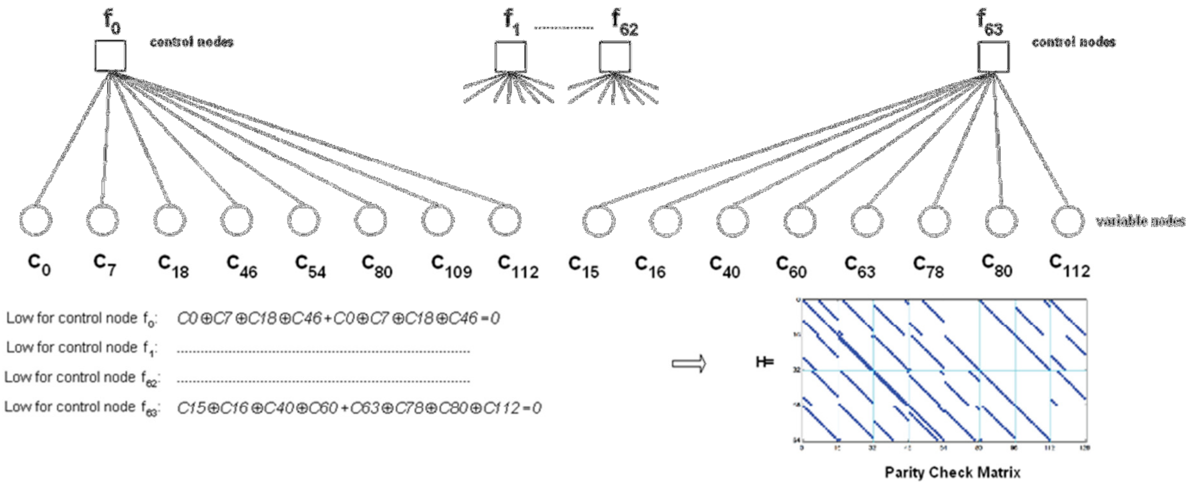

Figure 12: Check nodes for the referred (128, 64) code comprises 64 check nodes, each accepting systematically 8 bit from the variable node sequence.

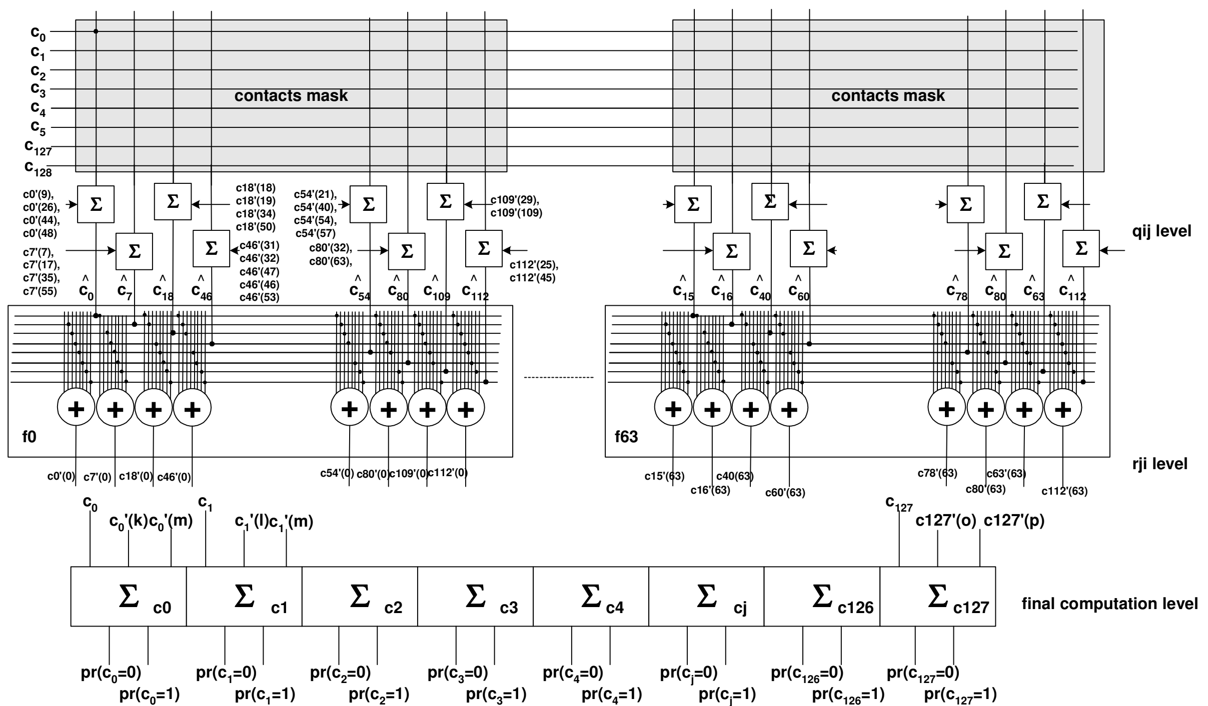

Figure 13: Low-level description of the min-sum algorithm applied to the parity check matrix of Figure 12

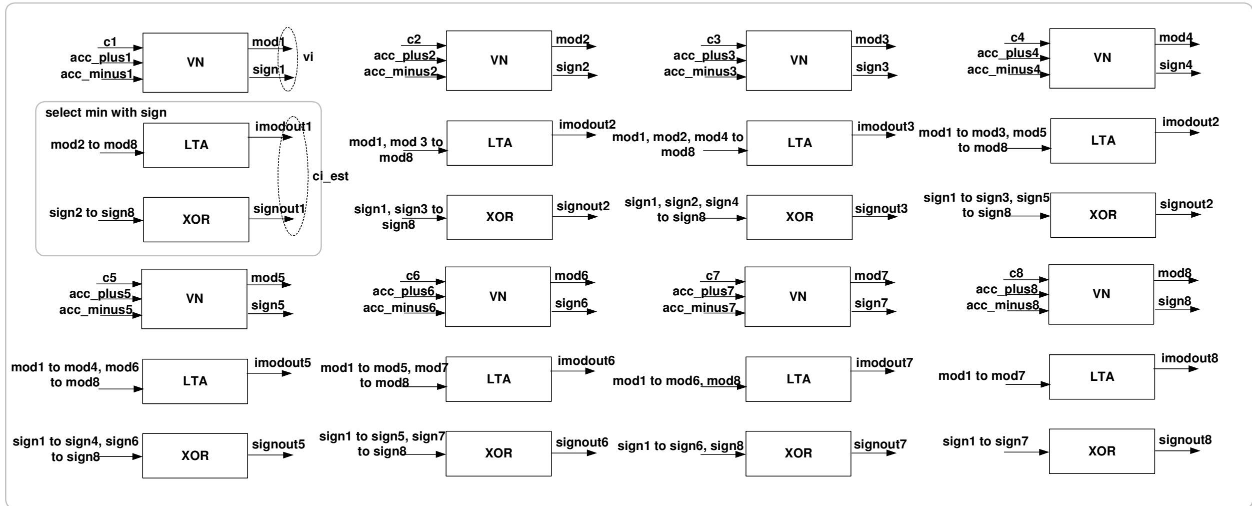

Figure 14: Basic 8-inputs check node cell.

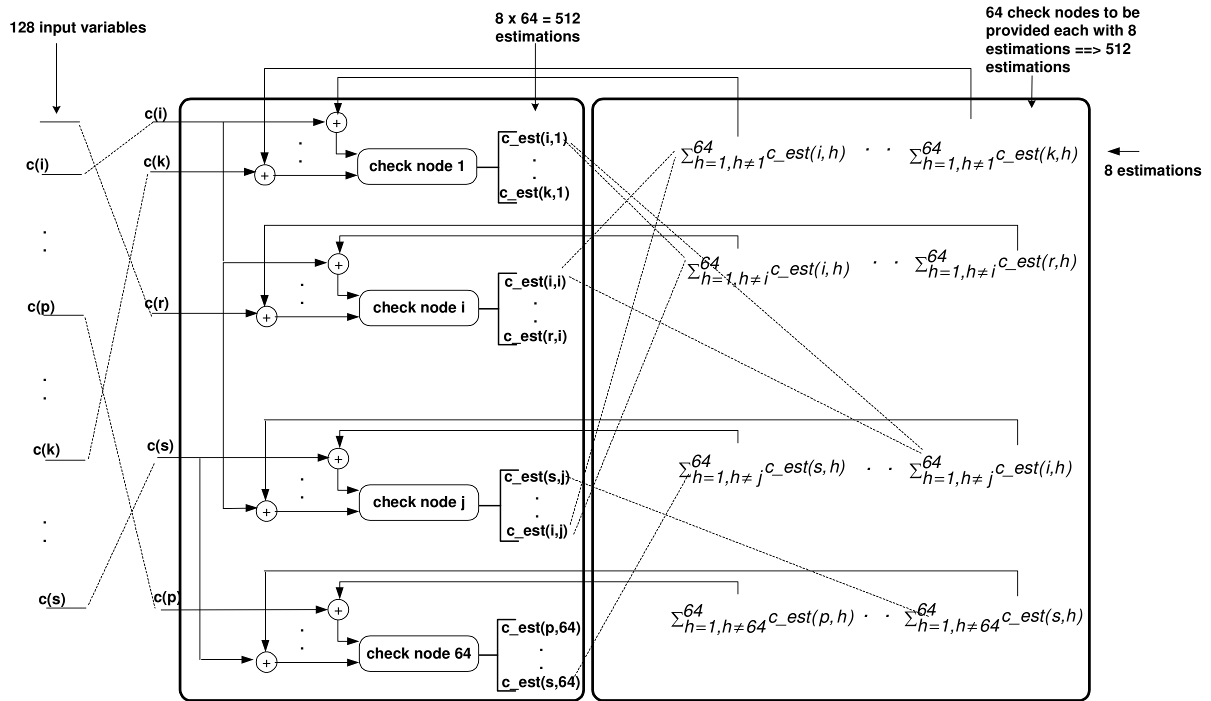

Figure 15: Decoder hardware organization: the left block is composed by the 64x8 inputs nodes and the right block is composed by 64x8 estimation adders.

Use of IHP's 0.25 μm BiCMOS Process in the Development of European LVDS Devices

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Abstract

Transmission of large amount of data is extensively used in communication among spacecraft and satellite onboard systems during a mission. LVDS (Low-Voltage Differential Signaling) Drivers and Receivers are key to provide means of sending/receiving data along twisted pair cables at very high data-rates with low power and excellent EMI performance. Rad-tolerant and Rad-hard ANSI EIA/TIA 644A complaint LVDS Drivers and Receivers products are essential in an extensive range of space applications. Typical applications with such needs are SpaceWire and clock distribution networks.

The purpose of this activity is the development of an LVDS Octal repeater in the frame of ESA's and ECI's European LVDS Driver Development intended to be used in space applications and built in IHP's 0.25-um BiCMOS process technology which has a good performance in terms of radiation, for both total dose and single event effects. Previous tests on this technology show no degradation up to 300kRad of total ionization dose (TID) and a single event latch-up (SEL) immunity up to 60MeV cm^2 mg^{-1} at least.

The key features of the octal LVDS repeater include cold sparing (essential for redundant systems architecture) up to 250MHz signaling rate per channel allowing 500Mbps transfer rates over SpaceWire, 3.3V single power supply, small propagation delay, low channel to channel skew, Tri-state output control, extended common mode on LVDS receivers and the minimum ESD tolerant rating of 8kV for human body model (HBM), 250V for machine model and +/- 500V for field induced charge device model. It also includes failsafe capabilities.

In order to validate and characterize the technology for the extended ESD tolerance an additional test vehicle chip has been built in the frame of the activity, with a set of ESD test vehicles that include NMOS clamps, PMOS clamps, and diodes.

I. INTRODUCTION

The capabilities of remote-sensing instrumentation are developing rapidly. As a consequence the data rates being handled on-board spacecraft are increasing. Photo and video data are a constant in many space missions. This pushes the need of connecting different systems with fast, reliable, low power links and to achieve this, Low-Voltage Differential Signaling (LVDS) addresses the need of high performance data transmission applications. The LVDS standard is becoming the most popular differential data transmission standard in the space industry.

LVDS delivers high data rates while consuming significantly less power than competing technologies. In addition, it brings many other benefits, which include:

- Low-voltage power supply compatibility
- Low noise generation
- High noise rejection
- Robust transmission signals
- Ability to be integrated into system level ICs. LVDS technology allows products to address high data rates in excess of hundreds of Mbps. For all of the above reasons, it has been deployed wherever the need for speed and low power exists.

LVDS is a differential, serial communication link, which uses low voltage differential signals (350 mV_p typ.), generated from a current source that delivers 3.5mA on a 100Ω termination resistor. It uses a typical common mode of 1.2V and limited slew rate to improve electromagnetic emissions. Point-to-point, single driver, single receiver and multipoint topologies, multiple drivers, multiple receivers, are compatible with LVDS devices where tri-state driver capability is present.

In this paper a LVDS octal repeater, with eight data channels plus and additional clock channel is presented. Each channel is made of an LVDS receiver and LVDS driver, with tri-state capability, to allow multipoint topologies. Failsafe feature is also included to ensure a known channel output in case of wiring or external driver failure. It works at a minimum of 500 Mbps data rate, at extended input common mode, with a typical 2.7 ns channel delay and extremely low channel-to-channel skew of 150ps. This repeater has Enable inputs for data and clock channels to set the LVDS outputs into tri-state mode. Cold spare functionality has also been included which means that the device input/outputs do not sink a significant amount of current if voltage is present at the pins while the device is at power off.

II. LVDS Octal Repeater Functionality

The LVDS Octal Repeater developed in the frame of ESA's and ECI's European LVDS Driver Development, has the following characteristics:

- Full ANSI EIA/TIA 644A compliance.
- Eight Data channels.
- One clock channel.
- Data channels enable pin.
- Clock channel enable pin.
- Tri-state driver capability.
- >500 Mbps data rate (250 MHz).
- Single 3.3 V Supply.
- Extended temperature range (-55ºC, +125ºC).
- Integrated voltage reference.
- Extended input common mode for LVDS inputs (-4V, +5V).
- Extended maximum absolute rating for LVDS inputs (-5V, +6V).
- TTL compatible digital inputs.
- Small channel delay, <2.7 ns typical, <3.5 ns over full temperature range.
- Low peak-to-peak jitter <236 ps (±3σ).
- Low channel to channel skew <150 ps typical, <250 ps over full temperature range.
- 8 kV HBM ESD enhanced protection.
- Fail-Safe functionality included.
- Cold Spare functionality.
- Radiation Hardness higher than 300 kRad (Si) TID with ELDRS and SEL immune up to 60 MeV cm2/mg LET.
- CQFP48 package.

III. Circuit Implementation

The block diagram of the circuit is presented in

Figure 1. It consists of nine channels, each of them using a LVDS driver and a LVDS receiver. In addition an integrated reference voltage and a linear regulator have been included.

A. Receiver

The receiver uses high frequency, high gain, rail-to-rail comparator to detect the LVDS differential signals present at the channel inputs. In order to accommodate the extended common mode range at the input, a frequency compensated attenuation network is placed at the input of the receiver. This reduces the signal to noise ratio of the signal, which makes the comparator design more complex. Fail-Safe circuitry is also included, which sets the output of the receiver in case an input is floating or the inputs are shorted together for more

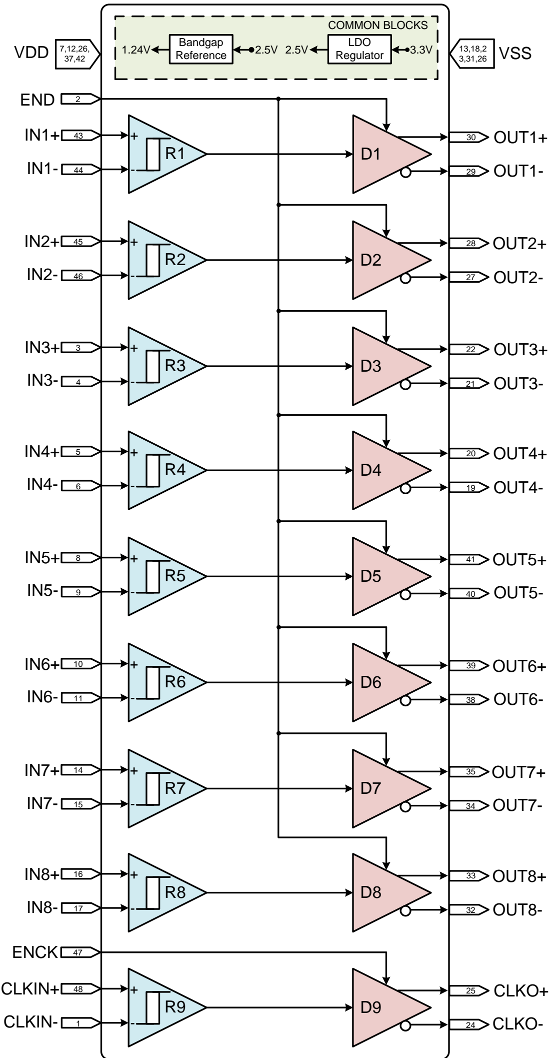

Figure 1. LVDS Octal repeater block diagram.

than 500ns. A fail-safe condition detector block checks when this condition is present and turns on an RC timer, than triggers after 500ns, setting the output of the receiver at high level, through a NAND gate.

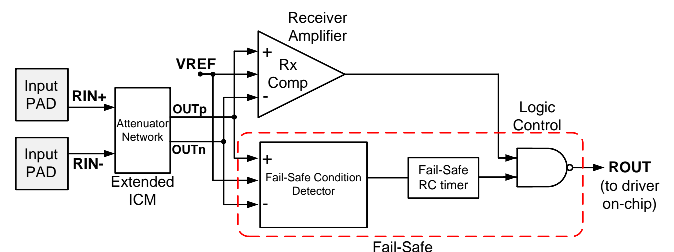

Figure 2. LVDS Receiver block diagram.

B. Driver

The driver consists of a driver core which generates the output currents (±3.5mA typ.) for the LVDS signals. The driver core has two current sources, which can be switched to sink or source current depending on the input level. The current levels are modified by the common mode feedback

loop in order to ensure the output voltage levels remain within certain limits that ensure that the common mode voltage is appropriate. The stability of the common mode loop is ensured by a minimum phase margin of 60º. The driver core is design to achieve a minimum data rate of 500Mbps.

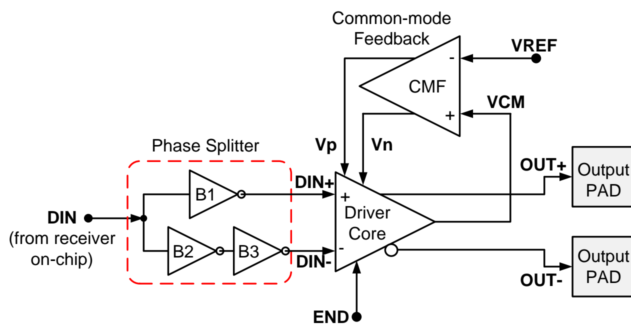

Figure 3. LVDS Driver block diagram.

The driver outputs have been designed to stand cold sparing. The enable input allows setting the output at high impedance.

Figure 4. Driver output at nominal conditions.

C. *Voltage Reference*

A 1.25V voltage reference has been included to generate the common mode voltages and biasing currents of the device. A first-order compensated bandgap reference was designed.

D. *Voltage Regulator*

A Low Drop Output voltage regulator is included to allow using a 3.3V supply for a core technology voltage of 2.5V.

E. *8kV HBM Pads*

Pads have been designed, including full custom devices, to achieve a minimum ESD protection of 8kV using a Human Body Model and 250V for Machine Model. These pads include analog input/outputs, power/ground pads and digital input pads. The digital pads were designed to be TTL compatible.

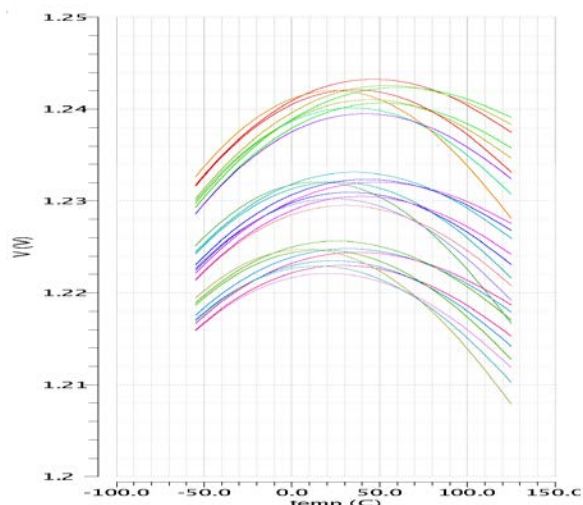

Figure 5. Bandgap output vs temperature in all corners.

F. *Hardening by Design*

Hardening By Design (HBM) techniques have been extensively used in the device design. Based on IHP SGB25RH technology, with radiation hardness heritage [1][5], techniques like systematic guard rings, custom digital cells, adequate W/L ratios or ELT for MOS transistors layouts among others have been used to achieve to a TID tolerance up to 300 krad(Si) at standard (1 rad/sec to10 rad/sec) and low dose-rate (0.01 rad/sec to 0.1 rad/sec). No bipolar transistors, excepting those used in the voltage reference, are used to improve LDRS. The design has been done to be SEL immune to LET levels higher than 60 MeV cm2/mg. Specific design rules provided by the manufacturer to improve radiation hardness have been used.

The SET sensitivity has been evaluated by the *Grupo de Ingeniería Electrónica*, from *Universidad de Sevilla*, using a proprietary software tool [2]. The tool injects certain charge in different circuit nodes to simulate a particle impact and analyses the transient on the relevant output. The results have mainly shown some sensitivity on certain nodes of the driver block, which in some cases can be outside of the LVDS voltage range, but results have to be correlated with the radiation tests to ensure SET hardness. Particle impacts in the common mode amplifier generate small output transients, due to the high CMRR of the driver. Transients at the output of the bandgap and the regulator have very little effect on the LVDS outputs, and no spurious glitches have been detected at the receiver output due to heavy ion impacts.

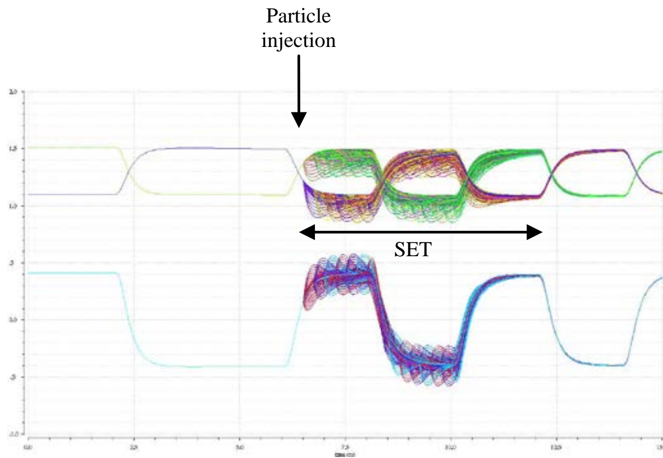

Figure 6. Example of intensive campaign of injected SETs at LVDS outputs and differential signal shown.

IV. SIMULATION RESULTS

The device has been extensively simulated in post layout, achieving full compliance with ANSI EIA/TIA 644A [3]. All simulations have been performed in the -55ºC up to +125ºC temperature range, including process and power supply variations when needed. The minimum data rate of 500 Mbps has been obtained, with an extended common mode of -4V to +5V. Small channel delay, lower than 3.5 ns and low channel to channel skew of 226ps have been achieved for worst case conditions. Cold sparing, tri-state and failsafe functionality have been also verified. The rise/fall times of the driver output are 412ps for a 1pF differential load [3], allows achieving a theoretical simulated maximum data rate of 728Mbps. The phase margin obtained in the common mode feedback loop is 72° in all conditions ensuring stability. In the regulator the minimum phase margin obtained is 90º. The bandgap has a minimum phase margin of 51° in worst case condition and 60º for typical ones.

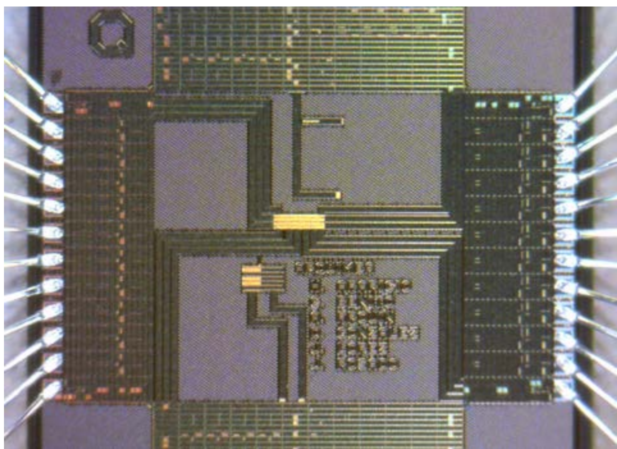

Figure 7. LVDS Octal Repeater die.

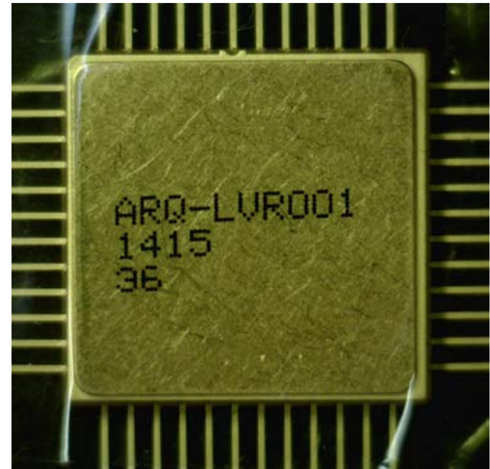

Figure 8 CQFP 48 Octal repeater package

V. EXPERIMENTAL RESULTS

The device has been implemented in a die of 2.06x2.06 mm^2, on IHP SGB25RH. A compact, low inductance, ceramic CQFP48 package has been used, to minimize channel to channel skew. ESD testing has been performed by IHP achieving more than 7.3kV for all pads, being the maximum voltage limited by the test equipment capability. Transmission Line Pulse technique has been used to perform the ESD testing.

Full temperature electrical characterization and radiation testing against TID and heavy ions is being performed by ALTER, not being finished at the time this paper is being published.

VI. CONCLUSIONS AND FUTURE DEVELOPMENTS

A radiation hard, Octal LVDS repeater has been designed and manufactured, showing a minimum data rate of 500 Mbps, small channel delay of 2.7 ns and low channel to channel skew of 150 ps. All this has been verified by extensive post layout simulations, over temperature, process and power supply variations. Full electrical characterization and radiation testing is being performed at the time this paper is being published. A theoretical simulated maximum data rate of 728 Mbps could be achievable.

A complete family of LVDS devices: driver, receiver, transceiver and crosspoint switch, with similar performances to the octal repeater, is under development by Arquimea as a result of this work.

A full evaluation/qualification of the device it is expected to be performed under an ESA contract.

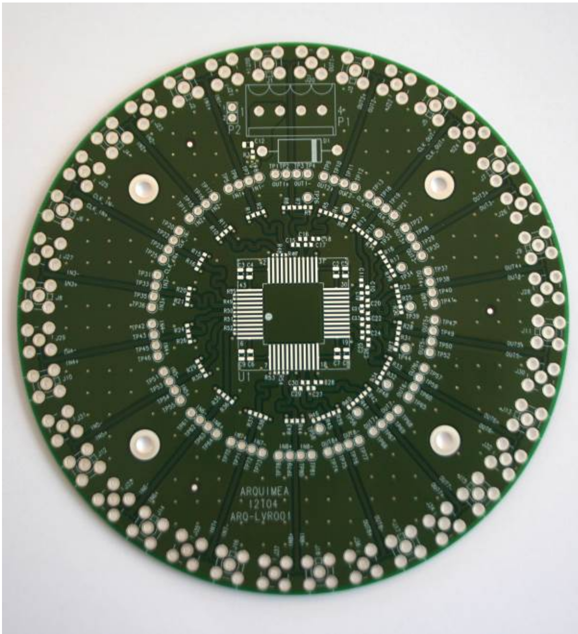

Figure 9 LVDS Octal repeater test board

ACKNOWLEDGMENTS

We would like to acknowledge the support of ESA for the Development of European LVDS Devices, on which this paper is based. We appreciate the assistance of the IHP team, René Scholz, Milos Krstic, Vladimir Petrovic and Florian Teply. For the design of the ESD protections, the support from Sofics, in particular from Bart Keppens and Olivier Marichal has also been appreciated.

REFERENCES

[1] Federico Faccio, B. Allongue, G. Blanchot, C. Fuentes, S. Michelis, S. Orlandi, and R. Sorge. "TID and Displacement Damage Effects in Vertical and Lateral Power MOSFETs for Integrated DC-DC Converters". IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 57, NO. 4, AUGUST 2010

[2] F. Márquez, F. Muñoz, F.R. Palomo, M.A. Aguirre and M. Ullán. "ANALYSIS OF SINGLE EVENT TRANSIENT EFFECTS IN ANALOGUE TOPOLOGIES" presented at 4th International Workshop on Analogue and Mixed-Signal Integrated Circuits for Space Applications AMICSA 2012.

[3] TIA/EIA-644-A, "Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits". Telecommunications Industry Association, February 2001.

[4] ESA-ESTEC Data Systems Division / Microelectronics Section, "ESA Handbook of Techniques for Radiation Effects Mitigation in ASICs and FPGAs", December 2011.

[5] Florian E. Teply, Dinesh Venkitachalam, Roland Sorge, René F. Scholz, Heinz-Volker Heyer, Miguel Ullán, Sergio Díez, and Federico Faccio "Radiation Hardness Evaluation of a 0.25 μm SiGe BiCMOS Technology with LDMOS Module", RADECS 2011 PROCEEDINGS.

[6] Xu Jian, Wang Zhigong, and Niu Xiaokang. "Design of high speed LVDS transceiver ICs", Vol. 31, No. 7 Journal of Semiconductors July 2010.

Rad-hard High Speed LVDS Driver and Receiver

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Abstract

A LVDS driver and a LVDS receiver have been processed in a 0.13um CMOS STMicroelectronics technology. It can operate over a large common mode input range from -4V to +5V, using a new architecture, to ensure immunity of ground shifting and driver offset voltage, while supply voltage is from 3 to 3.6V.To this aim, the common voltage input is sensed and adjusted to a fixed reference voltage 1.5V with an integrator loop and a class AB transconductor. These devices support data rates of 400 Mbps or 200 MHz .

These two LVDS circuits are designed for space applications. A total ionizing dose test campaign on elementary components has been performed to investigate the technology radiation hardness. The components have been radiated at high dose rate using a C060 gamma ray source. Specific mitigation techniques to achieve best in class hardness to total ionization dose and heavy ions have been applied. Moreover, the chosen technology has a substrate with very low resistivity which is very useful to decrease risks of latch up in general and more specifically Single Event Latch up.

One major challenge of these LVDS circuits has been to meet particular ESD specifications which were 16KV on LVDS receiver input and driver output combined with SEL immunity. Laser tests have been useful to best understand their behavior regarding latch up.

Both the receiver and driver have been evaluated in laboratory. Huge efforts and specific equipment have been necessary to measure properly propagation delays closed to 1.7ns with good accuracy (better than 100ps). Finally, 300 krad in high dose rate and 150 krad in low dose rate have been achieved. And heavy ions Single Events Effects tests have also been performed with good result

I. INTRODUCTION

A big challenge in data transmission is the constant increase in data-rate. Low Voltage Differential Signaling (LVDS), and high speed, low power general purpose standard interface is one of the key building blocks in transmission systems.

This paper presents LVDS driver and receiver circuits specifically designed, packaged and qualified for use in aerospace environment. The intended application of these devices (RHFLVDS31/32 quad drivers/receivers) is point to point baseband data transmission over controlled impedance media with a 100 Ω characteristic impedance. These devices support data rates of 400Mbps.

The Driver accepts low voltage TTL input levels and translates them to low voltage (350mV) differential output signals.

At the receiver side, a low voltage (100mV) differential LVDS input signals is transformed into TTL output levels. Moreover, a new architecture has been proposed in order to tolerate a large common mode input range (from -4V to +5V). It ensures immunity to ground shifting and to driver offset voltage, while supply voltage can vary from 3 to 3.6V.

These circuits feature an internal Fail-safe function to ensure a known state in case of shorted or floating inputs. In addition, all the pins have cold spare buffers to present a high impedance when VCC is tied to GND.

This paper is organized as follows: section II describes the configurations using these LVDS products. The design of driver and receiver are developed in section III. Section IV deals with Space specificities and cautions that have been taken in order to harden the design and the layout to the radiations.

Sections V et VI present respectively the ESD protections and the package used. Measurements results, electric and radiative follow in section VII. The paper ends with conclusion in section VIII.

II. SPACE WIRE CONFIGURATION USING LVDS

In this paragraph, we will first describe the different possible configurations for the LVDS cells in order to better understand the circuit requirements.

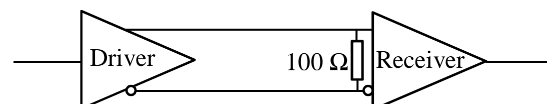


Fig. 1: **Point to point configuration schematic**

The **point to point configuration,** presented in Fig. 1, ensures the minimum discontinuities on the transmission line. It is interesting to avoid any stub problem on the line. A 100 Ω resistor, at the far end, terminates the two differential lines with matched impedance and provides the differential LVDS voltage with output driver current. Under the above conditions, the driver can drive a wire over 10 m at 200 MHz or 400 Mbps.

In the **bi-directional configuration,** shown in Fig. 2, data can flow in both directions, but only one a time. However the bus needs to be terminated at both ends. Therefore, two 100 Ω terminated resistors are necessary. These two resistors in parallel (100 Ω // 100 Ω = 50 Ω) will cut the output driver signal in half.

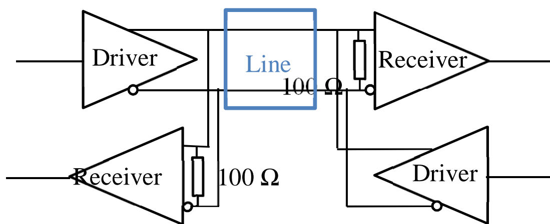


Fig. 2: **Bi-directional configuration schematic**

In the **multi-drop configuration,** described in Fig. 3, 10 receivers or more can be tied to the bus. Some receivers may be powered off while communication is from the driver to other receivers (powered on). However, if the stubs between line and the different receivers are too long, it may create reflections. It can also cause impedance discontinuity.

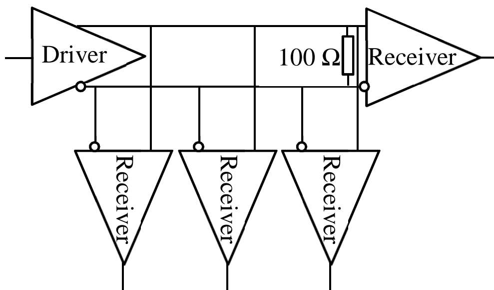


Fig. 3: Multi-drop configuration schematic

To solve this issue, a Receiver, followed by a Driver, can by use as a **Repeater** in the middle of the long line, as presented in Fig. 4.

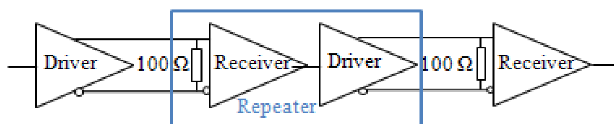


Fig. 4: Repeater configuration schematic

III. CIRCUIT DESIGN

A. Driver

The purpose of the Driver (Fig. 5) is to convert low voltage TTL input levels into low voltage differential output signals (350mV).

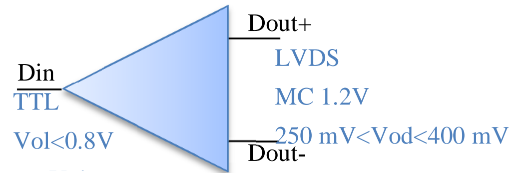


Fig. 5: Driver symbol

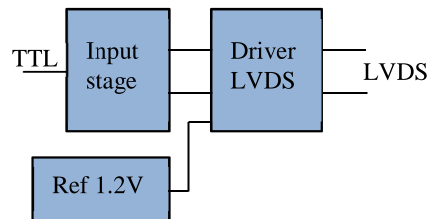


Fig. 6: Driver stages

For that purpose, the architecture depicted in Fig. 6 has been selected. The LVDS driver is mainly composed of two stages in cascade: the first stage is an inverters chain and the second stage a LVDS buffer.

Critical parameters are propagation delays (1.5 ns max), consumption (20 mA) and skew between two drivers (channel to channel skew 0.3 ns max).

The input stage architecture is described in Fig. 7:

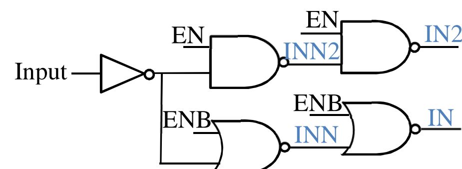


Fig. 7: Driver input stage schematic

A pull down in input, assures a low level in case of floating input. It is the fail-safe mode.

A CMOS band gap with vertical substrate pnp is used to generate the voltage reference of 1.2V stable versus supply and temperature. It is also used as current source for the other blocks.

As the driver block draws a high current, it can disturb the reference voltage. For that purpose, a buffer has been added between the bandgap and the driver in order to achieve a current isolation.

Based on the LVDS standard, defined in ANSI/TIA/EIA-644-A, the driver should be able to drive an external 100 Ω termination resistor with a voltage swing of Vod=250 to 400mV. Meanwhile, the common mode voltage of the output signal should remain within the range of Vos=1.125 to 1.45V. The following structure [1], presented in Fig. 8, has been chosen to meet consumption specifications (17 mA typical and 20 mA max).

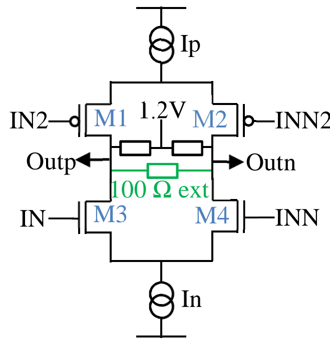


Fig. 8: Driver output stage

In this case, I=Vod/Rext=3.5 mA for 350mV. The drawback of this structure is that it is not 50 Ω matched. The common mode voltage is fixed by two 800ohms resistors connected to the 1.2 volts reference.

In order to minimize the common mode output voltage dc shift, the two current sources In and Ip must have values as closed as possible.

Some cautions, for the gates in input stage, have also to be taken to avoid simultaneous conduction, resulting in uncertainty zone for the outputs. In normal mode IN2=IN and INN2=INN.

For positive input, M1 and M4 are closed,

M2 and M3 are open.

For negative input, M2 and M3 are closed,

M1 and M4 are open.

This design structure is optimized for fast (or short) propagation time. As an example, by limiting the size of the output transistors, the parasitic capacitors are reduced thus improving the propagation time. At layout level, some precautions have also been taken to minimize routing of the critical nodes

B. Receiver

The Receiver, Fig. 9, converts low voltage (100mV) differential LVDS input signals into TTL output levels. It also can operate over a large common mode input range from -4V to +5V

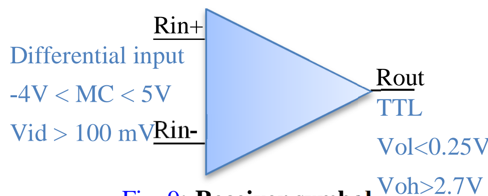


Fig. 9: Receiver symbol

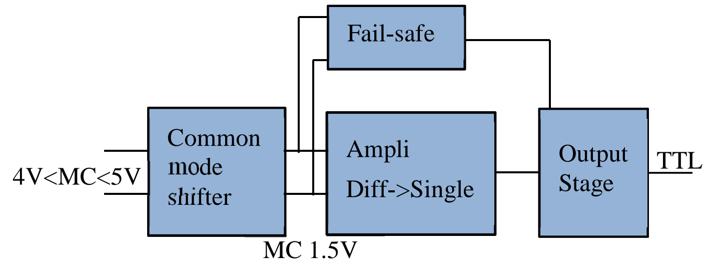


Fig. 10: Receiver stages

As shown in Fig. 10, the LVDS receiver is composed of three stages in cascade: the first one is a common mode shifter, the second one is a differential to single amplifier, and the third stage, an inverter chain, is the output stage.

In parallel with the second chain ,a fail-safe function stage is inserted

The input of the receiver should support a wide common voltage range: from -4V to 5V.The aim of the common mode shifter is thus to guarantee a stable 1.5V common voltage at the amplifier input, independently of this receiver common voltage, without attenuating the differential input signal. The high frequencies of the received signal put stringent requirements on the stability issue.

That's the reason why we finally came to the architecture described in Fig. 11.It has the advantage to isolate the input and the current sources thanks to an integrator.

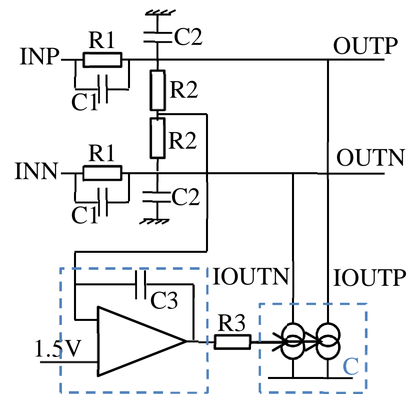


Fig. 11: Common mode shifter block diagram

The common mode shift is done through two resistors R1 in differential and two current sources Ioutp, Ioutn. The common voltage input is sensed and adjusted to a fixed reference voltage 1.5V with an integrator loop (noted I in Fig. 11) and a class AB transconductor, formed by R3 and a current conveyor C.

The system is equivalent to a high pass filter with respect to the common mode input voltage.

As stated before, the differential attenuation has to be as close as possible of unity. At low frequency, it is given by the following relation: DA=R2/(R1+R2)

R1 is chosen to meet input common range current specification for a 5.5V maximum common mode shift .

In parallel to the serial resistor C1, a small capacitor, is added to transfer the high speed LVDS signal (HF differential + HF common mode voltage). Moreover, an additional small capacitor C2 is added to get a flat gain from dc to high frequency. To keep the same attenuation at high frequency (Fig. 12), C2 should satisfy the following relationship:

DA= C1/(C1+C2) = R2/(R1+R2)

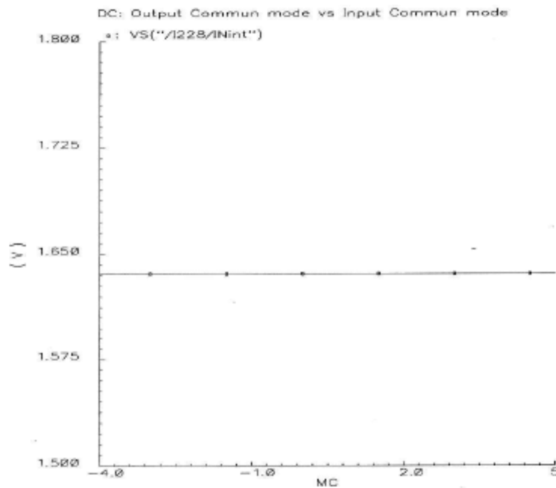


Fig. 12a: Common mode DC transfert function: common voltage is very well cancelled

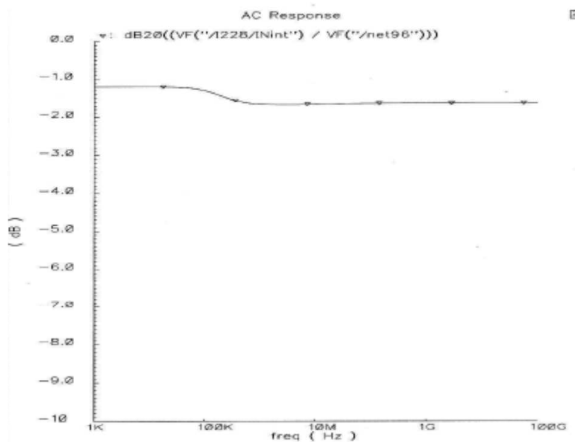


Fig. 12b:AC differential gain:attenuation:gain is only -1dB with a nearly flat response

However, these capacitors, **C1** and **C2**, cause poles at 200 kHz with **R1**, **R2** respectively. As a consequence to guarantee stability, the integrator cut off frequency (**R2C3**) has to be fixed much lower than these poles.

R3 is the feedback resistor of this current conveyor that fixes Ioutp=Ioutn=I(R3).

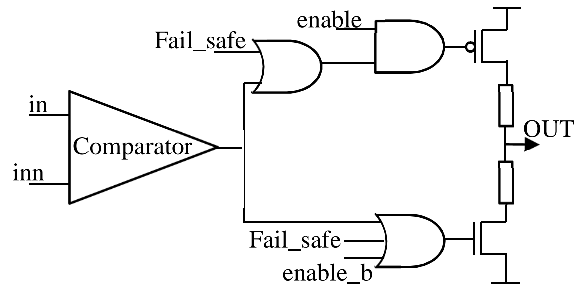


Fig. 13: Receiver principle schematic

Presented in Fig. 13, the differential to single amplifier is in fact a high speed comparator with dynamic hysteresis. The output of the main comparator is connected to one input of the differential pair responsible for the hysteresis.

To generate the TTL level the output stage of the receiver consists in a huge CMOS inverter.

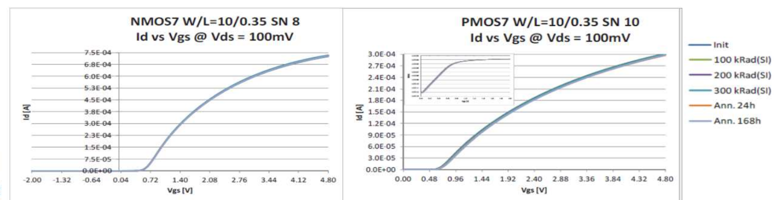
As the application imposes output impedance close to 50 ohms in order to minimize reflexions on line; serial resistors R have been added at the source of the output MOS transistors to reach this target. This constraint degrades speed performance. To compensate its impact, number of stages and area of output global stage have to be reduced. Finally, some optimized combination of NAND, NOR gates deal with signal, fail-safe and enable states. The output buffer manages the output drive of the receiver and its ability to drive a capacitance of 10pF

According to the common mode shifter block diagram, if V(IN) -V(INN) is lower than 100mV and if there is no more transition on these nodes, then we are considered in failsafe mode. This puts both output MOS transistors in high impedance mode by acting on their gate.

IV. SPACE SPECIFICITIES

The LVDS circuits are designed for space applications. A total ionizing dose (TID) test campaign on elementary components has been performed to investigate the technology radiation hardness. The components have been radiated at high dose rate using a Co60 gamma ray source. The results are presented in Fig. 14.

Fig. 14: NMOS and PMOS drift vs radiations



The TID test on PMOS confirms that threshold voltage shift is not an issue for advanced CMOS processes due to thin gate oxides. This is also confirmed on the NMOS components

with high W[3]. The CMOS G02 (gate oxide tox=8.5nm) can be considered rad-hard until a TID~100Krad (completely recovery of the Ioff leakage current). As our schematics are not sensitive to Ioff, they can support higher TID.

Moreover, the chosen technology has a substrate with very low resistivity which is very useful to decrease latchup risks in general and more specifically Single Event Latchup (SEL).

Some precautions have also been taken in order to harden the design and the layout to the radiations. The methodology was the following.

Firstly, Single Event Transient (SET) are simulated using double exponential current sources injected on each transistor. This allows us to evaluate the transistor sensitivity to the radiation Transient. Then, analyze has been done to identify the most sensitive transistors and the schematic has been improved accordingly to avoid too drastic events.

In layout, to prevent Single Event Latchup (SEL), all NMOS and PMOS have been layouted with deep nwell isolation as shown on the cross section below Fig. 15 .

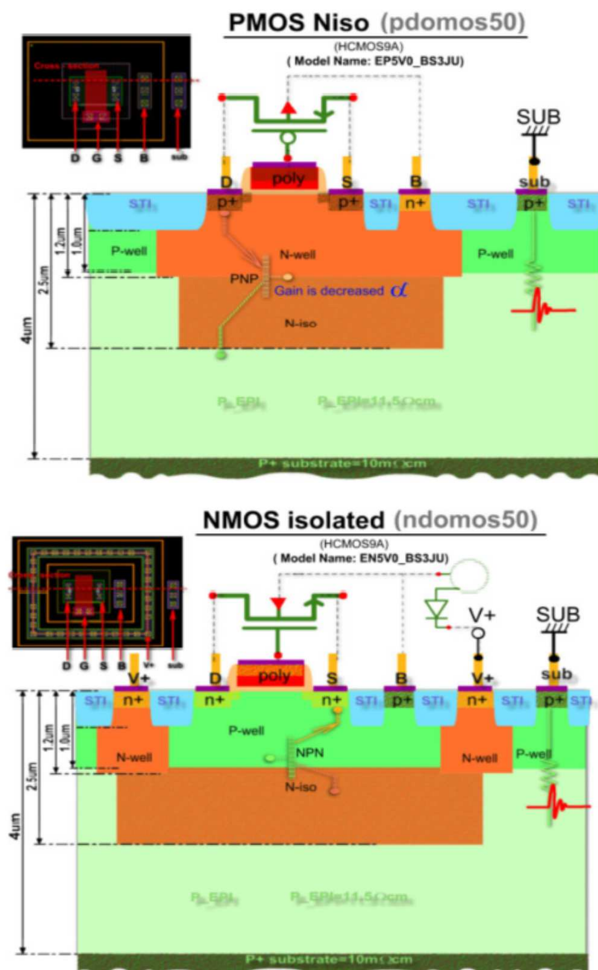


Fig. 15: Isolation layer and Guard ring for nwells , pwell

Systematic continuous tapping at NWELL & PWELL edges and also continuous substrate tapping at DNW edges have been used also.

A specific DRC for these SEL specificities was developed and used for final layout verifications.

V. ESD PROTECTIONS

One major difficulty to design these LVDS circuits has been to meet the particular challenging ESD specifications imposed at 8KV on LVDS receiver input and driver output combined with SEL immunity. The large common mode input range of -4V to +5Vwhich has to be tolerated at the receiver input makes the development even more difficult.

Two innovative ESD devices have been developed to protect input/outputs of LVDS links [8]. Both protections are isolated by deep well isolations layers for latch up immunity.

For outputs, a Silicon Rectifier (SCR) with its associate triggering system combined to a reverse diode has been used as standalone ESD protection. With this architecture output signal swing achieved was -0.7V up to 6V allowing large common mode.

Parasitic capacitance of overall output protection was 800fF for 16 KV HBM ESD target.

SEL immunity has been achieved using appropriate isolation strategy avoiding floating gate of SCR.

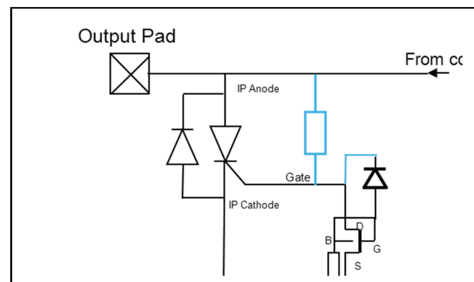


Fig. 16: Output ESD protection schematic.

Fig. 16 represent schematic of output ESD protection with, in blue, pull up resistor and well isolations linked SEL immunity.

For inputs, two back to back SCR, also called TRIAC with symmetrical triggering circuit have been used as standalone ESD protection. The use of TRIAC device allows us to achieve an input signal swing from -4 V up to 5V, compatible with large common mode voltage.

Parasitic capacitance of overall input protection was 960fF for 16 KV HBM ESD target. SEL immunity has been achieved using innovative isolation of triggering systems.

Fig. 17 shows schematic of input ESD protection with, in blue, well connection linked SEL immunity.

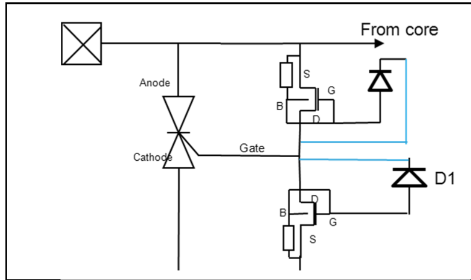


Fig. 17: Input ESD protection schematic.

ESD protection characterization has been done using Transmission Line Pulse (TLP) equipment. Equipment setup was 100ns pulse duration 10ns rise time to emulate energy of HBM ESD stress. Both protections were able to sustain ±9 Amperes TLP with a maximum overshoot of 8.5Volts. This performances show us the ability protection to sustain 16KV HBM stress. For final product qualification a conventional ESD tester has been used showing the ability of LVDS pins to resist to 8KV HBM (tester limit).

Laser tests have been useful to best understand their behavior regarding SEL immunity. The bench is composed of a microscope and a pico laser source (pulse energy from 100pJ to 6nJ). The laser beam is focused on the backside of the device. An infrared camera is used to visualize the internal structures through the silicon substrate. The consumption is monitored to detect every voltage breakdown.

VI. PACKAGE

These LVDS circuits: quad drivers and quad receivers are inserted in Flat 16 standard packages.

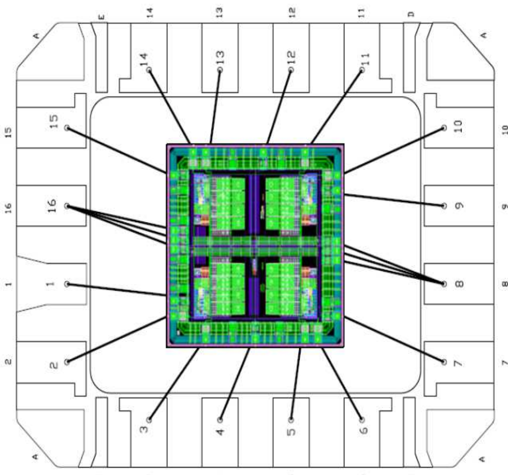


Fig. 18: LVDS31, die and package

The die size is defined to reduce bonding because the self-induced by bonding lead have an impact on dynamic performances.

Fig. 18 and Fig. 19 give the pictures of the 2.1 mm * 2.1 mm dies in the flat16 packages:

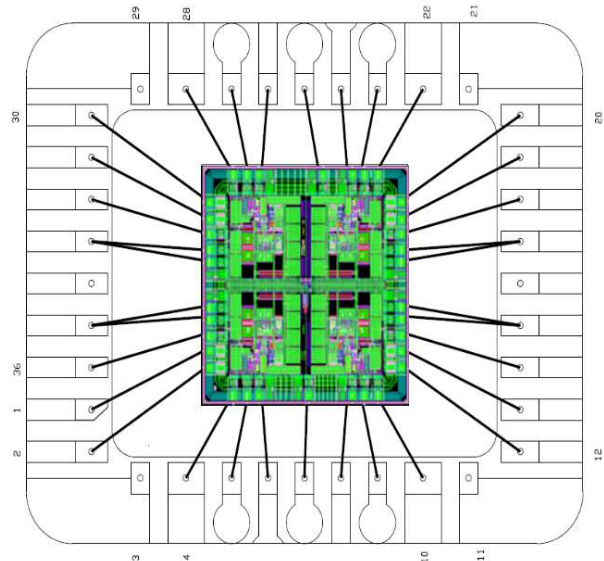


Fig. 19: LVDS32, die and package

For the receivers (LVDS32), as the output buffer signals have very short transition time (0.6ns) a huge peak current is taken from the power supply. In order to minimize inter channel cross talk, a lot of on chip decoupling capacitors have been added. Furthermore, each channel has its own couple of supply pads in order to minimize this crosstalk. A dedicated package with inter routing for power supplies has been developed in order to get a standard pinout.

VII. MEASUREMENT RESULTS

A. Electrical

Both the receiver RHFLVDS32 and driver RHFLVDS31 have been evaluated in laboratory. The evaluation boards are presented in Fig. 20 with measurement setup.

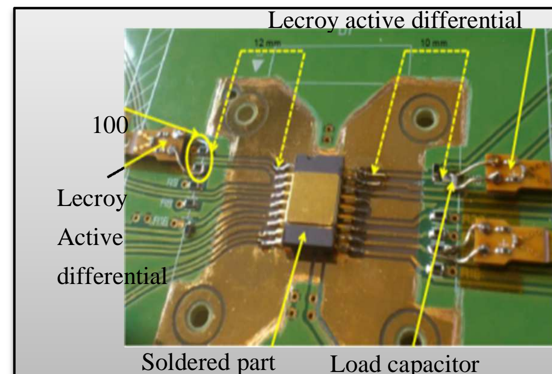


Fig. 20: Measurement evaluation board

Huge efforts and specific equipment have been necessary to measure properly propagation delays with good accuracy (better than 100ps).

Cautions have especially been taken on capacitive load, lines and reflections. Finally, propagation delays measured are around 1.85ns for the receiver as expected by the specification, as shown in Fig. 21.

Fig. 21a: LVDS Receiver, propagation delay

The eye diagram below has been performed with a driver(31) connected to a receiver(32) through a 183cm length line. We have got a total jitter of 616ps, a random jitter of 20ps and a determinist jitter of 336ps.

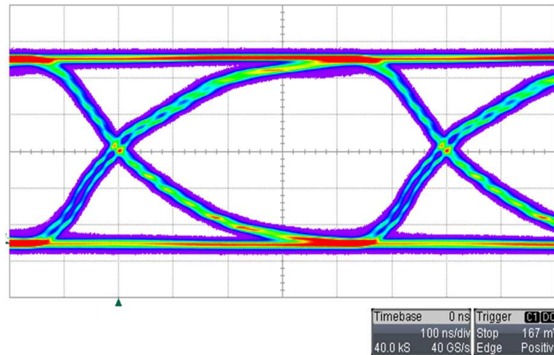


Fig21b: LVDS Receiver eye diagram

In the tables below (Fig. 22), major measurements results are compared versus specifications expected:

LVDS31		Specification			Measure
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Typ**
ICCL	Total enabled supply current		20 mA		16.5 mA
tPHLD	Propagation delay time, high to low			1.9ns	0.95 ns
tPLHD	Propagation delay time, low to high			1.9ns	0.95 ns
tSKP	|tPHLD-tPLHD|			0.3 ns	< 100 ps
tSK1	Channel to channel skew			0.3 ns	< 100 ps
tSK2	Chip to chip skew			0.7 ns	
tr / tf	Output signal rise / fall time		1.2 ns		0.820 ns
ESD	HBM: input LVDS		8 kV		OK
ESD	HBM: all other pins		2 kV		OK
TID	High Dose Rate(50-300 rad/sec)	300 k rad			OK
Heavy-ions	SEL immunity(at 125) up to:	110 MeV.cm2/mg			OK

Fig22a: Tables with major measurements results for Driver

LVDS32		Specification			Measure
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Typ**
ICCL	Total enabled supply current		15 mA		12.5 mA
tPHLD	Propagation delay time, high to low			3.1 ns	1.85 ns
tPLHD	Propagation delay time, low to high			3.1 ns	1.85 ns
tSKD	|tPHLD-tPLHD|			0.3 ns	< 100 ps
tSK1	Channel to channel skew			0.3 ns	< 100 ps
tSK2	Chip to chip skew			0.7 ns	
tr / tf	Output signal rise / fall time		1 ns		0.870 ns
ESD	HBM: input LVDS		8 kV		OK
ESD	HBM: all other pins		2 kV		OK
TID	High Dose Rate(50-300 rad/sec)	300 k rad			OK
Heavy-ions	SEL immunity(at 125) up to:	110 MeV.cm2/mg			OK

Fig22b: Tables with major measurements results for Receiver

B. Radiations

300krad in high dose rate and 150krad in low dose rate have been successfully achieved.

Heavy ions test were performed on both Driver and Receiver. The aim of the test was to evaluate the sensitivity of these devices versus SEL and SET.

No SELs were observed with the LET value of 67.7MeV.cm²/mg (Xenon heavy ions) at 125 degrees.

SETs were observed with a minimum LET of 67.7 MeV.cm²/mg. No SET was detected with a LET of 32.6 MeV.cm²/mg at 25 degrees.

VIII. CONCLUSION

The Rad-hard LVDS driver and receiver described in this paper, have been processed in a 0.13um CMOS STMicroelectronics technology with specific mitigation techniques, to achieve best in class hardness to total ionization dose and heavy ions.

The chips have been manufactured and verified from a functional perspective, as presented in this paper.

Radiation characterization and power-temperature stress test have also been done, to ensure 300 krad TID and 8 kV ESD on LVDS pins.

ACKNOWLEDGEMENTS

The authors would like to thank Francesco Toscano, Gilles Gasiot, Nicole DeBacker, Thibaut.Lardeau, Marc Rodary, Olivier Croisat, Jean-Louis Bernet, Andre Uguen, Adrien Soufflet, Gregory Gibault, Stella Gioanni for their major contributions to the success of this project.

REFERENCES

[1] Tajalli, Y. Leblebici, "A Slew Controlled LVDS Output Driver Circuit in 0.18 um CMOS Technology", *IEEE Journal of solid-state circuits, vol. 44, no. 2, February 2009.*

[2] M. Chen, J. Silva-Martinez, M. Nix, M. E. Robinson, "Low-Voltage Low-Power LVDS Drivers", *IEEE Journal of solid-state circuits, vol. 40, no. 2, February 2005.*

[3] F. Faccio and G. Cervelli, "Radiation-Induced Edge Effects in Deep Submicron CMOS Transistors", *IEEE Transactions on nuclear science, vol.52, no. 6, December 2005*

[4] RHFLVDS31A Datasheet "Rad-Hard Quad LVDS driver" *ST, March 2013*

[5] RHFLVDS32A Datasheet "Rad-Hard Quad LVDS receivers" *ST, March 2013*

[6] LVDSR2D2 Datasheet "Rad-Hard Dual LVDS driver-receiver" *ST, March 2013*

[7] LVDS-MUX8 Datasheet "Rad-Hard Dual 4*4 Crosspoint Switch LVDS" *ST, March 2013*

[8] Jimenez, J., Galy, P., Bourgeat, J., Heitz, B. "High swing low capacitance ESD RF protections in advanced CMOS technologies ", *IC Design & Technology (ICICDT), 2012 IEEE International Conference on IC Design & Technology*

Applications for Radiation Hardened Analogue and Mixed-Signal ASICs: Power and Micro-controllers and Signal Processors

A radiation-tolerant Point-Of-Load buck DC-DC converter ASIC

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Abstract

In view of application in upgraded particles detectors at its LHC accelerator, CERN has developed a radiation and magnetic-field tolerant DC-DC converter based on a radiation-tolerant ASIC, FEAST2. The circuit, designed in a selected commercial CMOS technology with high voltage capabilities, has been designed using 'Hardness-By-Design' (HBD) techniques and has been qualified with different radiation sources. Results of these tests are summarized evidencing that the achieved radiation tolerance satisfies the requirements of the LHC experiments in terms of Total Ionizing Dose (TID), Displacement Damage (DD) and Single Event Effects (SEE), making it also a possible good candidate for applications in Space. FEAST2 is now in production and CERN is using it to supply LHC experiments with full DC-DC plug-in modules.

I. Introduction

The particle detector systems at the CERN Large Hadron Collider (LHC) accelerator are preparing upgrades to improve their performance, in particular in view of the increased luminosity of the accelerator in the years to come. A serious limitation to the overall detector performance comes from the present distribution scheme, where the on-detector low-voltage electronics is directly powered from back-end supplies positioned tens of meters away, in the experimental cavern. The mass of the cables in such system is rather large, and it will not be possible to increase the supply current as required for improved detector performance without increasing the cables' mass further. This in turn is incompatible with the capacity of the detector to study the desired physics.

An obvious way of solving the problem is the distribution of power at higher voltage, with local (on-detector) conversion and regulation down to the voltage required by the front-end electronics. This task should be performed by a DC-DC converter installed in close proximity of the electronics, on the detector modules. The main specific requirements for this converter are radiation tolerance, compatibility with the magnetic field of (up to) 40,000 Gauss present in the central portion of the detector, low noise and small size (footprint, height) – coupled in some cases with extremely low mass. Since a converter satisfying the above requirements did not exist, CERN started an R&D activity to this purpose a few years ago.

To achieve the highest degree of integration, hence the smallest footprint and mass, we chose to go to an almost monolithic solution where all the active components are embedded in a single microcircuit, an Application Specific Integrated Circuit. The choice of the substrate technology for the design of the ASIC was not a simple affair: while the electrical specifications demanded the availability of high-voltage (above 12V) transistors for the power train and the on-chip regulators, at the same time the radiation tolerance requirements were hard to meet for such transistors. A long characterization phase, where 5 different candidate CMOS technologies were tested for radiation effects, was completed and eventually a suitable 0.35um process – commercially available for custom design – was selected [1].

The choice of the most appropriate converter architecture was driven by efficiency and mass/footprint considerations. The efficiency in principle achievable by different architectures in some of the candidate CMOS technologies was evaluated, and weighted over the number of passive components each of them required – with particular emphasis on the largest and more massive of them, the element storing the energy during switching (inductor or capacitor). At the end, the simplest architecture was chosen: the buck step-down converter that only uses one inductor and a few capacitors [2].

In parallel to the ASIC development, which required several prototyping cycles, extensive effort was dedicated to the integration of the circuit in a compact module reaching the Electromagnetic Compatibility (EMC) performance adequate for installation of a full DC-DC converter in very close proximity to the sensitive read-out electronics of the particle detectors [3]. The aim was the development of a unique and well-characterized plug-in module that would satisfy the requirements (electrical, footprint, height, radiation tolerance) of all detector systems.

After several years of R&D activity, the development has now reached full maturity and both the ASIC and the module are entering series production. The datasheet for both can be found in the public web page of the CERN DC-DC development project [4]. This paper describes the main features of the ASIC and details its radiation tolerance characterization.

II. FEAST2 features

FEAST2 is the production-grade buck DC-DC ASIC developed within the framework described above. The circuit has a size of 2.8 x 2.88 mm^2, and is manufactured in a commercial 0.35um CMOS process offering LDMOS transistors rated at 12V and above (different transistors are available with different V_{ds} capability). This process was developed mainly for automotive applications and offers a

wide palette of high-voltage devices, together with isolation from the substrate via wells that can also stand high voltage.

The ASIC integrates both the power train and all required control circuits, including the bootstrap diode for the driving of the High-Side power transistor, several linear regulators to derive the on-chip supply rails from the unique 10-12V input voltage, and reference voltage and current generators.

Being targeted for application in a radiation environment, the design makes extensive use of HBD for both TID and SEE tolerance. For TID, n-channel transistors are laid out as enclosed devices to prevent source-drain leakage currents – a design that is often called 'Enclosed Layout Transistors' (ELT) [5]. Also, p+ guardrings are systematically surrounding n+ wells and diffusions at different potential to cut any inter-device leakage path. For SEE hardening, several techniques are used in different circuit blocks. In some cases transistors and currents have been over-sized to increase the charge needed to upset the circuit's node. This same effect was reached in other cases by adding extra capacitance in the form of either metal-metal or MOS capacitors. Equivalent RC filters are used in 'slow' nodes to prevent the propagation of fast glitches (SET). Finally, essential control circuits whose upset could potentially have large impact on the full converter have been triplicated and their output voted.

Electrical specifications of FEAST2 include input voltage up to 12V, output voltage in the range of 0.6-5V, continuous output current up to 4A, maximum output power of 10W. The circuit is optimized to use an about 400-450nH inductor, hence it switches at a frequency of the order of 1-3MHz – the best compromise performance for efficiency and EMC being around 1.8MHz. The high frequency (150kHz) of the feedback loop, whose elements are almost entirely integrated on-chip, ensures a rapid response of the converter in case of load and line transients.

FEAST2 offers a number of safety features. To prevent excessive current in-rush at start-up, a Soft-Start procedure is executed every time the converter is enabled: the output voltage rises gently to the nominal value in about 470us. An Under-Voltage Lock-Out system (UVLO) monitors the input voltage and only allows the circuit to be functional in the presence of a sufficiently large input voltage (about 5V). The output current is monitored on a cycle-by-cycle basis: whenever the peak current during each switching cycle exceeds a pre-determined level the PWM signal keeping the High Side power transistor turned on is interrupted. This is part of the Over-Current Protection system (OCP), and in the event of persistent excessive current the converter practically enters a constant current supply mode with a decrease of the output voltage provided to the load. The junction temperature of the ASIC is monitored by an Over-Temperature Protection system (OTP) that disables the converter whenever it exceeds about 100ºC.

In terms of external control features, FEAST2 can be turned on/off via a dedicated enable pad compatible with any CMOS logic level between 1.0 and 3.3V. A Power Good signal is provided to the external world via a dedicated pad, which is connected internally to an open-drain NMOS transistor. With a pull-up connection to the appropriate voltage, this pad can provide valid CMOS logic levels up to 5V. The Power Good is normally asserted (logic 1) when the converter is correctly regulating the output voltage at the nominal value. If the output voltage exits a regulation window of about ±6.5%, or if the OTP detects excessive temperature, the Power Good is negated (logic 0).

FEAST2 is packaged in plastic QFN32 packages with exposed thermal pad to ensure sufficient chip cooling at high output power levels.

III. Irradiation Results

The radiation tolerance qualification of the ASIC required the measurement of samples in different radiation environments. Since the circuit needed several prototyping cycles before maturity, each prototype was in fact fully characterized to reveal weaknesses to be corrected in the next iteration. The results reported below refer hence not only to FEAST2, the production-ready version of the converter, but also to its immediate predecessor FEAST. The latter was almost meeting all specifications, but for the sensitivity to SEEs. Since the modifications required to improve the SEE response were minor and most of the circuit was unchanged, irradiation results for TID and DD obtained on FEAST samples are well representative of the final FEAST2 as well.

For TID the X-ray irradiation system installed within the CERN PH-ESE group was used. This system has characteristics very similar to the most widespread Aracor irradiation system [6] and can reach a dose rate of about 9 Mrad(SiO_2)/hour. Given the used radiation source for TID, all doses will be expressed in SiO_2 in the rest of the paper. For displacement damage, tests were run on different prototypes at either the CERN PS IRRAD1 facility, which provide an intense beam of 23 GeV/c protons, or at the Triga nuclear reactor of the Jozen Stefan Institute (JSI) in Ljubljana, Slovenia. Finally, the irradiation campaigns to study the sensitivity to SEEs took place at the Heavy Ion irradiation facility of the Cyclotron Resource Centre of Louvain-la-Neuve, Belgium.

A. Total Ionizing Dose

Several samples of FEAST2 were exposed to X-rays at either 25 or -30ºC. The latter temperature has been chosen to minimize the annealing of defects during irradiation, and because it is the temperature foreseen for the cooling system in some of the detectors planning to use the DC-DC converters. The circuit was mounted on a full DC-DC module and fully functional during irradiation and subsequent annealing: an output voltage of 2.5V was selected for the converters that were providing 1 or 2A to an external active load. Samples were irradiated up to a TID of 200 to 720Mrad and were constantly working during both irradiation and annealing. Testing was pushed to these extreme levels, well above any requirement for Space application, because some of the LHC detectors requiring DC-DC conversion will be exposed to doses of 200Mrad or more, so it was interesting to see if the ASIC had good margin for correct functionality at those levels.

All the main thresholds for the protection systems (UVLO, OCP, OTP) were measured and found not to shift significantly during the full test. The efficiency is rather

marginally affected by the irradiation (Figure 1), its variation being directly related to the radiation-induced leakage current and the increase of the on-resistance in the NMOS transistors of the power train. The peaked decrease of the efficiency, with minimum at around 2Mrad, is determined by the leakage current in the NMOS: some current finds its way from Vin to ground and determines additional losses. The leakage is the same whichever the load current, hence the efficiency drop it induces actually decreases considerably with the output load (it is almost negligible at 3 and 4A). It should be noted also that this leakage current has been found to anneal very quickly even at cryogenic temperature, therefore the efficiency drop in the application, at much lower dose rate, is expected to be considerably milder. To support this hypothesis, a sample has been irradiated at the high dose rate usual of our experiments up to 1.66Mrad (peak of the degradation) at -30ºC. With irradiation stopped, the sample was kept at the same T for 20 hours: the efficiency that had dropped by almost 4% during irradiation increased considerably due to the annealing at low T and was only 1% below the pre-rad value after 20 hours. At TID levels above 300Mrad, the gentle decrease of efficiency is instead traceable to a real degradation of the on-resistance of the power transistors. This is not expected to be subject to anneal (actually, because of the latent evolution of the interface states negatively affecting carriers mobility in the channel, annealing might even induce a further decrease of efficiency).

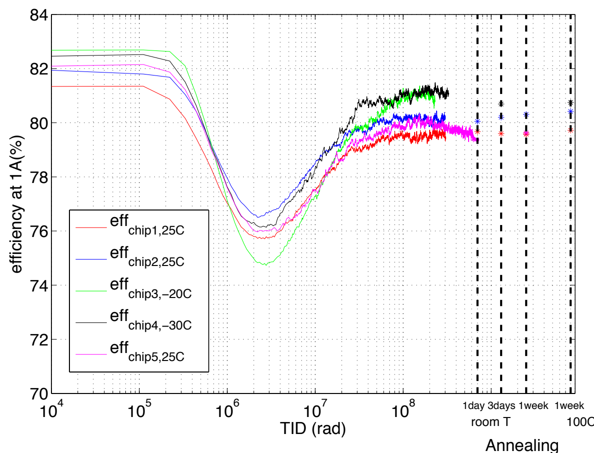

Figure 1: Efficiency evolution with TID for different FEAST2 samples at either 25 or -30ºC and for 1A load current. The drop up to about 2Mrad is due to leakage current independent on the load current: this drop is hence much reduced at larger loads.

Regulation properties like line and load regulation have been measured: line regulation is practically unaffected by even the highest TID levels, while load regulation tend to worsen slightly above some 300Mrad.

The bandgap reference voltage generator integrated in FEAST2 has very good TID performance, and as a consequence the variation of the regulated output voltage with TID is limited to below some 50mV after 200Mrad when regulating 2.5V, which represent a variation of about 2%. The sample irradiated to 720Mrad showed a further decrease of about 3%, for a total shift of 5%. Annealing both at room temperature and 100ºC does not help bringing the output voltage back to its pre-rad value.

B. Displacement Damage

At the time of writing, samples of FEAST2 are being exposed to neutrons at the JSI reactor. However, results of irradiation of previous prototypes (such as FEAST) are available and are well representative of the displacement damage effects in the production-ready ASIC. There are two relevant effects from displacement damage, which end up being the real limiting factor in the overall radiation tolerance of the converter circuit for HEP applications.

The first and most dramatic effect happens in the on-chip linear regulators providing the 3.3V for the analogue and digital control circuitry, as well as to the drivers of the gate of the power transistors. These regulators make use of p-channel LDMOS transistors rated at 80V in V_{ds}, and these transistors are very sensitive to displacement damage. Their current-voltage characteristics are degraded considerably already at an integrated flux of $1x10^{14}$ n/cm^2 (this and all successive fluences are expressed as 1-MeV neutron equivalent). Above $5x10^{14}$ n/cm^2 their current capability is so small that the regulators fail providing the 3.3V voltage to the power rails, and the full converter stops working. Failure happens between 5 and $7x10^{14}$ n/cm^2 since samples are functional at the first and failing at the second fluence.

The second effect is a sensible increase of the reference voltage from the bandgap voltage generator. This shift can be as large as 10% at $5x10^{14}$ n/cm^2, with a proportional increase of the regulated output voltage, and can be traced to the diodes used as basic elements to generate the reference voltage. A precise relationship between neutron fluence and reference voltage, with particular attention to levels below $3x10^{14}$ n/cm^2, will be obtained from the measurements of the FEAST2 samples currently irradiated at JSI.

C. Single Event Effects

Reaching the required level of tolerance to Single Event Effects was not simple. The first and foremost requirement for the circuit is the absence of destructive events. If latch-up can be avoided with the used HBD approach, where guardrings are systematically used to separate all wells, other destructive events can threaten high voltage technologies – the most notable of which for 12V-compliant devices being Single Event Burnout (SEB). While this destructive event was known to affect transistors and diodes rated above some 100V, recent work has shown that some LDMOS transistors can be sensitive to SEB at applied V_{ds} below 10V [7]. In our work, one of the candidate technologies for the development was discarded only because n-channel LDMOS transistor were found to be prone to SEB at even 8V when irradiated with Heavy Ions of LET below 10MeVcm^{2}mg^{-1} – and with a very large cross-section. Both n-and p-channel LDMOS in the chosen 0.35um technology were instead measured insensitive to this event in dedicated tests run up to an LET of 32MeVcm^{2}mg^{-1} (at normal incidence).

Heavy Ion irradiation of different prototypes of the converter ASIC confirmed the absence of destructive events – even at 60 degrees tilted irradiations for an equivalent LET of 64MeVcm^{2}mg^{-1}. However, different mechanisms for

sensitivity to SET (transients) were found where the circuit would go into a hard-wired reset procedure. In some cases, the circuit could also be stuck for tens of us in a state where the HS power transistor was constantly turned on, with an increase of the output voltage well above nominal. These mechanisms needed to be understood and their origin removed. A powerful tool in that respect was provided by pulsed laser tests at the Pulscan facility in Gradignan (France). Sample ASICs were scanned with the a narrow (1um in diameter) pulsed laser beam, the laser impinging from the back of the silicon die to avoid the shading from the 5 layers of metallization used in the circuit. At the same time, the output voltage and other critical signals were monitored for any sign of sensitivity. In this way, and by changing the laser power, it was possible to map the sensitive points in the full control circuitry and also have a relative indication of their sensitivity. This study was done on the FEAST prototype and guided the design of the revised FEAST2 version of the converter.

Irradiation of FEAST2 with heavy ions confirmed that the SEE tolerance goal has been reached. Exposed to a total integrated flux of 126×10^6 ions of increasing LET at different angles, up to an equivalent LET of $64 MeVcm^2mg^{-1}$, the ASIC constantly provided 2.5V (or 1.2V) to an external 1A load: no destructive event or reset (or other large transient at the output) was ever observed. SETs do in fact appear at the output of the converter, but with small amplitude and short duration. These will not affect the load in any application, however they have been carefully recorded by the measurement system. Fast comparators monitored the output voltage, their reference voltage being set above or below the nominal. Whenever the converter's output exceeded any of the pre-determined thresholds, the system recorded the event and measured its time duration. It was hence possible to measure the cross-section for SETs and catalogue them for their percentage amplitude with respect to the nominal (2%, 6%, 10% and 20% thresholds were used). This yield curves as the one shown in Figure 2 for negative SETs (below nominal). Negative SETs were more numerous and larger in value and time duration. It should be pointed out that the time duration of the events (time over threshold) gets shorter for larger amplitude: 2-4us for events with 2% thresholds, 1.5-2us for events with 6%, 1-1.5us for events with 10%. Only one event was recorded during the full test where the threshold was set at 20%, with the highest LET ion at normal incidence, and with duration of only 120ns. A typical SET at the output of the converter is shown in Figure 3.

The HI results above can be interpreted in view of using FEAST2 in the LHC detector systems. Since the LHC particle radiation environment relevant to SEEs is composed only by charged and neutral hadrons, only the HI results for LETs below $15 MeVcm^2mg^{-1}$ are relevant (this is the maximum LET from recoils in nuclear interactions of hadrons in silicon). Therefore, SETs will be limited to below 6% of the nominal voltage – only the 2% threshold was exceeded in the HI irradiation test below that LET.

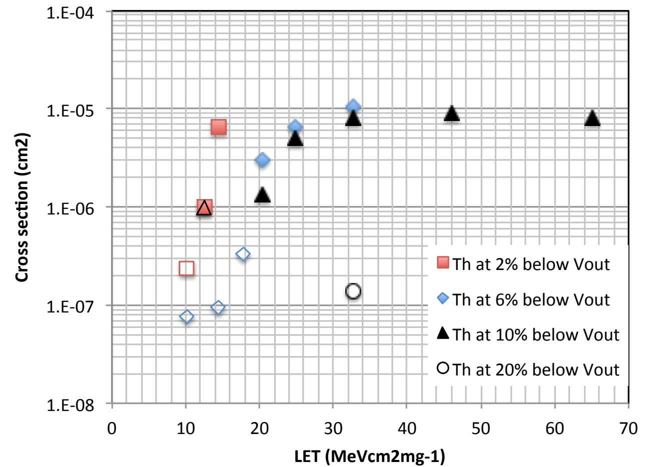

Figure 2: Measured cross-section for SETs at the output of the FEAST2 converter during Heavy Ion irradiation. In this case, the cross-section is for 'negative' glitches (below the nominal V_{out} of 2.5V). Empty points indicate 'limit' cross-sections where no errors were recorded (1 error is used to compute the limit value).

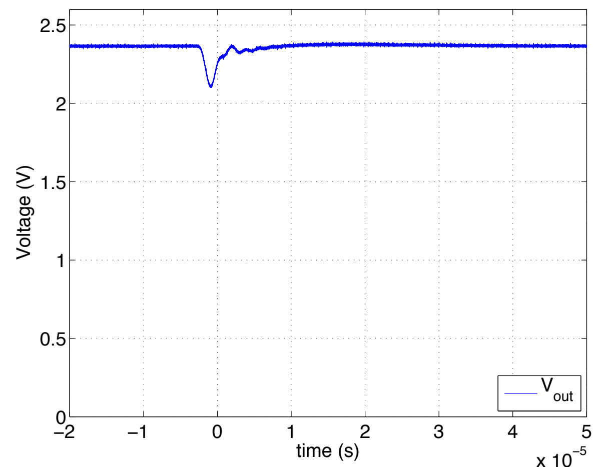

Figure 3: Typical SET at the output of the converter recorded by the oscilloscope constantly monitoring the V_{out} during the Heavy Ion irradiation test. In this case, the ion had an LET of $32 MeVcm^2mg^{-1}$ and was impinging on the ASIC at normal incidence.

IV. Conclusion

The CERN R&D project aimed at developing a radiation and magnetic field tolerant DC-DC converter for upgraded LHC detector systems has reached maturity, and CERN is moving to the production phase. FEAST2 is the production-grade ASIC that satisfies electrical and radiation tolerance specifications. Radiation qualification has been done for TID, DD and SEEs using different radiation sources. Functionality has been verified up to more than 700Mrad for TID, up to 5×10^{14} n/cm^2 for DD, and during HI irradiation up to an equivalent LET of $64 MeVcm^2mg^{-1}$. SET sensitivity with HI is limited to short (1-4us) and small (below 20% of the nominal in amplitude) glitches at the converter output. Packaged in plastic compact qfn32 packages, the ASIC is used in full DC-DC plug-in modules ready to be integrated in the electronic systems of the LHC detectors. These modules also use a

custom-developed toroid air-core inductor of 400nH that can operate in magnetic fields in excess of 40,000 Gauss. Thanks to an optimized module layout and choice of the passive components, these modules satisfy even the Class B requirements of the CISPR11 standard for EMC, and can hence be used in very close proximity to the sensitive particle detectors and readout electronics. CERN will very likely provide more than 20,000 such modules to the LHC experiments in the next few years.

V. REFERENCES

[1] F.Faccio *et al.*, "TID and Displacement Damage Effects in Vertical and Lateral Power MOSFETs for Integrated DC-DC Converters", IEEE Trans. Nucl. Science, Vol.57, No.4, August 2010, pp.1790-1797

[2] S.Michelis *et al.*, "Custom DC-DC converters for distributing power in SLHC trackers", proceedings of the Topical Workshop on Electroncis for Particle Physics, Naxos, Greece, 15-19 Sept.2008, pp.289-293

[3] C.Fuentes *et al.*, "Optimization of DC-DC Converters for Improved Electromagnetic Compatibility With High Energy Physics Front-End Electronics", IEEE Trans. Nucl. Science, Vol.58, No.4, August 2011, pp.2024-2031

[4] http://project-dcdc.web.cern.ch/project-DCDC

[5] G.Anelli *et al*., "Radiation Tolerant VLSI Circuits in Standard Deep Submicron CMOS Technologies for the LHC Experiments: Practical Design Aspects", IEEE Trans. Nucl. Science, Vol.46, No.6, December 1999, pp.1690-1696

[6] L.J. Palkuti, J.J. Lepage, "X-ray wafer probe for total dose testing", IEEE, Trans. Nucl. Sciences, Vol.29, No.6, December 1982, pp.1832-1837

[7] P.E.Dodd *et al*., "Development of a Radiation-Hardened Lateral Power MOSFET for POL Applications", IEEE Trans. Nucl. Science, Vol.56, No.6, December 2009, pp.3456-3462

A Mixed-Signal Radhard Microcontroller: the Digital Programmable Controller (DPC)

AMICSA 2014

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Abstract

Thales Alenia Space is engaged in the development of a radiation hardened mixed-mode circuit: the DPC (Digital Programmable Controller). This device is a major breakthrough in the availability of radiation hardened highly integrated european micro-controller. This component uses the IMEC RHBD DARE on UMC 0.18µ library and analog IP designed full custom by ICsense. The effective performance characterization of the DPC is currently evaluated in Thales Alenia Space laboratory.
The DPC is an essential building block for the development of intelligent RTU and other (power) distribution units in LEO and GEO satellites. Its large set of communication interface makes it usable in a broad range of applications such as scientific payload control, motors, actuators, battery management, power management … wherever a decentralized control makes the overall solution more efficient.
The presentation covers the key features of the DPC that have been made possible thanks to some extensions of the DARE library such as DPRAM, IO and clock gating. The analog functions such as ADC, DAC, PLL & bandgap have been designed such as to minimize the amount of external components needed around DPC (target being a system on chip). The E2prom containing the hardware configuration bitstream and the firmware remains, for this first generation, still an external device. Extreme care was taken to SET hardening of the critical analog functions: ICsense having developed automated and systematic charge injection verifications. Prevalidation activities and first tests results will be presented.

I. DPC Overview

A. *Development strategy*

The construction of the DPC is the result of a 4 party project involving IMEC, ICsense and Thales Alenia Space under an ESA development.
IMEC not only has provided the RHBD DARE on UMC 0.18µ library, but also extended it with additional features. Dual port memories are being used to transparently perform memory scrubbing in a seamless manner for the processing unit. The DPC embeds 95Kbytes of memory split over several banks. Clock gating cells have been also added. As the DPC embeds a large range of features, power consumption may become an issue if all of them would be active simultaneously. At boot time, a hardware configuration is loaded in the circuit to only deliver clock toward functions relevant to the target application.
IMEC also performed top level layout integrating digital netlist and analog macros, performing DRC to check for compliance to particular radiation hardening rules and finally the interface with UMC foundry.
ICsense has designed a large set of analog IP blocks which are included on chip. Concerning analog IO offered to the user, there are 4 analog to digital converters 13bits-1MSps with input multiplexing functions. There are also 3 current steering DAC each 12bits-50kSps / 8 bits-1MSps. As supporting function the DPC also includes an on-chip 100kHz RC oscillator for applications that do not require high precision frequency reference. This frequency reference is internally multiplied with a PLL delivering the internal master clock of the circuit. All these function are obviously supported by an on-chip bandgap. A set of internal low-drop voltage regulators converts the incoming 3.3V into +1.8Vdc to supply the digital core and to deliver "noise-less" supply to critical analog functions. This extensive set of analog function makes DPC a standalone system-on-chip (exception being for now the external E2prom).
Besides classical RHBD rules such a guard rings (Latchup) & margins for Vt shifts (dose up to 100krad), ICsense has

developed a powerful set of extension on top of (Cadence/Mentor) simulation tools to perform systematic charge injection verifications on each nodes of the circuit. ICsense has completed the design, layout and verifications. The analog macros were delivered to IMEC for integration into the final chip layout.
Thales Alenia Space Belgium has developed the RTL code to glue up all IP: the 16bits OpenMSP430 processor, mil-1553b, UART, CAN interfaces, memories, multipliers...
Challenge for such a complex mix-mode design resides into the verification of interfaces between analog macros and digital functions. This problem was tackled by the exchange of verilog Wreal models simulating the behavior of analog functions to be used in digital simulations. In the other way, stubs of RTL code have been delivered to simulate analog functions and their interface with digital functions.
Foundry was UMC and packaging has taken place at HCM. Wafer probe and package testing used facilities of µTest. The component is now back into the labs and under tests.

B. FPGA emulation

On top of the classical simulation at RTL, the DPC has been extensively validated on 2 FPGA platforms. The first one, named Core Validation BreadBoard CVBB, was used to validate all interaction modes foreseen in the DPC feature list. These are too complex (too long) to simulate, hence they have been executed on a clone of the RTL into a real hardware platform. This strategy allows to validate all the analog and digital interfaces and the digital functions a few months before tapeout.
The picture hereunder illustrates the FPGA emulator.

Figure 1: Core Validation BreadBoard

The second one, named DPC starter kit, was used to integrate the DPC with its software development environment. This was achieved; executable code for some typical applications was already running in real time in real environment prior to tape out. These two platforms raised the level of confidence in the overall solution: not only the RTL is most probably free of bugs, but also the component definition itself matches the user needs and firmware development tools.

C. Architecture and configuration

Figure 2 here below depicts the DPC internal architecture. Intentionally, the DPC embeds a very large set of functions. As compared to a µC from the industrial world this may be overkill. However, the economics of space components is very much different. Production volumes are very low as compared to consumer or industrial markets. Hence the silicon area account for a very small amount in the total cost breakdown of such a project. The circuit was therefore equipped with so many features, that it is nearly impossible to find a concrete application using all the available resources at once.

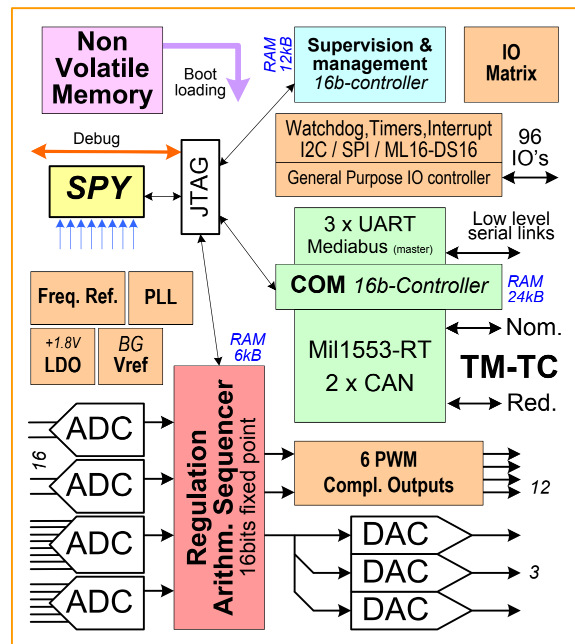

Figure 2: Block Diagram of the DPC

As a drawback, not only silicon area increases with the number of functions but also power consumption. Therefore, prior to firmware execution, the DPC enters a hardware configuration cycle. During this phase, a "hardware configuration" map is loaded from the non-volatile memory that defines which functions should be active (used for the application) and which functions will be made sleeping (clock gating and full sleep mode of analog blocks). Furthermore, operating frequency can be defined such as to match exactly speed performance and processing power needed for the target application. Using these mechanisms, the DPC power consumption can vary up to a factor 6, from minimalist low end use cases up to the unrealistic worse case where all functions are used at maximum operating frequency.

D. *Digital processing*

Processing is based on several instances of the OpenMSP430 fixed-point 16bits CPU core. This processor features the instruction set of the PDP11 (1970) from Digital Equipment Corp. The openMSP430 [**Error! Reference source not found.**] is a synthesizable 16bit microcontroller core written in Verilog. It can execute the code generated by any MSP430 tool-chain in a near cycle accurate way. To fasten the execution, the CPU is equipped with one hardware MACC function and one integer divide unit.

On one hand, digital control is offering new possibilities in driving smarter and more efficient systems. On the other hand connectivity is being more & more present in all applications. In order to avoid searching for complex & touchy compromises between robust loop control and communications or host functionality the architecture offers one CPU per task.

For communications to the outside world, the CPU has several hard wired units: 3 x UART, 2 x CAN bus and a mil-1553b remote terminal function.

Another CPU instance in the RAS is intended to execute a configurable & repetitive sequence of basic mathematical or logic instructions within a short cycle. This sequence can be programmed so that any mathematical expression typical of regulation scheme is realized: structures such as Proportional, Integral and Derivate (PID). This sequence can also be programmed to acquire and pre-process multiple sensors or pre-process signals before being generated to hardware signals.

Finally one CPU is available to perform all local (host) supervision & management functions.

The highly flexible hardware unit “USI” (Universal synchronous Serial Interface) is able to drive with quite various timing requirements the following communication protocols: SPI, I2C, ML16-DS16, serial in-parallel-out IO extenders.

II. DARE PLUS LIBRARY

The ESA activity “DarePlus – ASICS for Extreme Radiation Hardness & Harsh Environments” has as objective to provide a suitable and mixed-signal capable microelectronics technology platform. The existing DARE library elements in UMC 180nm were therefore improved and new elements added to increase the maturity to a level adequate for jovian missions.

Several of these DARE library enhancements were directly beneficial to the development of the DPC. Worth mentioning are the integrated clock gating cells, SET optimized inverters for clock trees, SET optimized combinatorial cells for set/reset trees and decoupling cells. Concerning the IO library extra drive strength cells were created, slew rate control was implemented to mitigate simultaneous-switching-output noise and all cells were made compatible with thick top metal processing. Finally, dedicated dual port SRAMs instances were implemented according to the specifications of the DPC during the development of the dual port compiler.

A lot of valuable feedback originating from DPC has been integrated into the DARE libraries as well. Examples are the SET optimization of digital input cells, the increased insensitivity to multi-bit upsets in the memory matrix of the SRAMs, the improved electro-migration tolerance in IO cells, the more elaborate manuals, etc...

The DPC ASIC uses a DARE library release that was generated with a more advanced characterization tool (ALTOS from Cadence) and a more accurate parasitic extraction flow (RC, previously only C). The timing and power data are also more accurate than before due to bigger look-up tables and better modeling of conditional arcs. With the previous characterization tool (ELC) not all timing arcs for all conditions of the inputs were present in the .lib. The correct timing and power analysis based on the new .lib files were compared with DPC silicon.

For design of the analog circuits in DPC a new ELT pcell symbol and layout was introduced to provide a means to check the inner and outer ELT diffusion connection correctly.

The "DARE analogue library" consists in the ADK (Analogue Design Kit) that forms an extention of the standard UMC PDK.

The existing radhard check was extended to cover the use of triple well nmos transistors and to report errors in more detail. The first implementation of a formal single event latch-up check was added to the radhard deck.

III. ANALOG BLOCKS

A. Overview

The DPC is a mixed-mode circuit that contains the following analog blocks:

- Reference voltage and current generation
- Power-management block with LDO's
- 120 MHz frequency reference system (PLL) to provide the clock to the digital part
- 100kHz reference oscillator
- 4 flexible 13 bit , 1MSps ADCs with extensive input muxing capabilities
- 3 12 bit, 3.75 MSps DAC current-mode outputs
- Power-on-reset circuit and under voltage detector
- Rail to rail comparators, PGA (0dB, 10dB, 20dB)

This paper only focuses on the test results of some of the analog blocks (PLL, ADC, bandgap). Some of these blocks have been explained in more details in [5; 6]. Radiation test data are not yet available, but the ICsense proprietary, automated SET hardening simulation environment has been employed to assess and decrease the SET sensitivity of the analog IP.

B. ADC

The DPC contains 4 ADCs that use a cyclic pipelined topology. The core of all ADCs is identical, but the amount of input muxing is different. Following functionality is foreseen for the ADCs and the input muxes:

- Up to 8 external analog single-ended inputs or 4 external differential inputs can be attached to a ADC core.
- An additional 8 internal analog inputs (or 4 differential) can be connected
- The channel selection and sampling times are fully controllable by the microcontroller.
- Sensing amplifiers are foreseen to enable measurements of very low differential voltages (currents in shunt).
- The on-chip temperature sensor can also be attached to one of the ADC cores.
- Offset calibration can be done by shorting the ADC inputs through the MUX.

The measurement results of the ADC show more than 11 ENOBs accuracy with an excellent THD of -74dB at 500 Hz. DNL is below 1 LSB and RMS noise is below 0.6 LSB. The ADC works with a single-ended input range of 0-2.5V and a differential range of +-1.25V. A plot is given below:

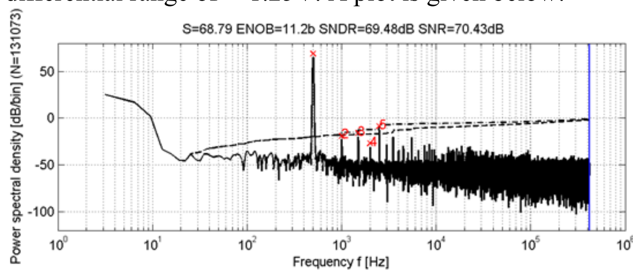

Figure 3: ADC performances

C. Reference Voltage

The reference voltage is generated by a bandgap circuit with an external decoupling capacitance. The bandgap uses a traditional topology without analog trimming. The SET sensitivity of the bandgap has been reduced by using large currents, additional buffer capacitances at sensitive nodes and a special startup circuit to ensure fast recovery after an SET event. The bandgap itself is made insensitive to SET and as a consequence an SET of 60 MeV/mg/cm^2 on the bandgap circuit itself never triggers a reboot of the bandgap and artifacts on reference voltage and currents are negligible.

D. PLL

For a reliable operation of the digital part, it is essential that the clock generation is without glitches (stable clock period and duty-cycle), even during SET events. 'Long-term' frequency spikes and phase shifts due to SET are minimized to not interrupt certain communication protocols. The complete PLL, including divider, loop filter and VCO is integrated on-chip. The measured output frequency of the PLL is 120MHz and the bandwidth 7kHz. The input frequency to the PLL is a 100kHz input source that is selectable between an off-chip reference oscillator or an integrated relaxation oscillator.

The integrated relaxation oscillator uses an external R and C to provide excellent stability and a small temperature drift. The relaxation oscillator uses triplicated comparators to achieve SET free operation. A special topology is used to achieve both low jitter and low temperature drifts; the latter is now dominated by the external components. First measurements show full functionality of this 100kHz oscillator.

The integrated 120MHz Voltage Controlled Oscillator (VCO) is based on a custom derivative of the Maneatis delay cell [1] with sufficient high current levels and capacitor values to ensure SET free operation.

E. DAC

The measurements of the DAC with output buffer show full 12 bit resolution with a DNL of less than 1 LSB and INL of less than 1.7 LSB for a data rate of 3.75MSps without dynamic element matching. When dynamic element matching is enables the data rate drops to 58kSps, but with a DNL of less than 0.7LSB and INL of less than 1.2LSB.

F. Top level mixed-signal verification methodology

To enable this first-time-right design of the DPC, a proven top-down bottom-up design strategy has been used. It consists of generating high-level models of each block to verify the functionality right from the start of the project.

The models use Verilog-AMS with wreal data types [4] for the analog parts. They can be simulated by a standard digital simulator in an event-based fashion. This leads to a very high simulation speed and therefore the possibility to check all analog-digital interfaces in the DPC and the functional operation of the most important use cases. The analog and mixed-mode simulations employ the same set of identical models, eliminating the risk of the analog and digital team having different representations of the same blocks. By

interchanging wreal models and actual circuits, good trade-offs between simulation accuracy, coverage and simulation speed can be obtained in complex mixed-mode designs.
The result of this state-of-the-art mixed-signal verification methodology allows to reach a functional ASIC from first silicon such that it can already be used in target applications.

G. *Rad hard analog Design methodology*

As an extension to its unique structured analog design environment [5], ICsense has deployed a rad hard analog simulation flow to enable rad-hard-by-design analog and mixed-signal IP blocks in the DPC. This flow is now used as the standard, qualified flow for rad-hard mixed-signal designs at ICsense and works as follows: the effect of an SET strike is simulated by injecting a double exponential current pulse on a certain node of the circuit [3]. The total inject charge corresponding to an LET of 60MeV.cm2/mg is 1.2pC. The design environment allows injecting this pulse in any circuit node at any wanted point in time, using the following flow:

- Inject an SET pulse in every circuit node under typical conditions. This produces a shortlist of sensitive nodes.
- Perform SET simulation for all these sensitive nodes over PVT (process, voltage, temperature) corners. An iterative procedure is carried out to devise countermeasures when specifications under radiation are not met.
- Final verification by injecting all nodes again in some of the worst-case corners for SET sensitivity.

For time generation circuits the timing of a SET strike is varied to find the most sensitive point in time in addition to the sensitive node detection.
To make the circuit robust for TID, a combination of various techniques are used:

- TID will result in Vth shifts of the devices, thus reducing the margins on the operating points of the transistors. The worst-case Vds-Vdssat across all PVT combination is monitored.
- The induced Vth shifts due to TID will depend on the bias conditions of the devices. Special care is taken to ensure identical operating points and biasings of all devices belonging to one matching structure under all operating modes.
- TID can generate leakage paths between N+ regions at different potentials. The DARE ADK provides an additional DRC rule check to flag N+ regions at different potentials that are not interrupted by P+ regions
- The analog blocks with highest matching sensitivities are put on 1.8V supply domain with thin-oxide devices to minimize TID sensitivity.
- For critical devices on the 3.3V domain, the enclosed layout transistors (ELT) from the DARE ADK are used.

IV. Conclusions

Thanks to an efficient cooperation with IMEC, ICsense and ESA, ThalesAleniaSpace Belgium has built an innovative highly integrated mixed signals controller (Figure 4).
First tests show that analog and digital blocks allows to reach a functional ASIC from first silicon such that it can already be used in target applications. Performance testing has just started. Next important steps are radiation tests to be perfomed in Louvain la Neuve in order to confirm preliminary results of test vehicles and RHBD techniques largely used in the DPC.
Its high level of configurability and its large set of communication interfaces allow the usage of the Digital Programmable Controller (DPC) in a broad range of applications such as scientific payload control, motors, actuators, battery management, power management … wherever a decentralized control makes the overall solution more efficient.

Figure 4: The DPC ASIC under test

V. References

[1] J. Carnes, I. Vytyaz, P. K. Hanumolu, K. Mayaram, and M. Un-Ku, “Design and analysis of noise tolerant ring oscillators using Maneatis delay cells,” in Proc. 14th IEEE Int. Conf. Electronics, Circuits and Systems (ICECS 2007), pp. 494–497.
[2] www.mathworks.com
[3] R. Garg and S. P. Khatri, “Analysis and Design of Resilient VLSI Circuits: Mitigating Soft Errors and Process Variations”, Springer, 2010.
[4] “Verilog-AMS Language Reference Manual”, Accellera
[5] G. Thys,S. Redant, E. Geukens, Y. Geerts, M. Fossion, M. Melotte, “ Radiation Hardened Mixed-signal IP with DARE technology” in Proc AMICSA 2012.
[6] Bram de Muer ICsense “Rad-hard, high-performance analog and high-voltage IP in 0.18um CMOS (DARE)” ESA IP-cores day Sept 2013

Scalable Sensor Data Processor: A New Mixed Signal Processor ASIC for Harsh Environments

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Abstract

Digital Signal Processors (DSPs) are key components for many data processing applications due to their high speed and low power consumption. This is also true for systems working in harsh environments such as those found in space and in some terrestrial application areas. Due to the specific requirements posed by these environments commercial components can be used only with severe restrictions, or not at all. For these cases specific components based on inherently reliable designs and processes must be used.

The Scalable Sensor Data Processor (SSDP) is a DSP component that meets the requirements of space applications and many specific terrestrial use cases. It is based on a well-tested prototype design and silicon-proven key architectural elements. Key specs include 1 GOps of processing power, up to 1 Mrad of Total Ionizing Dose (TID) tolerance, radiation hardened design, integrated mixed signal elements including ADCs, and low power consumption.

The development of this ASIC is ongoing and rad-hard prototypes are expected for end 2015, with flight models following 1 year later. The ASIC will be commercialized as a standard component.

I. Digital Signal Processing for Space Applications and other Harsh Environments

High Performance Digital Signal Processors are generally by far superior to General Purpose Processors in terms of power efficiency, performance for digital signal processing, and in real-time applications. In space applications, this makes them often the preferred type of processor for payload data processing units and similar subsystems. The only existing European space qualified DSP (TSC21020) is now completely outdated and at the end of its product lifecycle. Therefore, system and payload developers urgently need a reliable high performance replacement. In recent years, the European Space Agency has followed several technology routes for the development of new chips that can satisfy the user requirements.

The main properties that differentiate space qualified integrated circuits from typical commercial parts is the high reliability, radiation hardened design, and large operating temperature range. Therefore, ASICs developed for space applications are typically also compatible with the requirements of some terrestrial applications in harsh environments, such as those in R&D areas like particle physics or fusion research, and in nuclear industry (research facilities or nuclear power stations), or in specific application niches (high altitude platforms, borehole technology, etc.).

Due to the high cost of development and qualification or validation of space ASICs and the small production volumes the unit cost of space qualified ICs is typically orders of magnitude higher than that of similar commercial parts. However, the high reliability of these devices may still justify their use in some terrestrial applications where high reliability and / or high availability (minimized downtime) are key to success which may be the case in several of the aforementioned use cases.

The development of the SSDP ASIC therefore also considers terrestrial application cases where possible, and the authors appreciate feedback from potentially interested users.

II. Key SSDP Requirements

The main goal of the SSDP development is to satisfy the processing needs of typical space applications in particular in the areas of space exploration and earth observation. In addition to processing performance requirements, low mass and low power along with user friendliness as well as compliance to interface standards are considered essential [1]. The key SSDP requirements can be summarized as follows:

- Processing power > 1000 MOps
- Total Ionizing Dose (TID) tolerance >100krad (Si), with a goal of >300 krad (Si) … 1 Mrad (Si)
- Radiation hardened design (memories, registers, clock trees via EDACs / triplication etc.)
- Industry standard interfaces (SpaceWire, CAN, SPI, GPIO) and space standard peripherals (rad-hard frontend ASICs and detectors, SRAM, NVM, SRAM)
- High Quality Software Development Environment (SDE) and tools, DSP libraries
- High reliability, low power consumption, low mass
- Integration of analogue / mixed signal features, including ADCs and circuitry for housekeeping data acquisition from typical sensors
- No access restrictions for European users (ITAR free)

Based on these requirements, and on additional inputs from prototype testing / evaluation and future users, the final specification of the SSDP ASIC will be established.

III. SSDP HERITAGE

The development of the SSDP ASIC is based on several technology development activities that have been performed under ESA management in the recent past.

A. MPPB

The first one of those developments, the Massively Parallel Processor Breadboard (MPPB), demonstrated European fixed point DSP IP cores in combination with scalable Network-On-Chip (NoC) technology on FPGA based hardware [2]. It supports space typical features such as LEON2 general purpose processor (GPP) including the typical AMBA bus system and peripherals, SpaceWire (SpW) interfaces, ADC/DAC bridges, on-chip memories and other features. This system demonstrated the basic functionality of the individual elements and the scalability and significant bandwidth offered by the NoC. Data streams across the chip between DSP cores, on-chip memories, external memories, interfaces and external ADC/DAC were coordinated by the GPP by means of IRQs and DMAs, and the DSP core performance was demonstrated by means of relevant benchmarks [3].

Figure 1: FPGA based MPPB hardware (credits: RECORE)

On the software side, an SDE was developed and adapted that allows programming of the platform in C and assembly language. In addition to an API that supports efficient use of the architectural elements, an IEEE754 compatible floating point library was developed. The MPPB hardware was evaluated independently by external parties, and several improvements were implemented based on their feedback.

B. DARE+ Application ASIC

Following the successful design and development of the MPPB, a DSP prototype chip was developed in order to prove the key elements of MPPB in DARE180 [4] based silicon. This work, which was part of a larger activity (called DARE+, [5]) aimed at development and debugging of library elements for IMEC's DARE180 technology, was intended to pave the way towards future space DSPs based on the demonstrated technologies. The so-called DARE+ Application ASIC, which was implemented as a Multi-Project Wafer (MPW) based chip, included the following elements:

- Xentium® VLIW fixed point DSP with local instruction and data memories
- NoC routers
- Bridges to space qualified external ADC and DAC (STM RHF1401, ADI AD768)
- On-chip memory tile (also serving as DSP instruction memory)
- UART/GPIO programming interface
- SpW interface with RMAP target functionality

The basic architecture of the chip is illustrated in the following figure.

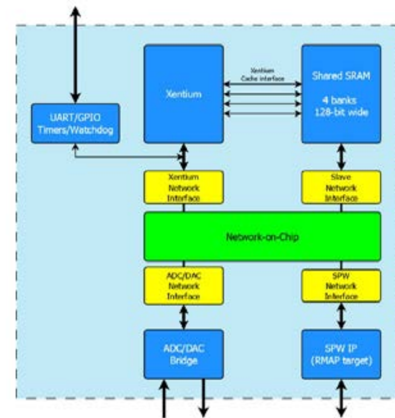

Figure 2: DARE+ Application ASIC architecture

The prototype chip has been fabricated successfully in DARE180, re-using a package that was developed for a previous activity. The chip was found to be functionally correct, with DSP core, interfaces, memories including EDAC protection, and other architectural elements working correctly also under exposure to radiation. The foreseen maximum clock speed of 100 MHz was however not reached due to excessive IRdrop (voltage drop across the on-chip power supply network) when performing DSP kernels with high memory access rates. This resulted at a reduced maximum clock speed of 50 MHz at slightly increased supply voltage. This problem, which is related to the limited chip/pad area available on the MPW-based prototype, will be analysed in detail and corrected as part of the SSDP prototype development. Figure 3 shows an image of the DARE+ Application ASIC die. The die used pads on only 3 of 4 sides due to MPW die size constraints.

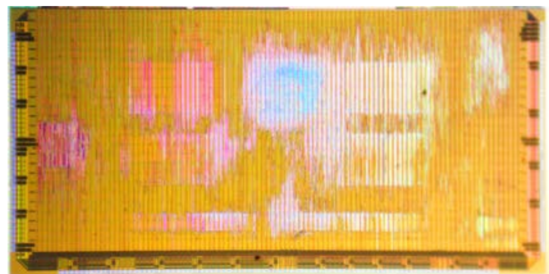

Figure 3: DARE+ Application ASIC die

A. *MPPB Evaluation by future SSDP Users*

Following the development of MPPB, independent external users with strong background in space data processing including Astrium (UK) [5] and RUAG (Austria) [6] have evaluated the platform with positive results, and have provided suggestions and requirements for future related chip designs and associated processor boards. These are taken into account for the final design of the SSDP ASIC.

IV. SSDP Baseline Architecture

The Scalable Sensor Data Processor (SSDP) is foreseen to replace the previous DSP (TSC21020), exceeding its performance significantly in particular for fixed point DSP applications, and become a key control, interface and DAQ ASIC especially for instrument designs. The baseline design features an architecture very similar to MPPB, providing a LEON General Purpose Processor (GPP), 2 VLIW Xentium® DSP cores, high-bandwidth NoC, and space typical interfaces (SpaceWire, ADC/DAC, CAN, SPI and others) for the digital part. Like the DARE+ prototype, the ASIC will be based on DARE180 technology which allows incorporation of analogue/mixed signal elements. It is expected that several mixed signal blocks will be integrated, such as a fast (up to 100 MSps) ADC for instrument data acquisition (15/16 bit), a second slow (ca 100 kSps) ADC with multiplexers for housekeeping data acquisition (12 bit), and others. Glue-less interfacing to external ADC/DAC, analogue frontend ASICs, next generation imagers and standard sensors will also be supported. The ASIC will run at a target clock speed of up to 100 MHz, providing in excess of 1 Giga-Ops for 16-bit data and 500 MOps for 32 bit fixed point data. The GPP will provide a floating point unit, and on-chip memories will be provided for fast data access in addition to external memories such as SDRAM, SRAM, and PROM. The ASIC will feature high radiation hardness (300krad min) and high reliability as well as low power consumption.

Figure 4: SSDP Baseline Architecture

The final chip architecture will be defined based on the requirements analysis and various trade-offs on memory architecture, adopted interfaces, on-chip memory sizes, package options and other key design factors. The core architecture of 1 LEON GPP with FPU plus 2 fixed point DSP cores will however be maintained.

V. Project Schedule

The development of the SSDP prototypes started in Q2 2014 with the kick-off of the corresponding contract with prime contractor TAS-E (Spain) [7] and key subcontractors IMEC (Belgium) providing the DARE180 technology and RECORE Systems b.v. (NL) as the key digital IP provider. Mixed signal IPs are provided by Arquimea Ingeniera S.L.U. (Spain), and ICsense N.V. (Belgium). The availability of SSDP prototypes and evaluation boards is expected in Q3/Q4 2015. An additional contract for the engineering model (EM) and flight model (FM) development and space qualification will be established in the second half of 2014, with availability of these chips expected in late 2016. The start of the commercialization phase for chips, SDE, and evaluation boards, along with customer support for these products, is expected for the same timeframe.

VI. Conclusions

Based on previous successful technology developments, the development of a successor to the TSC21020 space DSP is now underway. Due to its high performance, high radiation hardness, integrated mixed signal elements and low power it is expected to be suitable for both space applications and specific terrestrial applications in harsh environments. Chips for terrestrial applications and prototyping as well as evaluation boards should be available before 2016. Qualified / validated components for space use are expected by 2017. The progress of the activity will be publicized via relevant ESA webpages and at events announced there [8].

VII. References

[1] R. Trautner, " Next Generation Processor for On-board Payload Data Processing Application – ESA Round Table Synthesis", TEC-EDP/2007.35/RT, 2007. The report is available via [9].

[2] "Massively Parallel Processor Breadboarding Study", ESA contract Nr. 21986, 2008-2012. Final presentation materials are available via [9].

[3] R. Trautner, "Next Generation Space Digital Signal Processor Software Benchmark" , TEC-EDP/2008.18/RT, 2008. The document is available via [9].

[4] S. Redant, et. al., "The Design Against Radiation Effects (DARE) Library", 5th RADECS Workshop. Madrid, Spain, 2004.

[5] "DARE plus – ASICs for Extreme Radiation Hardness and Harsh Environments", ESA contract Nr. 4000104087, 2011-2014/2015.

[6] "European Digital Signal processor Trade-off and Definition study", ESA contract Nr. 22645/09/LvH/NL, 2009 - 2012. Final presentation materials are available via [9].

[7] "Next generation Astronomy Payload Processor", ESA contract Nr. 4000107815/13/NL/EL/fk, 2013 – 2014.

[8] "Scalable Sensor Data Processor", ESA contract Nr. 4000109670/14/NL/HB, 2014 – 2016/2017.

[9] ESA On-board Data Processing Website, http://www.esa.int/TEC/OBDP/

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Applications for Radiation Hardened Analogue and Mixed-Signal ASICs: Data Converters

RCADA - 65nm 12b 3Gspc Rad Hard dual ADC dual DAC

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Abstract

The RCADA mixed signal chip is currently under development by Ramon Chips and Silantrix, combining the rad-hard RadSafe™ libraries and methodologies from Ramon Chips and Silantrix proprietary architecture for data converters.

The extreme wideband capabilities of RCADA require very high performance digital processing, as well as high bandwidth digital communication capabilities. The digital processing capability will be provided by RC64, Ramon Chips' many-core DSP processor, which is under development. The two devices will be integrated in a multi-chip module (MCM). The key capabilities of RC64 will be presented [1].

RCADA will be provided either as standalone device, or integrated with RC64 in a single MCM package, to form is a multi-purpose data converter that aims to support the majority of high performance applications in advanced space missions including telecommunication, SAR, beam forming, navigation and earth observation.

RCADA integrates two matched ADC cores, 1.5Gsps 12b each, which can be interleaved, forming a single 3.0Gbps 12b ADC. Similarly, it includes two DAC cores, which can be configured as either a dual 1.5Gbps 12b DAC or as a single 3.0Gbps DAC. It can also be configured as a single ADC and a single DAC, 1.5Gbps 12b each, operating simultaneously. Within the MCM, RCADA interfaces RC64 via 48 pairs of bi-directional LVDS buffers, operating at 750Mbps each. RCADA will be fabricated using 65nm CMOS technology. It will operate with 1.2V and 2.5V supplies. Target power consumption is less than 500mW. It will provide very high immunity to TID and to latchup and no sensitivity to single event effects.

I. INTRODUCTION

Data converters are needed for wide range of space applications. Some applications require high sampling rate, which typically consume high power, and some require high resolution. Since the space market is relatively small, data converters that provide solution for wide range of applications is highly desired.

Analog circuits, such as used in data converters, might demonstrate degradation of performance due to TID stress. The advanced silicon technologies, such as 65nm, are more prone to these effects due to the use of thin gate oxide and thin STI between devices. However, this advanced process is more sensitive to NBTI effect, which might degrade the performance after aging. Self calibration capability complements the mitigation of these effects by performing periodic correction of INL/DNL inaccuracies, extending the effective lifetime of the devices.

In typical RF systems, the high speed electronics is placed close to the antennas, and long transmission lines, carrying analog signals, which are sensitive to noises and interferences, connecting them to the data converters in the main system board. By converting the high speed analog signals to digital close to the antennas, and compressing the digital data by high performance digital processor, it is possible to transfer the digital data with limited number of traces, to long distance, without degradation of signal quality. Mixing the RC64 - high performance DSP, with high performance data converter will enable such application.

Current high speed data converters for space are processed with fairly obsolete process flows, and the high speed capabilities are achieved by using Bipolar or BiCMOS technologies, or by using high speed circuit techniques, such as CML. These techniques consume a significant amount of power. For improved INL/DNL performance it is necessary to use a large device, which increases the area, thus limit the bandwidth, and high current is necessary to compensate for that. The use of advanced process technology, such as 65nm CMOS, enables very fast digital processing and conventional digital design flow. Implementing the analog core with smaller devices, provide higher speed and reduced INL/DNL accuracy. However, complementary digital mechanism that corrects these inaccuracies in the analog circuits provides the optimum solution, and exceeding the traditional Figure Of Merit (FOM) rules for data converters.

The use of 65nm cell libraries, complemented by proprietary RadSafe™ Rad Hard By Design (RHBD) libraries, which provides very high immunity to all radiation effects, enables high speed, low power and high immunity to radiation effects.

Most of the data converters available today are using one type of converter, DAC or ADC, and uni-directional data flow. The integration of ADC and DAC in the same die enables the self calibration, enables configuring the direction of the data flow between the data converter and the processor, thus providing unified solution for wide range of applications. In addition, it enables optimizing the cost of inventory to the system companies, and unified screening and qualification flow to the component vendor.

II. MICRO ARCHITECTURE OF RC64

The RC64 processor micro-architecture is described in Figure 1. It is currently at advanced design phase. It integrates 64 DSP cores, with can operate simultaneously, as controlled and scheduled by as S/W controlled scheduler. Each one of the cores can access to any of the 256 shared memory banks. When operating with clock frequency of 250MHz it can reach the peak performance of 16GIPS (???).

The RC64 can interface other systems by either 12 ports of 3.125Gbps SERDES, DDR2/3 I/F, configurable direction LVDS port, 2 SpaceWire ports and synchronous and asynchronous Flash I/F. In addition, it integrated JTAG I/F for testing.

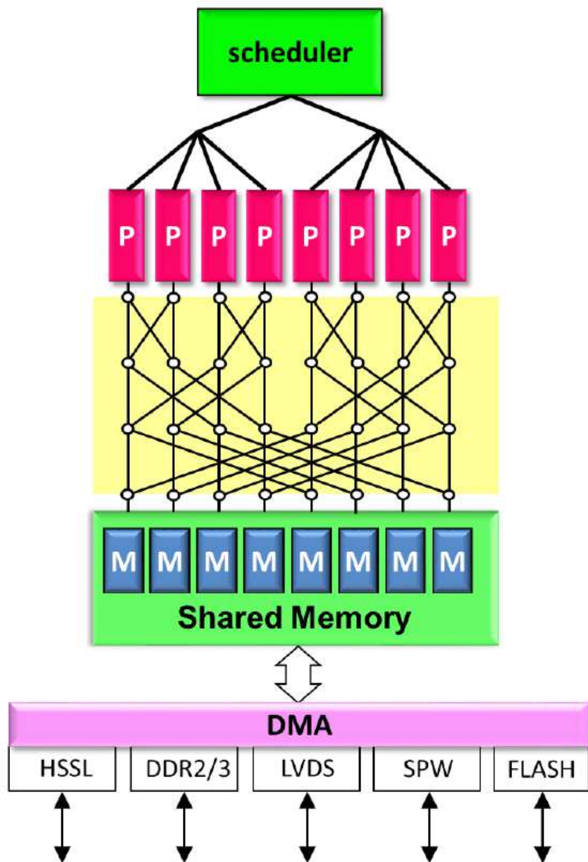

Figure 1: Micro-architecture of RC64 processor

III. MICRO ARCHITECTURE OF RCADA

The micro architecture of RCADA is described in Figure 2. 48 LVDS signal pairs, with configurable direction, will connect the RCADA to the processor, such as RC64. The data rate is 750Mbps/pair in DDR mode, or 375Mbps in SDR mode. The maximum transfer rate is 36Gbps, or 3Gsps with 12 bit resolution.

Two ADC cores, 1.5Gsps 12b each, are connected to external terminated pairs. Both are sharing the same voltage and timing references, and same resistor ladders, thus provide fully matched and synchronized digital outputs. Such matching is necessary, for example, when sampling the I and Q channels in RF communication. When shorting the inputs of both ADC pairs, and configuring the ADC to operate in interleaving mode, ADC0 will sample at clock rising edge, and ADC1 will sample at clock falling edge, doubling the data rate.

Similarly, the DAC can operate at either dual 1.5Gsps, or single 3Gsps when shorting the two DAC output pairs. It is possible to activate ADC0 and DAC1 simultaneously, thus enabling single ADC/single DAC operation, at 1.5Gsps each.

The key features of the ADC are:

- Muxing of parallel data by 1X/2X/4X @interleave mode
- Maximum data rate – 3Gsps
- Maximum data rate on LVDS outputs - 750Mbps/pair
- Resolution - 12 bit; ENOB - >10 bit
- Power @3Gsps - <500mW

The key features of the DAC are:

- Muxing of parallel data by 1X/2X/4X @interleave mode
- Maximum data rate - 3Gsps
- Maximum data rate on LVDS inputs - 750Mbps/pair
- Resolution - 12 bit; ENOB - >10 bit
- Power @3Gsps - <500mW

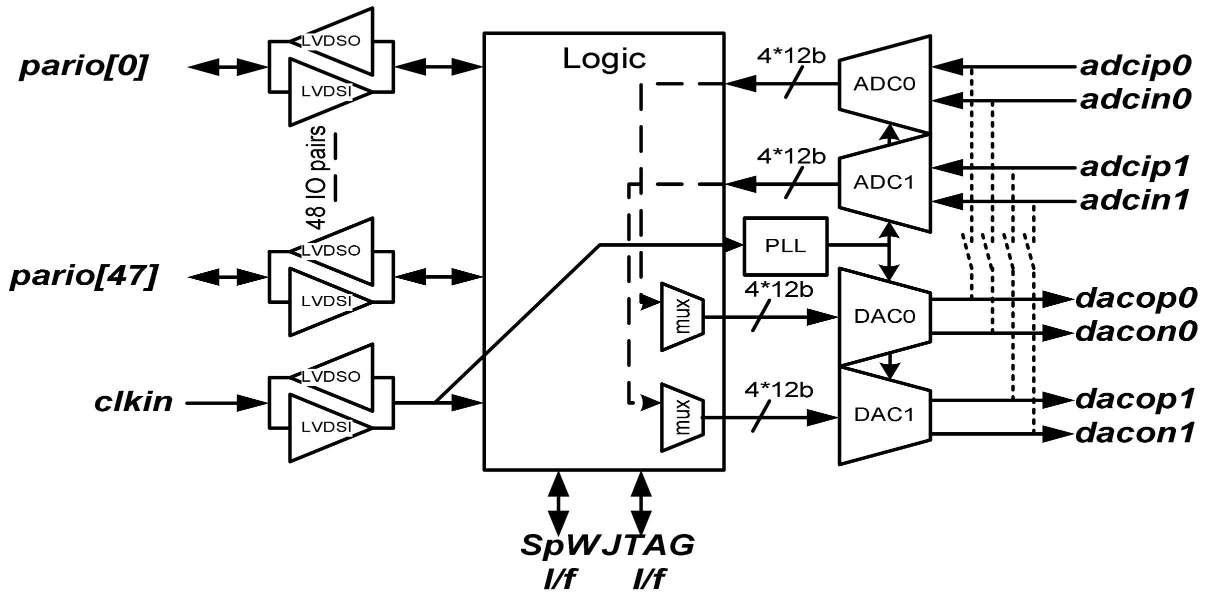

Figure 2: Micro-architecture of RCADA

The floor plan of the RCADA is presented in Figure 3.

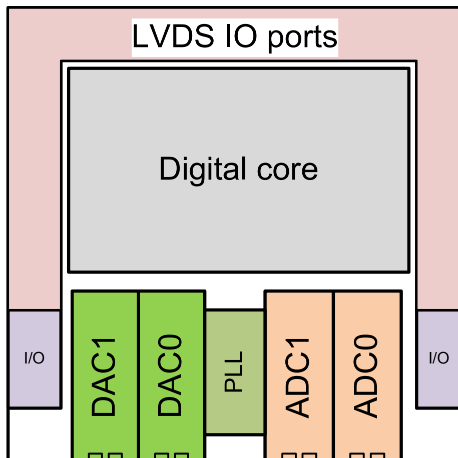

Figure 3: Floor plan of RCADA chip

The DAC0 and DAC1 are placed adjacent to each other to enable sharing the references for improved matching. Similarly, ADC0 and ADC1 are also adjacent to each other. The PLL is multiplying the clock reference to the desired sampling frequency. The frequency of the ADC and DAC is the same, to enable the periodic self calibration.

IV. Digital Model Inversion

The use of Digital Model Inversion (DMI), which is a proprietary technology by Silantrix Ltd., is mandatory for achieving the high performance data conversion process.

In conventional ADCs, the sampler is providing an accurate conversion of each analog sample to its digital equivalent. This requires very small variance of transistor's parameters, and also very low capacitance, which are conflicting requirements. With DMI, the sampler can be less accurate, compromising the performance for speed, power and area. The digital representation of the input analog signal can be calculated. There is no need to calibrate the sampler for inaccuracy of its devices, since it is done digitally. This characteristic can compensate not only for process variations, but also to stress related changes in device parameters, such as NBTI or TID. More specifically, the gains and offsets of the sampler are not modified in order to achieve digital representation of the sampled analog signals featuring better accuracy. There is still need for some calibration, but only for insuring those values are in their proper range.

The digital processor, which is part of the digital core, reconstructs the signal from the inaccurate analog sampler, providing accurate results. The reconstruction algorithm, which uses mostly adders, is design by conventional design flow. The use of 65nm process, with high speed rad-hard cell library, operating at 1.2V, provides the low power, high speed, noise insensitive, fully testable solution.

V. Competitive Analysis

The expected performance of the RCADA is compared to the existing available data converters available in the market. The highest performance ITAR free data converters for space available today are from E2V. The comparison table between the existing components and the expected performance of RCADA is presented in Table 1.

Table 1: Comparison between existing data converters and RCADA

	EV10AS180AGS	EV10AS180AGS	RCADA (target)
Function	ADC	DAC	2*ADC+2*DAC
# of bits	10	12	12 (each)
ENOB	8÷8.4	8.6÷9	>10
Sample rate	1.5Gbps	3Gbps	2*1.5Gbps /3Gbps (each)
Power	1.75W	1.3W	<0.5W

VI. Mitigation of radiation effects

The impact of TID on 1.2V devices of 65nm is expected to be very low. It is affecting mostly the digital logic. The analog circuits, which are powered mostly at 2.5V, are well guard ringed. In addition, the self calibration mechanism will compensate for variations caused by NBTI or TID.

SEL is not expected at 1.2V domains when using 65nm process technology and libraries with taps in each cell. In the 2.5V domains, the guard rings are expected to provide the required immunity.

SEU/SET in the logic parts are mitigated by using RadSafe™ library, which is well protected for these effects. The analog sampler of the ADC might be affected by SET. This effect will be partially mitigated by the digital processing. The fact that the data is temporary makes SEU related errors less critical. In communication channels, such errors are corrected and/or detected by using the error handling mechanisms embedded in the communication protocols.

VII. Summary

RCADA is a high performance rad-hard dual ADC and dual DAC device, with significantly higher performance than the existing available data converters.

It will be offered either as stand alone, or integrated with RC64 many-core DSP processor in a single MCM package. It will enable significant optimization of space systems, like SAR, beam forming and more.

VIII. References

[1] R. Ginosar et al, DASIA 2012, "RC64: A many-core high-performance digital signal processor for space applications"

[2] US20060222128 patent, Aug 2004, " Analog Signal Sampler Providing Digital Representation Thereof"

Very High Resolution Analog-to-Digital Converter at 1 kHz for Space Applications

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Abstract

We present a monolithic, very high resolution Analog-to-Digital Converter (ADC) suitable for high precision space applications. The converter is a low-noise, low sampling rate, radiation hardened device optimized to operate in a frequency range from 0.1 mHz to 1 kHz with nominal output sampling frequency of 6 kHz. System architecture is based on a 2nd order, discrete-time Sigma-Delta (ΣΔ) modulator with 1-bit quantizer and oversampling ratio (OSR) of 64 to 2048. The modulator employs Correlated Double Sampling (CDS) to defeat flicker noise (1/f) and to perform auto-zeroing function. Sampling rates of up to 96 kHz are possible thanks to the selectable OSR feature. The ASIC is implemented in a radiation tolerant 0.15μm CMOS process of Atmel, using a well established and rigorous mixed-signal design flow. An SFDR of 110 dB has been demonstrated with simulations.

I. Introduction

The commercial availability of high resolution hardened ADCs is rather limited. A market search for high-performance and high reliability converters reveals devices of up to 16 bit resolution, with the majority of the devices offering accuracy between 12 and 14 bits. The power consumption of the available devices is relatively high, and in many cases exceeds 100mW. On the other hand, modern space electronic platforms are becoming lighter, more compact and consume less power. As the scope of the planned space missions becomes ever more challenging, there is a constant need for low power, high-reliability and high-performance signal processing blocks. Apart from the high speed data converters operating at speeds of Msps to Gsps serving the telecommunication applications, there are certain on-board functions that demand low sampling rate and low noise signal processing. Such applications include instrumentation and measurement of slowly changing physical parameters, as well as the accurate monitoring of system parameters for the implementation of reliable spacecraft housekeeping functions. The provision of input for the calibration of current sources or other onboard voltage reference circuits, as well as the implementation of high accuracy control servo-loops, are among the application possibilities. Although the majority of modern microcontrollers feature embedded ADCs, these are low to medium resolution devices. The functions requiring high resolution necessitate the use of an external component.

Based on the aforementioned motivational aspects, we are targeting the very high resolution end of the space ADC market, by proposing an ADC design capable of offering an effective resolution of more than 16 bits over its entire operating bandwidth. Since the device is intended to support low frequency functions, the upper frequency limit of 1 kHz is considered more than adequate. The lower frequency limit is set to the remarkably low value of 0.1 mHz, aiming to serve as a dual specification for a complementary DAC, which was designed and developed under an ESA contract in the past [1], [2].

II. System Architecture

A. Overview

The very high resolution and low frequency operation of the ADC implies the use of a ΣΔ based oversampling architecture. Oversampling architectures with noise shaping of quantization error are suitable for low and medium speed applications when there is a trade off between accuracy and speed [3], [4], [5].

One fundamental characteristic of the ADC design is that the implementation of the ΣΔ modulator (SDM) is realized in the analog domain. In the literature, as well as in the market, we find that Switched Capacitors (SC) discrete time circuit implementations are preferred to Continuous Time (CT) ones due to a number of advantages. Firstly, the discrete time circuits offer the advantage of loop filter scalability with respect to the modulator sampling frequency. This feature allows the use of the same ADC across several applications requiring different sampling rates with minimum modifications (within a limited range). Secondly, the ability of implementing several sampling techniques has the advantage for reducing the typical non ideal effects of active and passive components and especially flicker (1/f) noise. Furthermore, they offer increased robustness in process variations and insensitivity to clock jitter.

In practice CT circuits are implemented as mixed topology architectures, having a first CT amplifier followed by SC amplifiers. The evaluation of mixed-mode CT/SC ΣΔ modulators was performed in [6]. Although they can significantly reduce the anti-aliasing requirements and also be designed for very low levels of thermal noise power, they are

very sensitive to clock transition uncertainties. For these reasons, SC architecture was chosen for the implementation of the SDM.

B. Block diagram

The system consists of a 2nd order, SDM, followed by a digital decimation filter. The latter, reduces the sampling frequency by a factor of the OSR, to the nominal output sampling frequency of 6 kHz. Note that the Nyquist frequency is three times the signal bandwidth by specification.

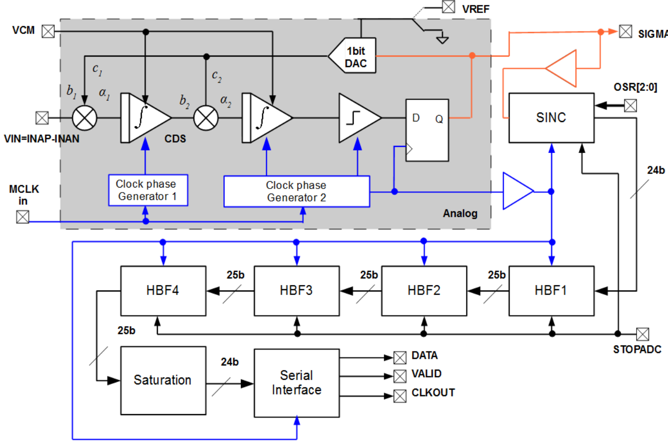

Figure 1: ADC block diagram

The analog voltage to be sampled is applied as a differential signal at the INAP, INAN inputs and is modulated in 1-bit ΣΔ modulation by the SDM block. The discrete-time SDM requires two reference voltages. VCM sets the output common mode voltage of the amplifiers implementing the integrators to obtain a balanced swing and maximize their dynamic range. The 1-bit DAC uses VREF to generate the feedback signals for the integrators.

Two embedded clock generators generate all the required phases for the modulator using an externally provided clock, while the output D Flip-Flop latches the result of the dynamic comparator and drives the ΣΔ modulated signal to the digital part along with the clock. The on-chip decimator can be bypassed using the SIGMA output with different, off-chip filters implemented inside an FPGA or DSP processor for example. This might be useful for mating the modulator with differently tuned filters better suited to the needs of a particular application. The decimator is implemented as a 4th order SINC filter offering selectable oversampling ratios in the range of 64 to 2048, followed by 4 Half-Band Filters (HBF). Each digitized sample is transmitted in 24 bit words over a simple serial output interface along with the clock. The operation of the decimator can be suspended through the STOPADC input to save power, if needed.

III. ASIC DESCRIPTION

A. ΣΔ modulator

The modulator is a single-stage, 2nd order topology with 1-bit quantizer (Figure 2). It follows the model introduced in [3], and consists of two delayed integrators, each within a gain of 0.5, followed by a comparator acting as a two level quantizer.

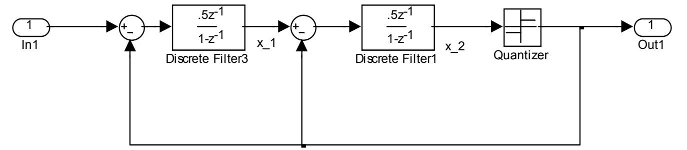

Figure 2: Modulator loop block diagram

The low output sampling frequency of 6 kHz allows the use of an OSR as high as 2048, since it leads to a modulator sampling frequency of 12.288 MHz which is acceptable. Such an OSR with the modulator of Figure 2 was shown to achieve 141 dB of SQNR with regards to quantization noise, with Noise Transfer Function (NTF) given by Eq. 1 and graphically represented in Figure 3.

$$NTF(z) = \left(1 - z^{-1}\right)^2 \quad (1)$$

Note that the formula predicting the SQNR assuming a linear noise model is 154 dB. The toolbox of Schreier [7], however, takes into account the nonlinear nature of the quantizer and results in a realistic prediction of the SNR.

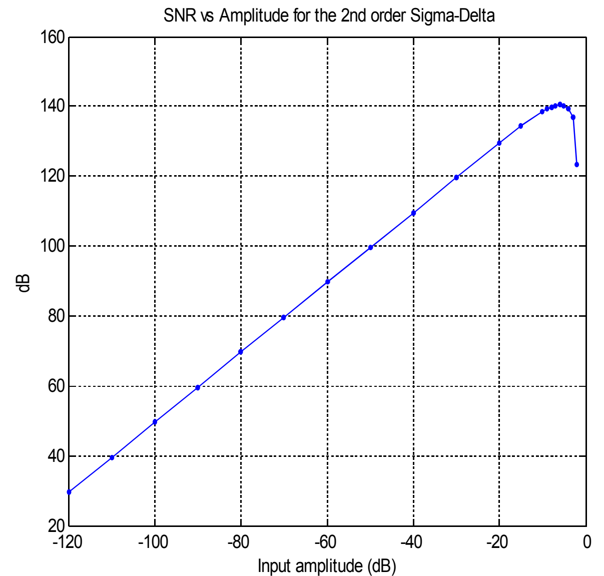

Figure 3: SNR vs. amplitude for a 2nd order modulator based on the describing function approach

Note that the magnitude of the gain of the second integrator is irrelevant as it is followed by a 1-bit quantizer whose output only depends on the sign of the integrator output. The same behaviour would have been obtained by a gain of 2, which leads to an NTF = $(1\text{-}z^{-1})^2$. The effective gain of the quantizer is actually amplitude dependent. This fact is taken into account by the result of Figure 3.

Stability can be guaranteed for second order modulators, while tonal behaviour is not expected to be a problem for this high an OSR.

The ΣΔ output signal is fed back to both integrators using a 1-bit DAC. The feedback and feed-forward scaling coefficients α_i, b_i, c_i depicted in Figure 1 are implemented as inter-stage capacitance ratios. The applied values are shown in Table 1, where Cs_x, Ci_x and Cf_x correspond to the sampling, the integrating and feedback capacitances of each SC integrator, and $x \in \{1,2\}$ denoting the first and second integrator respectively. The values are normalized to the feedback gains c_1, c_2.

Table 1: SDM coefficients

α_1	Cf_1/Ci_1	1/7
α_2	Cf_2/Ci_2	0.222
b_1	Cs_1/Cf_1	1
b_2	Cs_2/Cf_2	5/2
c_1	1	-1
c_2	1	-1

The schematic topology of the modulator is based on the circuit presented in [8]. That implementation uses a single voltage reference +Vref in contrast with most existing implementations utilizing a symmetrical ±Vref. This simplification, which benefits the component integration at system level, is done at the expense of additional switches to manage the ΣΔ feedback signal. The nominal Vref level equals the supply voltage and is provided externally. To avoid conversion errors, the voltage reference should not be allowed to drop more than ½ LSB. The maximum allowed output impedance corresponding to 18 bit resolution is 86 mΩ.

The implementation of the SC modulator requires two identical non-overlapping clock generators, one level quantizer and two fully differential Operational Transconductance Amplifiers (OTAs) for the realization of integrators. All the analog switches are implemented as passgates. The 1-bit feedback DAC is realized as combination of switches with respect to Vref. SC integrators and the OTA cell

The SC integrators are based on a fully differential stray insensitive topology for improved CMRR and dynamic range [9]. The simplified schematic is shown in Figure 4.

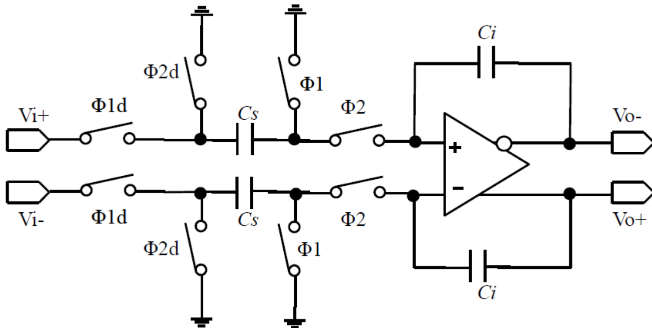

Figure 4: Differential switched capacitor integrator

Each SC integrator requires at least a two phase non-overlapping clock Φ1, Φ2 as shown in Figure 5. However, clock feedthrough from the switches can cause undesired offsets in the form of charge injection, which may distort the original sampled signal. Although the charge injected offset appears as a common mode signal at the amplifier inputs and is largely suppressed by the input differential stage, sensitivity to clock-feedthrough can be further reduced by using two additional clock phases as shown in Figure 5 [10]. The delay at the trailing edge of each clock pulse t_d aids in sinking the stray charge towards the input and ground, during the sampling and integrating phases respectively. The amount of delay was set to 3ns.

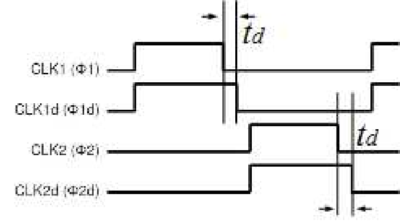

Figure 5: 4-phase clock

The amplifier of each integrator is implemented as a rail-to-rail two stage OTA (Figure 6). The first stage consists of a differential amplifier with current source active loads, followed by a common source stage. The necessary bias voltages are generated internally by a voltage bias network using a fixed current of 5μA generated by a current reference cell. To ensure proper operation of the amplifier a transistor based Common-Mode Feedback Circuit (CMFB) is added to the output to regulate the output common-mode voltage irrespective of the output voltage swing. The entire cell operates from a single 3.3V power supply and dissipates around 2mW. The RC network consisting of X1/X7 and X2/X0 attenuates the feedback signal at high frequencies to prevent oscillations and improve the stability.

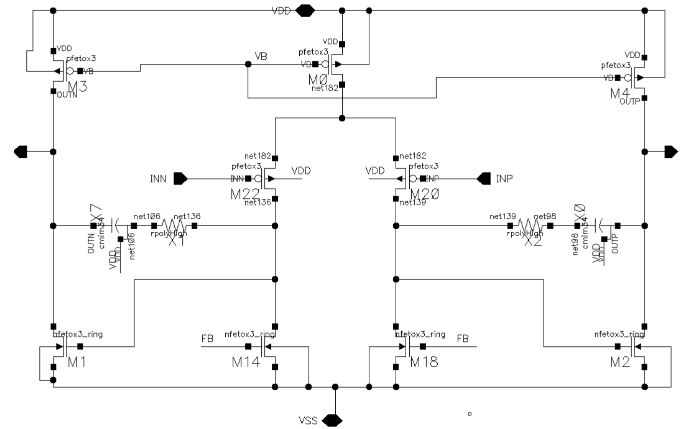

Figure 6: OTA schematic

Despite the relatively high GPBW of the amplifier, which measures 146 MHz and its output slew-rate reaching 225V/μs, the overall performance of the modulator is significantly degraded at switching frequencies higher than 7 MHz. Consequently, the circuit was optimized for operation at half the theoretical modulator frequency, which equals 6.144 MHz. This practically limits the maximum OSR at 1024, which in turn reduces the SNR from 141dB to 125dB.

B. Sampling capacitor

Apart from the non linear nature of the modulator, another limiting factor is the sampling capacitance value.

It can be shown that the minimum value of sampling capacitance which is required in order to achieve a certain SNR figure for a given OSR, is provided by Eq. 2 [4].

$$C_{\min} = \frac{8kT\, SNR^2}{V_{IN}^2\, OSR} \tag{2}$$

where, the SNR is in linear scale of value $10^{125/20}$, k is the Boltzmann constant 1.38 x 10^{-23} JK^{-1}, T the maximum temperature for full performance in K and V_{IN} the full scale input voltage for maximum SNR in V. The factor of 8 accounts for the two paths through which thermal noise is sampled during each phase (Φ1 and Φ2) and the fully differential topology of the circuit.

Thus in our case:

$$C_{\min} = \frac{8 \times 1.38 \times 10^{-23} \times (273+50) \times 10^{12.5}}{3.3^2 \times 1024} \tag{3}$$
$$= 10\,pF$$

This value of capacitance was proven to be large for the actual circuit, after the entire schematic was initially simulated. Due to that limitation, a capacitance of 0.7pF was eventually realized, which further limits the achievable SNR to 113dB.

C. Low frequency noise reduction

The reduction of flicker (1/f) noise is an important consideration, since the ADC is required to operate well below the sub-Hz region. Two effective techniques exist in the literature, which offer significant amplifier flicker noise reduction, the Chopper Stabilization Method (CHS) and the Correlated Double Sampling (CDS). Both techniques can be applied quite easily in SC circuits because of their inherent sampling process.

The CDS technique can be treated as a particular case of auto-zeroing (AZ), where the amplifier noise and offset are sampled twice in each clock period and stored in an extra capacitor [11]. The stored noise plus the offset are then subtracted from the input sample. The CDS technique can be readily applied to SC amplifiers to reduce amplifier's offset and noise as well as to lower the effect of the finite amplifier gain [11]. Due to the sensitivity of CHS to the switching signal shape as well as layout parasitics [12], CDS was the low frequency noise reduction technique selected for the ADC. In terms of implementation, CDS requires one additional switch and one capacitor per polarity in the first integrator only. The addition of CDS to the second stage is not necessary, since the noise and offset of the second amplifier are noise shaped by the modulation process, and their effect on the overall performance is considered as minimal.

D. 1-bit quantizer

The 1 bit quantizer is implemented as a regenerative latched comparator followed by a D flip-flop (Figure 7). The topology is based on the work performed in [13] and was selected because of its high-speed and high-sensitivity operation.

The block consists of two stages; the circuit consisting of M10, M6 and M9 comprise an amplifier, which amplifies the voltage difference between inputs INP and INM as $V_D=V_{INP}-V_{INM}$. The second stage consisting of M1-M4 forms a regenerative latch that compares V_D to the ground potential (0V). The two possible output states of the comparator depend on the magnitude of V_D with respect to the zero potential; if $V_D>0$ the output goes to VDD (logic high), and when $V_D<0$ the output goes to 0 (logic low).. Transistors M0, M7 and M8 operate as switches enabling the comparison process only when CLK is High. In fact, M7, M8 isolate the amplifier stage from the regeneration stage while M0 clears the previous latched state and initializes the output for a new comparison cycle. The comparator is biased from an external reference at the gate of M9, which sets the tail current of differential pair M10, M6 and consequently the gain of the amplifier stage. The achieved sensitivity is less than 10 μV.

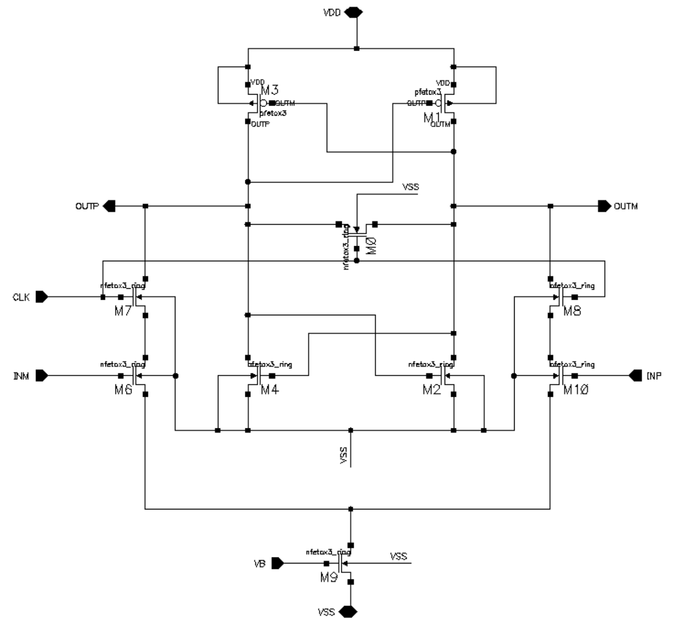

Figure 7: Comparator schematic

E. Clock phase generator

Since all of the switches are implemented as pass gates, complementary clock phases are also required. The embedded clock generator of Figure 8 generates eight non-overlapping clocks synchronized with the modulator clock. The circuit is instantiated twice (one per integrator stage). This is to obtain a symmetrical and simplified layout and to minimize the trace length, thus avoiding synchronization problems between the different stages.

F. Decimator Filter

The Decimator filter consists of two main sections: (i) the SINC decimation stage and (ii) the multiple Half-Band decimation stages. Since the nominal OSR is 2048 we had a factor of 128 implemented by a 4th order SINC followed by four stages of HBF realizing a factor of 16, so that 128 * 16 = 2048.

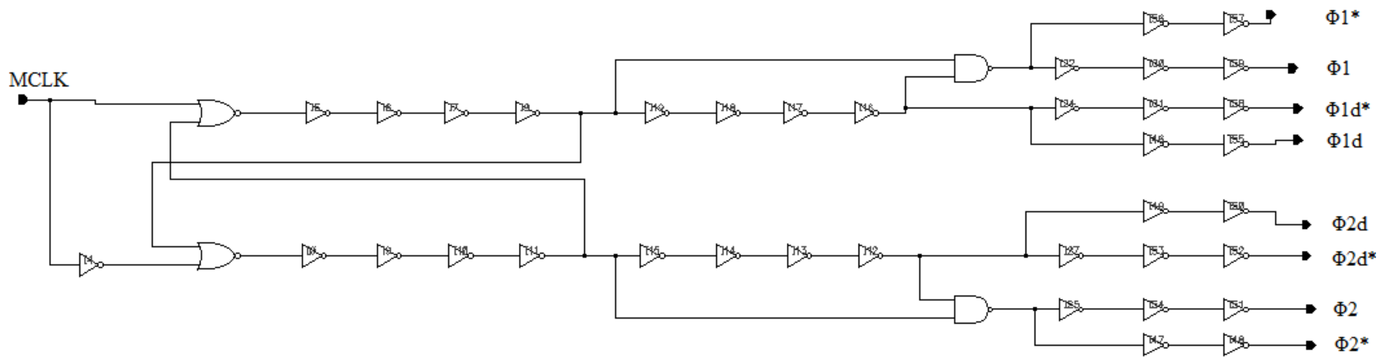

Figure 8: Clock phase generator schematic

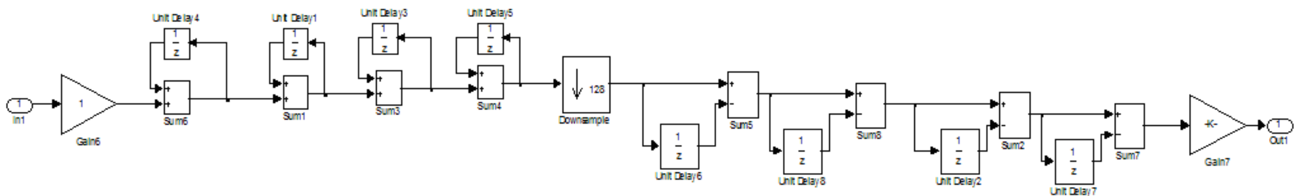

Figure 9: CIC SINC block diagram

1) SINC filter

The fourth order SINC is equivalent to a cascade of four rectangular moving average filters. A Cascaded Integrator-Comb (CIC) implementation is chosen as shown in Figure 9. The CIC implementation is very efficient both in terms of arithmetic computation and in terms of required memory elements. The input comes from the quantizer and it is a +1 or a -1 which may be described by two bits. Following is a cascade of four integrators/accumulators. Following the accumulators there is a decimator by 2^7=128 and following that is a cascade of four difference filters. All the arithmetic is implemented by 30 bit wide accumulators and differentiators. Any scaling is performed at the end of the chain. The accumulators do actually overflow, however the result is correct, provided the bit width is at least 30. The group delay of the SINC filter is 4x (128/2) = 256 taps of the input frequency or 1/8 sample at 6 kHz which is 0.02 ms.

2) Half Band Filters

Four half band filters (HBF) are used each realizing a decimation by a factor of two starting from a frequency of 16 * 6 kHz = 96 kHz. All filters have pass-band of 1 kHz and stop band of Nyquist frequency minus 1 kHz. These are equiripple filters that result in all even order coefficients being zero apart from the center one. These filters may be determined by their order and their pass-band frequency normalized by the Nyquist frequency at the input of their filter stage: $F_O = F_p / (F_s/2)$. The design parameters of each HBF are summarized in Table 2.

Table 2: HBF design parameters

Filter ID	Order	Normalized pass-band frequency (Fo)	Sampling frequency (kHz)
HBF1	6	1/48	96
HBF2	10	1/24	48
HBF3	14	1/12	24
HBF4	22	1/6	12

The group delay of the combined HBF is: 129 / 96 = 1.344 ms. The low-frequency end of the overall decimator magnitude frequency response is plotted in Figure 10.

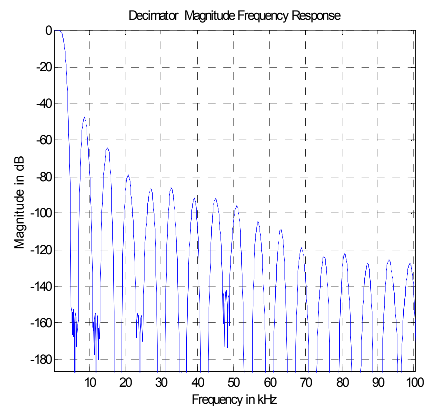

Figure 10: Magnitude response of decimation filter up to 100 kHz

All the frequency regions that will be aliased onto the pass-band (0 to 1 kHz) after decimation are suppressed to at least -140dB. These frequency regions are centred around integer multiples of the output sampling frequency of 6 kHz plus-minus the pass-band frequency F_p = 1 kHz. The in-between bands are not suppressed and are used as transition zones to help reduce the order of the filters.

Note that the first (lowest frequency) zero pair from SINC comes at 96 kHz. The SINC order is chosen so that from 95 to 97 kHz the response lies below -140 dB. The stop-bands at frequencies below 96 kHz are contributed by the HBF.

IV. RADIATION HARDENING

The ADC is implemented in a single-poly, 5-metal, 0.15µm CMOS on SOI radiation hardened process of Atmel. The digital part is synthesized using the robust cells from the library, including latches and flip-flops with increased area. Triple Modular Redundancy (TMR) is used for every flip-flop and finite state machine along with voting scheme, as a highly effective fault tolerance technique in masking Single Event Effects (SEE). As an added measure, the reset is synchronized with the clock.

The analog part is hardened using relaxed layout rules, guard rings and extensive use of enclosed layout NMOS transistors (ELT). ELT transistors can greatly improve the analog degradation due to TID effects, which can be caused by radiation induced charge trapping in the oxides or at the Si interface [14]. The layout is almost totally immune to Single Event Latch-up (SEL) thanks to the deep trench isolation option (DTI). Each CMOS structure is isolated using a deep trench extending down to the buried oxide of the SOI, as shown in Figure 11. This arrangement cuts away the parasitic SCR devices inherently present in the CMOS structure that may trigger SEL events. The target LET for SEL immunity is greater than 70 MeV/mg/cm^2. The target figure for TID tolerance is 100 krad (Si).

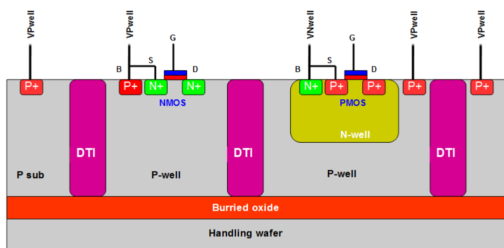

Figure 11: layout cross-section

V. SIMULATION RESULTS

Due to the small size of the analog core compared to the digital one, the chip layout is pad limited as shown in Figure 12. The total area including the core and the I/O pads measures 9.0mm^2. All the capacitors in the signal path are of MIM type.

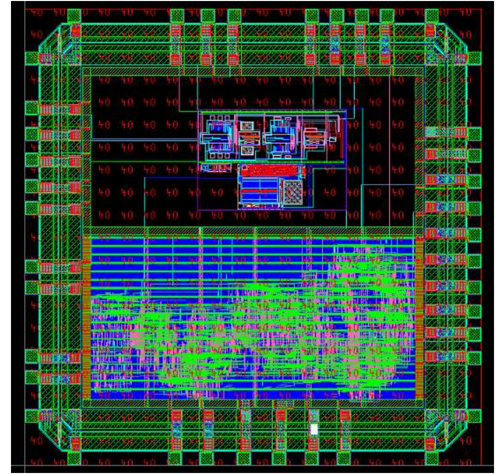

Figure 12: ADC chip floorplan

The dynamic performance of the SDM was evaluated by running post layout transient simulations in Spectre^{TM}, followed by FFT analysis. The block is driven with a 750Hz sine wave signal and amplitude 3.2Vpp differential. Then a transient simulation is run for two complete sine wave cycles and the ΣΔ modulated output is obtained at the time domain. Due to the very long simulation times, it is not practical to acquire more cycles. The frequency spectrum is then generated by performing post FFT analysis on the simulation data using Matlab^{TM}. Note that the ΣΔ signal is partially filtered before the FFT by passing it through the first stage of the decimator SINC.

The output spectrum of the ADC and the reconstructed output waveform at 25°C are shown in Figure 13 and Figure 14 respectively. The obtained performances of the ADC are summarized in Table 3.

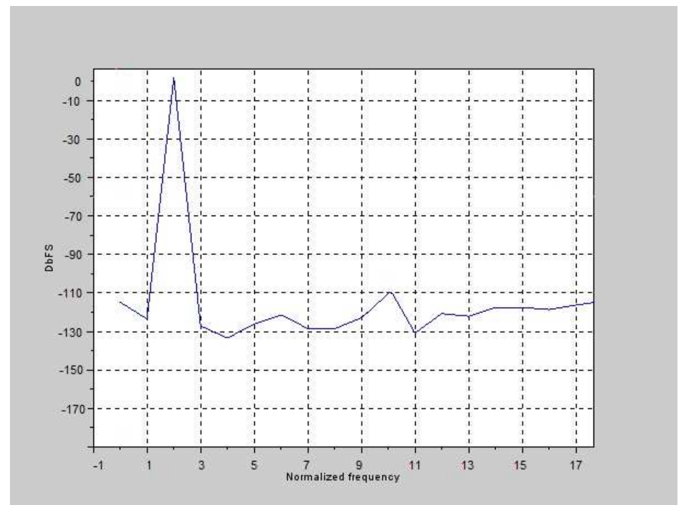

Figure 13: FFT sine 750Hz 0dBFS at 25°C

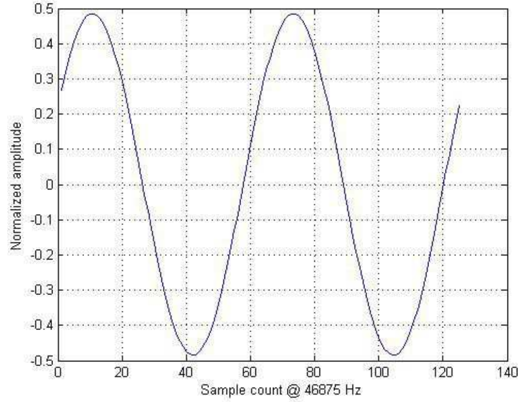

Figure 14: reconstructed signal at the output of the decimator

Table 3: ADC Performance Summary

Sampling Rate	6ksps to 96ksps
Rated bandwidth	0.1 mHz – 1 kHz
Practical bandwidth	DC to 16kHz
Clock frequency, nominal	6.144 MHz
Differential input swing	± 1.6Vpp
SFDR	110 dB
Digital power supply	1.8 V
Analog power supply	3.3 V
Power Consumption (modulator only)	2.2mA
Area (core & I/O)	9.0 mm^2

VI. CONCLUSION

A low speed, very high resolution, radiation hardened ADC was designed in CMOS. Simulation demonstrated a resolution of 18 bits while the analysis indicated the capability of the selected architecture to exceed 22 bits. The detailed design process reveals that the ΣΔ modulator is the most critical part of the design, yet the most challenging to optimize for low noise and high-speed operation. The chip validation in silicon will demonstrate how closely the theoretical performance limit could be reached by this ADC.

VII. REFERENCES

[1] D. Mitrovgenis, et al., "On the Design of a Very High Resolution DAC at 1kHz for Space Applications", *Proc. of the Second International Workshop on Analog and Mixed Signal Integrated Circuits for Space Applications (AMICSA)*, Cascais/Sintra, Portugal, pp. 47 – 54, Aug. – Sept. 2008.

[2] K. Makris, et al., "Validation Results of a Radiation Hardened 24–bit Digital-to-Analogue Converter", *Proc. of the Third International Workshop on Analogue and Mixed Signal Integrated Circuits for Space Applications (AMICSA)*, Noordwijk, The Netherlands, pp. 78 – 85, Sept. 2010.

[3] Norsworthy S.R., R. Schreier and G.C. Temes, "Delta-Sigma Data Converters: Theory Design, and Simulation," IEEE Press, 1997.

[4] Schreier R. and G.C. Temes, "Understanding Delta- Sigma Data Converters," IEEE Press & J.Wiley and Sons, 2004.

[5] Maloberti, F., "Data Coverters," Springer, 2007.

[6] V.F. Dias, G. Palmisano and F. Maloberti, "Noise in mixed continuous-time switched capacitor sigma-delta modulators", Proc. IEE, Part G, pp. 680-684, Dec. 1992.

[7] Schreier R., "Delta Sigma Toolbox," MATLAB Central, 2011, http://www.mathworks.gr/matlabcentral/fileexchange/19-delta-sigma-toolbox

[8] Nieminen T. and Halonen K., "A second-order low-power ΔΣ modulator for pressure sensor applications", NORCHIP, 2010.

[9] Razzavi B, "Design of Analog CMOS Integrated Circuits", Mc.Graw Hill, 2000.

[10] D.G. Haigh, B. Singh, "A switching scheme for switched capacitor filters which reduces the effect of parasitic capacitances associated with switch control terminals", *Proceedings of the ISCAS'83*, Vol.2, 1983.

[11] C.C.Enz, and G.C.Temes, "Circuit Techniques for Reducing the Effects of Op-Amp Imperfections: Autozeroing, Correlated Double Sampling, and Chopper Stabilization", *Proceedings of IEEE*, Vol. 84, No.11, Nov. 1996.

[12] Gildas Leger et al., "On Chopper Effects in Discrete-time ΣΔ Modulators", *IEEE Trans. on Circuits and Systems-I*, Vol.57, No.9, Sept. 2010.

[13] Aizad. N, "Design and Implementation of Comparator for Sigma-Delta Modulator", *Thesis, Linköping*, 2006.

[14] Faccio F., and Cervelli G., "Radiation-Induced Edge Effects in Deep Submicron CMOS Transistors", *IEEE Trans. on Nuclear Science*, Vol. 52, No.6, pp. 2413 – 2420, Dec. 2005.

ACKNOWLEDGMENT

The authors would like to thank Mr. Michel Porcher and Dr. François Braud of Atmel S.A.S for their continuous support. Also, Mr. Richard Jansen of ESA for his valuable comments and suggestions.

Development of a high-speed and high-resolution ADC for image processing applications

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Abstract

The abstract will present the ESA project for developing a high-speed and high-resolution ADC, performed by SPACE ASICS together with Kayser-Threde GmbH. The built-in analog front-end is discussed as well as the key performance requirements and functional requirements of such an ADC. Because verification of such an ADC is very challenging a previous test setup is shown and verification methods and algorithms are presented. Conclusions for testing of the ADC are drawn from the results and evaluation of the previously acquired data.

Additionally, the abstract will address potential ADC users and will request their feedback regarding the functional and performance requirements of the ADC.

I. INTRODUCTION

Today there is no space suitable solution in Europe for high-speed (e.g. 20 Msps) and high-resolution (16-bit) Analog-to-Digital Converters (ADC) to process and digitise analog output signals from image sensors or other high resolution instruments. Such devices would enable new applications with higher performance. In addition, it would guarantee European independence and reduce the dependence on COTS devices and their associated screening costs and time.

Therefore, ESA has initiated a program for developing such a high-speed and high-resolution ADC. In the framework of this program SPACE ASICS (Greek) will develop such an ADC together with Kayser-Threde GmbH (Germany) and others.

As the ADC application is targeted to image processing with CMOS and CCD sensors an analog front-end is also implemented in the ADC providing typical analog processing as used for readout of imaging sensors.

Verifying the characteristics of an ADC with such high dynamic performance can prove very challenging as the evaluation environment has to be designed such that it provides even better performance than the device-under-test (DUT). Eliminating any kind of noise caused by signal generators or external circuitry is a key aspect designing the test environment. Additionally, the choice of suitable measurement techniques and test conditions is important for an accurate determination of the performance characteristics and demanded test equipment.

II. REQUIREMENTS

Modern CMOS and CCD imaging applications call for high-speed ADCs with sampling rates of about 20 Msps. Currently, space qualified ADCs are only available with a sampling rate of about 4 Msps with appropriate resolution. This small sampling rate is a restriction for many applications, therefore, a high sampling rate of 20 MHz is required in the framework of this project. In addition, high precision data acquisition is also required for such type of application, which results in an ADC resolution of 16-bit. This high-speed and high-precision performance shall be reached with a quite low DC power consumption of about 100 mW, at a maximum sampling rate, which is very challenging because the process selection is limited to space suitable SiGe processes only. Table 1 lists the key performance requirements to be considered for the development of the ADC.

Table 1: Converter performance parameters

Parameter	Value
No. of bits	16
Max. sampling rate	20 Msps
Full scale input voltage (diff.)	max. 4 Vpp
INL (integral nonlinearity)	±5 LSB
DNL (differential nonlinearity)	±1 LSB
SNR (signal-to-noise ratio)	> 92 dB
ENOB (effective number of bits, SNR based)	15 Bit
Power consumption	<100 mW (@ 20 Msps and serial output)
Temperature range	-55 °C to 125 °C
Radiation tolerance	TID: 100 krad(Si) SEE: 70 MeV-cm^2/mg

It can be seen that also a very challenging noise requirement of signal-to-noise ratio (SNR) of 92 dB exists. This can be directly converted to an SNR-based effective-number-of-bits (ENOB) of 15 bits.

III. ARCHITECTURE

After an investigation and evaluation of typical imaging space applications on the basis of CCD or CMOS sensors, a preliminary block diagram of the ADC is consolidated in the

first phase of the activity. This preliminary block diagram is shown in Figure 1. A high degree of user configuration capability is considered for this design as well as appropriate testing capabilities, realized by analog in- and outputs or user configurable switches.

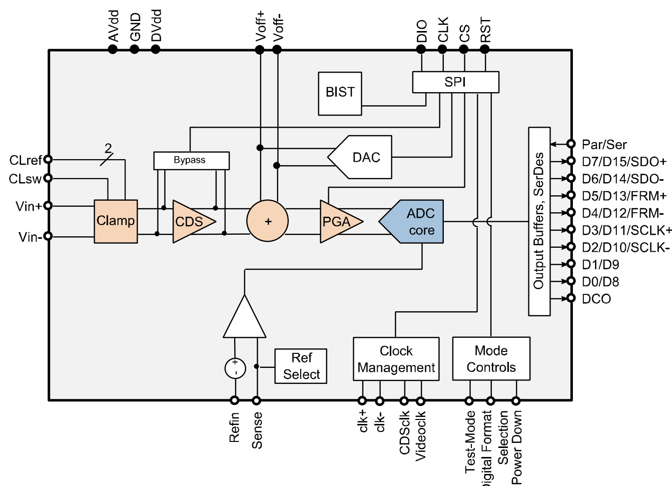

Figure 1: Simplified converter architecture

A. *Key features*

Besides the ADC core building block a complete analog front-end is integrated inside the chip for easy sensor readout without the need for additional and complex discrete electronics before the ADC chip. Some applications may require just a small line driver close to the sensor. The built-in analog front-end consists of .

- Analog adjustable and switchable clamping circuit
- Correlated double sampling with switchable bypass
- Offset correction, adjustable by analog input or by digital configuration interface
- Gain amplifier, programmable via digital configuration interface.

Besides the analog front-end functionalities the ADC will provide the following features in order to enable a user friendly configuration:

- Integrated and configurable clock management
- SPI configuration interface
- Digital output interface, switchable by hardware pin to 2x8 bit parallel output (CMOS) or serial LVDS output.

IV. TEST ENVIRONMENT

The measurement setup for the analog-to-digital converter, including the evaluation board and the test equipment, must offer high performance, so the specified parameters can be verified. The requirements for the test setup are derived in such a manner that these specifications are still measurable considering the measurement techniques based on the descriptions made in the IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters [1].

Figure 2 gives an overview of a general ADC measurement setup with sine-wave input signals. The evaluation board can be split into the following sub-circuits which are

- Analog front-end
- Clock distribution
- Power distribution
- Digital interface.

A close-up figure of the evaluation board is shown in Figure 3 corresponding to those parts.

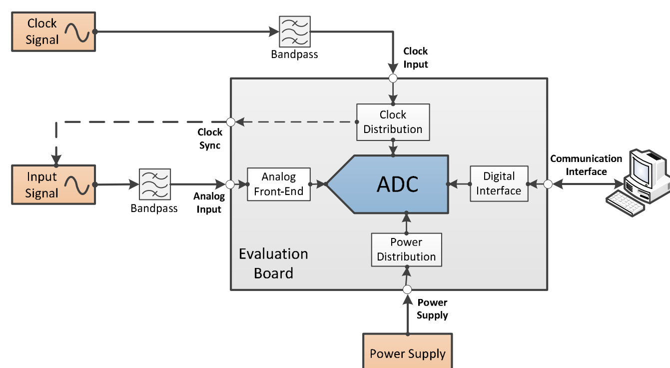

Figure 2: Block diagram of the test setup

Apart from the ASIC, the measurement setup includes the external power supply, a sine wave signal source followed by a bandpass filter which is used as the analog input signal and another sine wave source as clock input. The clock source is fed back to the input signal source as a reference signal to achieve phase synchronization between these instruments.

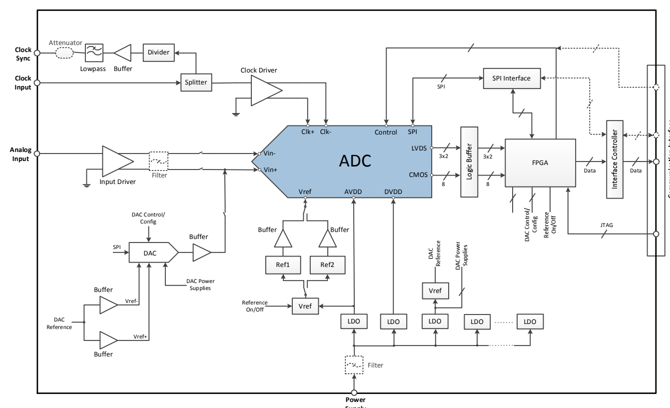

Figure 3: Detailed view of the test environment

A. *Static parameters testing*

The key static parameters include the integral nonlinearity (INL) and differential non-linearity (DNL) as well as the offset and gain error.

There are several methods available to test linearity of ADCs such as feedback loop, static code transition measurement or statistical approaches. Statistical analysis is simple and easy to apply so that it is one of the most typical test methodologies. The basic idea of this method is to count the number of times one of the 2N output value bins of the converter is hit. This number has to correlate to the input in a

certain way depending on the input signal form. The deviation from the ideal distribution of the output values is represented in the static parameters.

Accurate narrow-band test signals are generated with a high spectral purity. Consequently, the sine wave stimuli have gained increasing interest as the input signal to be used when estimates are needed of the converter non-linearities. Nevertheless, the setup is built in a way that we can use a high precision digital-to-analog-converter (DAC) to measure the monotony of the device-under-test (DUT) which makes it also possible to verify the static parameter using different approaches (for example feedback loop).

B. Dynamic parameters testing

The dynamic parameters include the total harmonic distortion (THD), spurious-free dynamic range (SFDR), signal-to-noise ratio (SNR), signal-to-noise-and-distortion (SINAD) and the effective number of bits (ENOB).

Few general test setups can be used testing the ADC parameters. Sine wave, arbitrary waveforms, and pulse signals are commonly used evaluating the mentioned parameters. The architecture of the proposed test environment is designed to allow testing with all mentioned stimuli sources.

V. ACKNOWLEDGMENT

This work was supported by the European Space Agency (ESA).

VI. REFERENCES

[1] IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters," IEEE Std 1241-2010 (Revision of IEEE Std 1241-2000) , vol., no., pp.1,139, Jan. 14 2011.

Methodologies for Radiation Hardening on Analogue Circuits at Cell Level, Circuit Level, and System Design Level

AFTU, an Analog Single Event Effects Automatic Analysis Tool

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Abstract

The Analog FTU Hardware Debugging System (AFTU) is an End-User Development (EDU) software tool for the analysis of Single Event Effects on microelectronic designs. AFTU takes user inputs as the design netlist, VLSI technology type, injection points and analysis heuristics classes to generate an expert software with two main functions: management of a simulation set through Spectre and a heuristic based inference engine to classify and analyze the simulation results.

The actual AFTU 1.0 simulates single event effects through current injection models. The simulation sets of results are organized by the inference engine and selected under heuristic based inferences, in order to present a Single Event Effects (SEE) vulnerability assessment to the microelectronics designer.

I. Introduction

With the scaling of CMOS technologies, microelectronic devices have increased their error sensitivity, demanding more attention for the design of radiation-hardened systems. In many applications, such as nuclear or spatial electronic systems, circuits can be exposed to high energy particles which can lead to Single Event Effects (SEE). In modern technologies, a well-known threat such as Single Event Transient (SET) errors generated from heavy-ion strikes is becoming even more influential nowadays [1]. Tools like TCAD [2] can extract exhaustive and accurate information of the effects on the proper design layout. However, dealing with the analysis of complex analog circuits is a challenging task, especially when the number of transistors increases leading to great computational costs.

In this sense, a systematic method of analysis for radiation tests in analog circuits by means of Spectre-based simulation tools was proposed [3]. Following previous experiences on digital technologies -like the European Space Agency (ESA) project FT-UNSHADES, [4]-, a fault injection simulation tool -AFTU- for SET analysis of analog and mixed-signal circuits is currently being developed by GIE (University of Seville) under ESA activities. This tool automatically modifies the circuit netlist, adding configurable current sources emulating the current injection produced by particle impacts. The ionization model applied in electrical simulation is a current source with double exponential dynamics, as illustrated in the next equation:

$$I_{rad} = \frac{Q_c}{\tau_d - \tau_r}\left(e^{-\frac{\tau}{\tau_d}} - e^{-\frac{\tau}{\tau_r}}\right) \qquad (1)$$

where τ_r is the rise time related to the plasma track dynamics, τ_d is the down time related to charge drift and diffusion in the transistor, and Qc is the net charge associated to the transient current through the transistor node. This is a well-known model widely described in literature [5] that can be implemented using a VerilogA model.

As a particular case of study, a D-latch with some combinational logic in a 130 nm CMOS technology of ST Microelectronics has been analyzed using AFTU to determine the critical charge required to generate a Single Event Upset (SEU) at its output.

II. Tool Description

The Analog FTU Hardware Debugging System is a tool to evaluate the SEE sensitivity of analog/mixed signal circuits at transistor level. To perform this task, the tool takes an Spectre netlist from the circuit under test and emulates radiation conditions by means of adding configurable sources. The user can define all the required parameters to perform a test campaign using some configuration files, and the tool will automatically apply the selected heuristics for SET sensitivity analysis and generate an output file with statistical results allowing a vulnerability study of the target circuit.

From a given netlist, extracted from a user transient test-bench, the tool will automatically create an instrumentalized netlist with incorporated SET injection models and an identically functional performance. Using this netlist as a starting point, it generates Ocean-based scripts to inject SETs to the circuits under test and extract the information from their performance. Using Cadence OCEAN Scripts, the ionizing particle impacts can be simulated in Spectre at every selected node and time chosen by the user. The generated scripts allow performing a set of parametric simulations dependent on the intensity of the particle impacts in one (or several) nodes at different times chosen by the user.

The tool allows several global parameters for simulation and analysis to be configured by the user:

- Devices where an impact on any transistor of the design should be emulated. The user is able to consider all possible devices or to focus the campaign in a specific part of the circuit.
- Total amount of charge injected for every selected node where an impact is emulated.
- Times in which the impacts are considered to be emulated. For a same node, different impact times allow the circuit evaluation in all possible working points.

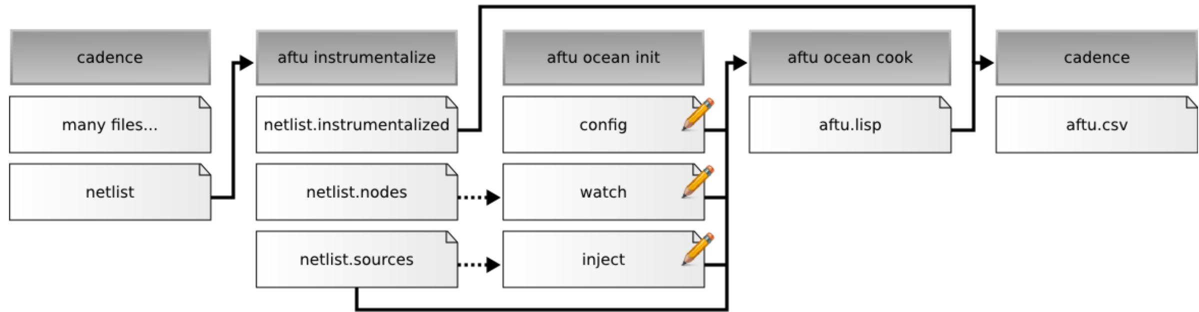

Figure 1: Analog FTU toolchain

- Circuit nodes in which the effects of a possible SET should be analyzed and reported. Differential signals and algebraic expressions can be considered in addition to single-ended outputs.
- Parameters related to the analysis of the signals, such as voltage thresholds, simulation time, simulation step, signals range definitions, etc.
- Information about the technology employed (dependent on the design kit used)

With this information, the response of the circuit under test with injected SETs is compared to a non-irradiated version of the considered outputs, determining the most relevant information to the user (designer of the circuit).

III. AFTU TOOLCHAIN

In Figure 1, the Analog FTU toolchain is presented, comprising a user interface, a full compiler from user input to code generator in SKILL language and an end analysis presentation file. The output code is the expert software, to be interpreted by Cadence OCEAN. The process simulation flow, commanded by the expert software, generates a set of simulations of the microelectronic design under several SEE situations, coded as injection models, in different design elements.

For a target circuit to be analyzed, the tool requires the netlist generated from a Spectre transient simulation as an input. This file can be taken from the original test bench used by the designer to test the circuit functionality. The tool will automatically generate (aftu-instrumentalize) an instrumented version of the netlist with added SET injection models that do not modify the circuit properties but allows to emulate radiation conditions, and two files with all the required information of available transistors where an impact can be emulated (*netlist.sources*) and observable nodes where the effects of injected SETs can be evaluated (*netlist.nodes*).

After this step, aftu-ocean-init generates three files (*config, inject, watch*) that can be used by the user as a template to define all the necessary parameters and criteria to define the test campaign. The information contained in *netlist.nodes* and *netlist.sources* files can be used as a feedback by the user to complete these files. *Config* file contains necessary information for analysis configuration: paths, times, applied heuristics, initial values, etc. *Watch* file allows the user to define all elements in the circuit to be observed during the simulation. *Inject* file allows to define where, when and how much charge can be injected (radiation emulation).

Once these files have been properly filled by the user, aftu-ocean-cook generates a script-based file (*aftu.lisp*) which includes all the paths and data required and implements the heuristics defining the way the simulation has to be performed and results analyzed. The user will take this file and run it in Cadence to emulate radiation conditions over the target circuit and will obtain a results file (*aftu.csv*) with all the statistical processed data, allowing a SET sensitivity evaluation of the circuit under test at transistor level.

IV. CASE STUDY

The target circuit is a D-latch cell with some combinational logic in a 130 nm CMOS technology of ST Microelectronics, as shown in Figure 2.

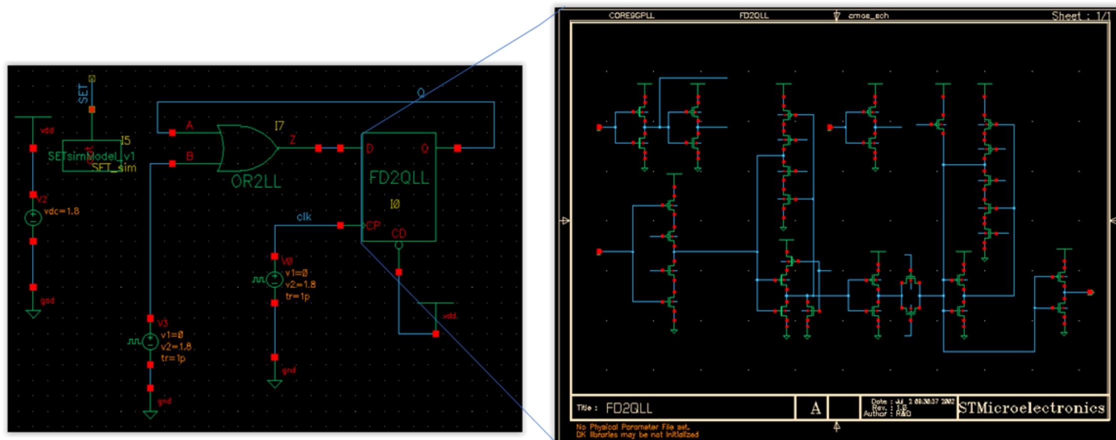

Figure 2: D-latch transient test bench and schematic view of the digital cell

Critical charge will be dependent on several factors such as the injected amount of charge, biasing point of transistors, emulated impact times, transistors affected, etc. Using AFTU, an analysis of different injected charges in every transistor in every possible impact time can be performed, as described in next paragraphs.

For the analysis of this circuit, all the required parameters will be properly configured in the *config* file, setting a 3 ns simulation (three signal periods) time with the appropriate analysis heuristic and including all the necessary paths and parameters for simulation. The applied heuristic is based on defining an error threshold for every observable signal to measure its maximum deviation (referred to the non-irradiated signal) as a consequence of emulated impacts and the recovery time in which its value can be greater than the user-defined threshold (Figure 3).

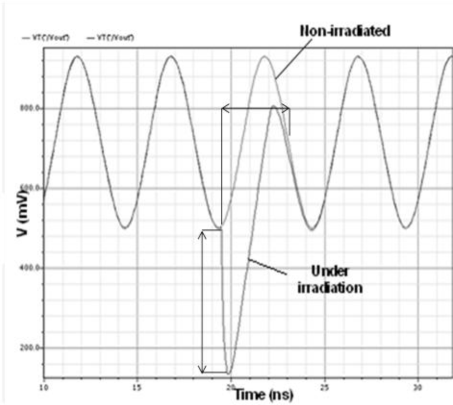

Figure 3: Applied heuristic description

The idea of the proposed analysis is to evaluate the response of the latch during three periods (3 ns): the first one is for signals initialization and settling, the second for injection of emulated SETs and the third for observation of the selected outputs. This test campaign will be defined by means of the *watch* and *inject* files.

On the one hand, we will select the observable signals to watch during the performed SET analysis in the *watch* file:

```
watch Q = /Q :
        threshold = 0.975 ;
```

Figure 4: Format of the *watch* file

where the name of the output (Q) is extracted from the correspondent *netlist.sourcelist* file. The threshold has been set to 0.975, as it is the value for high-low commutation in this latch. In this way, when the signal changes from high to low state (or vice versa) it will be detected and processed by the heuristics applied

On the other, hand, the *inject* file (Figure 5) is defined to select the different values of charge that will be injected in every selected transistor of the target circuit. The idea is to perform an injection for different values of charge in every transistor every 0.1 ns during one signal period. In this way, the SEE sensitivity can be evaluated by determining the required value of charge as a function of the impact time to generate a SEU at the output. With the analysis of these data given by the generated script, a SEU probability can be estimated with a 10% precision (as ten impacts per period are being emulated) for one signal period. As previously stated, information of the available sources for charge injection can be taken from the *netlist.sources* file generated using aftu-instrumentalize.

```
inject I0_MN20:
        Q = .025p, .05p, 0.1p, .2p, .5p, .75p, 1p, 1.5p;
        t = 1.0n : 1.9n : 0.1n;
inject I0_MP19:
        Q = .025p, .05p, 0.1p, .2p, .5p, .75p, 1p, 1.5p;
        t = 1.0n : 1.9n : 0.1n;
inject I0_MN19:
        Q = .025p, .05p, 0.1p, .2p, .5p, .75p, 1p, 1.5p;
        t = 1.0n : 1.9n : 0.1n;
inject I0_MP18:
        Q = .025p, .05p, 0.1p, .2p, .5p, .75p, 1p, 1.5p;
        t = 1.0n : 1.9n : 0.1n;
...
```

Figure 5: Format of the *inject* file

The script *aftu.lisp* is generated and after its execution in Cadence, a *results.csv* file is generated that allows obtaining the necessary information to evaluate the SEU sensitivity of the cell. A representative part of this results file is shown in Figure 6:

Output	ImpactNode	Qinj	Timp	Trec	Vmax
V_Q	I0_MN11	2.5e-14	1e-09	0.0000	0.006827
V_Q	I0_MN11	2.5e-14	1.9e-09	0.0000	0.016568
V_Q	I0_MN11	5e-14	1e-09	0.0000	0.017084
			. . .		
V_Q	I0_MN11	5e-14	1.3e-09	0.0000	0.005371
V_Q	I0_MN11	5e-14	1.4e-09	1.6100	1.806680
V_Q	I0_MN11	5e-14	1.5e-09	1.5000	1.806814
V_Q	I0_MN11	5e-14	1.6e-09	1.4000	1.805740
V_Q	I0_MN11	5e-14	1.7e-09	1.3000	1.802925
V_Q	I0_MN11	5e-14	1.8e-09	0.2400	1.404223
			. . .		

Figure 6: Format of the *results.csv* file

For the case a low level output is expected, it can be observed that there are several values of recovery time (T_{rec}) greater than 1 ns. This means there has been a change at the output which has been captured by the latch, generating a SEU at the output.

Considering the ten impact instants emulated for every transistor and different values of charge, a SEU probability can be estimated for the injection period. Taking the MN11 transistor as an example, for an injected charge of 0.05 pC there are generated SEUs for five impact times (from 1.4 to 1.8ns), leading to a 50% of SEU probability for this value of charge. Extending this evaluation to the rest of transistors of the circuit, it is possible to obtain a sensitivity map of the resulting SEUs under irradiation conditions for the target circuit analyzed using AFTU, as shown in Figure 7 for the considered case study.

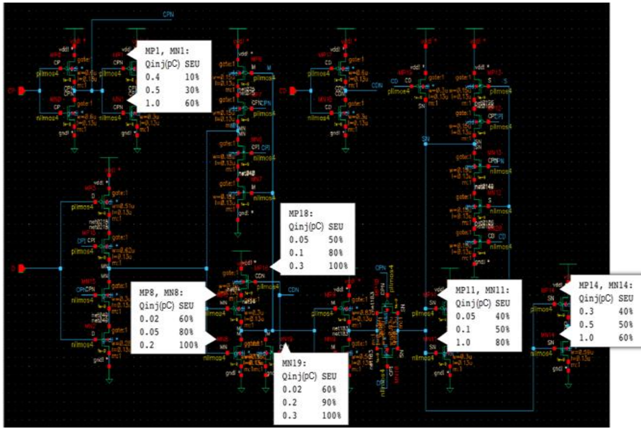

Figure 7: SEE sensitivity map of the target circuit

V. CONCLUSIONS

A tool for automatic analysis of analog/mixed signal circuits affected by radiation has been developed and tested. AFTU allows impact emulation, based in current injection models, in every transistor of a given design by means of configuration files edited by the user. The analysis of every node of the circuit and different signals defined by the designer can be performed applying several heuristics in different available technologies. Thanks to the automated placement and script generation, massive injection campaigns can be performed over target circuits to diagnose their SEE sensitivity following heuristic criteria for error discrimination defined by the user.

VI. ACKNOWLEDGEMENTS

This work was partially supported by the Spanish Ministry of Economy and Competitiveness under the project TEC2010-22095-C03-01 and developed under a collaboration agreement between the European Space Agency and University of Seville.

VII. REFERENCES

[1] P. Jaulent, V. Pouget, D. Lewis and P. Fouillat, "Study of Single-Event Transients in High-Speed Operational Amplifiers". IEEE Transactions on nuclear science, vol.55, nº 4, Aug. 2008

[2] J.M. Mogollón, F.R. Palomo, M.A. Aguirre, J. Napoles, H. Guzmán and E. Garcia, "TCAD Simulations on CMOS Propagation Induced Pulse Broadening Effect: Dependence Analysis on the Threshold Voltage", IEEE Transactions on nuclear science, vol.57, nº 4, Aug. 2010

[3] Marquez, F.; Munoz, F.; Palomo, F.R.; Aguirre, M.A. and Ullan, M., "Analysis of Single Event Transient Effects in Analogue Topologies" 4th International Workshop on Analogue and Mixed-Signal Integrated Circuits for Space Applications (AMICSA '12). Aug. 2012.

[4] Aguirre, M.A.; Tombs, J.N; Muñoz, F.; Baena, V.; Guzman, H.; Nápoles, J.; Torralba, A.; Fernández-León,A; Tortosa-López, F. and Merodio, D., "Selective protection analysis using a SEU emulator: testing protocol and case study over the LEON2 processor," IEEE Transactions on Nuclear Science, 54(4), pp.951,956, 19-21 Sept. 2007.

[5] G. Messenger, "Collection of Charge on junction nodes from ion tracks", IEEE Transactions on nuclear science, vol.29, nº 6, Dec. 1982.

Radiation Hardened Technology for Mixed-Signal IC

SEE Characterization of a Magnetometer Front-End ASIC Using a RHBD Digital Library in AMS 0.35µm CMOS

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Abstract

A radiation-hardened-by-design (RHBD) digital library, developed for the Austria Microsystems (AMS) 0.35µm CMOS technology, has been applied in a mixed-signal ASIC that operates as a multi-channel data acquisition system for magnetometers using anisotropic magneto-resistances (AMR) as sensing elements. The circuit has been tested in the Heavy-Ion facilities of the Université Catholique de Louvain-la-Neuve (HIF-UCL). The experimental results demonstrate a LET threshold of 16.5 MeV·cm²/mg and absence of latchup up to 80.8 MeV·cm²/mg. This radiation-tolerant performance is obtained at the cost of a penalty in area and power with respect to the unhardened technology.

I. INTRODUCTION

This work is part of a planned long-term effort and collaboration between Instituto de Microelectrónica de Sevilla (IMSE), Universidad de Sevilla (US), and Instituto Nacional de Técnica Aeroespacial (INTA) to develop the infrastructure (design flow, technology characterization, libraries) needed for the development of space-grade circuits. The results are initially being applied in the design of scientific instrumentation for missions to Mars.

There is currently a trend in space applications towards small sized (nano-, pico-) satellites that is putting the development of spacecrafts at the reach of small industrial and academic groups. More than in other space applications, small weight and size together with a reasonable development cost are a strict requirement for components in that type of small satellites. The availability of an affordable and performant mixed-signal ASIC technology with known radiation behaviour will help in the design of the instrumentation for those miniature spacecrafts.

This paper presents the results of SEE tests carried out in the cyclotron facilities of UCL using as test vehicle an ASIC, implemented in the AMS 0.35µm CMOS technology, and designed to serve as a 16-bit mixed-signal front-end for a tri-axial magnetometer using low-cost anisotropic magneto-resistances (AMR) as sensing elements.

The following sections briefly present the system and circuit description and give details about the SEE characterization and test results. More details on system and circuit can be found in references [1-2].

II. SYSTEM DESCRIPTION

Fig. 1 shows a simplified block diagram of the proposed triaxial magnetometer. Only one of the three axes is shown in the diagram for simplicity. The magnetometer comprises two main elements, the first one is a linear magnetic field sensor that provides an output voltage proportional to the applied

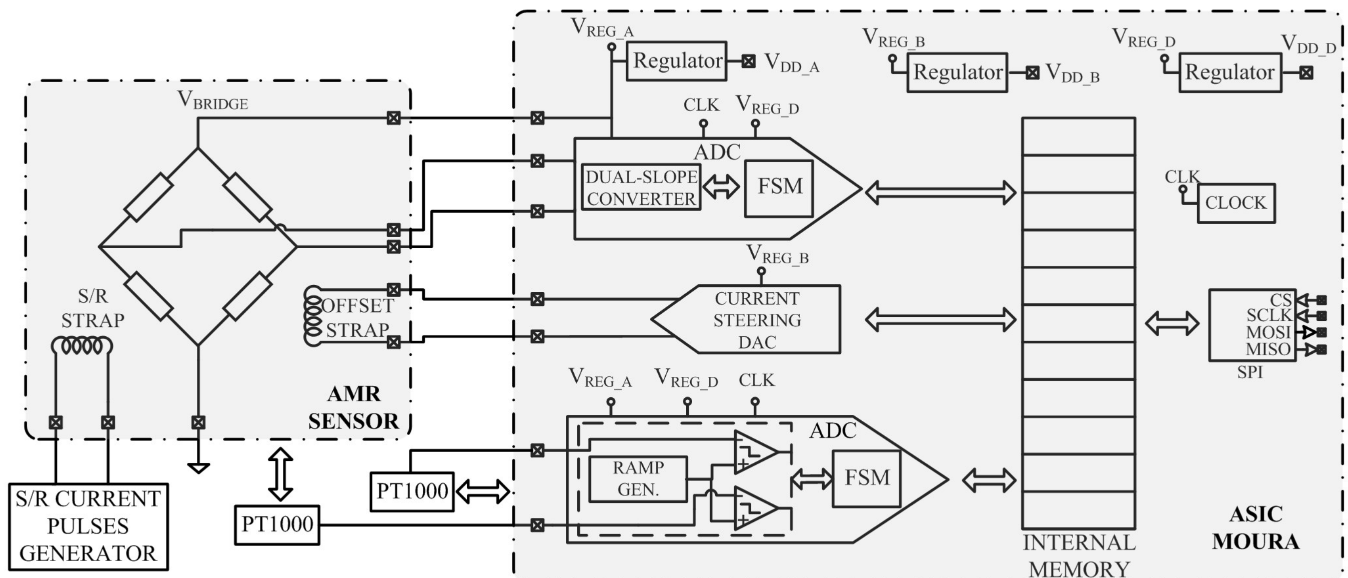

Figure 1: Block diagram of the full system, including external magnetic field and temperature sensors.

magnetic field in the sensitive direction. The second one is a mixed-signal ASIC wich is responsible for conditioning and digitizing the voltage signal from the sensor. The ASIC also performs calibration functions, and communications tasks to capture the ADC outputs and upload system configuration parameters. It has been designed with a high level of configurability that makes possible its use in other space applications with a need for a set of rad-hard low-speed high-resolution ADCs and/or DACs.

The ASIC has been designed in the 0.35 µm CMOS technology from AMS. The circuit is able to work with two alternative AMR sensors having different sensitivities. Their maximum ranges and resolutions are ±1 G, 30 µG for the high-sensitivity type and ±3.3 G, 100 µG for the type with low sensitivity. The ASIC contains six dual-slope 16-bits ADCs that permit the simultaneous capture of the signals from two triaxial magnetosensors. When a 100 Mhz main clock is used, the resolution of those ADCs is 16 bits (15 bits plus sign) at a maximum sampling frequency of 2.6 kS/s and 12 bits (11 bits plus sign) at 20 kS/s. In addition the chip contains four general purpose single-slope ADCs, using self-biased comparators, with a resolution of 15-bit at a maximum of 3 kS/s (10-bit at 77 kS/s) and three 9-bit monotonic current-steering DACs. Two finite-state machines (FSMs) control the operation of the dual-slope and the single-slope ADCs. All the operation and configuration options are programmed in an internal register bank that also stores the output values of the ADCs. The internal memory is read and written using a Serial Peripheral Interface (SPI). The converters clock frequency is programmable up to 100 MHz. The chip has a total area of 4.5 mm x 4.5 mm. The complexity of the digital part is approximately 7 kgates.

A detailed description of the circuit, covering the operation of the dual- and single-slope converters is given in [1].

III. SEE TESTS

A SEU Tests

SEU tests have been performed using as test vehicles the 208 bits of the configuration registers included in the chip. During SEU tests, the registers are written once and then read repeatedly under control of an FPGA through the SPI port at a rate of 35 times per second, comparing each time the values read with those previously written. Any discrepancy is considered a SEU and recorded in a file. Once a SEU has been recorded, the registers are rewritten and the upset monitoring process continued.

Irradiation was carried out at the UCL-HIF using ion cocktail #1 (high-LET). An efective flux of 10^4 $cm^{-2}\cdot s^{-1}$, was used for the ions with lower LET (up to Ar at 55º), and $5\cdot 10^3$ $cm^{-2}\cdot s^{-1}$ for the higher LET ions. Irradiation was stopped after reaching a total fluence of 10^7 $ions\cdot cm^{-2}$ for the lower LET ions, or until $5\cdot 10^6$ $ions\cdot cm^{-2}$ for higher LET ions. At least 200 errors were recorded in all tests with the lowest fluence. Two different ASIC samples were tested.

Because the ion energies are located around the Bragg peak, LET values have been corrected to take into account the effect of the top passivation, metal and oxide layers situated over the active surface of the sensitive junctions. Multiple bit errors in the same reading are assumed to be caused by SET and removed from the SEU error count. This is reasonable given the very low probability of two ions hitting the sensitive area within one polling period lasting only 35 milliseconds. Cross-sections for oblique incidence have been corrected to take into account geometric effects, assuming an RPP model, and adjusted to Weibull and Log-Normal curves [3]. The results are shown in Fig. 2, that also gives a comparison with the results obtained in measurements performed in other chips using an earlier version of the RHBD digital library [4]. LET threshold has increased from 12 to 16.5 $MeV\cdot cm^2\cdot mg^{-1}$, at the cost of a slightly larger saturation cross-section and power consumption. The new library shows a considerable level of hardening, with a FoM of $3.78\cdot 10^{-10}$ $MeV^2\cdot cm^2\cdot mg^{-2}$ [5], resulting in an estimated upset rate of $3.59\cdot 10^{-8}$ $upsets\cdot bit^{-1}\cdot day^{-1}$ for a 90% worst-case geostationary orbit with 100 mils of Al shielding [5].

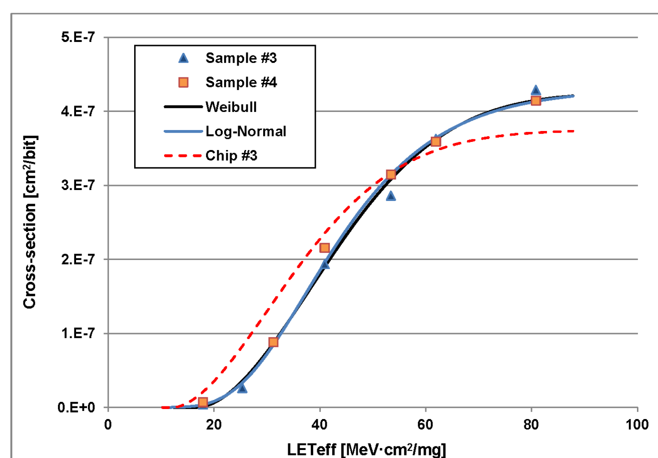

Figure 2: SEU cross-sections comparing current (MOURA) and previous (CHIP#3) RHBD libraries

B Data Converters

The analog circuitry of integrating converters, because of its inherent low-pass characteristic should not be much affected by SETs; however, the combinational and sequential elements in the digital counters and in the Finite-State Machines (FSMs) controlling the operation of the converters can be more sentitive to SEEs, and are assumed to be the reason for the output values showing large deviations from the expected value. Ion-hits in sensitive nodes of the analog circuitry can produce random charge injections that together with hits in the LSBs of the counters should be assumed to be responsible for any increase in the standard deviation (larger RMS error) in the output values. For those reasons, the effect of heavy-ion radiation on the A/D converters has been evaluated using two different metrics: the change in the RMS error (standard deviation) and the number of samples laying outside a +/-4σ interval centered in the mean value.

During the irradiation period a fixed input voltage, close to the middle of their positive range, was applied to the input of the data converters. The converters operated continuously with a clock frequency of 25 MHz, giving a conversion time of 2 ms for the dual-slope converters and 1.3 ms for the single-slope converters. The converter outputs were read 35 times per second, and their output values stored for later processing. Approximately thirty thousand values per converter were stored for each LET value.

Because the converters are reset at the beginning of each conversion, only the ion fluence during the conversion time has to be considered for each reading. Therefore the total fluence applied during the experiments has to be scaled by a factor given by the the ratio of conversion-time to time-between-readings (0.069 for dual-slope, 0.045 for single-slope).

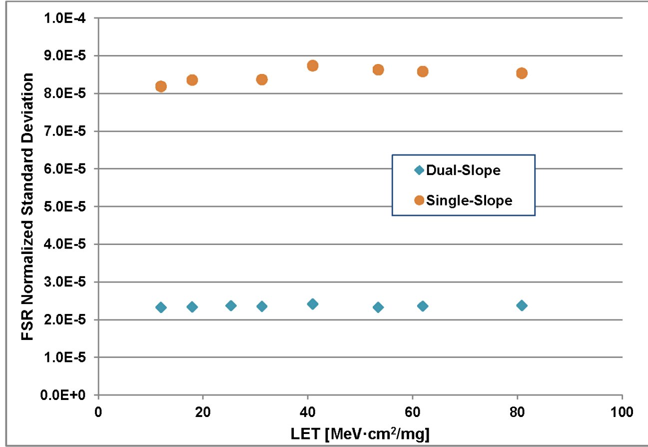

Figure 3: Normalized Standard Deviation versus LET for Single- and Double-Slope AD converters

The long series of experimental datapoints, collected for each LET value during an interval of around 15 minutes, shows drift caused by temperature, electrical interferences and TID effects that can be comparable or even larger than the RMS error. Therefore all those effects have to be removed as much as possible by postprocessing to be able to determine the number of errors that can be attributed to SEEs and not to other random errors. Post-processing of the converter data has been performed in four steps: a) the standard deviation for each converter was calculated, and those output values with a deviation larger than 4σ were excluded from the measurement set; b) linear detrending coefficients were then obtained from the reduced dataset and applied to the original data set; c) a new standard deviation was then calculated using the detrended original data, and the values beyond 4σ excluded to leave a new reduced data set; d) a moving average was applied to filter short-term baseline variations, and the final value for σ was obtained from that reduced dataset. Points falling outside four times the final σ have been considered as

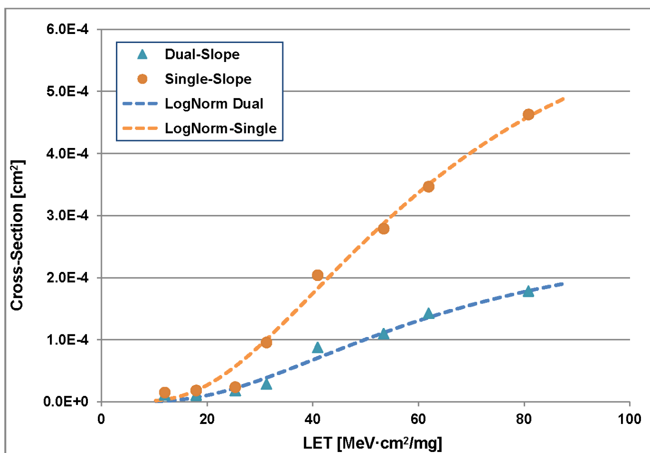

Figure 4: Log-normal cross-section of single- and dual-slope data converters for errors larger than 4σ

measurement upsets due to ion-hits in the converters and used to determine the converter error cross-section. The 4σ used to differentiate bad measurements corresponds to approximately 6 LSBs for the dual-slope converters, and 12 LSBs for the single-slope type.

Figure 3 shows the the dependence with LET of the standard deviation normalized to full-scale range of the single and dual-slope ADC outputs. Although conditions in the irradiation chamber are not ideal for high resolution measurements, the recorded RMS errors are similar to those obtained in standard laboratory conditions, and are not affected at the highest LETs measured. After post-processing, eliminating the datapoints with deviations larger than 4σ, the RMS error is approximately 1,5 LSBs for the dual-slope ADC, and 2,5 LSBs for the dual-slope ADC.

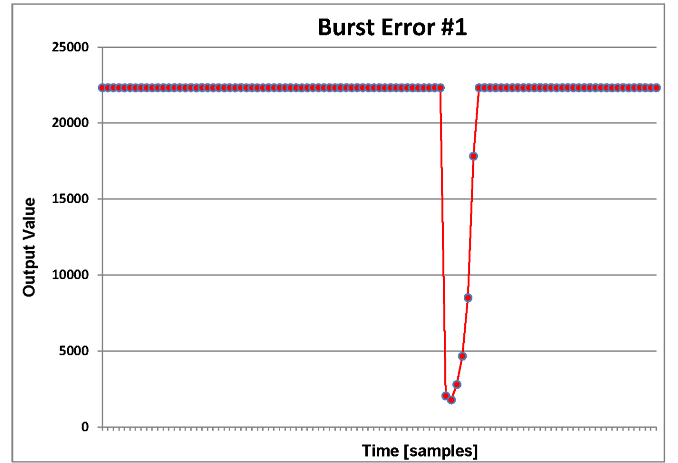

Figure 5: Burst error at the output of a single-slope converter

Fig. 4 presents the converter cross-sections for errors larger than 4σ and a log-normal approximation using a least-square fit of the data points. From the log-normal parameters the saturation values are $2.63 \cdot 10^{-4}$ cm^2 for the dual-slope converters, and $6.70 \cdot 10^{-4}$ cm^2 for the single-slope type.

The larger cross-section of the single-slope converters can be partly explained by the effect of ion-hits in the circuit for automatic adjustment of the ramp slope. Although the converter counters are reset at the beginning of every conversion cycle, an error in the ramp controller, which is common to all four converters will last for several cycles, effectively increasing the exposure time window and inducing a burst of erroneous measurements. An example of such an occurrence is shown in Fig. 5. The dots represent samples spaced 35 ms.

Table 1: Number and average length of burst errors

Ion	Angle	LET[Si]	Burst Errors	Average Length
Ne	55	11,9	0	0
Ar	0	17,9	0	0
Ar	55	31,2	2	2,5
Kr	0	40,9	12	3,0
Kr	40	53,4	22	4,4
Xe	0	61,9	32	3,2
Xe	40	80,8	72	3,6

The number of registered burst errors and their average

length (in number of measured samples) at different LET values is shown in Table 1. The errors happen simultaneously in all the four single-slope channels of a chip, confirming that their origin is in the ramp controller. It has to be taken into account that only one in 22 samples are read during the experiment, so for a converter running at full speed the length of the error bursts would need to be multiplied by 22.

C Converter Error Rate

To get an estimation of the converter error rate in geostationary orbit, the experimental cross-section data are translated to the probability of deposited energy over the track of the incident ions in the sensitive volume. To have a worst-case analysis, the largest drain diffusion in the FSM latches was taken as the sensitive volume to calculate the deposited energy. The integral spectral distribution of ions versus deposited energy in a given environment can be obtained using CREME-96 [6], and combining it with the measured cross-sections allows to estimate the error rate for that environment. As an example, for a geostationary orbit, at the maximum of cosmic rays flux, and with 100 mils of Al shielding, the estimated SEE error rate per converter (values outside 4σ) is $2.1\cdot10^{-5}$/day for the double-ramp converters operating continuously at 500 samples per second and $3.4\cdot10^{-5}$/day for the single-ramp converters operating at 770 samples per second.

IV. CONCLUSIONS

A complete mixed-signal design flow has been demonstrated and tested, using a RHBD digital library and radiation hardening rules for the analog part. The design flow has been applied to the design of a medium-complexity mixed-signal ASIC.

Heavy-ion radiation tests have proved a radiation tolerance to SEEs of the full chip adequate for geostationary orbit applications and for missions to Mars. The robustness against SEE of single and double slope converters is demonstrated.

V. ACKNOWLEDGMENT

This work has been partially supported by the Spanish Plan Nacional de Investigación of the Ministerio de Ciencia e Innovación (MICINN) under projects MEIGA (AYA2011-29967-C05-05, AYA2009-14212-C05-04 and AYA2008-06420-C04-02), in turn partially funded by FEDER.

VI. REFERENCES

[1] Sordo-Ibáñez, S., et al., "*A Front-End ASIC for a 16-Bit Three-Axis Magnetometer for Space Applications Based on Anisotropic Magnetoresistors*", 28th Conference on Design of Circuits and Integrated Systems (DCIS 2013); San Sebastián (Spain).

[2] Sordo-Ibáñez, S., et al., "*An Adaptive Approach to On-Chip CMOS Ramp Generation for High Resolution Single-Slope ADCs*", 21st European Conference on Circuit Theory and Design (ECCTD-2013); Dresden (Germany).

[3] Petersen, E.L., "*Single-Event Data Analysis",* Nuclear Science, IEEE Transactions on, 2008. **55**(6): p. 2819-2841.

[4] Ramos-Martos, J., et al., "*Evaluation of the AMS 0.35 um CMOS Technology for Use in Space Applications"*, Fourth International Workshop on Analog and Mixed-Signal Integrated Circuits for Space Applications, AMICSA2012, European Space Agency: ESA/ESTEC, Noordwijk, The Netherlands.

[5] Petersen, E.L., "*The SEU figure of merit and proton upset rate calculations"*. Nuclear Science, IEEE Transactions on, 1998. **45**(6): p. 2550-2562.

[6] https://creme.isde.vanderbilt.edu/CREME-MC

Mixed-Signal Design Methodology for Various Radiation Environments with Applications to a 0.35µm, 65V Quadruple-Well BCD Technology

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Abstract

There is a need for high voltage (>5V <100V) mixed-signal integrated circuits (ICs) in a variety of applications having ionizing radiation environments, such as satellite/space, medical diagnostic imaging, nuclear power control & monitoring, and radiation oncology therapy. In some of these environments, the ionizing radiation includes ions (space, proton therapy) while in others, there the ionizing electromagnetic radiation is accompanied by neutrons (nuclear power, radiation therapy). Designing to the worse case radiation environment can impose severe design limitations that result in higher power, poorer performance, and higher cost than is really necessary for the intended application. We discuss a unified design flow where different radiation environments are accommodated (but not over-accommodated) by the use of distinct sets of design rules, cell libraries, and design tools.

I. Introduction

After selection of a target wafer fabrication technology, the process of installing market-specific process design kits (pdk) begins with the design and fabrication of a technology characterization vehicle (TCV). The TCV contains at least one (but usually several) instantiations of each active and passive device that are intended to be used by the designers. The fabricated TCV is packaged and electrical test data collected for each device type, e.g. drain current (Id) vs gate voltage (Vg) and Id vs drain voltage (Vd) curves for metal oxide semiconductor (MOS) transistors of various channel lengths (L) and widths (W). Devices are then irradiated using either x-rays or gamma rays to a give total ionizing dose (TID) level, and the same electrical data immediately collected after irradiation.

Sequential digital cells are designed to meet the single event upset (SEU) requirements of the given application environment. The SEU rate is predicted a-priori by the use of two proprietary design tools, Qsim and SETsim, that were described previously [1,2]. The SEU rate is then validated by irradiating the TCV containing such cells, typically configured in large memory arrays, with heavy ions and/or protons as appropriate at various values of linear energy transfer (LET) up to ~110 MeV cm^2/mg. Several, distinct libraries are then created, each having a TID and single event latch-up (SEL) rating for each cell, a digital single event transient (DSET) for each non-sequential cell, and an SEU rating for each sequential cell. In this way, each of the distinct libraries has an overall rating for radiation environment.

Neutron testing is also performed for cells to validate their use in nuclear reactor environments. Analog/Mixed-Signal cells are designed to meet certain recovery times for analog SET (ASET). An analog-to-digital converter (ADC) might have a design target of ASETs having duration of less than two sample clocks for an LET < 40 MeV cm^2/mg. Comparators may be rated by the on-set LET that causes a false reading when the input is within, e.g. 10mV of the trip-point, etc.

Using the a-priori rating system (with validation by TCV testing), completed mixed-signal libraries are formed, labeled and segregated as to their possible radiation environments. The program manager and product development team select the proper mixed-signal library based upon the specification for the mixed-signal IC.

Throughout the rest of this paper, we use the example of a 65V quadruple-well, 4 level metal (4LM) Bipolar-CMOS-DMOS (BCD) process, containing isolated 3.3V CMOS devices in addition to 40V and 65V LDMOS devices.

II. TID Test Procedures

The radiation source used for this testing is an Aracor 4100 X-ray irradiation source and microprobe station. This system produces X-rays with energies ranging from 10 keV to 60 keV a peak energy at 10 keV with dose rates ranging from 2 to 200k rad(Si)/min.. Irradiations for this study occurred at 3,000 rad(Si)/sec. Four high voltage TCV devices were irradiated and tested at room temperature (T = 22 °C ± 6 °C) as shown in Table I. All devices were tested within one hour after X-ray exposure. Stepped X-ray total ionizing dose (TID) values were 50 krad(Si), 100 krad(Si), and 300 krad(Si). All MOS devices were biased statically during X-ray exposure with 110% of the nominal, maximum Vgs applied to the device. NMOS devices used accelerated gate-to-body (gate-to-channel) biasing in a MOSCap type configuration. PMOS devices used the "inverter off" configuration with the gate, body and source tied to 110% of the nominal Vdd and the drain grounded.

Table I: High Voltage TCV Devices

Device Type	W (µm)/L (µm)/M
40V NLDMOS	10/0.2/1
40V PLDMOS	10/0.2/1
65V NLDMOS	10/0.2/1
65V PLDMOS	10/0.2/1

III. TID RADIATION TEST RESULTS

Figure 1 shows Id-Vg data for the Aeroflex-designed 40V NLDMOS devices in a 0.35 µm quadruple-well BCD technology for TID levels of 0, 50, 100, and 300 krad(Si). The minimum, average, and maximum threshold voltage shift from the population of devices irradiated as a function of TID is shown in Figure 2. Figures 3 and 4 show the Id-Vg and the minimum, average, and maximum threshold voltage shifts for the 40V PLDMOS device respectively. Figures 5 and 6 show the Id-Vg and the minimum, average, and maximum threshold voltage shifts for the 65V NLDMOS device respectively. Figures 7 and 8 show the Id-Vg and the minimum, average, and maximum threshold voltage shifts for the 65V PLDMOS device respectively.

As can be seen for Figures 1, 3, 5, and 7, there is no appreciable change in the subthreshold slopes of any of the Id-Vg curves, and that the transistor off leakage (Idoff) is essentially the same as the pre-irradiation values of leakage for all four high voltage device types.

As can be seen in Figures 2, 4, 6, and 8, the threshold voltage shifts for the PLDMOS devices is about twice as great as for the NLDMOS devices. The maximum NLDMOS threshold voltage shifts was less than 25 mV for both the 40V and 65V devices, while the maximum PLDMOS threshold voltage shift was less than 95 mV for both the 40V and 65V devices.

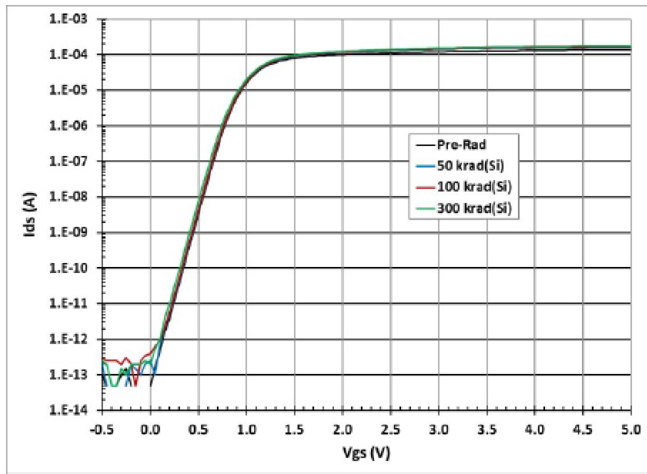

Figure 1: Id-Vg Curves for the 40V NLDMOS Device

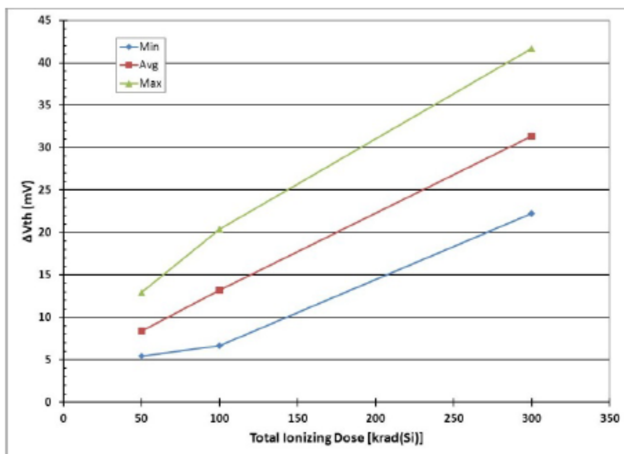

Figure 2: Minimum, Average, and Maximum Threshold Voltage shift in the 40V NLDMOS Device

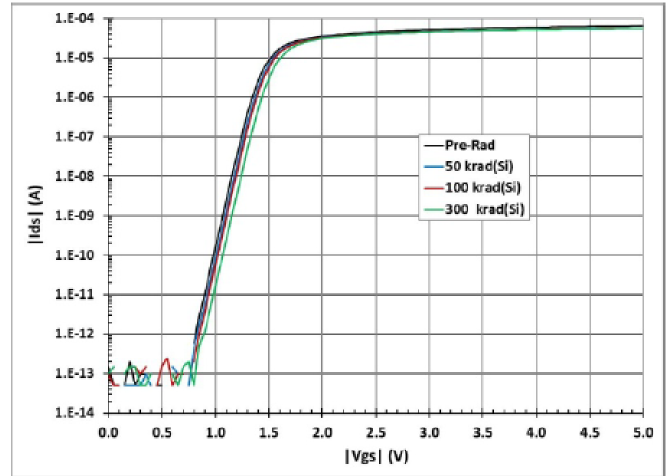

Figure 3: Id-Vg Curves for the 40V NLDMOS Device

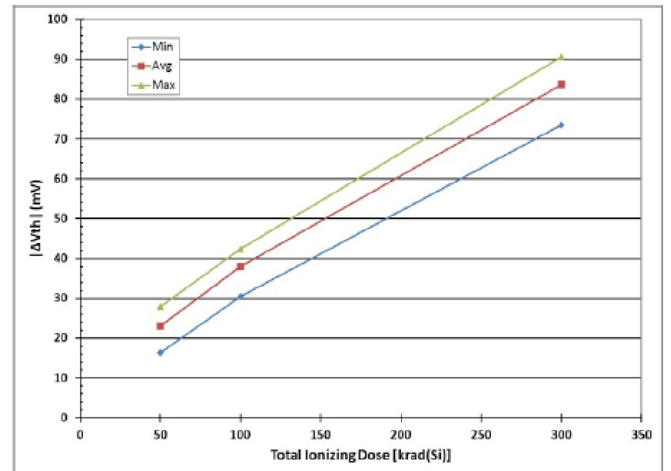

Figure 4: Minimum, Average, and Maximum Threshold Voltage shift in the 40V PLDMOS Device

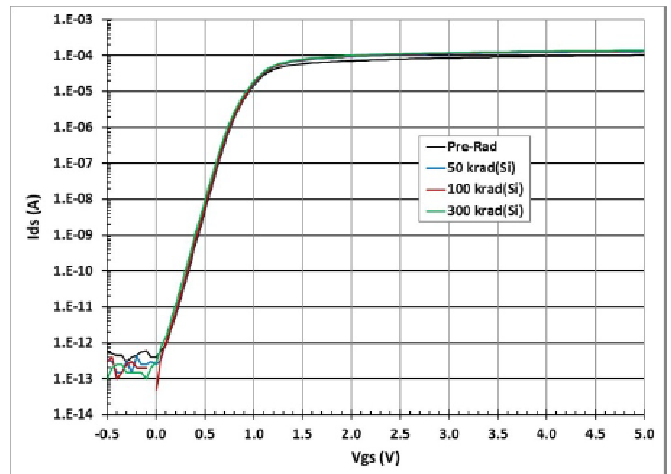

Figure 5: Id-Vg Curves for the 65V NLDMOS Device

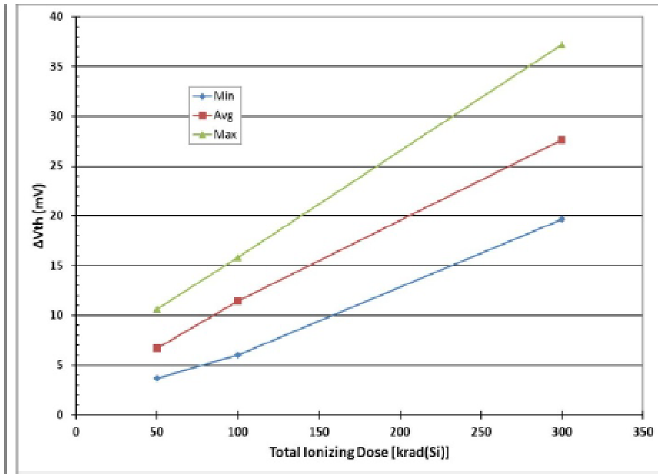

Figure 6: Minimum, Average, and Maximum Threshold Voltage shift in the 65V NLDMOS Device

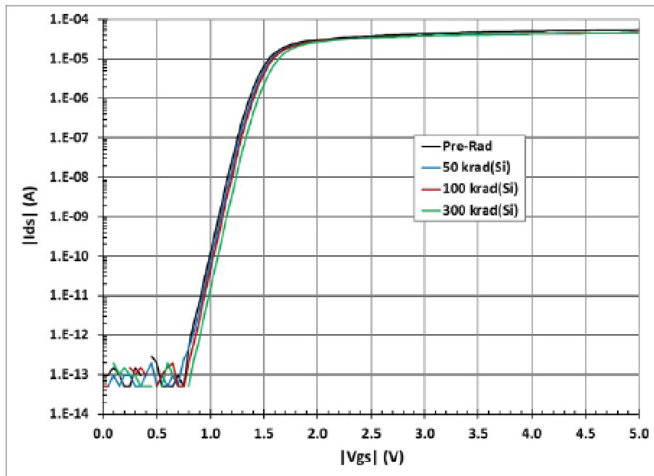

Figure 7: Id-Vg Curves for the 65V PLDMOS Device

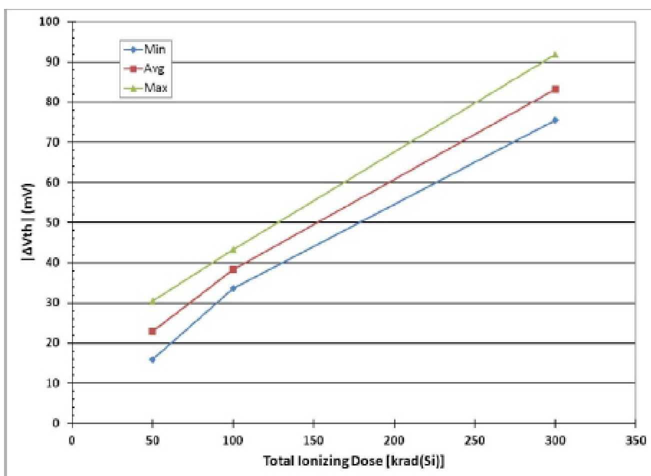

Figure 8: Minimum, Average, and Maximum Threshold Voltage shift in the 65V PLDMOS Device

III. Single Event Effects (SEE) Testing

SEE testing was performed at the Texas A&M University Cyclotron Facility on February 25, 2014. The 40V NLDMOS and PLDMOS were irradiated with broad-beam Xe ions for various drain voltages at either 125ºC or at room temperature (RT). The angle of the beam with respect to the device under test (DUT) normal was varied to vary the effective LET. The results are shown in Table II. As can be seen, all of the 40V PLDMOS devices performed well with a drain voltage of 35.2 and 40V (runs 1, 3, 4, and 8). The n-channel LDMOS devices (runs 2, 5, 6, 7, and 9 through 20), failed at drain voltages greater than 32V for a LET of 55 MeV cm_2/mg, and at voltages greater than 30V for a LET of 110 MeV cm_2/mg. (It should be noted that serial number 7, a 40V NLDMOS device, was irradiated six times to a fluence of 1E7 ions/cm^2 each irradiation, before it failed at a drain voltage of 30V with a LET of 110 MeV cm^2/mg and a cumulative fluence of 6E7 ions/cm^2. However a fresh device irradiated at a drain voltage of 30V with an effective ion LET of 110 MeV cm^2/mg to a fluence of 1E7 ions/cm^2 passed just fine.

IV. Discussion

The analysis of TID results in this technology indicates that the TID performance is acceptable for almost any market including medical imaging, space/satellite, nuclear reactor monitoring, etc. However, the 40V SEE data indicates that, while the 40V PLDMOS can operate up to its nominal value of 40V at the maximum LET of 110 MeV cm^2/mg, the NLDMOS is limited to ~30V or less for the space/satellite markets. Preliminary results on the 65V devices, still in test, indicate that some sort of de-rating for use in space is required.

Table III shows the available libraries in this technology, along with maximum voltages. While neutron testing has not yet been completed, we do not expect the same type of failures of the high voltage devices as seen with heavy ions.

Table III: Voltages by Market for 0.35 µm BCD Technology

Device Type	Voltage for Space Market (V)	Voltage for Medical Imaging Market (V)	Voltage for Nuclear Reactor and Radiation Therapy (V)
3.3V NMOS	3.6	3.6	3.6
3.3V PMOS	3.6	3.6	3.6
3.3V i-NMOS	3.6	3.6	3.6
5V NMOS	5.5	5.5	5.5
5V PMOS	5.5	5.5	5.5
5V i-NMOS	5.5	5.5	5.5
40V NLDMOS	30	40	TBD
40V PLDMOS	40	40	TBD
65V NLDMOS	TBD	65	TBD
65V PLDMOS	TBD	65	TBD

IV. References

[1] D.B. Kerwin, A. Wilson, Y. Lotfi, K. Merkel, and A. Zanchi, “MIXED-SIGNAL DESIGN METHODOLOGY USING A PRIORI SINGLE EVENT TRANSIENT RATE ESTIMATES”, *4th*

International Workshop on Analog and Mixed Signal Integrated Circuits for Space Applications (AMICSA 2012), 26 - 28 August 2012 ESA/ESTEC, Noordwijk, The Netherlands.

[2] D.B. Kerwin, A. Zanchi, A. Wilson, K. Merkel, J. Colley, "ADVANCES IN RADIATION HARDENED MIXED-SIGNAL TECHNOLOGY", *4th International Workshop on Analog and Mixed Signal Integrated Circuits for Space Applications (AMICSA 2012),* 26 - 28 August 2012 ESA/ESTEC, Noordwijk, The Netherlands.

Table II: Summary of 40V N- and PLDMOS SEE Testing

Run #	V_{DD} drain (V)	Temp. (ºC)	S/N	Device Type	Ion	Normal LET (MeV·cm²/mg)	Angle (°)	Effective LET (MeV·cm²/mg)	Pre-I_{DS} Current (mA)	Post-I_{DS} Current (mA)	Eff. Fluence (ions/cm²)	Damaged? y/n
1	35.2	125	2	40V PLDMOS	Xe	55.0	60	110	50.6	49.5	1.0E+7	n
2	35.2	125	3	40V NLDMOS	Xe	55.0	60	110	52.0	500.0	1.8E+6	y
3	35.2	125	3	40V PLDMOS	Xe	55.0	60	110	51.0	50.9	1.0E+7	n
4	35.2	125	4	40V PLDMOS	Xe	55.0	60	110	50.8	50.7	1.0E+7	n
5	35.2	125	4	40V NLDMOS	Xe	55.0	60	110	51.9	500.0	5.0E+4	y
6	35.2	125	5	40V NLDMOS	Xe	54.4	48	81	52.2	500.0	5.5E+4	y
7	35.2	125	6	40V NLDMOS	Xe	53.8	0	54	52.2	500.0	1.7E+4	y
8	40.0	125	6	40V PLDMOS	Xe	55.0	60	110	57.8	57.6	1.0E+7	n
9	5.0	RT	7	40V NLDMOS	Xe	55.0	60	110	0.136	0.137	1.0E+7	n
10	10.0	RT	7	40V NLDMOS	Xe	55.0	60	110	0.280	0.281	1.0E+7	n
11	15.0	RT	7	40V NLDMOS	Xe	55.0	60	110	0.430	0.430	1.0E+7	n
12	20.0	RT	7	40V NLDMOS	Xe	55.0	60	110	0.583	0.585	1.0E+7	n
13	25.0	RT	7	40V NLDMOS	Xe	55.0	60	110	0.741	0.742	1.0E+7	n
14	30.0	RT	7	40V NLDMOS	Xe	55.0	60	110	0.899	0.430	1.0E+7	y
15	30.0	RT	8	40V NLDMOS	Xe	55.0	60	110	0.879	0.899	1.0E+7	n
16	35.2	RT	8	40V NLDMOS	Xe	55.0	60	110	1.07	500.0	4.6E+5	y
17	35.2	RT	9	40V NLDMOS	Xe	55.0	60	110	1.1	486.9	3.1E+4	y
18	30.0	RT	11	40V NLDMOS	Xe	53.8	0	54	0.934	0.945	1.0E+7	n
19	32.0	RT	11	40V NLDMOS	Xe	53.8	0	54	1.011	1.018	1.0E+7	n
20	34.0	RT	11	40V NLDMOS	Xe	53.8	0	54	1.085	500.0	2.0E+6	y

Radiation-Tolerant Low-Voltage ASIC Library Evaluation for Space Applications

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Abstract

The needs for increasingly low cost, low space occupancy and reduced weight in the space industry have made mixed-signal ASIC integration mandatory. In a first contract, the CNES and ID MOS selected the mixed-signal XH035 LV ASIC process to design a set of rad-tolerant Low Voltage ELT transistors, checked their robustness up to 100Krads and their immunity to the SEL.
The aim of the project was to develop radiation tolerant libraries that enable designers to develop Analogue and Digital circuits for the Space Applications.

I. INTRODUCTION

ID MOS selected the XFAB XH035 mixed-signal technology for its modularity and the set of devices provided in the standard XFAB process to develop Analogue and Digital functions. This standard technology targets automotive, telecommunication and industrial applications; it has been widely used and tested for various applications, it is a mature technology. To develop circuits, a design kit is provided for each technology by XFAB. This tool box is based on the characterisation of basic devices (transistors, diodes, resistance, capacitor...), it includes the electrical, the synthesis, the simulation models and the layout of those elements, the standard cells, the I/O pads and all scripts to perform the verifications. The XFAB target is to access the markets with high volumes where the price unit is a key factor linked with the die size. To reach the objective, they have to optimize the layout of the basic elements to integrate the maximum of functions on a minimum of Silicon area. Unfortunately, it is incompatible with Space applications. The drawing of the basic transistors has to be completely redefined to reach the TID and SEU targets. A set of transistors covering most of the analogue low voltage applications have been selected and harden by ID MOS. A test chip including different modules, to perform the characterisation, to check the insensitivity to SEL and to reach the defined TID level has been launched for fabrication. This first step has been 100% successful allowing us to prepare the next phase.

The tasks performed in this contract are the following:

- Characterisation of the basic devices: P/N Transistors, Resistance, Capacitor.
- Development of the Spectre models for the electrical simulations.
- Development of the Process Design Kit (PDK)
- Development of the Standard cell library
- Development of the I/O pads library
- Update of the Verification tools
- Supply a set of scripts to add automatically digital functions to minimize SEU and SET effects: Triplication, pulse filter.
- Integration of those elements to provide a Design Kit
- Validation phase

II. THE TEST VEHICLE

To fulfil Space application projects, a LV radiation-tolerant test chip has been designed. Its target is to be characterized up to 100 krads. insensitive to SEL up to 67, 7 Mev/cm²/g.
From the XFAB library the following N and P transistors have been selected:

- NMOS (nmos4, nmos3, nha, ioh_ne)
- PMOS (pmos4, pmos3, ioh_pe)

Those transistors have been hardened using an enclosed layout (ELT) and guard rings. Structures have also been used to break leakage paths. Those cells have been tested electrically before and after TID.
As example, we can compare the I/V curve of the nmos transistor extracted from the standard XFAB libray and the equivalent ELT transistor before and after TID. We choose the smallest enclosed transistor size used for digital cells (W/L=5.4/0.35µm)

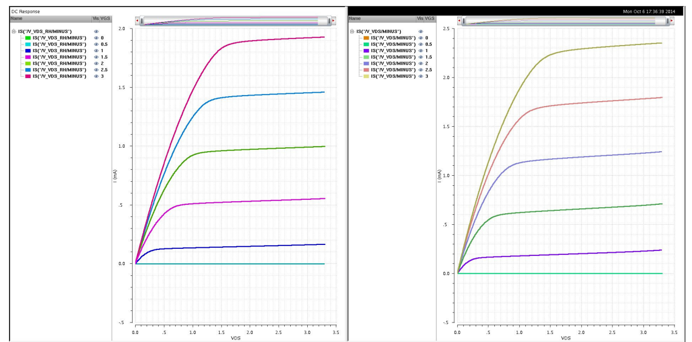

Figure 1: I/V curve (With and without ELT)

I (mA) VDS = 3,3v	nmos3 (rh)	nmos3 (rh_100Krad)	nmos (std)
VGS= 1.0v	0.16 mA	0.17 mA	0.21 mA
VGS= 1.5v	0.55 mA	0.56 mA	0.70 mA
VGS= 2.0v	0.99 mA	1.00 mA	1.22 mA
VGS= 2.5v	1.46 mA	1.47 mA	1.80 mA
VGS= 3.0v	1.92 mA	1.93 mA	2.35 mA

Table 1: I/V curve

For a same size the curve are slightly different between standard and enclosed transistor nmos before radiation, but no significant deviation before and after radiation (100Krads) for the enclosed transistor.

A. *Description :*

The test chip includes seven blocks:

- Digital : Basic digital cells & functions
- Monitoring : Basic devices with ESD protection
- Analogique : Basic analogue cells & functions
- Pads : Input/Output/Bidirectional
- Memories : Std XFAB SRAM/CEEPROM
- Module : Basic devices

The peripheral blocks are used for Electrical and Radiation tests. The bloc Module is used for characterization.

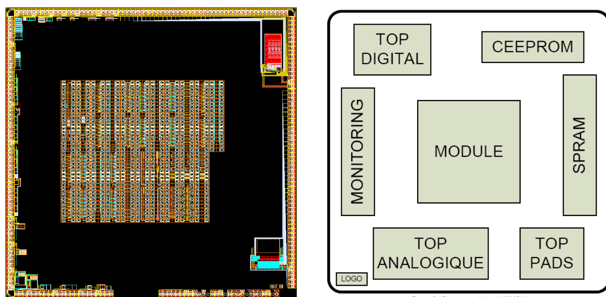

Figure 2 : Low Voltage Test Chip

B. *Description & results of the radiation tests:*

The total dose tests have been carried out with a Cobalt 60 source on 6 reference pieces up to 100 krads at a low dose rate of 310 rad/h. An annealing of 24h/25°C plus 168 h/100°C has been performed.

The SEL tests have been performed at the university of LOUVAIN (Belgium) using Xenon ions with energy of 1217 MeV and a LET on die surface of 67.7 MeV.cm²/mg at a temperature of 125°C.

TID tests have shown no functional or parametric problems up to 100 krads on hardened structures. The non-RT Cells are limited: The non-hardened oscillator and counter present an important increase of their supply current at 30Krads.

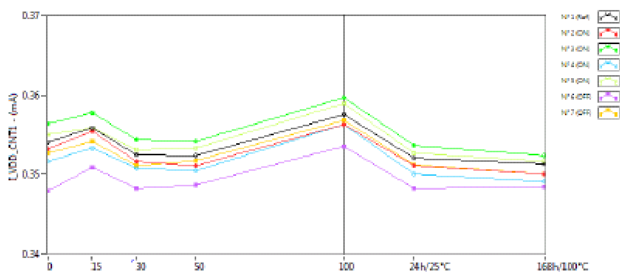

Figure 3: Asynchronous counter based on RT Cells

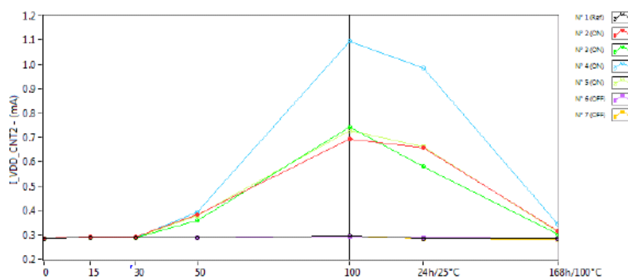

Figure 4: Asynchronous counter based on Std Cells

No SEL has been detected on the Rad-Tolerant cells.
SELs were observed on the non-hardened counter, the non-hardened oscillator and the non-hardened E2PROM. It justifies the necessity to implement protections against SEL.

III. Description of the Design Kit

The ID MOS Radhard Design Kit is an extension of the official XH035 DK provided by XFAB. The advantages are multiple: maintenance, enhancement, no training, no time lost in using it.
It provides a database of models, primitive devices, digital cells, I/O cells, configuration scripts and tools needed to design Rad-Hard-by-Design mixed-signal Analogue/Digital Integrated circuits, according to ID MOS custom rules.

A. *Project Design Flow*

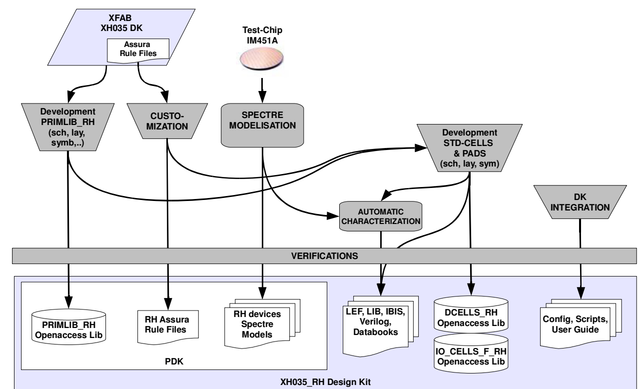

Figure 4: Project Design Flow

B. *Process Design Kit (PDK)*

The PDK is the core of the RH Design Kit. It includes all the low-levels Cadence libraries, configuration files and scripts to develop and simulates Rad-hard functions.

It provides the following primitive devices:

- ⇨ 4-pin regular annular NMOS
- ⇨ 3-pin abutted annular NMOS (Source/Bulk shorted)
- ⇨ 4-pin regular annular PMOS
- ⇨ 3-pin abutted annular PMOS (Source/Bulk shorted)
- ⇨ 12V NMOS with thin oxide
- ⇨ Special NMOS transistor for ESD protections
- ⇨ Special NMOS transistor for ESD protections

It consists of three main parts.

1) *SPECTRE Models :*

The spectre models of annular transistors are "Scalar" allowing to simulate devices of various shape. They are compliant with the devices identified by the extraction tool (ASSURA) and with the primitive cells embedded in the PRIMLIB_RH Cadence Library (consistent names and parameters).

2) ASSURA Tool Kit :

It is a Customization of XFAB Assura rule files to add support of annular transistors, both for LVS and DRC.

3) Library PRIMLIB:

The PRIMLIB is composed of a set of low voltage transistors hardened against radiation.

This library is backward compatible with the original one. They can be used simultaneously. The models are scalable and allow different shape

Gate Length (µm)	Gate Width (µm)
0.35	5.4, 6.5, 7.6, 8.7 (1.10 µm step)
	10.8, 21.6, 43.2 (10.8 × 2N µm)
0.70	6.8, 8.2, 9.6, 11.0 (1.4 µm step)
	13.6 , 27.2, 54.4 (13.6 × 2N µm)
1.4	9.6, 19.2, 38.4 (9.6 × 2N µm)
2.8	15.2, 30.4, 60.8 (15.2 × 2N µm)
5.6	26.4, 52.8 (26.4 × 2N µm)

Table 1: W/L Combinations for PRIMLIB_RH nmos and pmos Transistors

C. STD-CELLS & I/O Libraries

It includes a library of digital standard cells (~40) and 3V digital/analogue standards pads (~15) suitable for logic synthesis and automatic P&R:

- ⇨ Schematics + Layouts + Abstracts + symbols
- ⇨ Liberty library
- ⇨ Verilog Library
- ⇨ LEF Library
- ⇨ Tutorial(s)
- ⇨ Detailed description of SEU-hardening procedure(s).
- ⇨ IBIS Models of Digital Pads
- ⇨ Library databook

1) Electrical Characterization conditions :

- Voltage : 1,8V up to 3,6v
- Temperature : -55°C ; 25°C ; 125°C
- Process : Slow/Fast
- With/without radiation

D. Design Kit Integration :

The integration of the design kit consists in assembling all the libraries and configuration files into a portable database, and to allow easy access to this database from user's working environment, together with the XFAB mainstream DK.

IV. DESIGN KIT VALIDATION

A set of verifications has been done to ensure:

- ⇨ The main features of the PDK;
- ⇨ The efficiency of the ASSURA toolkit
- ⇨ The reliability of analogue simulations
- ⇨ The expected behavior of standard-cells and pads;
- ⇨ The capacity to synthesize a complex digital VHDL model targeting the Rad-hard standard-cells library.
- ⇨ The capacity to automatically Place & Route the standard-cells.
- ⇨ The capacity to produce a DRC-free and LVS-free complex digital design.
- ⇨ The capacity to run accurate post-extracted simulations of analogue and digital circuits.

A. PDK Verification :

1) Spectre.

The Analogue macrocells, embedded on the test-chip (POR, Band-gap, Ring-Oscillator, AOP, and Current Source) have been simulated (from schematics or from extracted layout views) and the results compared to the measurement results.

2) PRIMLIB

All standard-cells and Standard-pads have been simulated, using the PDK.

3) ASSURA ToolKit

All the standard-cells and pads have been checked using the Assura toolkit. (DRC/LVS)

B. DK Verification :

1) D-CELLS & I/O-CELLS

All the deliveries listed have been realized and checked
The whole design has been validated on a representative circuit of about 1 KGates (including pads), with scan-test insertion. (Synthesis, simulations, P&R, final DRC/LVS verification)

2) DK INTEGRATION

The installation instructions and Usage guidelines of the final Design Kit are detailed in the "Reference Manual"

V. CONCLUSION

The XH035-RH Design Kit is ready to be used by ID MOS for Space Applications. The two first circuits will help to intensively use it. A full digital circuits (40Kgates) has been fabricated and electrically tested successfully, the density reaches 4Kates/mm²
The next step is to extend the Design Kit for High Voltage Applications. It is the object of a new project by using the same methodology.

References

Single event effects test method and guidelines ESA/SCC basic specification N°25100 Iss 1, oct 95
Space Product Assurance-ASIC and FPGA development (ECSS-Q-ST-60-02C)
ESA-ESTEC- Space engineering, product assurance
Techniques for Radiation Effects Mitigation in ASICs and FPGAs (ESA-HB-XX-XX rev. 6)

Radiation-Tolerant High-Voltage ASIC Library Evaluation for Space Applications

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Abstract

This research and development project is performed for the Neosat project with Airbus DS as prime contractor and is under CNES contract, with ID-MOS partner for ASIC design

Increasing needs for low costs, low space occupancy and reduced weight in the space industry have made ASIC integration of recurrent functions mandatory. Today, ASICs are mainly used for digital applications, but the use of mixed ASIC would increase the integration of the platform equipment that are designed and manufactured by Astrium Elancourt. Such designs require an ASIC process having high voltage capabilities up to 100V. Airbus DS has selected with partners and CNES the XH035 HV process. A LV rad-tolerant digital library has already been designed under a previous contract. The aim of this activity is to develop a set of rad-tolerant High Voltage transistors and to test them against TID, SEL and SEB/SEGR.

I. INTRODUCTION

Airbus DS selected the XFAB XH035 mixed-signal technology for its modularity and high-voltage extensions. This technology targets automotive, telecommunication and power management markets; therefore it has been widely used and tested for various applications and is a mature technology. Furthermore, digital and mixed-signal ASICs for space applications have already been designed in this technology and their radiation tolerance has been tested but, to our knowledge, the high-voltage functionalities have never been used in this context.

The XH035 HV process mainly differs from the standard process by its deep epitaxial layer and a thick gate oxide..

The rad-tolerant library has already been designed for the XH035 standard LV process by IDMOS under a previous CNES contract. This library has been tested against TID and SEL and could be re-used with the XH035-HV process since the design rules are the same for the low voltage structure. But the change of the epitaxial layer leads to re-run the TID and SEL tests using the same test vehicle with the HV process to check whether the electrical performance, the SEL insensitivity and the TID characteristics are still acceptable.

The tasks performed in this contract are the following:

- Design a rad-tolerant library of HV N and P transistors, with protection pads, and isolated logic cells.
- Design a test vehicle (#2) to test the HV structures against TID and SEL
- Design a test vehicle (#3) to test the HV structures against SEB and SEGR
- Implement the test vehicle (#1) already designed for the low voltage digital library on the HV process
- Manufacture the 3 test vehicles
- Perform assembly of the 3 test vehicles
- Perform the TID tests on #1 and #2 vehicles
- Perform the SEL/SEE tests on #1 and #2 vehicles
- Perform the SEB/SEGR test on #3 vehicle
- Analyze and synthetize the results
- Prepare next phase

II. MATERIAL AND METHODS

A. Design of the HV transistors and cells

To fulfil Airbus DS needs, a HV radiation-tolerant library has been designed. Its target is to be functional and characterized up to 100 krads.

22 N and P transistors have been selected in XFAB library amongst the various types :

- 14 NMOS (nmos, nha, nmva, nhv, ngmmv, ndha, nmosia, ndhc, ndhe, ndhg, nhvg1, ndhc1, ndhe1,ndhg1)
- 8 PMOS (pmos, pmva, phv, pgmmv, pmosia, phvb, phvd, phvf)

These transistors have been hardened using an enclosed layout (ELT) and guard rings. Structures have also been used to break leakage paths. Although the medium gate oxide should be less sensitive than the thick gate oxide against TID effect, the thick gate oxide has been chosen due to its better expected immunity to SEGR (Single Event Gate Rupture).

Other structures have been designed and hardened:

- Power output buffers (18 V, 45 V, 70V, 90 V), with 100 mA current capability, and associated driver
- Logic isolated basic cells (Not, Nand gates, etc…),
- Logic isolated structures (Ring Oscillator),
- PADs (HV and LV PADs),

B. Description of the test vehicles

1) Test Vehicle #1 – High Voltage Structure

Test Vehicle #1 has been previously designed to test the low voltage logic elements of the XH035 standard process. It is

unchanged except that the wafer has a deep epitaxial layer. It contains mainly digital elements (Input & Output pads and cells). In order to have a reference, a counter and an oscillator are implemented both in tolerant and non-tolerant version. An unhardened E2PROM is also implemented (only the charge pump is hardened).

2) Test Vehicle #2 – High Voltage Structure

Test vehicle #2 is mainly composed of high voltage and/or isolated transistors hardened against radiations.
The package is a PGA 256 and die size is 8.7mm x 8.5mm.
Some transistors can be connected via bonding and pins for TID and SEL tests. But others will only be accessible by internal test points for measurements using probes. These transistors will be used at a later development stage to create the transistor models for analog simulation of TID-induced drifts.

3) Test Vehicle #3 – High Voltage dedicated to SEB SEGR

The test vehicle n°3 is only composed of high voltage and/or isolated transistors hardened against radiations. It is dedicated to the SEB/SEGR test. It contains mainly a block of transistors in the center of the die at about 1 mm from the pads. This geometry allows focusing the particles on the transistors and not the pads.

C. *Description of the tests*

The Total dose tests have been carried out with a Cobalt 60 source on 6 test vehicles #1 and #2 up to 100 krads at a low dose rate of 310 rad/h. An annealing of 24h/25°C plus 168 h/100°C has been performed.

The SEL tests have been performed on test vehicle #1 and #2 at RADEF (Jyväskylä, Finland) using Xenon ions with energy of 1217 MeV and a LET on die surface of 60 MeV.cm²/mg at a temperature of 125°C.

The SEB/SEGR tests have been performed using test vehicle #3 at RADEF (Jyväskylä, Finland). Krypton ions with a LET of 37 MeV.cm²/mg and Xenon ions with a LET on die surface of 65 MeV.cm²/mg have been selected. The SOA (Safe Operating Area) has been measured using [1 and 2]. SEGR has been characterized with PIGS (Post irradiation Gate Stress) method.

III. Results

A. *Test Vehicle #1 – Low voltage Logic*

TID tests have shown no functional or parametric problems up to 100 krads on hardened structures. The non-RT E2PROM fails in read at 14 krads for biased parts and 30 krads for unbiased parts. The non-hardened oscillator and counter experience an important increase of their supply current.

No SEL has been detected on the Rad-Tolerant cells.
SELs were observed on the non-hardened counter, the non-hardened oscillator and the non-hardened E2PROM. It justifies the necessity to implement protections against SEL.

A. *Test Vehicle #2 – High Voltage Structure*

The PMOS HV transistors keep their electrical characteristics up to 100 krads.

The NMOS HV transistors have a behaviour that depends on their design. The hardened NMOS NDHE NDHG NDHG1 have a deep change in their characteristics at 10 krads, the leakage current is increased by 10^5, these transistors cannot be switched off any more. The other hardened NMOS transistors have a better behaviour and can be used up to 100 krads.

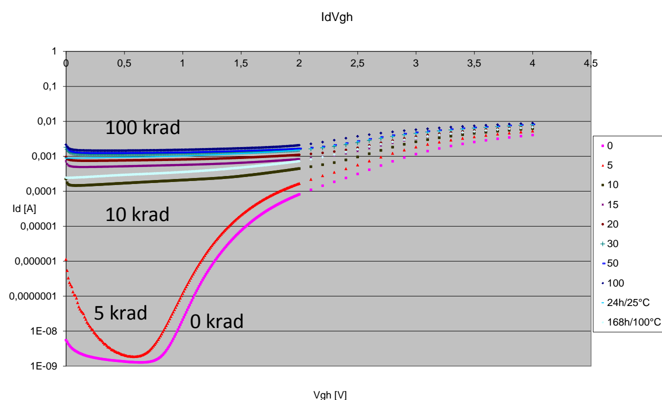

Figure 1 : NDHE HV NMOS losing its switching-off capability at 10 krads

The HV output buffers exhibit an increase of their rise time of about 20% at 15 krads because their design include sensitive N transistors.

No SEL has been detected on test vehicle #2. The HV transistors are correctly protected against latch-up.

B. *Test Vehicle 3 – High Voltage for SEB SEGR*

Since this is an ASIC technology, overblocking is not possible and SEGR was characterized at V_{GS}=0V for NMOS and max rating for PMOS.
N-Channel MOSFETs are sensitive to SEB and SEGR. Even for small voltages the SOA is smaller than VDS max. The highest safe rating is 72V for a 100V NMOS transistor.
P-Channel MOSFETs are sensitive to SEGR, but transistors below 45V are immune. The highest safe rating is 45V for a 45V PMOS transistor.
Pads are sensitive neither to SEB nor to SEGR.
The results are provided in Figure 2. In order to be in agreement with Radiation Hardness Assurance requirements, only the SOA obtained with heavy ions having LET ≈ 38 MeV.cm²/mg is displayed here.

Device IM466A3			Kr (38 MeV)
Device type	Max Voltage (V)	tested devices	SOA (V)
N MOSFET	100	Nhvg1	**72**
	90	Ndhg	**40**
		Ndhg1	**40**
	70	Ndhe	**37**
		Ndhe1	**62**
	45	Ndha	**17**
		Ndhc	**22**
		Ndhc1	**45**
		Nhv	**22**
	18	Nmva	**18**
	14	Ngmmv	**14**
P MOSFET	90	Phvf	**40**
		Phvf_std	**40**
	70	Phvd	**45**
	45	Phvb	**45**
	40	Phv	**40**
	18	Pmva	**18**
	14	Pgmmv	**14**
Pad	92	Hvp11	**92**
	90	Hvdd12	**90**
	50	Hvdd7	**50**
		Hvp6neia	**50**

Figure 2 : SOA of HV transistors and pads

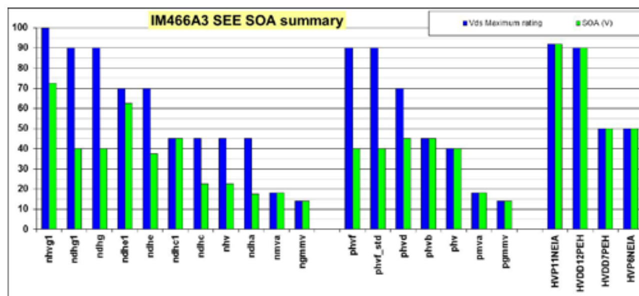

Figure 3 : Summary of SOA of HV transistors and pads

IV. CONCLUSION

This project has succeeded in designing radiation tolerant high voltage transistors and in characterizing them against TID, SEL and SEB/SEGR. A very good behaviour has been obtained for most of them against TID. No SEL has been detected. PMOS have a good protection against SEGR up to 45V. NMOS are sensitive to SEB and a higher design margin will have to be applied for them.

In the next phase, the transistors will be electrically characterized to generate the DK and the PDK.

V. REFERENCES

[1] Single event effects test method and guidelines ESA/SCC basic specification N°25100 Iss 1, oct 95

[2] Single Event Burnout and Single Event Gate Rupture, MIL-STD-750E, Method 1080

180nm CMOS Mixed-Signal Radiation Hard Library as base for a full ASIC supply chain

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Abstract

In recent years the importance of mixed-signal ASIC supply for Space Applications in Europe has grown. Along with this perception, customers like to see Europe getting more independent from other worldwide sources in obtaining these components on the market. Following the newest trends, IMST is currently working together with TESAT Spacecom towards a mixed-signal library as part of an ESCC qualified ASIC supply chain.

This paper presents the IP blocks of IMST, which are developed using innovative design and radiation hardened techniques. These blocks are going to go through a program of evaluation and qualification tests. The radiation hardened library of IMST, called HARD Library (HARD= Hard Against Radiation Design) is built from I/O cells for 3.3V and 5.0V supply voltages, reconfigurable multifunctional operational amplifier, voltage and current references, memory cells, data converters and other analog and digital IP blocks, which will be described in this paper. The HARD Library is based on the 180nm CMOS technology from XFAB, which is a modular mixed signal high voltage technology. It supports operation by negative supplies, which is one of the characteristics of the HARD Library elements. Another feature of this technology is offering different modules for low power, high temperature, high voltage and non volatile memory all in one platform. XFAB's 180nm CMOS technology is already tested with good results against radiation effects.

Furthermore, in this paper different scenarios of design flows will be presented, about how a customer can use the HARD Library. Since the project is still in progress, evaluation test results are not available yet. Finally the paper will show IMST´s capability to operate as a supplier for full space qualified ASICs to the market, handling the full supply chain in one hand.

I. PREFACE

The development of the radiation hardened library for mixed-signal ASICs is a German Government funded project by DLR. The aim of the project is for IMST to earn the status of capability approval under the ESCC system as a manufacturer for space qualified RadHard ASICs.

In a pre-study TESAT Spacecom commissioned IMST to investigate a proper CMOS semiconductor technology for the following work on the capability approval. In this study the XFAB's XH018 process has been selected as best suited for this purpose. Radiation tests have been performed on components and test circuits to find out SE effect sensitivities and TID behavior. This information has been used for the design of the presented HARD library.

II. HARD LIBRARY ELEMENTS

As the main aim is to develop a "state of the art" Mixed Signal ASIC for space applications, the library elements are selected in such way, that they are able to provide a full set of useful circuit blocks, which are needed to build up a wide range of different ASICs.

For the design radiation hardened IP blocks, several mitigation techniques are considered in the analog designed circuits to minimize SEE and TID effects. One layout technique to reduce SET effects in differential circuits is called "Differential Charge Cancellation" DDC proposed in [2]. The orientation of the transistor arrays is done in that way, that a SE strike affects both paths in the differential signal resulting in a common mode pulse. Due to the common mode rejection of differential circuits the pulse will be suppressed and has minor effects on the differential signal.

Circuit topologies to minimize SET effects in single ended circuit like biasing networks are described in [3]. Sensitive nodes are stabilized against transient signals induced by a SE strike. The technique is called "Sensitive Node Active Charge Cancellation", SNACC. Another mitigation technique is filtering analogue signals, as described in [1]

An example for TID effect reduction is "Dynamic Base Leakage Compensation", DBLC, that can be used in band gap circuits to protect the sensitive bipolar transistors against leakage current variation [4].

For digital designs like SPI controller and the state machine for RAM control radiation hardening has been realized by triple mode redundancy TMR [1].

The following list gives an overview of the library elements with their key features and status of design:

IP Block	Main Characteristics	Status
4-Wire SPI Interface	1.8V, 16 registers, 12 bit, each	Silicon/ testing
I/O Cells	3.3V & 5.0V digital + Analog I/O	Silicon/ testing
LVDS Driver	1.8V, Fmax=800MHz	Silicon/ testing
LVDS Receiver	1.8V and 3.3V, Fmax=800MHz	Silicon/ testing
Reconfigurable Multifunctional Operational Amplifier	•Inverting OpAmp with variable gain: -10 dB … +30 dB; 1dB step size •Non inverting OpAmp with variable gain: -10 dB … +30 dB; 1dB step size •Low Pass Filter (LPF); 3 different cut off frequencies •Current to Voltage Converter with different input ranges •Schmitt Trigger with adjustable hysteresis •Voltage buffer	Silicon/ testing

IP Block	Main Characteristics	Status
Bandgaps	1.8V & 3.3V trimable	Silicon/ testing
Reference Bias Generators	1.8V & 3.3V with PTAT and constant currents & adjustable voltage references	Silicon/ testing
Temperature sensor	1.8V, temperature range from -40°C…+150°C	Silicon/ testing
POR Generator	POR delay: 5µs	Silicon/ testing
LDO	Input voltage: 3.3V Output Voltage: 1.8V with adjustable short protection	Silicon/ testing
Level shifter High-Low	input signals with 0V…1.8V output signals with -5V…-3.2V	Silicon/ testing
Level shifter Low-High	input signals with -5V…-3.2V output signals with 0V…1.8V	Silicon/ testing
Digital Level shifter High-Low	3.3V-1.8V	Silicon/ testing
Digital Level shifter Low- High	1.8V - 3.3V	Silicon/ testing
16bit MUX	Max. signal frequency: 800MHz	Silicon/ testing
11 bit ADC	charge-scaling SAR ADC fast mode: 200KS/s	Silicon/ testing
Memory cell	256x10 bit RAM module Clock frequency: 25MHz.	Silicon/ testing
12 bit DAC	segmented current steering DAC	Silicon/ testing
Memory cell	OTP	Future design
Serializer / Deserializer	Data Rates: 600 Mbps with a reference clock Power: <500 mW	Future design
Clock PLL with integrated VCO	output clock frequency range: CMOS = 6 MHz … 300 MHz LVDS = 12.25 MHz…600 MHz period jitter: 50ps (PK-PK)	Design
DCXO	Supports 6 MHz … 50 MHz crystals	Design

Table 1: Summary of HARD library elements

4-wire SPI interface

The SPI interface consists out of two sub-modules. The serial interface module is the communication interface to the external master. The register module stores the received data from the serial interface and provides readable register content to the serial interface. One serial interface module can be connected to two register modules. This modular approach makes it possible to store 8 or 16 registers with a width of 12 bit.

I/O cells

Several 3.3V digital I/O cells, with different driver capability, are provided by the HARD Library. All of them provide separated supply voltage domains for the 3.3V I/O, the 3.3V intermediate buffer and the 1.8V chip core.

One dedicated 5V digital I/O cell is provided by the HARD Library. It provides separated supply voltage domains for the 5V I/O, the 5V intermediate buffer and the 1.8V chip core

The HARD Library also provides an analog I/O pad with serial low resistances and ESD structures to supply and ground rails

LVDS Interfaces

For digital high speed interfaces outside the chip, LVDS receivers and drivers are designed with a wide range of common mode voltage and supply variations to cover various applications. Both, the LVDS driver and LVDS receiver circuits, contain configurable termination resistors (100Ω) for a maximum flexibility of possible applications.

Analog to Digital Converter

The provided SAR-ADC is a charge-scaling type ADC with binary weighted capacitor arrays as DAC. The ADC is optimized for low-power. Two modes are available: a default low power mode, for slower conversion (up to 100kS/s) and a high-speed mode (up to 200kS/s) where the power is approximately doubled.

Operational Amplifier

The operational amplifier (OpAmp) provided in the HARD Library is an universal circuitry with 3.3V rail to rail input/ output stage. Optionally a negative supply voltage can be applied to the ground node to work on a +/- supply. Reconfigurable circuitry is added to the OpAmp core to obtain an inverting and non-inverting amplifier with a voltage gain range from -10dB up to +30 dB in 1dB steps. A low pass filter with three cut off frequencies at 0.1 MHz, 1 MHz and 10 MHz is another function. Furthermore a I to V converter with different transimpedances, a Schmitt Trigger with controllable hysteresis and a voltage buffer is selectable.

Level shifter

The digital level shifter (LH) element converts digital input signals from the core voltage domain (VDD=1.8V) to output voltages in the 3.3V supply voltage domain and in the other way around (HL) it converts digital input signals from the I/O voltage domain (VDDO=3.3V) to core voltage domain (VDD=1.8V).

LDO

The LDO works in a source follower configuration with a NMOS transistor as pass device. A short circuit protection circuit will switch off the LDO as soon as a selected current range is exceeded.

Analog MUX

The test MUX is a 16 to 1 MUX which is build up using cascaded transmission gates. A logic is included to select one of the 16 inputs to be connected to the output. The internal control voltages of the transmission gates use the 3.3V supply rail and therefore can handle analog voltages from 0V to 3.3V.

Digital to Analog Converter

The provided Digital to Analog Converter is a 12 bit segmented current steering DAC.

The DAC output is a differential voltage, which is proportional to the DAC input voltage. The input voltage can either be provided by the internal band gap or by an external constant voltage. The input voltage is converted into an input current. In order to achieve the 12 bit resolution, this input current is calibrated to set the gain of the DAC within the correct range. The DAC output voltage is buffered by a differential amplifier.

RAM

Aim of the RAMTEST module is to save a 10 Bit width word within any of the 256 addresses and recognise radiation effects on the stored data. Due to the Dual-Port feature of the RAM it is possible to write/read simultaneously two RAM addresses.

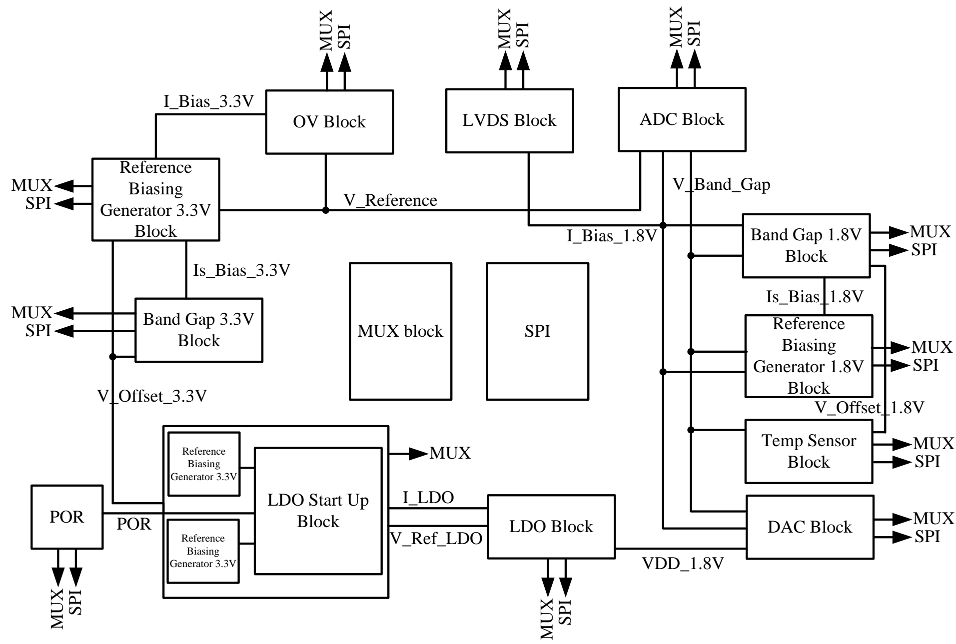

Figure 1: Block diagram of Test Chain

III. SEE and TID tests

A. Test Chip

In the current stage of the project, a test chip for evaluation has been designed, containing all library elements for single measurement. In order to investigate the interaction of the circuit blocks with each other, a test chain has also been placed on the test chip with test points on all interfaces. Figure 1 shows the block diagram of this test chain. The 3.3V and 1.8V domains are working with each other with internal level shifter. Figure 2 shows the floor plan of the produced die with markers to identify each of the circuit blocks. The test chip is packaged in a ceramic package with 132 pins.

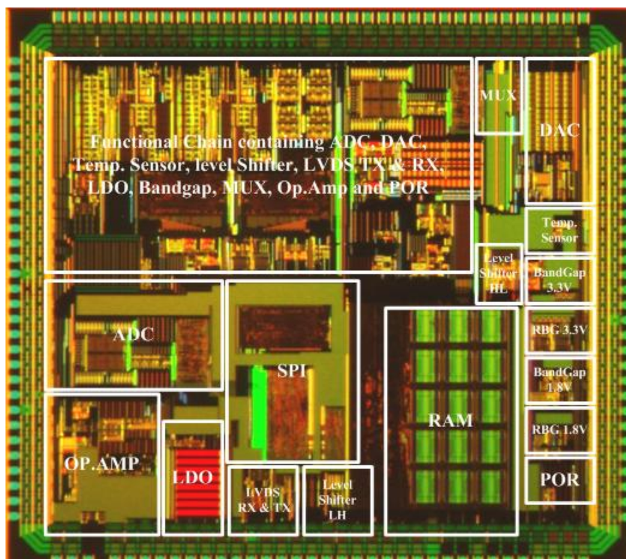

Figure 2: Photo of the Test Chip

B. SEE test

The SEE test is taking place at the CYCLONE110 facility on the Cyclon Resource Centre Louvain-la-Neuve. For the SEE testing a PCB has been designed with special ability to monitor SEL, SET and SEU. The board is shown in Figure 3. On the main board 4 DUTs are mounted and in the lower side the latch up protection is to be seen. Hidden under the adapter board, multiple comparators are used to detect and count SET pulses on each analog block. The adapter board has I/O multiplexers with relays to route all chip pins to SMA connectors. A FPGA board is used to control the chip setting and PCB setting during irradiation with heavy ions.

SEL monitoring: The supply current on each circuit block is monitored and can be switched off (Latch Up protection), when reaching a predefined limit, which is set to approx. 100% higher current as typical operating mode current. While switching off the supply, a flag, which corresponds to this SEL, is sent to the FPGA board, that stores the event for later evaluation.

SEU monitoring: Only digital circuits can be tested for SEU. The SPI controller is repeatedly writing a test pattern, which is read back and compared with the original sent pattern. On the ADC test, outputs are continuously written out, without changing the input, in order to monitor any upsets. The RAM model is hardened by TMR techniques. For SEU tests of the RAM block, a special build in self test is designed. The state machine writes consecutively different test patterns into all memory cells and compares the read result directly after it. During erroneous data read several read attempts are done. Therefore the algorithm is able to distinguish between errors in the memory cell and errors during the read/write process. Further on, the algorithm is also able to determine in which TMR line this error occurs.

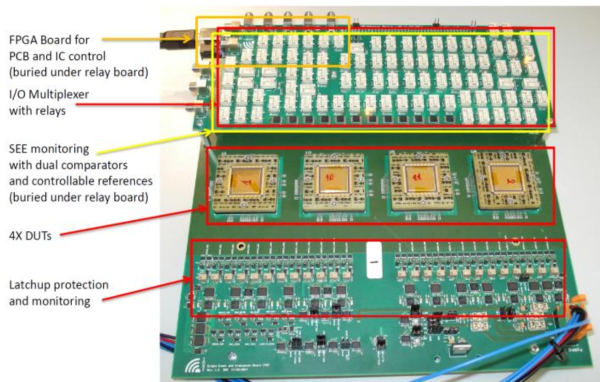

Figure 3: SEE and EV test board

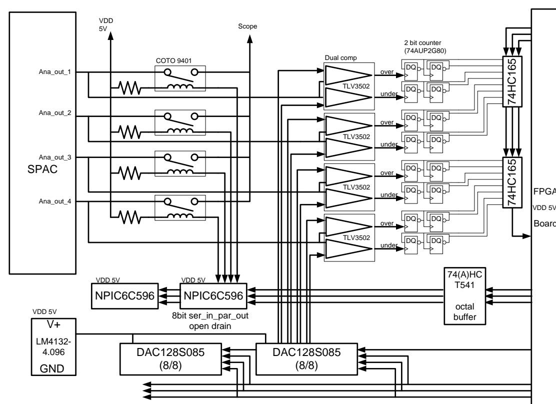

Figure 4: SET test concept

In case of an SEU an error output frame word is sent out with detailed information on the error location and if an error has been corrected or not using the TMR structure.

SET monitoring: Figure 4 shows the concept of monitoring the SET effects. All single circuit blocks have outputs routed to a dual comparator. The reference voltage of the comparator can be controlled in mV steps by a DAC output individually for each comparator. With this approach two threshold levels can be set: One threshold level some mV below the DC signal level and one threshold level some mV above it, in order to detect SET. The comparator outputs are routed to counters and their values are stored into the FPGA. For a qualitative evaluation of the SET signals, each output can be multiplexed to an oscilloscope, that is able to save screenshots, whenever a SET triggers the oscilloscope.

C. TID test

Figure 5 shows the TID test board together with the supply board. The supply board contains a FPGA board to generate stimulus files for the IC during irradiation like clock signals for the data converter or LVDS signals. A special GUI and a test sequence are programmed in MATLAB to set the chip and evaluation board settings, in order to evaluate and measure the test chip before and after the Total Ionizing Dose test as well as during the irradiation breaks.

The same board is used for the screening and burn in.

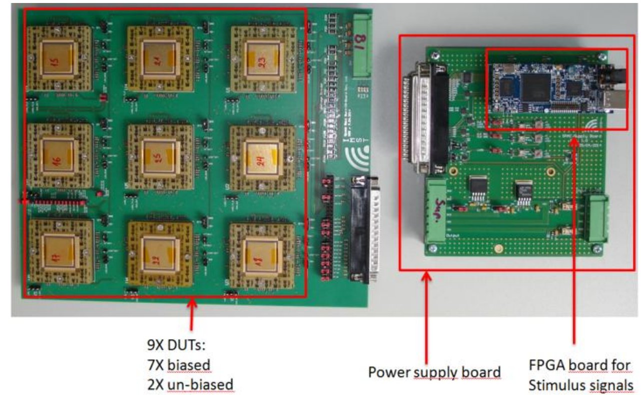

Figure 5: TID test board and supply board

IV. Measurement results

Since the project is still in progress and the radiation test are scheduled for this year, measurement results of the test chip will be presented at a later point. These results will be used to enhance the performance of the actually space qualified developed ASIC at the end of the project.

V. ASIC supply chain and Design Flow

Designing ASICs usually requires a close collaboration between the customer who is using the ASIC in his application and the design house. Having the Capability Approval status, IMST is able to design and deliver space qualified ASICs, without needing for every developed ASIC new, long lasting and expensive evaluating and qualifying test procedures. Having this status, IMST is able to offer variation, inside its defined capability domain, according to the customer's needs and assure a qualified manufacturing procedure and screening of the product. IMST is using its HARD library elements based on a customer's specification and offers different business models for delivering the agreed ASIC, always according to the European standards and rules. Table 2 shows typical design steps from the specification to the RadHard ASIC delivery for three different business cases: Turn-key, Interactive and IP licence case.

In the turn key design, IMST takes over the ASIC Flow and deliver tested and qualified RadHard ASICs based on customer specification.

In the interactive design, IMST and the customer are co-designing the ASIC. IMST is responsible for the final layout and tape in and delivers tested and qualified RadHard ASICs. Table 2 (black path) shows the different interactive steps which can be executed either by IMST or the customer.

For the IP license case, IMST can offer IP license of dedicated circuit blocks to the end-customer. The customer will get simulation models of the IP blocks and X-FAB will place the layouts of the IP's as part of the tape-in procedure. In this case, IMST will not produce the tested and qualified RadHard ASICs. Only wafers will be delivered by X-FAB.

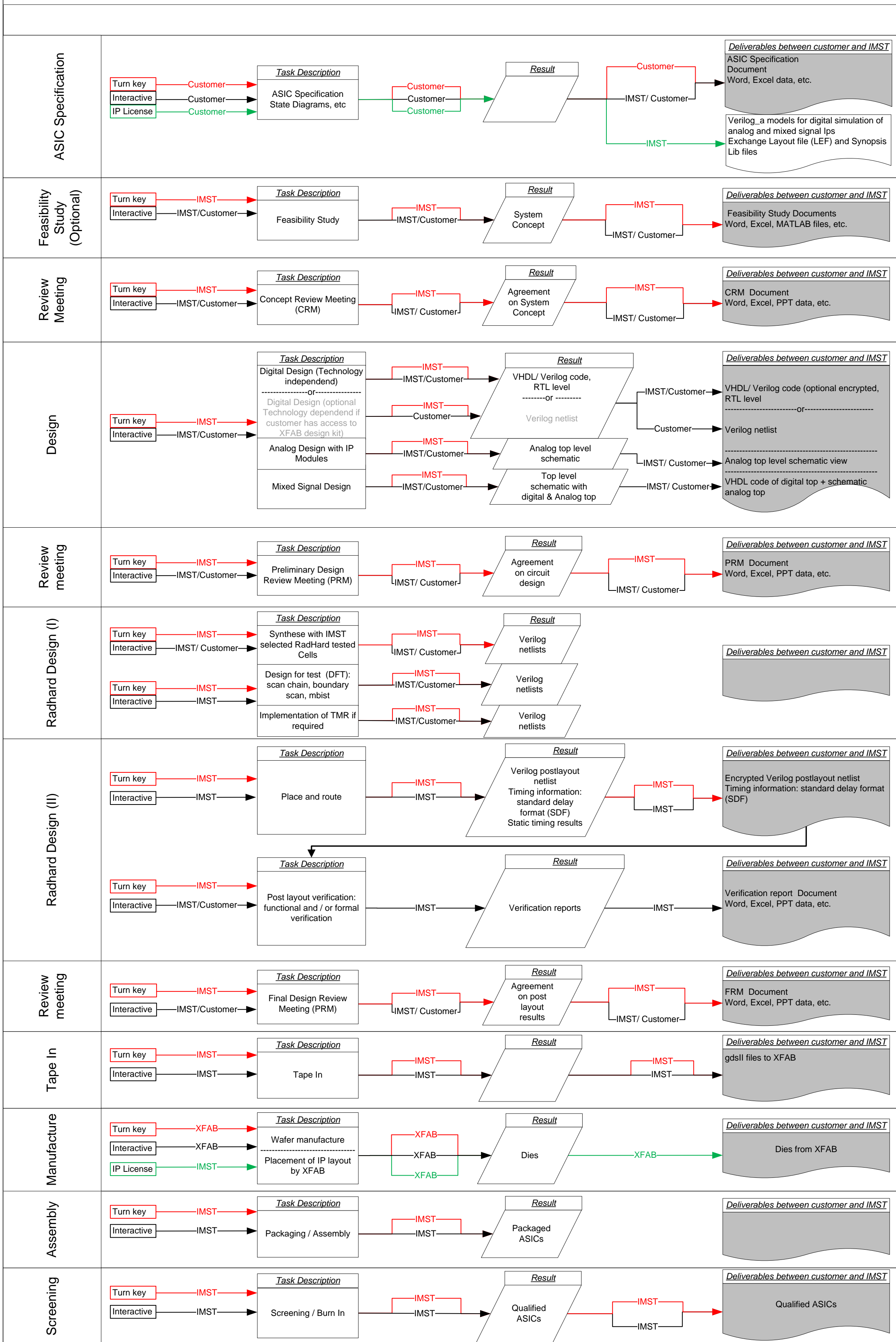

Table 2: Supply Chain Scenarios

VI. CONCLUSION

A set of radiation hardened analog and mixed-signal IP's are presented to be used within an ASIC supply chain. For customers, different scenarios are shown, on how they can interface with IMST and interact in the design of the ASIC. Building up this supply chain, finishing the design and tests of the HARD library and getting the ESCC approval is the aim of the funded project by DLR. The planned finish of the project is in Summer of 2016.

VII. REFERENCES

[1] ESA Requirements and Standards Division. Space engineering, product assurance. Techniques for Radiation effects. Mitigation in ASICs and FPGAs. 2009 © ESA for the members of ECSS

[2] Raymond W. Blaine, Nicholas M. Atkinson and more. A Single-Event-Hardened CMOS Operational Amplifier Design. RADECS 2011 Proceedings-B-2

[3] R. W. Blaine, S. E. Armstrong and more. RHBD Bias Circuits Utilizing Sensitive Node Active Charge Cancellation. IEEE Transaction on nuclear science, Vol. 58, No. 6, December 2011

[4] Ying Cao, Wounter De Cock, Michiel Steyaert and Paul Leroux. A 4.5 MGy TID-Tolerant CMOS Bandgap Reference ircuit Using a Dynamic Base Leakage Compensation Technique. IEEE Transaction on nuclear science, Vol. 60, No. 4, August 2013

DARE180X: A 0.18µm mixed-signal radiation-hardened library for low-power applications

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Abstract

DARE180X is a mixed-signal library solution for radiation applications implemented in the low-power 0.18 µm commercial technology from XFAB. This set of libraries comprising core standard cells, digital and analog I/O cells, analog IP and SRAM memory blocks is currently being developed using a guard-ring shielding approach to guarantee TID tolerance higher than 100 krad as well as SEL hardening for LET values higher than 60 MeV/cm^2.mg.

The DARE180X core library aims to offer good SEE hardening and low-power consumption capabilities by combining high density standard cells with SET hardened-by-drive-strength combinational cells and SEU hardened-by-design sequential cells. The DARE180X libraries also include a broad list of digital and analog I/O cells as well as several radiation-hardened analog IP blocks such as bandgap, ADC, DAC, PLL, etc.

This paper details the development of the DARE180X library and analyses its features and simulation results. A comprehensive comparison with the existing DARE180 library solution implemented in the UMC 0.18 µm technology is also presented.

I. Introduction

Harsh radiation environments constitute an essential challenge for space applications. Pervasive particles from cosmic rays induce cumulative and transient effects that can cause soft errors or even permanent damage in electronics circuits.

Mixed-signal integrated circuits implemented in deep submicron commercial technologies have already been qualified as a cost efficient solution for satellites and radiation applications [1]. Besides the low cost, these thin gate oxide technologies are inherently hardened against total ionizing dose (TID) and offer high speed, low power consumption and high yield.

Although commercial libraries are largely available they often present high single event latch-up (SEL) sensitivity when used in mixed-signal ICs. On the other hand, radiation hardened libraries are designed using special layout techniques to cope with such issues and still provide high density and low power consumption. As well, system designers can use these libraries within their traditional standard cell design flow.

The existing DARE180 library solution implemented in UMC 0.18 µm technology has already been validated in several space applications [2][3]. DARE180 was designed for general radiation systems and offers a very high TID tolerance at the cost of higher power consumption and lower gate density than commercial libraries.

The new DARE180X library platform aims to provide a solution tailored for space applications that require TID tolerance higher than 100 krad while keeping power consumption and gate density closer to the commercial libraries. Similarly to its UMC-based counterpart, DARE180X includes blocks specially designed to mitigate various single event effects (SEE).

II. Microelectronics Platform

The DARE180X libraries are part of a mixed-signal microelectronics platform that will deliver digital libraries, analog IP and memory blocks suitable for radiation hardened applications.

The 0.18 µm CMOS technology (XH018) from XFAB was selected because it provides high voltage devices and non-volatile memory blocks that may be interesting for a wide range of applications. This technology features triple-well junction isolation and transistor devices with different voltage thresholds.

A. DARE180X libraries

The DARE180X libraries are implemented using the junction-isolated low-power devices available in the XH018 technology. Junction isolation is used to improve SEL immunity in mixed-signal applications whereas high-Vt low-power devices are used to reduce leakage power consumption.

1) Digital core library

The digital core library comprises numerous combinational cells, SET-hardened cells and SEU-hardened sequential cells. All cells are designed to offer good SEL hardening in a very compact standard cell template. General library figures are listed in Table 1.

Several combinational functions and drive-strength variants are available to allow designers to synthesize and optimize their digital designs. These cells are intentionally not hardened against single event transient (SET) and should be

used in non-critical logic circuitry where low linear energy transfer (LET) thresholds are acceptable.

Table 1: DARE180X core library figures

Parameter	Value
Number of cells	86
Raw gate density	59 kGates/mm^2
Averaged cell area	127 µm^2
Horizontal pitch	0.62 µm
Vertical pitch	0.62 µm
Cell height	11 tracks

Critical logic paths such as set/reset and clock trees can be implemented using special SET-hardened cells available in the library. These cells are designed to withstand LET values of at least 60 MeV.cm^2/mg.

All the flip-flops and latches available in the core library were designed to be immune to single event upsets (SEU) due to LET values higher than 60 MeV.cm^2/mg. Since set/reset and clock trees are supposed to be implemented with the SET-hardened cells the SEU-hardened sequential cells were not designed to be immune to SET at their inputs. For this reason, flip-flops featuring SET filters at their data inputs are also included in the library.

The core library also includes several place & route cells such as filler cells, decap cells, tie cells and antenna cells.

2) I/O library

The I/O library includes several digital and analog pad-limited I/O cells. As in the core library, all I/O cells are hardened against SEL effects. Digital input I/O cells are also hardened against SET to prevent events from propagating to the core logic.

An extensive list of tri-state output, bidirectional and 5V-tolerant bidirectional I/O cells with different driving capabilities is available. The library includes fast slew-rate and slew-rate controlled versions of these I/O cells.

Power and ground I/O cells as well as breaker cells are available for the definition of multiple I/O power domains. Besides regular 3.3V analog I/O cells the library also includes high-voltage supply and I/O cells to be used with high-voltage blocks.

3) SRAM blocks

A set of five dual-port SRAM memory blocks is available in the DARE180X platform. The basic memory cell uses straight transistors and it is optimized for area and power consumption.

The memory blocks are designed to be insensitive to multi-bit upsets (MBU). This is achieved by arranging the bits of a same word far enough from each other. In this case every two bits of a same word are separated by 16 bits which corresponds to an interleaving distance higher than 60 µm. This way an error detection and correction circuit (EDAC) can be used to mitigate soft errors due to single-bit upsets (SBU) [4].

4) Analog blocks

Table 2 lists the most important analog blocks currently in design phase.

Table 2: Available analog cells

IP block	Supply	Provider	Status
PLL, 120MHz	1.8V	ICsense	Design
Bandgap	3.3V	ICsense	Design
Bandgap Low Power	3.3V	ICsense	Design
PoR / UVLO	3.3V	ICsense	Design
Relaxation Oscillator 100kHz (R/C)	1.8V	ICsense	Design
12b DAC 3.75MS/s	3.3V	ICsense	Design
13b ADC 1MS/s	1.8V / 3.3V	ICsense	Design
Linear Regulator 1.8V, 36mA	3.3V	ICsense	Design
HV Linear Regulator, Vout 3.3V	[4 – 16.5] V	ICsense	Design

a) Bandgap reference voltage

The bandgap reference can be considered the most critical analog block because it serves as a reference to all other analog cells. A large spike or bump on this reference voltage will translate into a decrease of analog performance and can be potentially harmful to the ASIC (e.g. over-voltage in case of an LDO).

The bandgap reference is made insensitive to SET by using techniques like for example the insertion of filtering caps and high current levels.

Table 3: Bandgap reference specifications

Parameter	Value
Reference voltage	1V ± 2%
Temp. drift	± 0.6%
Temp. drift (dig. comp.)	± 0.1%
SET hardening	60 MeV/mg/cm^2

b) 13b ADC 1 MS/s

A 13b cyclic ADC has been developed together with a passive sample-and-hold structure and a 16-channel multiplexer. The ADC is capable of measuring both single-ended and differential signals.

The ADC is designed to recover fast from SET events in order to have only a single sample affected. This affected sample can be easily filtered by digital post-processing.

Table 4: 13b ADC specifications

Parameter	Value
Resolution	13b
Data rate	1 MS/s
Input range SE	[0 – 2.5] V
Input range DIFF	$\pm 1.25V_{diff,ptp}$
DNL	1 LSB
INL SE *(better in DIFF)*	6 LSB

c) 12b DAC

A monotonic 12b PMOS current DAC has been developed. Several techniques are used to minimize artifacts from non-uniform ageing and TID drifts.

Table 5: 12b DAC specifications

Parameter	Value
Resolution	12b
Output range	[0 – 4] mA
DNL	< 1 LSB
INL	3 LSB

d) 120 MHz PLL

A 120 MHz PLL is realized completely on-chip. SET-hardening techniques are used to create a very stable clock-period and duty-cycle.

Table 6: PLL specifications

Parameter	Value
Fout	[100 – 120] MHz
Fin	100 kHz
LPF cut-off	7 kHz
PLL order	3rd
Fout max. deviation during SET (peak)	±10%
SET hardening	60 MeV/mg/cm^2

e) 100 kHz Relaxation Oscillator

The implemented relaxation oscillator uses external components (R and C). A special topology is chosen for low jitter and temperature drift. In fact the temperature drift is dominated by the external components. The oscillator is hardened against SET.

Table 7: 100 KHz oscillator specifications

Parameter	Value
Fout	100 kHz
Temp. drift	< 5000 ppm
Temp. drift with ideal external components	< 1000 ppm

B. Radiation hardening by design methodology

1) TID & SEL hardening

All cells in the DARE180X libraries are designed to tolerate TID rates above 100 krad and to be immune to SEL under LET values higher than 60 Mev.cm^2/mg.

Thin gate oxide technologies already offer good TID hardening for most space applications. Radiation tests have shown that basic straight transistors in the XH018 technology can tolerate TID rates of at least 100 krad. Higher TID hardening could eventually be achieved by using enclosed layout transistors (ELT) [5] at the cost of higher power consumption and lower area density.

Fully enclosing P+ guard-rings together with junction-isolated devices (triple-well) are used to guarantee very good SEL hardening [6]. These guard-rings also help to reduce the impact of TID as they isolate possible leakage paths between N+ diffusions at different potentials. An example of this layout approach is shown in Figure 1.

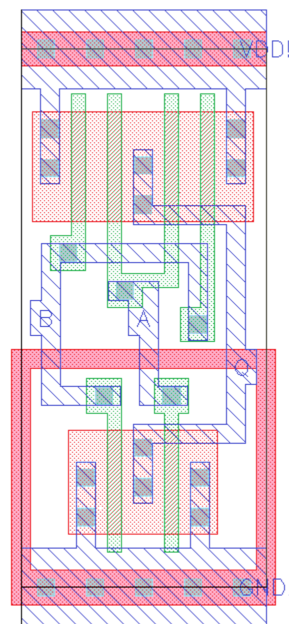

Figure 1: Guard-ring protections in core standard cell

2) SET-hardened cells

SET hardened cells were included in the library to be used in very critical paths such as set/reset and clock trees. These cells were hardened using a hardening-by-drive-strength approach where transistors are dimensioned to provide higher gate capacitance and driveability. Larger gate capacitances induce a higher critical charge on the driver's net whereas higher driveability increases the restoring strength on the driven net affected by a charge strike [7].

The hardening of a cell can be verified using charge injection simulations where critical charges corresponding to the desired LET threshold are individually injected on every cell node while the cell outputs are monitored for an event propagation. Every cell under test is connected to a load cell that matches the weakest flip-flop input stage in the library so that cell under test is considered hardened when no events propagate across this load cell. The charge injection in these simulations is modelled by a double-exponential current source [8].

3) SEU-hardened sequential cells

Flip-flops and latches are implemented using a Dual Interlocked Cell (DICE) architecture [9]. These SEU-hardened cells are based on redundant storage nodes and present very good SEU hardening.

C. DARE180XL core library

As already mentioned the XH018 technology features different flavours of transistors. The DARE180X libraries are implemented using the high-Vt low-power devices which provide low driveability and consequently higher SET

sensitivity. For this reason, a core library using low-Vt transistors (DARE180XL) was also implemented.

The DARE180XL core library contains the exact same cell set as the DARE180X one and the equivalent cells in both libraries have the exact same footprint, i.e. same size and pin placement. Moreover, the cells from both libraries are fully compatible and can be abutted in the same layout. These features provide designers with different alternatives for power and timing optimization.

Low-Vt devices offer twice the driveability of high-Vt transistors at the cost of higher leakage power consumption.

III. DARE180X and DARE180 Comparison

The UMC DARE180 library implementation focused on general radiation applications that could require very high TID tolerance, above 1 Mrad. This was possible with the use of ELT devices combined with guard-rings. The downside of using this kind of transistor in a standard cell library is that the smallest feasible device has an equivalent W/L five times bigger than the minimum W/L allowed in this technology.

Besides the area penalty, this limitation leads to high cell input capacitances in the whole library which cause synthesis tools to use cells with high drive-strengths. As well, multiple stage cells cannot be effectively optimized for optimal delay and low internal power consumption as the input stages are limited by this minimum W/L value. All these elements contribute to increase power consumption in end-user system designs.

On top of that, the ELT's outer diffusion is relatively larger than diffusion areas of a straight transistor with equivalent W/L which can lead to higher cross-section values in some cases. Even if LET threshold is the most important parameter to define the SET sensitivity of a cell, it is also important to consider the cross-section value which depends on the node's diffusion sensitive area and denotes the probability of a strike on the node.

1) Cell-level comparison

Table 8 compares a NAND gate between the UMC library and the two versions of the XFAB library. Similar comparison is presented for the NOR gate in Table 9. Timing performance is compared in terms of fanout-of-4 (FO4) which gives a valid comparison figure that takes into account the different input capacitances in each library.

Table 8: NAND2 cell comparison (typical corner)

	DARE180	**DARE180X**	**DARE180XL**
Cell name	NAND2	NA2JIX4	NA2JILVTX4
Relative drive strength	X1	X4	X4
LET threshold	35 MeV.cm^2/mg	17.5 MeV.cm^2/mg	35 MeV.cm^2/mg
Saturation cross-section	3.45 cm^2	0.86 cm^2	1.31 cm^2
Cell area	39.5 μm^2	29.6 μm^2	29.6 μm^2
Rise FO4 delay	90 ps	140 ps	81 ps
Fall FO4 delay	66 ps	95 ps	61 ps
Average input capacitance	15 fF	15 fF	14 fF
Average leakage	52.68 pW	3.76 pW	2306.98 pW

Table 9: NOR2 cell comparison (typical corner)

	DARE180	**DARE180X**	**DARE180XL**
Cell name	NOR2	NO2JIX4	NO2JILVTX4
Relative drive strength	X1	X4	X4
LET threshold	12.5 MeV.cm^2/mg	12.5 MeV.cm^2/mg	25 MeV.cm^2/mg
Saturation cross-section	0.58 cm^2	1.43 cm^2	1.43 cm^2
Cell area	28.2 μm^2	29.6 μm^2	29.6 μm^2
Rise FO4 delay	159 ps	152 ps	119 ps
Fall FO4 delay	58 ps	88 ps	60 ps
Average input capacitance	12 fF	16 fF	15 fF
Average leakage	42.85 pW	4.2 pW	2441.5 pW

In general, the X1 cells from the DARE180 library compare to the X4 cells from the new DARE180X and DARE180XL libraries in many aspects. The new libraries also offer weaker drive-strength variants that can be used for power and timing optimizations in system designs but a trade-off between power consumption and SET hardening exists. For instance, the low driveability of high-Vt low-power devices in the DARE180X core library result in worse timing performance and higher SET sensitivity.

Sequential cells in DARE180X libraries were implemented using DICE cells whereas the ones in DARE180 library were based on the Heavy Ion Tolerant (HIT) architecture [10]. Although both designs offer very good SEU-hardening, DICE cells present some advantages such as lower power consumption and easier implementation. The flip-flops and latches implemented in DARE180X are also slightly smaller than the ones available in DARE180.

2) System-level comparison

Cell-level comparisons may be useful to evaluate aspects intrinsic to the technologies such as speed and leakage but timing performance and power consumption in entire designs

depend also on library characteristics such as the number of functions and drive-strength variants available.

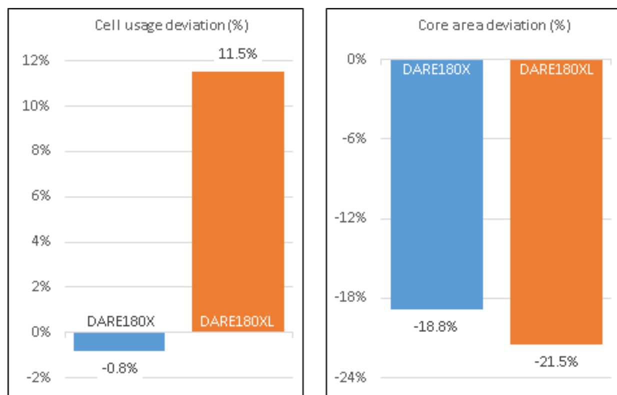

Figure 2: Synthesized design area variation from DARE180

A complex design was synthesized using the different core libraries in order to assess their efficiency regarding area and power consumption. Figure 2 and Figure 3 respectively show the synthesis and power analysis results achieved with the DARE180X libraries in terms of deviations from the results obtained with the DARE180 library.

As expected, both versions of the DARE180X core library are able to deliver better area and power consumption results. Even if leakage penalty with DARE180XL is high the total power consumption in absolute values is reduced.

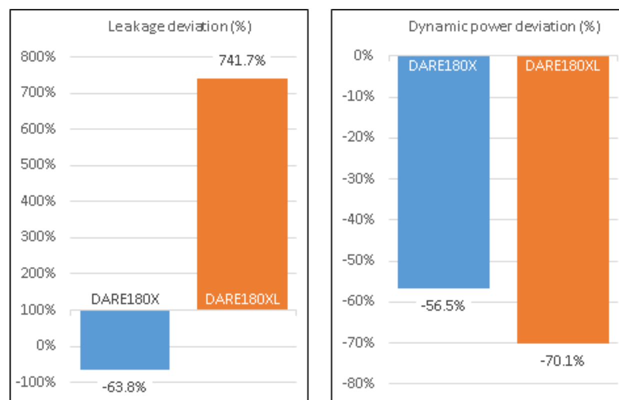

Figure 3: System-level power variation from DARE180

An overall comparison between DARE180 and DARE180X library sets is summarized in Table 10.

Table 10: Comparison summary of DARE180X vs. DARE180

	DARE180	DARE180X
Technology	UMC 0.18 µm	XFAB 0.18 µm (XH018)
Process	Mixed-mode/RF	Junction-isolated (triple-well)
Metal support	6 layers	6 layers
Core supply range	1.8 V ± 10%	1.8 V ± 10%
I/O supply range	3.3 V ± 10%	3.3 V ± 10%
Temperature range	-55 ºC to 125 ºC	-55 ºC to 125 ºC
TID tolerance	> 1 Mrad	> 100 krad
Transistor type	ELT	straight
Sequential cell hardening	HIT	DICE
Raw gate density	25 kGates/mm^2	59 kGates/mm^2
# core cells	130	86
# I/O cells	83	48
SRAM	Single-port/dual-port SRAM compiler	5 dual-port blocks available

IV. Further Work

Currently the SRAM and the analog blocks as well as the I/O library are being finalized. The complete DARE180X library platform is scheduled to be available by the end of June. A test chip is scheduled to be made after the official library release.

The test chip shall include test structures to assess the radiation hardening and verify the functionality of the different libraries elements.

V. Summary

This paper introduced the development of a new radiation-hardened library platform for mixed-signal space applications. A set of libraries including numerous core cells, I/O pads, SRAM blocks and analog circuits is being developed and will offer a complete solution for low-power applications that require TID tolerance above 100 krad.

These libraries are implemented in the 0.18 µm technology from XFAB which includes triple-well junction isolation and high-voltage devices. Different design and layout techniques are used to mitigate SEE and improve TID immunity.

The core library is available in both low-power and low-Vt versions which are compatible with each other. Cell-level and synthesis comparisons show that DARE180X core libraries are able to give better results in area and power consumption than the DARE180 core library.

The I/O library, SRAM and analog blocks are currently being designed and scheduled to be released in June. Further investigation on performance and radiation hardening of these new libraries is planned to be done through a test chip.

VI. REFERENCES

[1] S. Redant, R. Marec, L. Baguena, E. Liegeon, J. Soucarre, B. Van Thielen, G. Beeckman, P. Ribeiro, A. Fernandez-Leon, B. Glass. (2004, September). The Design Against Radiation Effects (DARE) Library. Presented at 5th RADECS Workshop.

[2] G. Thys, S. Redant, L. Folens, J. Tsouhlarakis. (2010, September). Mixed Signal Tolerant Design with DARE Library: KNUT. Presented at 3rd International Workshop on Analog and Mixed-Signal Integrated Circuits for Space Applications (AMICSA 2010).

[3] G. Thys, S. Redant, E. Geukens, Y. Geerts. (2012, August). Radiation Hardened Mixed-Signal IP with DARE Technology. Presented at 4th International Workshop on Analog and Mixed-Signal Integrated Circuits for Space Applications (AMICSA 2012).

[4] D. Radaelli, H. Puchner, S. Wong, S. Daniel. (2005, December). Investigation of Multi-Bit Upsets in a 15 nm Technology SRAM Device. IEEE Transactions on Nuclear Science. Vol. 52 (6), pp. 2433-2437.

[5] G. Anelli, M. Campbell, M. Delmastro, F. Faccio, S. Florian, A. Giraldo, E. Heijne, P. Jarron, K. Kloukinas, A. Marchioro, P. Moreira, W. Snoeys. (1999, December). Radiation Tolerant VLSI Circuits in Standard Deep Submicron CMOS Technologies for the LHC Experiments: Practical Design Aspects. IEEE Transactions on Nuclear Science. Vol. 46 (6), pp. 1690-1696.

[6] N.A. Dodds, N.C. Hooten, R.A. Reed, R.D. Schrimpf, J.H. Warner, N.J. Roche, D. McMorrow, S. Wen, R. Wong, J.F. Salzman, S. Jordan, J.A. Pellish, C.J. Marshall, N.J. Gaspard, W.G. Bennett, E.X. Zhang, B.L. Bhuva. (2012, December). Effectiveness of SEL Hardening Strategies and the Latchup Domino Effect. IEEE Transactions on Nuclear Science. Vol. 59 (6), pp. 2642-2650.

[7] Q. Zhou, K. Mohanram. (2004, April). Transistor Sizing for Radiation Hardening. Presented at 42nd IEEE International Reliability Physics Symposium.

[8] R. Garg, S.P. Khatri. (2010 edition). Analysis and Design of Resilient VLSI Circuits: Mitigating Soft Errors and Process Variations. Springer.

[9] T. Calin, M. Nicolaidis, R. Velazco. (1996, December). Upset Hardened Memory Design for Submicron CMOS Technology. IEEE Transactions on Nuclear Science. Vol. 43 (6), pp. 2874-2878.

[10] D. Bessot, R. Velazco. (1993, September). Design of SEU-hardened CMOS Memory Cells: the HIT Cell. Presented at 2nd European Conference on Radiation and its Effects on Components and Systems (RADECS 1993).

VII. ACKNOWLEDGEMENTS

The authors would like to thank ESA, imec, ICSense and Thales Alenia Space for their contributions in the specification, design and implementation of this project.

The development of a radiation tolerant low power SRAM compiler in 65nm technology.

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Abstract

With the upcoming upgrades of the LHC experiments, it will be necessary to improve the performance and reduce the power consumption of the detector readout electronics. CERN has chosen to use a 65nm technology for part of the new generation of ASICs targeted to these upgrades. For this technology the SRAM memories within the readout circuitries need special attention as the commercially available IP blocks don't give the necessary radiation tolerance.

This paper will describe the design of a SRAM compiler design platform with a custom SRAM design underneath. The generated SRAMs have clock synchronous write/read operations and pseudo dual-port addressing.

They are implemented in the LP (Low Power) version of the technology and are designed to be radiation tolerant to reduce excessive power leakage due to TID (Total Ionizing Dose) and to minimize the impact of SEE (Single Event Effects) in the memory address decoding circuitry. The generated SRAMs can handle a TID >200Mrad and Linear Energy Transfer (LET) of 15 MeV.cm^2/mg. The max. frequency is at least 80MHz. This is also verified post-layout in all PVT corners. An additional challenge for these SRAMs is to keep the dynamic power consumption to a minimum whilst maintaining the radiation tolerance.

I. INTRODUCTION

The Large Hadron Collider (LHC) upgrade forces higher requirements to the electronics of many sub-detectors to be installed in the experimental chambers. With respect to the previous generation of front-end systems, the upgrade will need lower power consumption, smaller mass, volume and faster data channels, in addition to the robustness to a harsher radiation environment. A step towards more modern integrated circuit CMOS technologies was necessary to fulfil these requirements and 65nm is currently the chosen node to be used in the design of near-future particle detectors for LHC applications.

SRAM memories are used extensively in front-end chips in particle physics instrumentations. These memories are used for several functions, the main one being the temporary buffering of data waiting to be shipped off-detector after a triggering event. This trigger system allows to reduce greatly the quantity of data to be transmitted from inside to outside the experimental chamber, saving power and volume occupied by cabling resources.

This paper describes the design of an SRAM compiler, a software capable of generating SRAM blocks of different sizes starting from a custom design in the chosen technology.

As the target application of these memories will be in an intense radiation field, the design is such to be robust to both Total Ionizing Dose (TID) effects and Single-Event Effects (SEE). The techniques used to assure this radiation robustness are discussed in this article.

II. SPECIFICATIONS

A. *General specifications*

The generated SRAMs are designed in a 65mn technology using only standard-Vt devices, and occupy only the 4 lowest levels in the metal stack so that the upper layers can be used for routing or for the power grid.

The generated SRAMs can do simultaneous read and write operations, even though in the primary application will do more frequently write operations.

Description	Value	Unit
Supply	1.2 ±10%	V
Frequency	> 80	MHz
TID hardening	>200	Mrad
LET threshold	>15	MeV.cm^2/mg

Table 1: General specifications

B. *Timing diagram*

The SRAM has 3 possible working states within the same clock cycle : either a read, a write or both read and write operations. In the latter, first a read operation will be executed and then a write.

At the rising edge of the clock, the read & write address and the data to be written in the memory need to be available at the input terminals. See figure 1.

After the rising edge, the data read from the memory will be available at the output port.

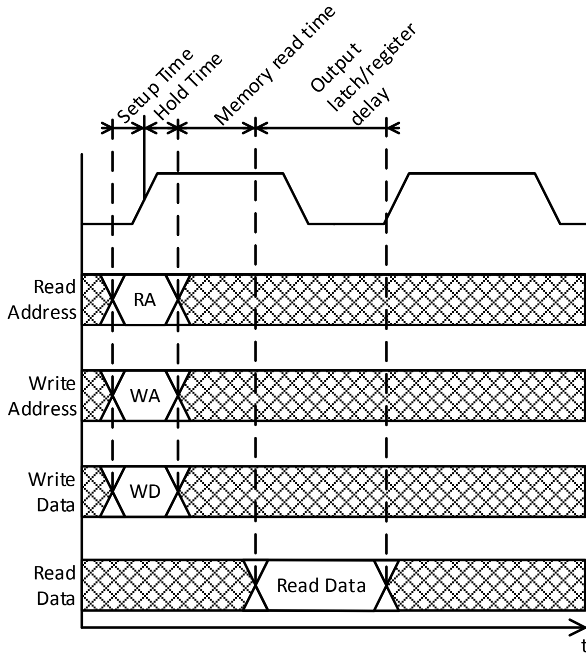

Figure 1: Timing diagram

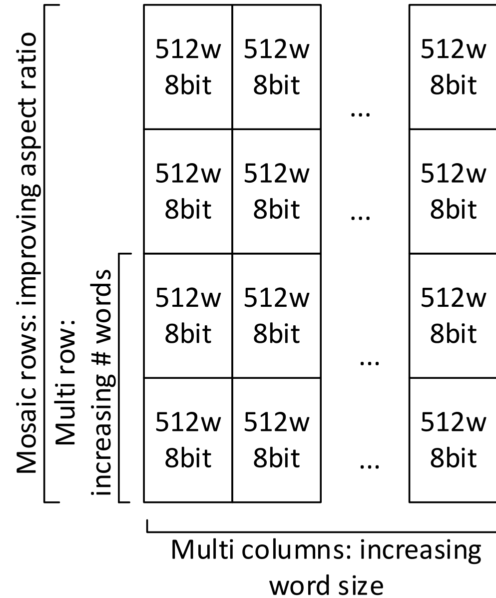

Figure 2: Scalability of the SRAMs

III. SRAM ARCHITECTURE

A. Radiation hardening

The applied strategy for making the generated SRAMs radiation hardened attacks the issue on 2 levels, TID and SEE. The hardening for SEE of the addressing circuit is done by drive strength. This prevents reading or writing the wrong word. Protection against latch-up is foreseen by placing p+ guard bands between all n- regions. It has been chosen to not protect the data within the memory cells in a hard way: an error-correction code can be used for such purpose as an additional external layer. In order to minimize TID effects (drive loss, Vt shift) no minimal width transistor are used in the design but a larger width was chosen for the nMOS and pMOS transistors based on TID measurement data [1]: all nMOS are larger than 200nm and all pMOS are larger than 500nm.

B. Architecture

The SRAM is composed out of a set of memory blocks either in series (increasing word size), in parallel (increasing # words) or a combination of both. A bank of flip-flops is foreseen to store the target address of the word. A self-timing clock generator will generate all the clock signals at the correct time. 2 sets of decoders will convert the address to select the correct word. A buffer to insure signal integrity. Figure 3 illustrates the architecture more clearly. To achieve the required pseudo dual-port behaviour, there are 2 banks of flip-flops that will clock in the write address in one bank, and read address in another. The address is decoded in 3 pieces, the 3 LSB will be used for selecting the interleaved word (more info in subsection E. Periphery), the MSB (1 or 2 bits) will be used to select the memory block row, and the intermediate bits will select a specific memory block.

To improve the aspect ratio in case of big word sizes, the SRAM can be cut into X pieces and stacked on top of each other. To prevent confusion with multiple memory rows for increasing # words, these stacked rows are called mosaic rows. To calculate how many mosaic rows are needed to get the aspect ratio below a specific amount; the formula below is used to define numbers of rows needed to get a targeted aspect ratio:

$$\#mosaic\ rows = \sqrt{\frac{current\ aspect\ ratio}{target\ aspect\ ratio}}$$

C. The Memory cell

For the memory cell the classic 6-transistor design was used. The schematic was changed to fulfil the requirements of the minimal transistors widths for TID mitigation. The design was verified across process/voltage/ temperature (PVT) variations to confirm that the specifications for speed and stability are met. The static noise margin is larger than 18% of the supply voltage over the full PVT range.

D. The DICE flip-flop

The DICE flip-flop [3] is the cornerstone of the SEU protection strategy for the periphery and addresses storage. They have been hardened against SEU thanks to the well-known DICE latch structure (see figure 4). Internal SETs in the flip-flops are mitigated thanks to the redundancy of the DICE memory and the addition of cCell. In the DICE memory there are 2 times 2 identical outputs (see figure 4: A=C & B=D). This redundancy may be used to filter internal SET in the flip-flop by using A and C or B and D as input of the cCell. In case of SET, only one of the inputs is affected/toggled, it means that the cCell is in high impedance (i.e. the SET is not propagated).

For the hardening of the flip-flops used to store the write and read address, the output cCell has been sized such that the

cCell itself is insensitive to SET (hardening by drive strength).

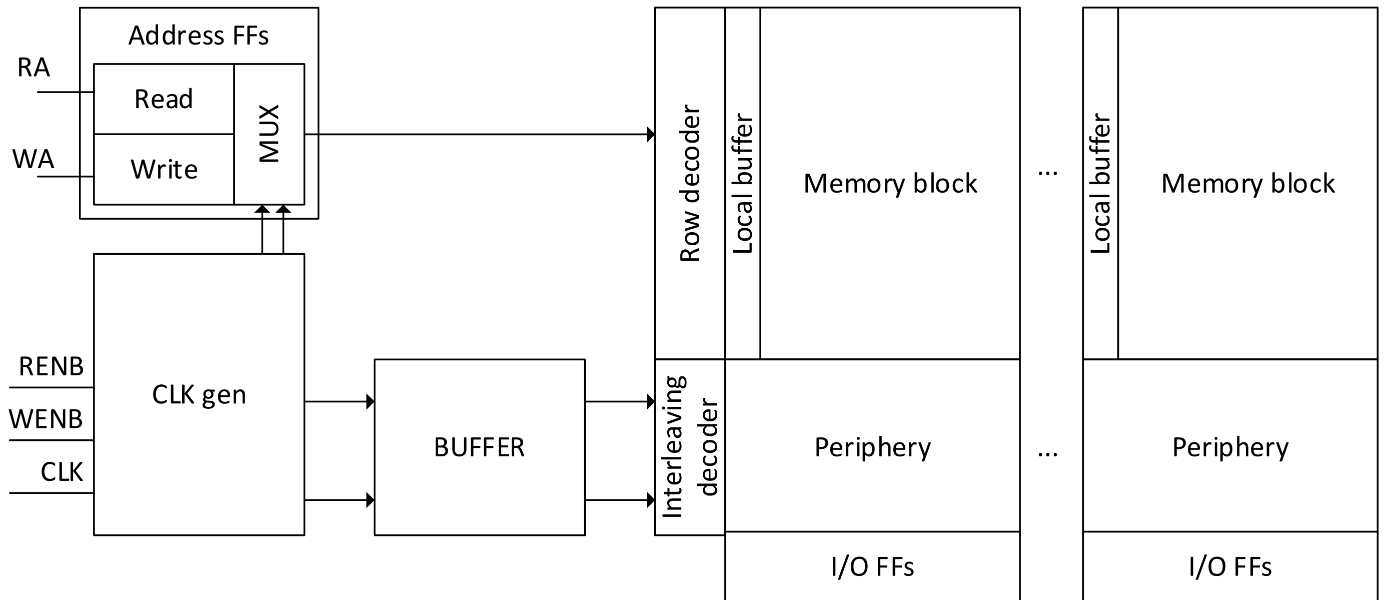

Figure 3: Block diagram of the architecture

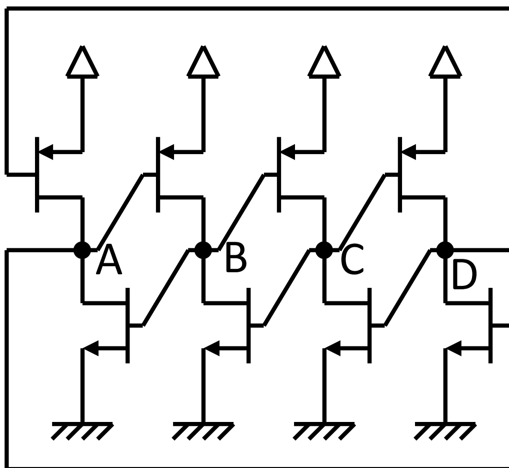

Figure 4: The Dice latch structure

E. Periphery

The memory cells in the memory block are interleaved by 8 words. This has a dual benefit. First of all it improves the aspect ratio to have 8 words on 1 row. Second of all it provides extra radiation hardening. When a charged particle hits the memory block under an acute angle, the particle can hit 2 neighbouring cells and alter both contents. A multi bit upset (MBU) would occur if these 2 bits belong to the same word.

To correct this, multiple parity bits would need to be added to the word. Alternatively by interleaving (figure 5), the particle will not hit 2 bits in the same word, causing less corruption within the data word. To decode this interleaving during write and/or read operations MUXs have been foreseen between the BIT-lines and the sense amplifier.

Figure 5: Interleaving

F. Memory block

Memory blocks have been made in 2 flavours, 128 words by 8 bits and 512 words by 8 bits, respectively 16 word lines and 64 word lines high. As mentioned before 8 words are interleaved per word line.

The word line itself is split up into multiple sections with one backbone, a global word line that is buffered inside every memory block. The advantage is that the local buffers inside the memory blocks can be better optimized for the load than one big central buffer.

All memory blocks have multiplexing gates on the outputs, so that multiple rows can be used to increase the number of words without shorting any outputs directly.

G. Clock generation

The timing of all signals is generated with continuous calibration on the background. This self-timing is achieved with a dummy memory block at the end of the memory. The clock generator will control the charge and discharge cycle of the BIT lines dummy block.

The Clock generator will also select the needed address from the flip-flop banks, either the read address or the write address.

The clock generator is build around 2 flip-flop. One controls the read and write phase, the other one read discharge duration.

The radiation hardening for the flip-flops is done by using DICE flip-flops. Other nodes in the clock generator are not hardened by drive strength, but the cross-section is low enough for the application.

IV. LAYOUT

The layouts are built upon 2 floorplans, one for 128w memory blocks and one for 512w memory blocks.

All block are optimized for compiler assembly and have been simulated post layout in all PVT corners.

The floorplan is always built up with the clock generator, address flip-flop banks, buffers and decoders located on the left side. Data flip-flops are located on the bottom of the flip-flop. The dummy memory is located the furthest form the clock generator to be sure that all parasitics are taken into account in the self-timing. Dimensions for a 1024w x 32b is approx. 450um x 375um.

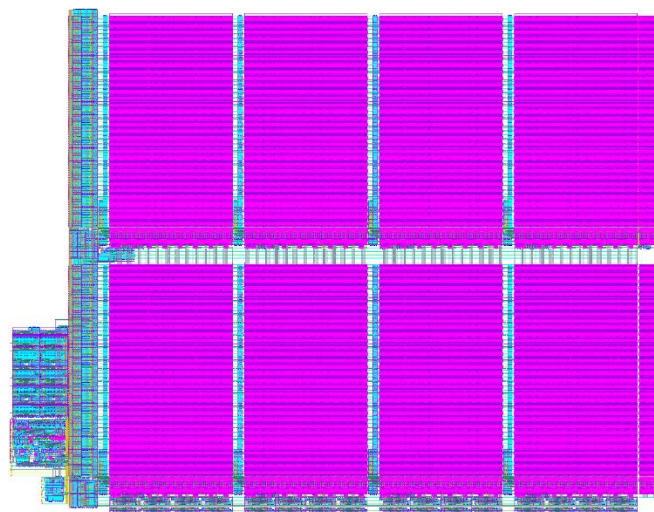

Figure 6: Layout of 1024word x 32bit SRAM

V. COMPILER

The compiler is build up out of 2 layers, a virtual design layer which is abstraction of SRAM design and an implementation layer that will generate the actual SRAM design database.

The compiler works in 2 stages. In the first stage the user can try out different possible designs and immediately see key parameters of that design e.g. physical dimensions, buffer configuration, etc. The name of this layer is "Virtual Design Layer". In the second stage the Implementation Layer, will create the requested SRAM design.

The communication between the 2 layers happens via a TCP connection. This has the advantage that the implementation layer can run on a powerful server, while virtual design layer runs on a workstation.

Characterisation is done by interpolation between multiple pre-characterized instances. This has the major advantage that no expensive tools are needed for creating the liberty files at the user site.

The output from the compiler is an OA library containing the schematics, layouts, abstracts and symbol views. Additionally it will generate the needed liberty file, lef file and verilog model.

VI. FURTHER WORK

The first compiler version will be finished by the mid of Q3 2014. Two SRAM instances will be put on a test chip in July 2014 to prove the functionality in silicon.

VII. SUMMARY

In this paper, the development of a 65nm SRAM compiler was described. The SRAMs have clock-synchronous write/read operations and pseudo dual-port addressing, and are using the LP version of the technology with only standard Vt devices.

Synchronous write/read operations are controlled by the clock generation module. This module uses a dummy memory block with continuous calibration in the background.

The SRAMs are designed to be radiation hardened against cumulative and transient effect (TID and SEE). This is done by restricting the minimum dimensions of the devices, using DICE flip-flops and drawing p+ guard bands between the n-regions

The SRAM memories exist of combinations of memory blocks of either 128w x8b or 512w x8b. The word lines of these memory blocks are buffered locally to reduce power consumption. Additionally 8 words are interleaved per word line to mitigate MBU.

The compiler has the ability to first build a virtual design of the SRAM, so that the engineer, project leader or manager can use the tool to get an idea of the physical dimensions and the buffer sizing. When the virtual design satisfies the user, it can be fully generated and characterized.

VIII. REFERENCES

[1] S. Bonacini, P. Valerio et al. (2012, January). . "Characterization of a commercial 65nm CMOS technology for SLHC applications". JINST, vol. 7, P01015

[2] Stefan Cosemans. (2010, Octobre). Variability-aware design of low power SRAM memories [PhD desertation]

[3] T.Calin, M. Nicolaidis, R. Velazco. (1996, December). Upset Hardened Memory Design for Submicron CMOS Technology. IEEE Transactions on Nuclear Science. Vol 43 (6), pp. 2874-2878