A Mixed-Signal Radhard Microcontroller: the Digital Programmable Controller (DPC)

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Abstract

Thales Alenia Space is engaged in the development of a radiation hardened mixed-mode circuit: the DPC (Digital Programmable Controller). This device is a major breakthrough in the availability of radiation hardened highly integrated european micro-controller. This component uses the IMEC RHBD DARE on UMC 0.18µ library and analog IP designed full custom by ICsense. The effective performance characterization of the DPC is currently evaluated in Thales Alenia Space laboratory.

The DPC is an essential building block for the development of intelligent RTU and other (power) distribution units in LEO and GEO satellites. Its large set of communication interface makes it usable in a broad range of applications such as scientific payload control, motors, actuators, battery management, power management … wherever a decentralized control makes the overall solution more efficient.

The presentation covers the key features of the DPC that have been made possible thanks to some extensions of the DARE library such as DPRAM, IO and clock gating. The analog functions such as ADC, DAC, PLL & bandgap have been designed such as to minimize the amount of external components needed around DPC (target being a system on chip). The E2prom containing the hardware configuration bitstream and the firmware remains, for this first generation, still an external device. Extreme care was taken to SET hardening of the critical analog functions: ICsense having developed automated and systematic charge injection verifications. Prevalidation activities and first tests results will be presented.

I. DPC Overview

A. Development strategy

The construction of the DPC is the result of a 4 party project involving IMEC, ICsense and Thales Alenia Space under an ESA development.

IMEC not only has provided the RHBD DARE on UMC 0.18µ library, but also extended it with additional features. Dual port memories are being used to transparently perform memory scrubbing in a seamless manner for the processing unit. The DPC embeds 95Kbytes of memory split over several banks. Clock gating cells have been also added. As the DPC embeds a large range of features, power consumption may become an issue if all of them would be active simultaneously. At boot time, a hardware configuration is loaded in the circuit to only deliver clock toward functions relevant to the target application.

IMEC also performed top level layout integrating digital netlist and analog macros, performing DRC to check for compliance to particular radiation hardening rules and finally the interface with UMC foundry.

ICsense has designed a large set of analog IP blocks which are included on chip. Concerning analog IO offered to the user, there are 4 analog to digital converters 13bits-1MSps with input multiplexing functions. There are also 3 current steering DAC each 12bits-50kSps / 8 bits-1MSps. As supporting function the DPC also includes an on-chip 100kHz RC oscillator for applications that do not require high precision frequency reference. This frequency reference is internally multiplied with a PLL delivering the internal master clock of the circuit. All these function are obviously supported by an on-chip bandgap. A set of internal low-drop voltage regulators converts the incoming 3.3V into +1.8Vdc to supply the digital core and to deliver “noise-less” supply to critical analog functions. This extensive set of analog function makes DPC a standalone system-on-chip (exception being for now the external E2prom).

Besides classical RHBD rules such a guard rings (Latchup) & margins for Vt shifts (dose up to 100krad), ICsense has

developed a powerful set of extension on top of (Cadence/Mentor) simulation tools to perform systematic charge injection verifications on each nodes of the circuit. ICsense has completed the design, layout and verifications. The analog macros were delivered to IMEC for integration into the final chip layout.
Thales Alenia Space Belgium has developed the RTL code to glue up all IP: the 16bits OpenMSP430 processor, mil-1553b, UART, CAN interfaces, memories, multipliers...
Challenge for such a complex mix-mode design resides into the verification of interfaces between analog macros and digital functions. This problem was tackled by the exchange of verilog Wreal models simulating the behavior of analog functions to be used in digital simulations. In the other way, stubs of RTL code have been delivered to simulate analog functions and their interface with digital functions.
Foundry was UMC and packaging has taken place at HCM. Wafer probe and package testing used facilities of µTest. The component is now back into the labs and under tests.

B. *FPGA emulation*

On top of the classical simulation at RTL, the DPC has been extensively validated on 2 FPGA platforms. The first one, named Core Validation BreadBoard CVBB, was used to validate all interaction modes foreseen in the DPC feature list. These are too complex (too long) to simulate, hence they have been executed on a clone of the RTL into a real hardware platform. This strategy allows to validate all the analog and digital interfaces and the digital functions a few months before tapeout.
The picture hereunder illustrates the FPGA emulator.

Figure 1: Core Validation BreadBoard

The second one, named DPC starter kit, was used to integrate the DPC with its software development environment. This was achieved; executable code for some typical applications was already running in real time in real environment prior to tape out. These two platforms raised the level of confidence in the overall solution: not only the RTL is most probably free of bugs, but also the component definition itself matches the user needs and firmware development tools.

C. *Architecture and configuration*

Figure 2 here below depicts the DPC internal architecture. Intentionally, the DPC embeds a very large set of functions. As compared to a µC from the industrial world this may be overkill. However, the economics of space components is very much different. Production volumes are very low as compared to consumer or industrial markets. Hence the silicon area account for a very small amount in the total cost breakdown of such a project. The circuit was therefore equipped with so many features, that it is nearly impossible to find a concrete application using all the available resources at once.

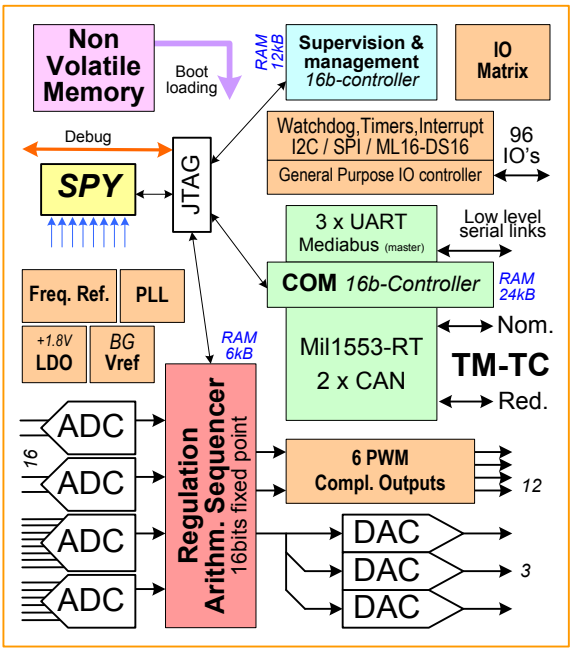

Figure 2: Block Diagram of the DPC

As a drawback, not only silicon area increases with the number of functions but also power consumption. Therefore, prior to firmware execution, the DPC enters a hardware configuration cycle. During this phase, a "hardware configuration" map is loaded from the non-volatile memory that defines which functions should be active (used for the application) and which functions will be made sleeping (clock gating and full sleep mode of analog blocks). Furthermore, operating frequency can be defined such as to match exactly speed performance and processing power needed for the target application. Using these mechanisms, the DPC power consumption can vary up to a factor 6, from minimalist low end use cases up to the unrealistic worse case where all functions are used at maximum operating frequency.

D. *Digital processing*

Processing is based on several instances of the OpenMSP430 fixed-point 16bits CPU core. This processor features the instruction set of the PDP11 (1970) from Digital Equipment Corp. The openMSP430 [**Error! Reference source not found.**] is a synthesizable 16bit microcontroller core written in Verilog. It can execute the code generated by any MSP430 tool-chain in a near cycle accurate way. To fasten the execution, the CPU is equipped with one hardware MACC function and one integer divide unit.

On one hand, digital control is offering new possibilities in driving smarter and more efficient systems. On the other hand connectivity is being more & more present in all applications. In order to avoid searching for complex & touchy compromises between robust loop control and communications or host functionality the architecture offers one CPU per task.

For communications to the outside world, the CPU has several hard wired units: 3 x UART, 2 x CAN bus and a mil-1553b remote terminal function.

Another CPU instance in the RAS is intended to execute a configurable & repetitive sequence of basic mathematical or logic instructions within a short cycle. This sequence can be programmed so that any mathematical expression typical of regulation scheme is realized: structures such as Proportional, Integral and Derivate (PID). This sequence can also be programmed to acquire and pre-process multiple sensors or pre-process signals before being generated to hardware signals.

Finally one CPU is available to perform all local (host) supervision & management functions.

The highly flexible hardware unit "USI" (Universal synchronous Serial Interface) is able to drive with quite various timing requirements the following communication protocols: SPI, I2C, ML16-DS16, serial in-parallel-out IO extenders.

II. DARE PLUS LIBRARY

The ESA activity "DarePlus – ASICS for Extreme Radiation Hardness & Harsh Environments" has as objective to provide a suitable and mixed-signal capable microelectronics technology platform. The existing DARE library elements in UMC 180nm were therefore improved and new elements added to increase the maturity to a level adequate for jovian missions.

Several of these DARE library enhancements were directly beneficial to the development of the DPC. Worth mentioning are the integrated clock gating cells, SET optimized inverters for clock trees, SET optimized combinatorial cells for set/reset trees and decoupling cells. Concerning the IO library extra drive strength cells were created, slew rate control was implemented to mitigate simultaneous-switching-output noise and all cells were made compatible with thick top metal processing. Finally, dedicated dual port SRAMs instances were implemented according to the specifications of the DPC during the development of the dual port compiler.

A lot of valuable feedback originating from DPC has been integrated into the DARE libraries as well. Examples are the SET optimization of digital input cells, the increased insensitivity to multi-bit upsets in the memory matrix of the SRAMs, the improved electro-migration tolerance in IO cells, the more elaborate manuals, etc...

The DPC ASIC uses a DARE library release that was generated with a more advanced characterization tool (ALTOS from Cadence) and a more accurate parasitic extraction flow (RC, previously only C). The timing and power data are also more accurate than before due to bigger look-up tables and better modeling of conditional arcs. With the previous characterization tool (ELC) not all timing arcs for all conditions of the inputs were present in the .lib. The correct timing and power analysis based on the new .lib files were compared with DPC silicon.

For design of the analog circuits in DPC a new ELT pcell symbol and layout was introduced to provide a means to check the inner and outer ELT diffusion connection correctly.

The "DARE analogue library" consists in the ADK (Analogue Design Kit) that forms an extention of the standard UMC PDK.

The existing radhard check was extended to cover the use of triple well nmos transistors and to report errors in more detail.

The first implementation of a formal single event latch-up check was added to the radhard deck.

III. Analog Blocks

A. Overview

The DPC is a mixed-mode circuit that contains the following analog blocks:

- Reference voltage and current generation
- Power-management block with LDO's
- 120 MHz frequency reference system (PLL) to provide the clock to the digital part
- 100kHz reference oscillator
- 4 flexible 13 bit , 1MSps ADCs with extensive input muxing capabilities
- 3 12 bit, 3.75 MSps DAC current-mode outputs
- Power-on-reset circuit and under voltage detector
- Rail to rail comparators, PGA (0dB, 10dB, 20dB)

This paper only focuses on the test results of some of the analog blocks (PLL, ADC, bandgap). Some of these blocks have been explained in more details in [5; 6]. Radiation test data are not yet available, but the ICsense proprietary, automated SET hardening simulation environment has been employed to assess and decrease the SET sensitivity of the analog IP.

B. ADC

The DPC contains 4 ADCs that use a cyclic pipelined topology. The core of all ADCs is identical, but the amount of input muxing is different. Following functionality is foreseen for the ADCs and the input muxes:

- Up to 8 external analog single-ended inputs or 4 external differential inputs can be attached to a ADC core.
- An additional 8 internal analog inputs (or 4 differential) can be connected
- The channel selection and sampling times are fully controllable by the microcontroller.
- Sensing amplifiers are foreseen to enable measurements of very low differential voltages (currents in shunt).
- The on-chip temperature sensor can also be attached to one of the ADC cores.
- Offset calibration can be done by shorting the ADC inputs through the MUX.

The measurement results of the ADC show more than 11 ENOBs accuracy with an excellent THD of -74dB at 500 Hz. DNL is below 1 LSB and RMS noise is below 0.6 LSB. The ADC works with a single-ended input range of 0-2.5V and a differential range of +-1.25V. A plot is given below:

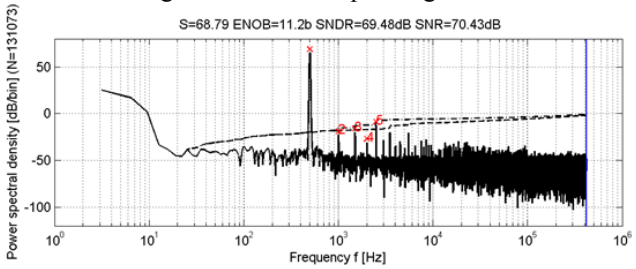

Figure 3: ADC performances

C. Reference Voltage

The reference voltage is generated by a bandgap circuit with an external decoupling capacitance. The bandgap uses a traditional topology without analog trimming. The SET sensitivity of the bandgap has been reduced by using large currents, additional buffer capacitances at sensitive nodes and a special startup circuit to ensure fast recovery after an SET event. The bandgap itself is made insensitive to SET and as a consequence an SET of 60 MeV/mg/cm^2 on the bandgap circuit itself never triggers a reboot of the bandgap and artifacts on reference voltage and currents are negligible.

D. PLL

For a reliable operation of the digital part, it is essential that the clock generation is without glitches (stable clock period and duty-cycle), even during SET events. 'Long-term' frequency spikes and phase shifts due to SET are minimized to not interrupt certain communication protocols. The complete PLL, including divider, loop filter and VCO is integrated on-chip. The measured output frequency of the PLL is 120MHz and the bandwidth 7kHz. The input frequency to the PLL is a 100kHz input source that is selectable between an off-chip reference oscillator or an integrated relaxation oscillator.

The integrated relaxation oscillator uses an external R and C to provide excellent stability and a small temperature drift. The relaxation oscillator uses triplicated comparators to achieve SET free operation. A special topology is used to achieve both low jitter and low temperature drifts; the latter is now dominated by the external components. First measurements show full functionality of this 100kHz oscillator.

The integrated 120MHz Voltage Controlled Oscillator (VCO) is based on a custom derivative of the Maneatis delay cell [1] with sufficient high current levels and capacitor values to ensure SET free operation.

E. DAC

The measurements of the DAC with output buffer show full 12 bit resolution with a DNL of less than 1 LSB and INL of less than 1.7 LSB for a data rate of 3.75MSps without dynamic element matching. When dynamic element matching is enables the data rate drops to 58kSps, but with a DNL of less than 0.7LSB and INL of less than 1.2LSB.

F. Top level mixed-signal verification methodology

To enable this first-time-right design of the DPC, a proven top-down bottom-up design strategy has been used. It consists of generating high-level models of each block to verify the functionality right from the start of the project.

The models use Verilog-AMS with wreal data types [4] for the analog parts. They can be simulated by a standard digital simulator in an event-based fashion. This leads to a very high simulation speed and therefore the possibility to check all analog-digital interfaces in the DPC and the functional operation of the most important use cases. The analog and mixed-mode simulations employ the same set of identical models, eliminating the risk of the analog and digital team having different representations of the same blocks. By

interchanging wreal models and actual circuits, good trade-offs between simulation accuracy, coverage and simulation speed can be obtained in complex mixed-mode designs.
The result of this state-of-the-art mixed-signal verification methodology allows to reach a functional ASIC from first silicon such that it can already be used in target applications.

G. *Rad hard analog Design methodology*

As an extension to its unique structured analog design environment [5], ICsense has deployed a rad hard analog simulation flow to enable rad-hard-by-design analog and mixed-signal IP blocks in the DPC. This flow is now used as the standard, qualified flow for rad-hard mixed-signal designs at ICsense and works as follows: the effect of an SET strike is simulated by injecting a double exponential current pulse on a certain node of the circuit [3]. The total inject charge corresponding to an LET of 60MeV.cm2/mg is 1.2pC. The design environment allows injecting this pulse in any circuit node at any wanted point in time, using the following flow:

- Inject an SET pulse in every circuit node under typical conditions. This produces a shortlist of sensitive nodes.
- Perform SET simulation for all these sensitive nodes over PVT (process, voltage, temperature) corners. An iterative procedure is carried out to devise countermeasures when specifications under radiation are not met.
- Final verification by injecting all nodes again in some of the worst-case corners for SET sensitivity.

For time generation circuits the timing of a SET strike is varied to find the most sensitive point in time in addition to the sensitive node detection.
To make the circuit robust for TID, a combination of various techniques are used:

- TID will result in Vth shifts of the devices, thus reducing the margins on the operating points of the transistors. The worst-case Vds-Vdssat across all PVT combination is monitored.
- The induced Vth shifts due to TID will depend on the bias conditions of the devices. Special care is taken to ensure identical operating points and biasings of all devices belonging to one matching structure under all operating modes.
- TID can generate leakage paths between N+ regions at different potentials. The DARE ADK provides an additional DRC rule check to flag N+ regions at different potentials that are not interrupted by P+ regions
- The analog blocks with highest matching sensitivities are put on 1.8V supply domain with thin-oxide devices to minimize TID sensitivity.
- For critical devices on the 3.3V domain, the enclosed layout transistors (ELT) from the DARE ADK are used.

IV. CONCLUSIONS

Thanks to an efficient cooperation with IMEC, ICsense and ESA, ThalesAleniaSpace Belgium has built an innovative highly integrated mixed signals controller (Figure 4).
First tests show that analog and digital blocks allows to reach a functional ASIC from first silicon such that it can already be used in target applications. Performance testing has just started. Next important steps are radiation tests to be perfomed in Louvain la Neuve in order to confirm preliminary results of test vehicles and RHBD techniques largely used in the DPC.
Its high level of configurability and its large set of communication interfaces allow the usage of the Digital Programmable Controller (DPC) in a broad range of applications such as scientific payload control, motors, actuators, battery management, power management … wherever a decentralized control makes the overall solution more efficient.

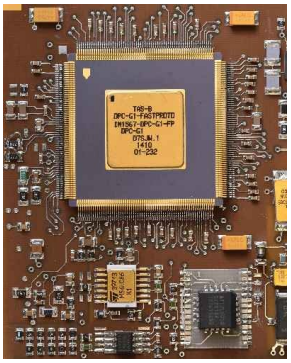

Figure 4: The DPC ASIC under test

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