## Background Information

CERN manages a complex of many particle accelerators which are interconnected like product lines in a factory. Our final products are different particle beams going to different destinations. The synchronization of the different accelerators is managed from a central timing facility which sends messages using a dedicated timing network. Hundreds of receivers listen to these messages and react to them by generating either interrupts or front panel pulses or both. These receivers exist in VME, PCI and PMC formats. After (almost) completion of the new Large Hadron Collider, CERN's control group is launching a renovation project for its injector complex. In this context, timing hardware technology will be reviewed and a new system will be chosen for the next 10-20 year period. The process of this review will be started with a timing workshop (CERN, 15 February 2008) to gather different people from all of Europe who either have similar needs or can provide interesting solutions. We will have presentations in the morning and discussions in the afternoon. We hope that the workshop will be a seed from which a fruitful collaboration can start developing.

## Current timing system at CERN

The current system is based on fiber transmission for long stretches followed by RS-422 multidrop over shielded twisted pair, with a bandwidth of 500 kb/s. Time is broken up in milliseconds, during which 8 events max. can be sent. The master is driven by a Pulse Per Second (PPS) pulse and a 10 MHz from a GPS Disciplined Oscillator (GPSDO) so as to have complete UTC synchronization. We have one master card (VME) per accelerator due to bandwidth constraints. Communication is exclusively downstream.

Here is a summary description of the vertical slice of control system concerning timing:

- Operators in the control room use Java graphical applications to draw timing diagrams of what different accelerators should be doing at every moment.
- These diagrams are converted into objects sent to the Central Beam and Cycle Manager (CBCM), a set of VME crates hosting CPU modules and Timing Generator cards.
- Timing generator cards receive "programs" from the CPU modules and execute them in a fully deterministic way using the CERN-made CPU inside their FPGA. These programs are very simple: send X, wait x ms, send Y, loop, etc. There is a double buffer in the card: while the CPU sends 1.2 seconds worth of program to the Generator's buffer A, the generator is executing buffer B, then roles are reversed.
- The result is timing messages on the network, which are listened to by timing receivers. These receivers can be configured remotely using CERN's control system (as happened with the master).

- The end result is front panel pulses and software interrupts all around the accelerator complex.

## CERN's vision for a future timing system

We are happy with everything concerning the current system except for:

- The lack of bi-directionality in the timing link, which prevents us from implementing fiber or copper delay compensation schemes and also from having effective diagnostics independent of control system infrastructure (e.g. the technical network).
- Small bandwidth imposes unnatural choices on us, such as having a different master for each accelerator.

In addition, CERN is going to insource the support for the WorldFIP field bus, up to now guaranteed by Alstom. WorldFIP is basically based on a master acting as an orchestra director and prompting each slave to talk at a given time slot, therefore avoiding collisions. The basic physical layer is differential shielded twisted pair. It would be very interesting for CERN to support in addition a high speed bidirectional optical link so that our timing system looks from outside like just another instance of a WorldFIP field bus. Some initial investigations lead us to believe that the concept of Passive Optical Networks (PONs) is well suited for our needs, but our research is at a very preliminary stage.

In terms of hard specs, we would like to synchronize 1000 receivers all around the accelerator complex to within 1-10 ns. We would also like every receiver to be able to recreate the original UTC 10 MHz as sent from the GPSDO with an accuracy to be defined.

## CERN participants for the workshop

Hermann Schmickler (AB-CO Group Leader), Javier Serrano (AB-CO-HT Section Leader, hardware specialist), Julian Lewis (AB-CO-HT Timing activity leader, software specialist), Pablo Alvarez Sanchez (AB-CO-HT, main timing hardware designer), Bruno Puccio (AB-CO-MI Section Leader), Benjamin Todd (AB-CO-MI, hardware designer).