Sub-Nanosecond Machine Timing for the FERMI LLRF System

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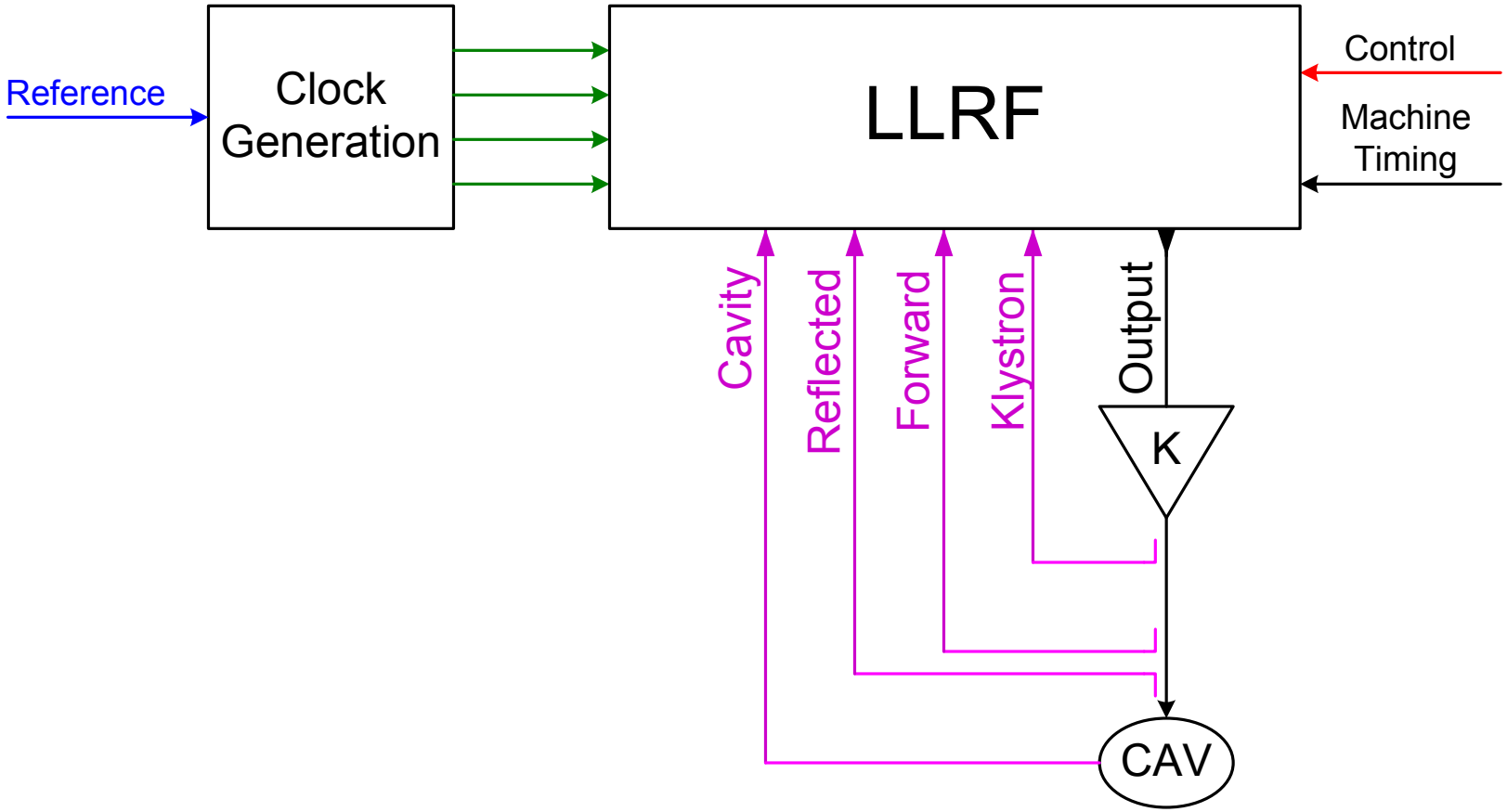
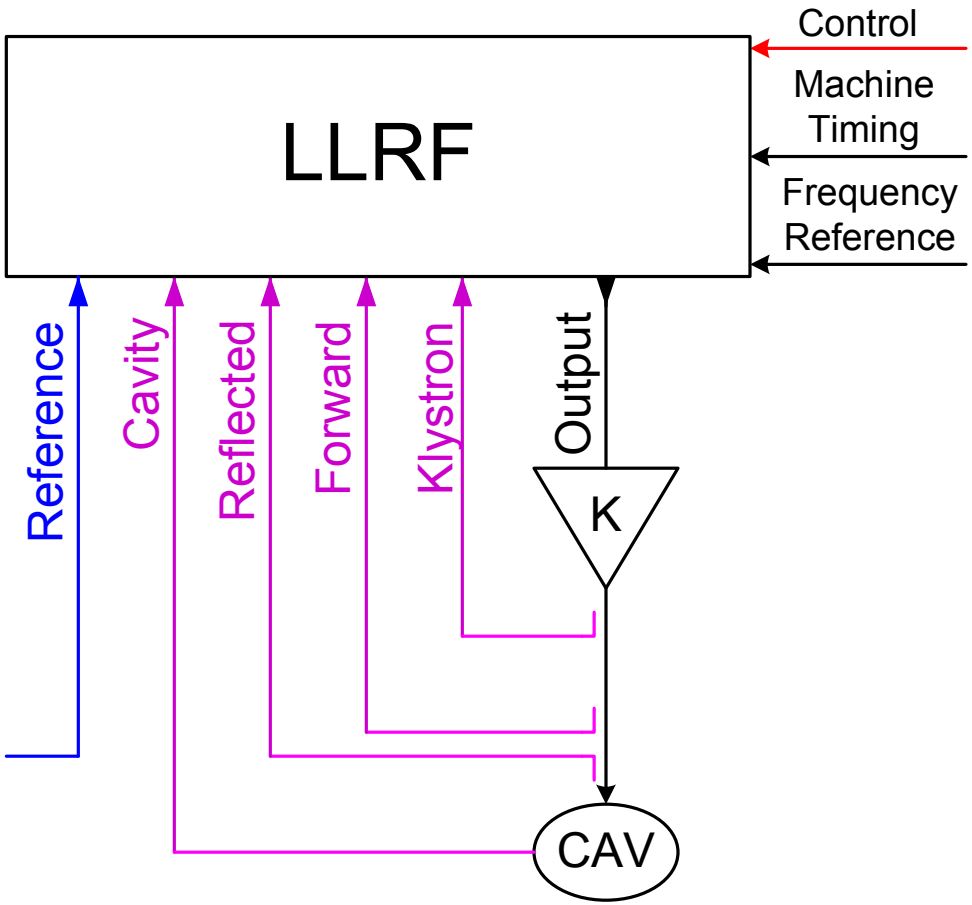
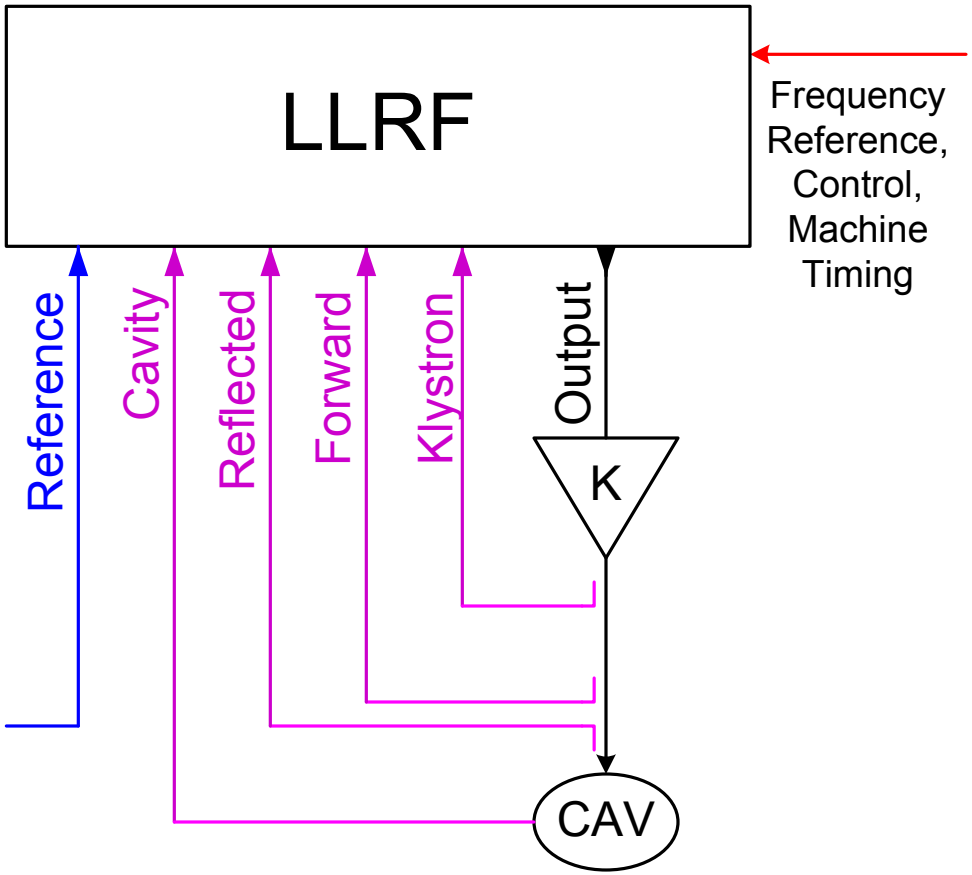
LLRF Layout: Basic



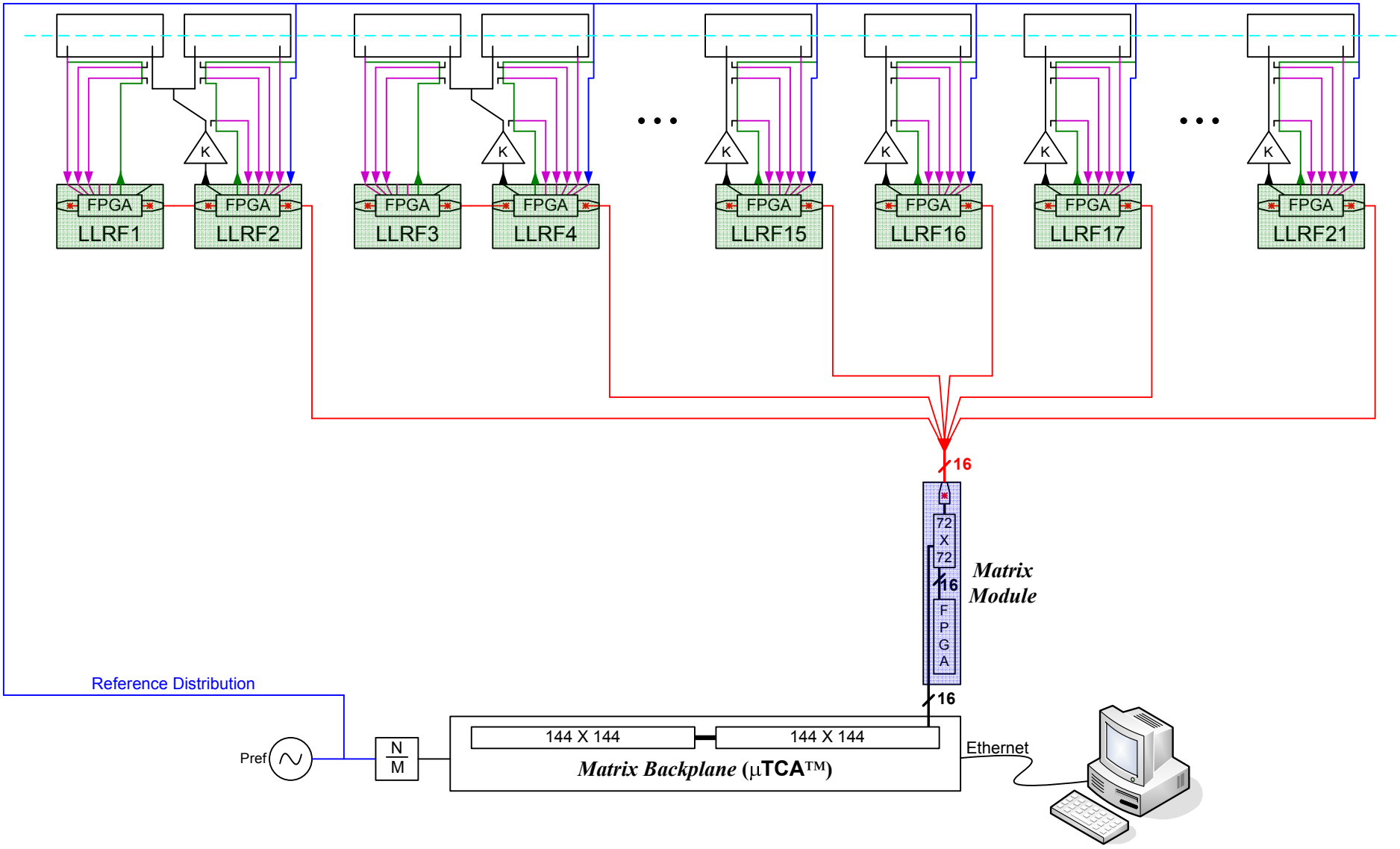
LLRF Layout: Reference as Input



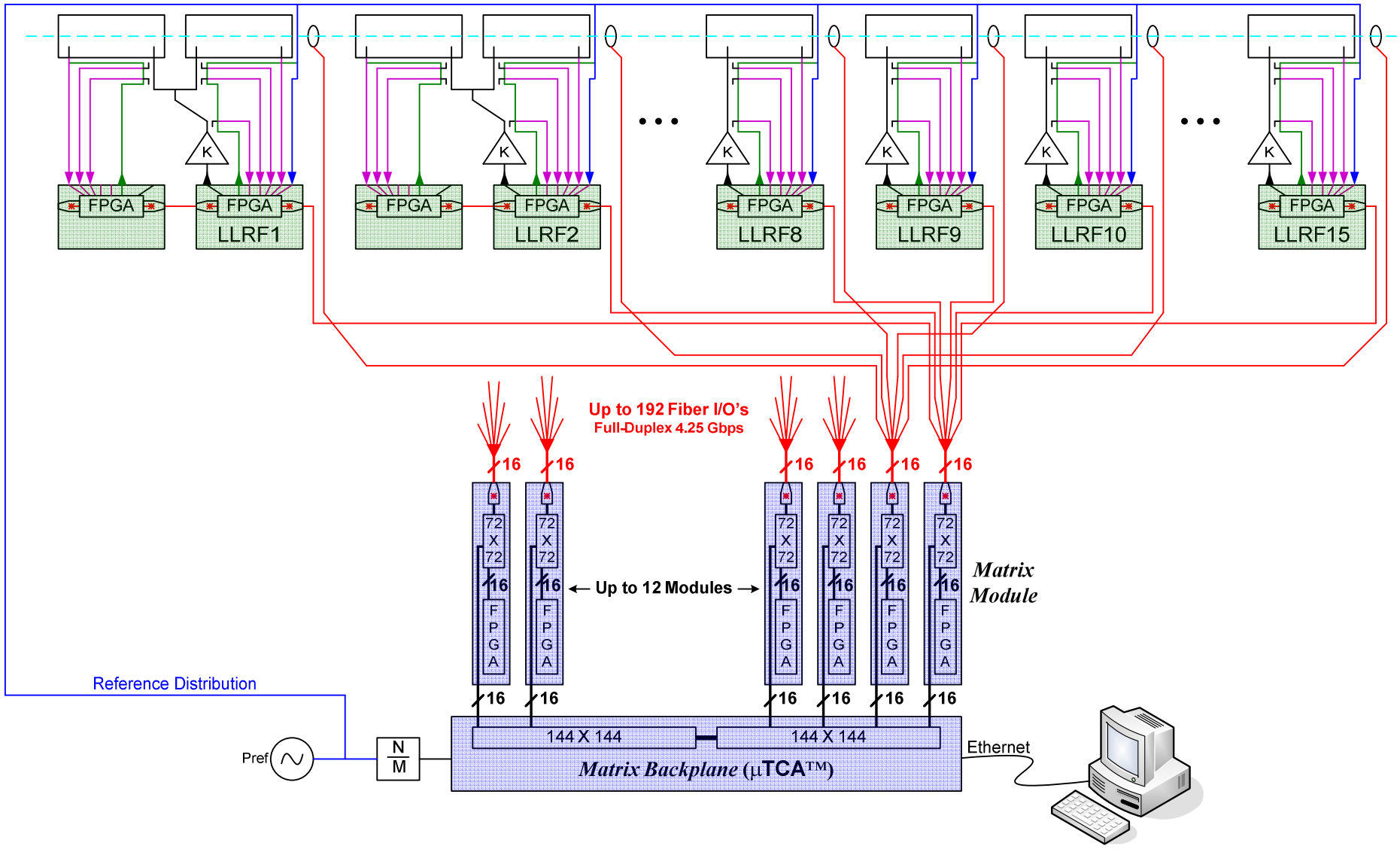
LLRF Layout: Single Input Timing and Control



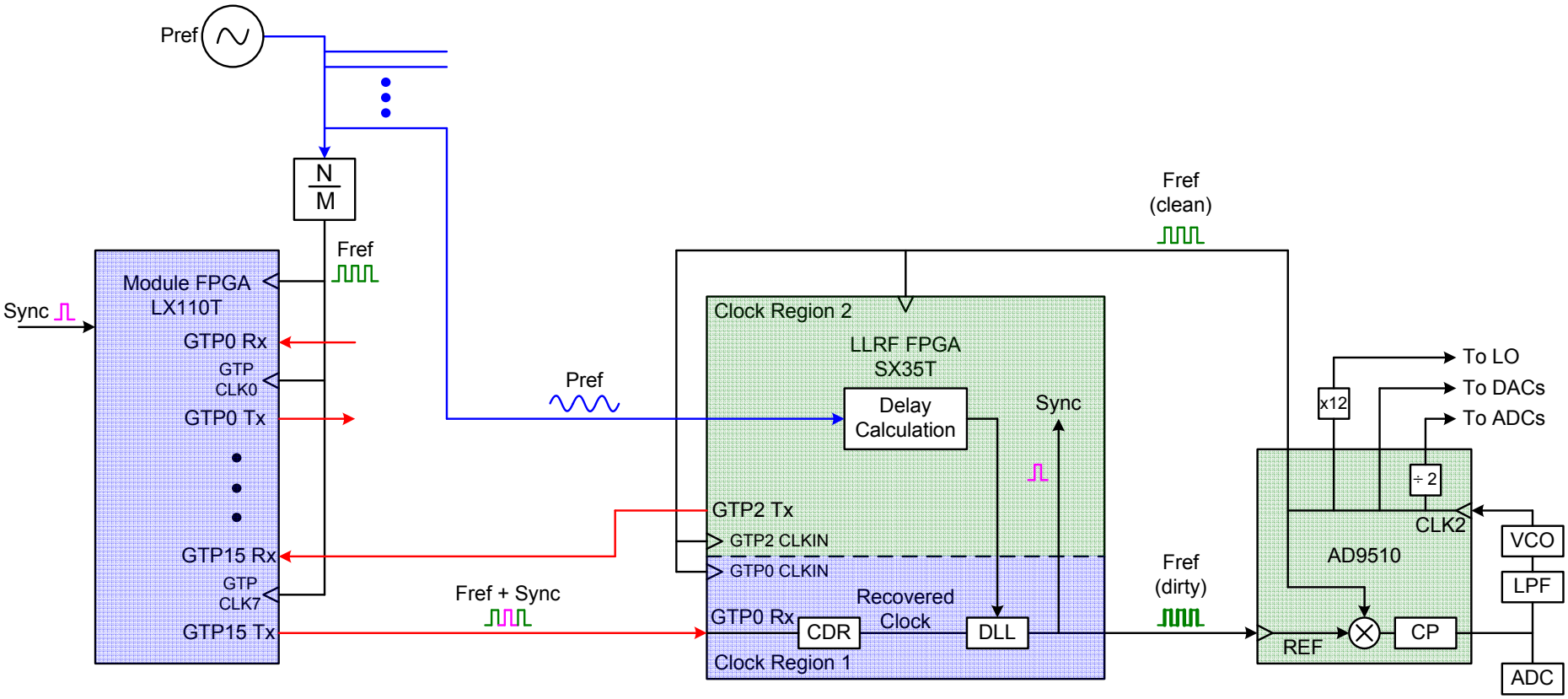
Global Communication and Control via 'The Matrix': 1 Module



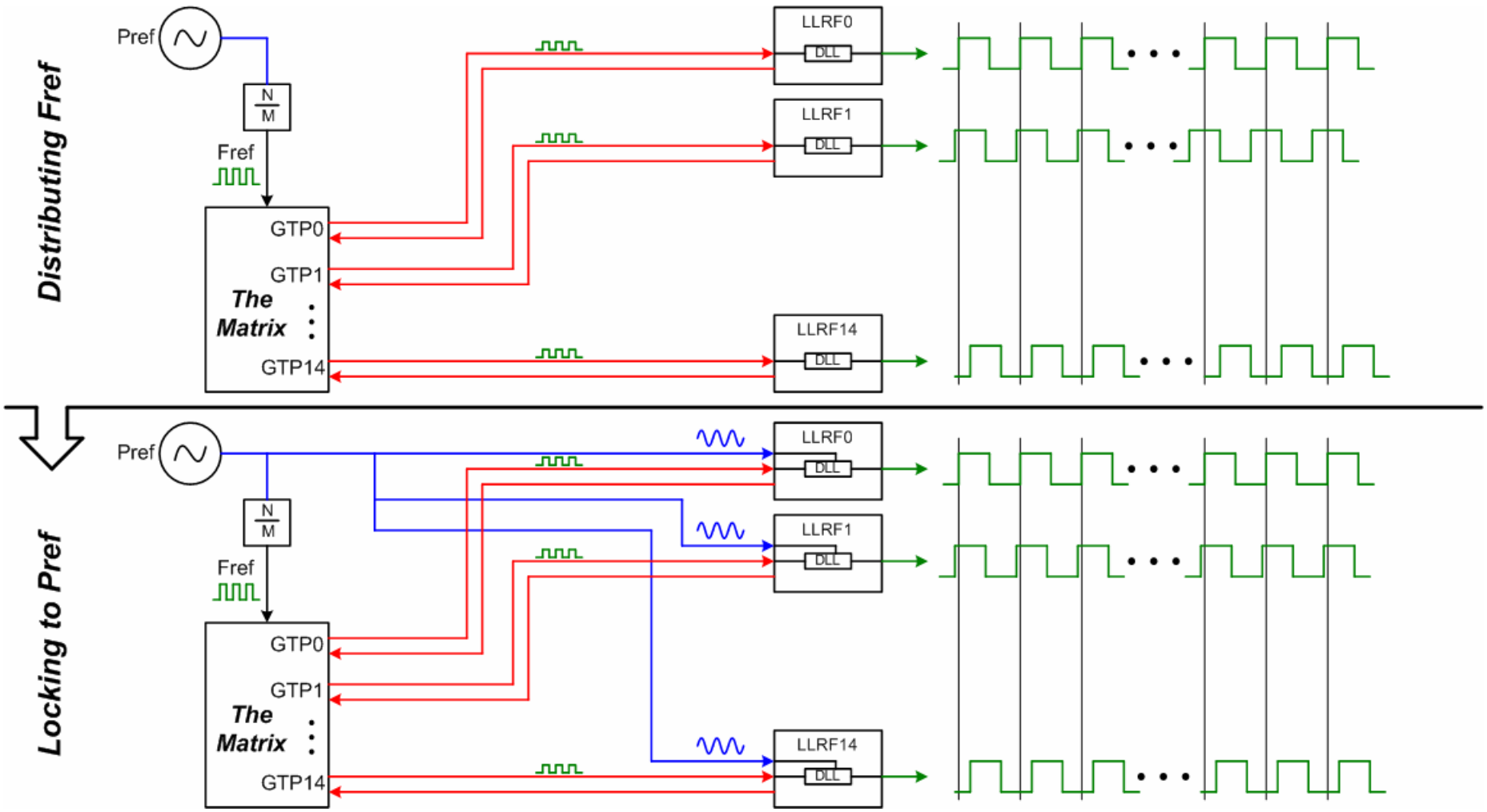
Global Communication and Control via 'The Matrix': 12 Modules



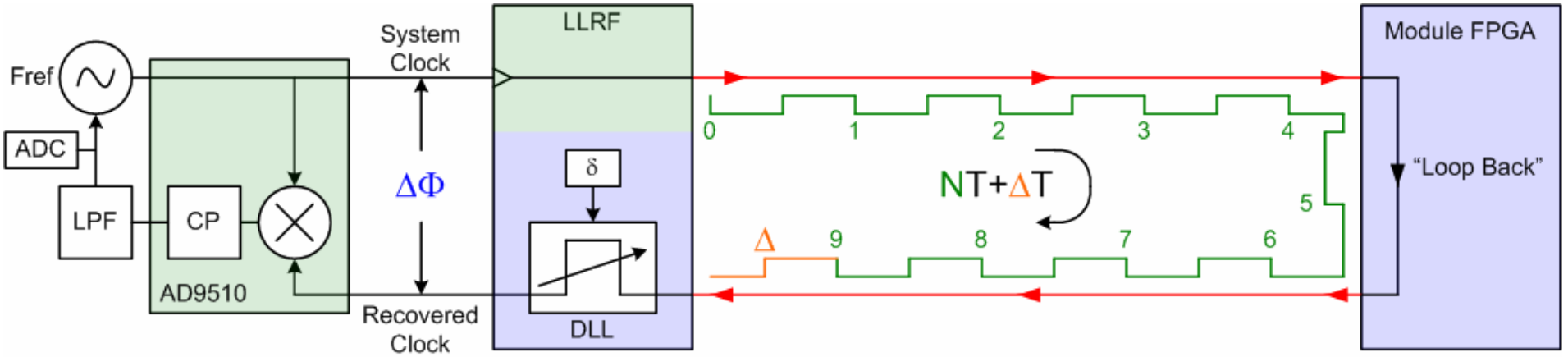
Frequency Reference, Time and Trigger Distribution Scheme

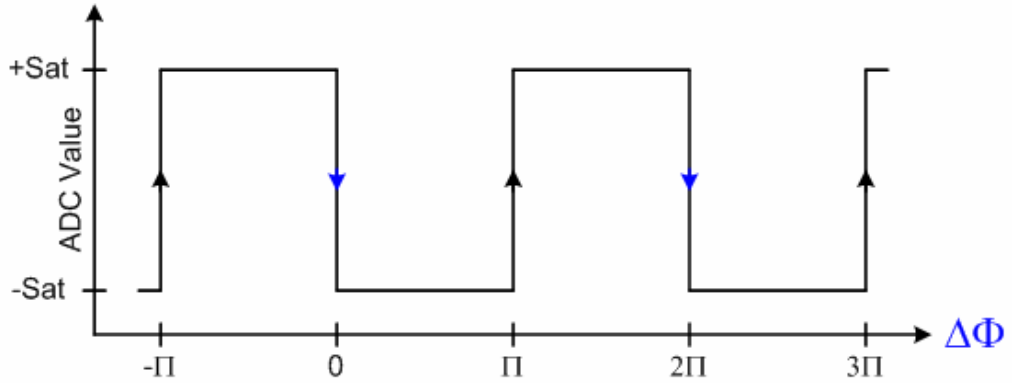


Frequency Reference, Time and Trigger Distribution Scheme

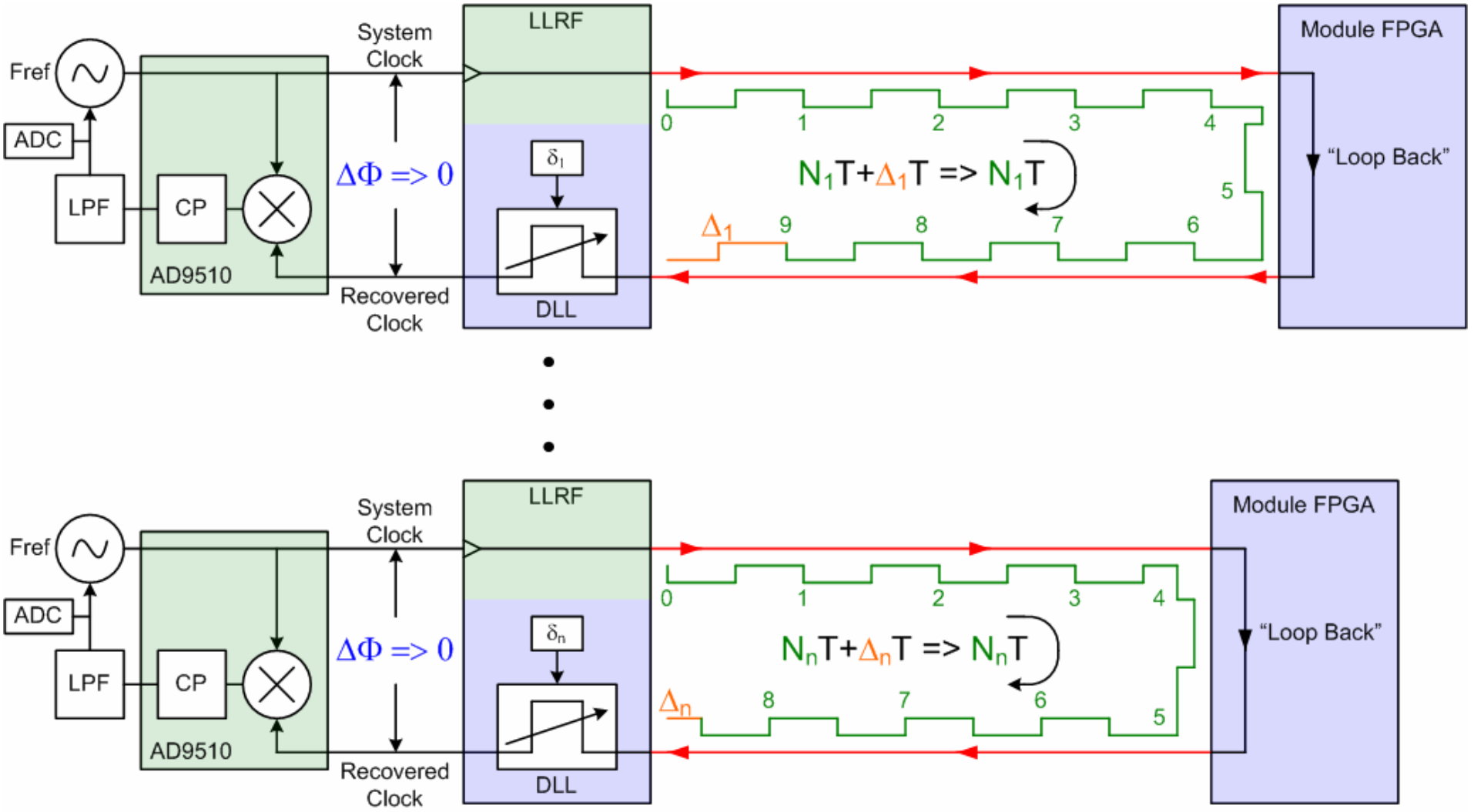


Frequency Reference, Time and Trigger Distribution Scheme

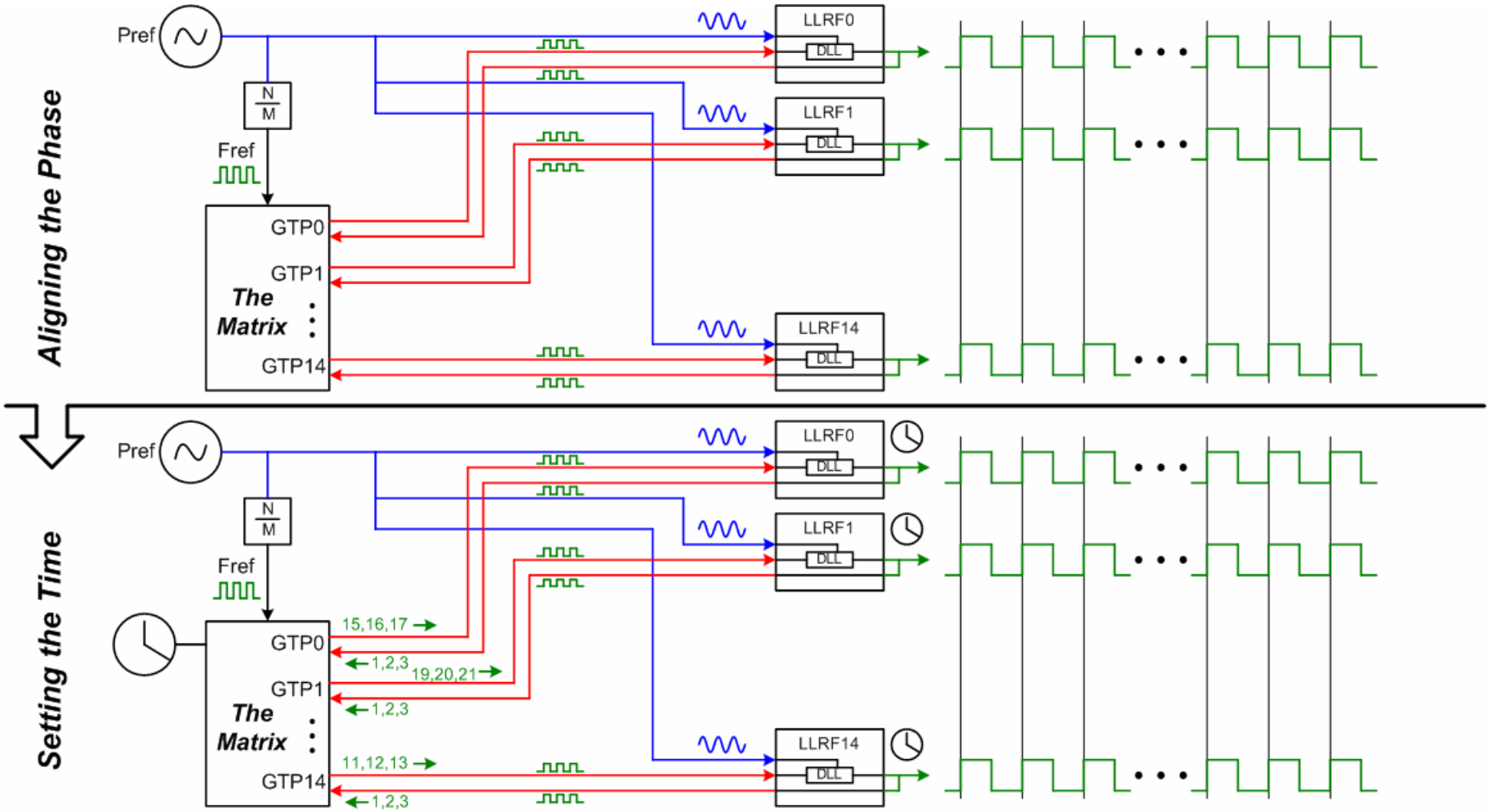




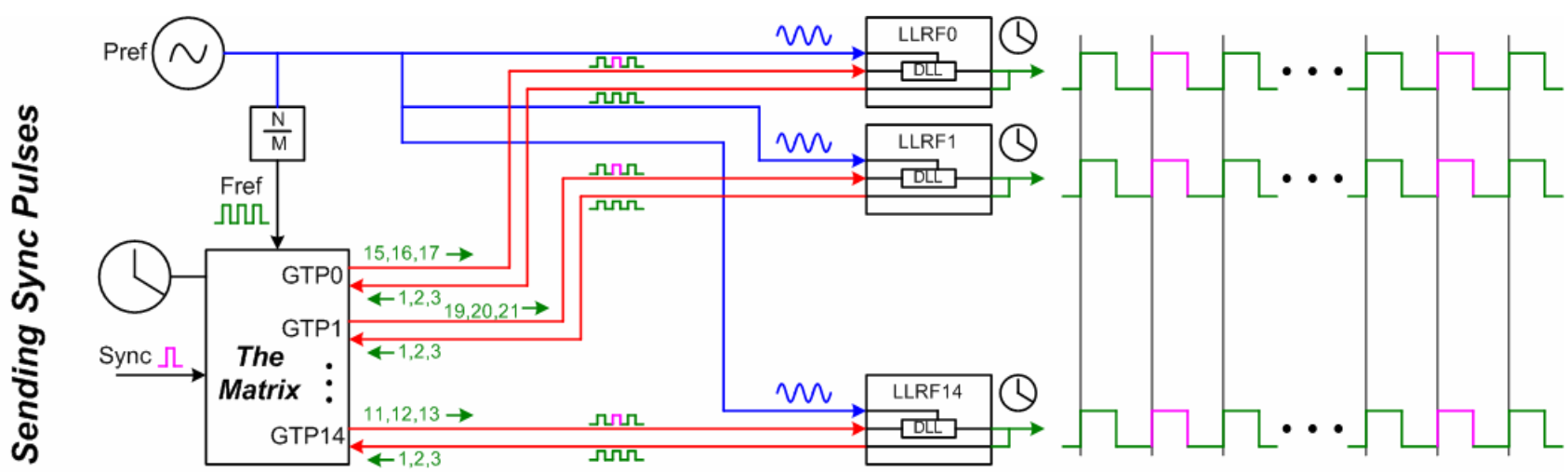
Frequency Reference, Time and Trigger Distribution Scheme



Frequency Reference, Time and Trigger Distribution Scheme



Frequency Reference, Time and Trigger Distribution Scheme



Requirements at Receiver:
- **FPGA with high speed serial I/O**
- **External PLL with good VCO**

Requirements at Master:
- **FPGA with multiple high speed serial I/O's**

What you get:
- **Frequency Recovery (at noise quality of VCO)**
- **Line length drift compensation**
- **Multiple FPGA clocks aligned to 1/256 of a cycle (16 ps @ 240 MHz)**
- **Time accurate to 1/256 of a cycle (for stamping and event scheduling)**

Conclusion: Live a better life through FPGA's!