Synchronization over Ethernet

Standard for a Precision Clock Synchronization Protocol according to IEEE 1588

Synchronous Ethernet according to ITU-T G.8261

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Who is
ZHAW – Zurich University of Applied Sciences?

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- The School of Engineering is a department of the Zurich University of Applied Sciences (ZHAW)
- ZHAW‘s Institute of Embedded Systems has a strong commitment to industrial communications in general and to Ethernet in particular, e.g.
  - Real-time Ethernet (Ethernet Powerling, ProfiNet, etc.)
  - Synchronization (IEEE 1588)
  - High-availability Ethernet add-ons (MRP, PRP, etc.)
- The related R&D activities and services include
  - Hardware assistance and off-load (IP)
  - Protocol stacks
  - Support
  - Engineering and consultancy

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Preliminary remark

- only Ethernet solutions are taken into account in this presentation (according to workshop planning)
- this requires some compromises to be accepted
- the big advantage to be exploited is that the same infrastructure can be used for both data transmission and synchronization

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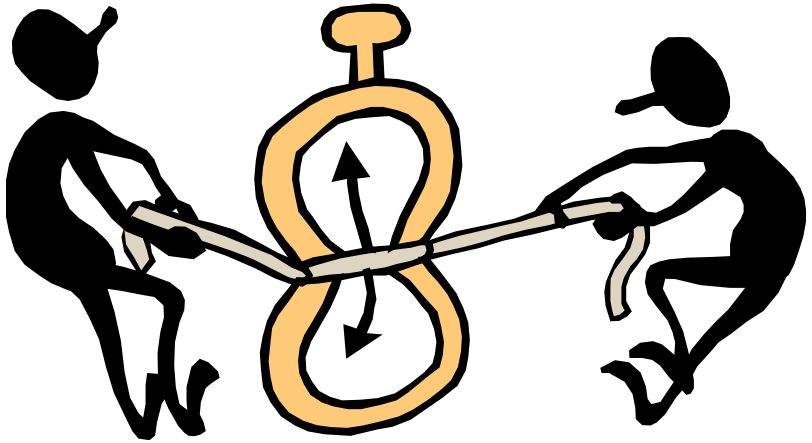
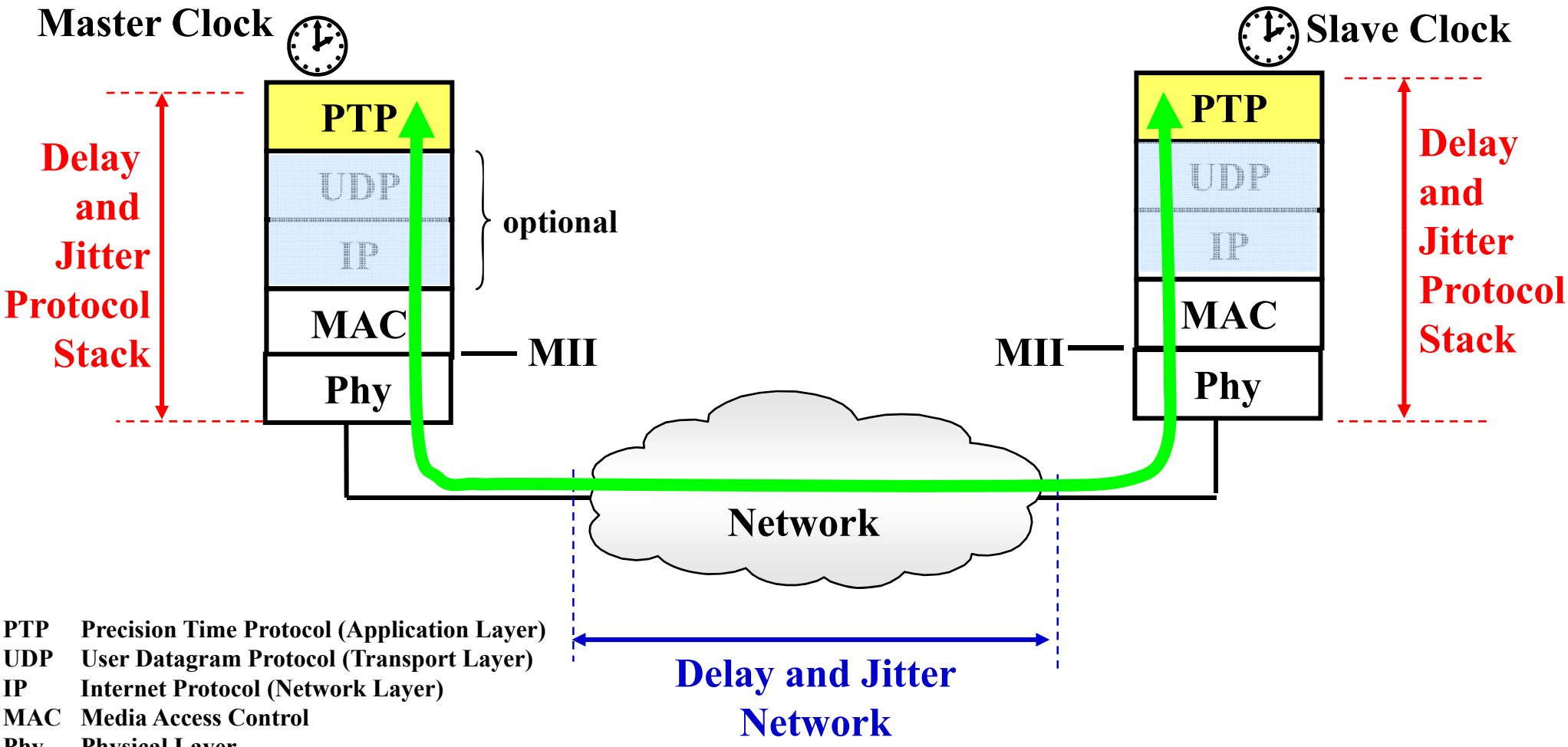
The Standard IEEE 1588



The Standard IEEE 1588

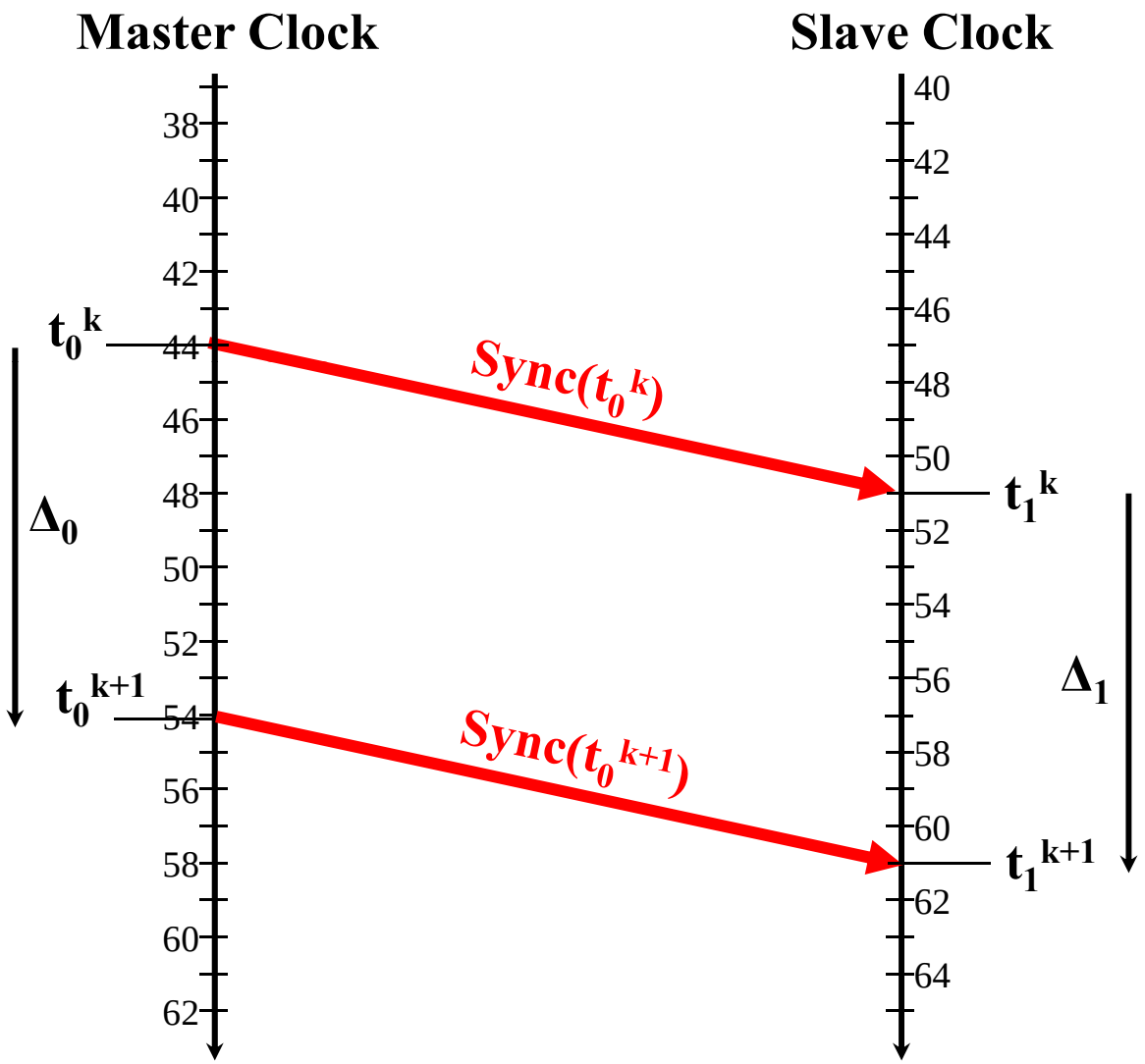
PTP Message Exchange



PTP	Precision Time Protocol (Application Layer)
UDP	User Datagram Protocol (Transport Layer)
IP	Internet Protocol (Network Layer)
MAC	Media Access Control
Phy	Physical Layer

The Standard IEEE 1588

Determination of Phase Change Rate (Drift) – one step



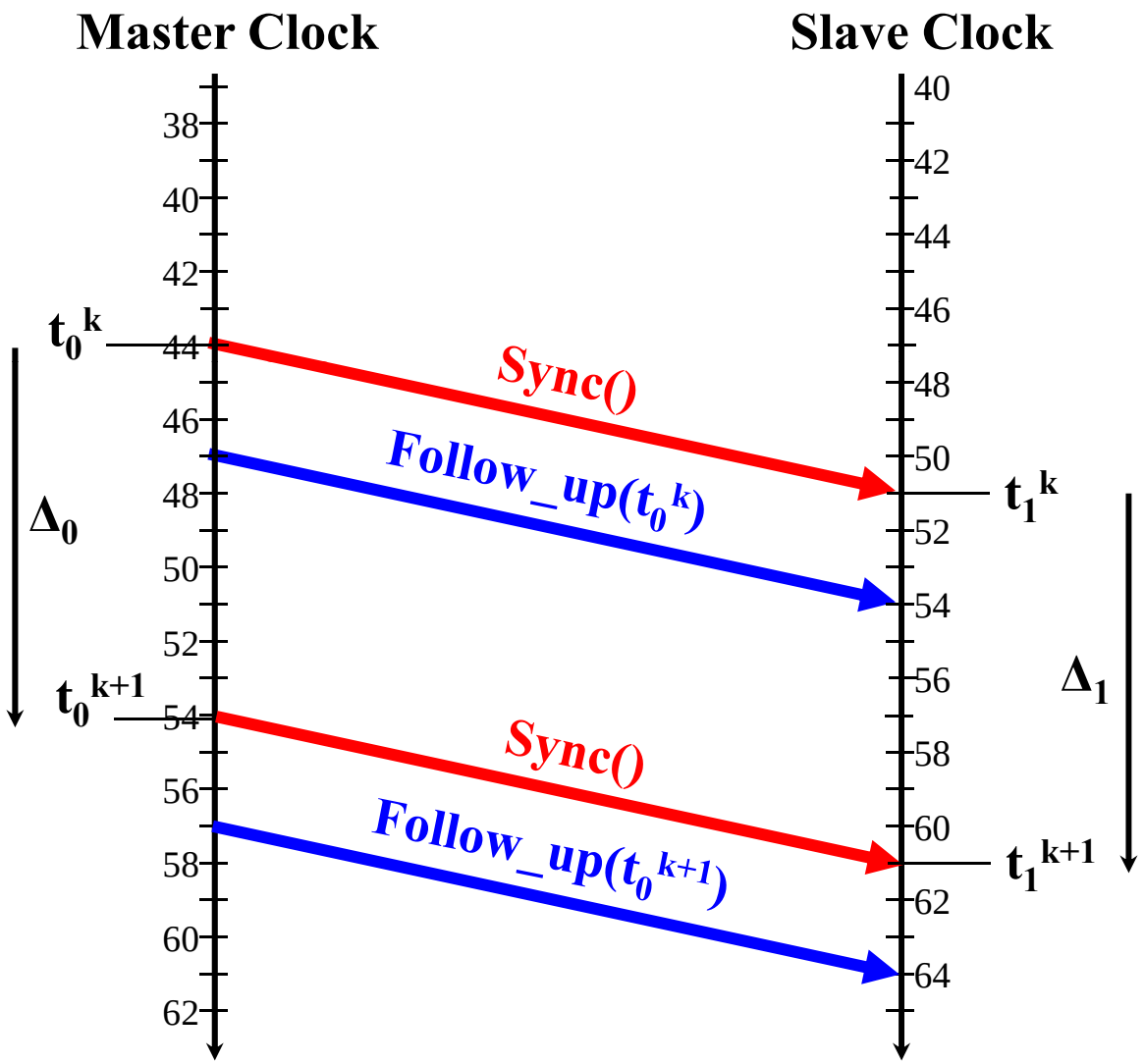
$$\Delta_0 = t_0^{k+1} - t_0^k$$

$$\Delta_1 = t_1^{k+1} - t_1^k$$

$$\text{Drift} = \frac{\Delta_1 - \Delta_0}{\Delta_1}$$

The Standard IEEE 1588

Determination of Phase Change Rate (Drift) – two step



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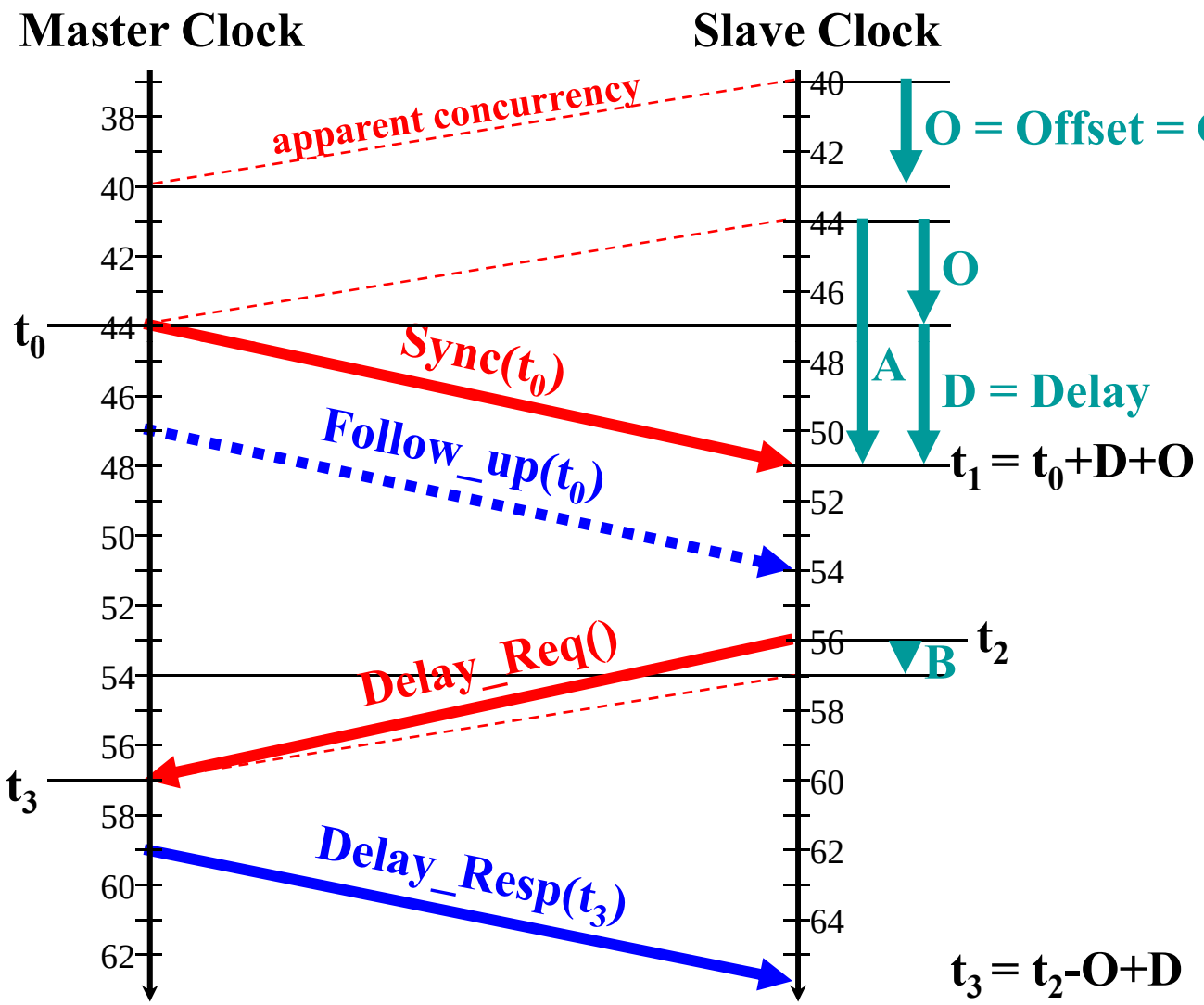
The Standard IEEE 1588

Determination of Delay and Offset



measured values t_0, t_1, t_2, t_3

$A = t_1-t_0 = D+O$

$B = t_3-t_2 = D-O$

$$\text{Delay } D = \frac{A+B}{2}$$

$$\text{Offset } O = \frac{A-B}{2}$$

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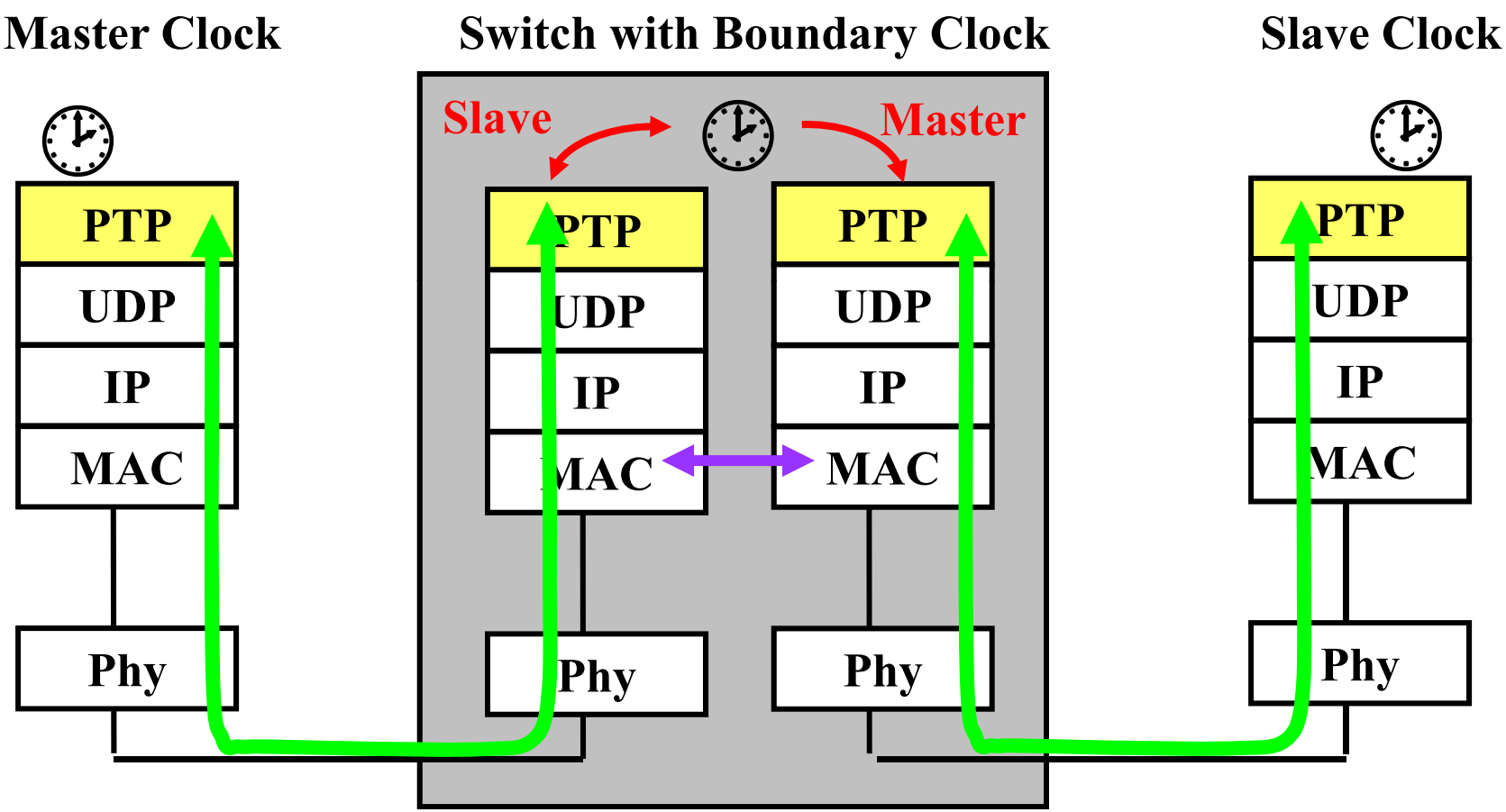
Boundary Clock copes with the Network's Delay Fluctuations



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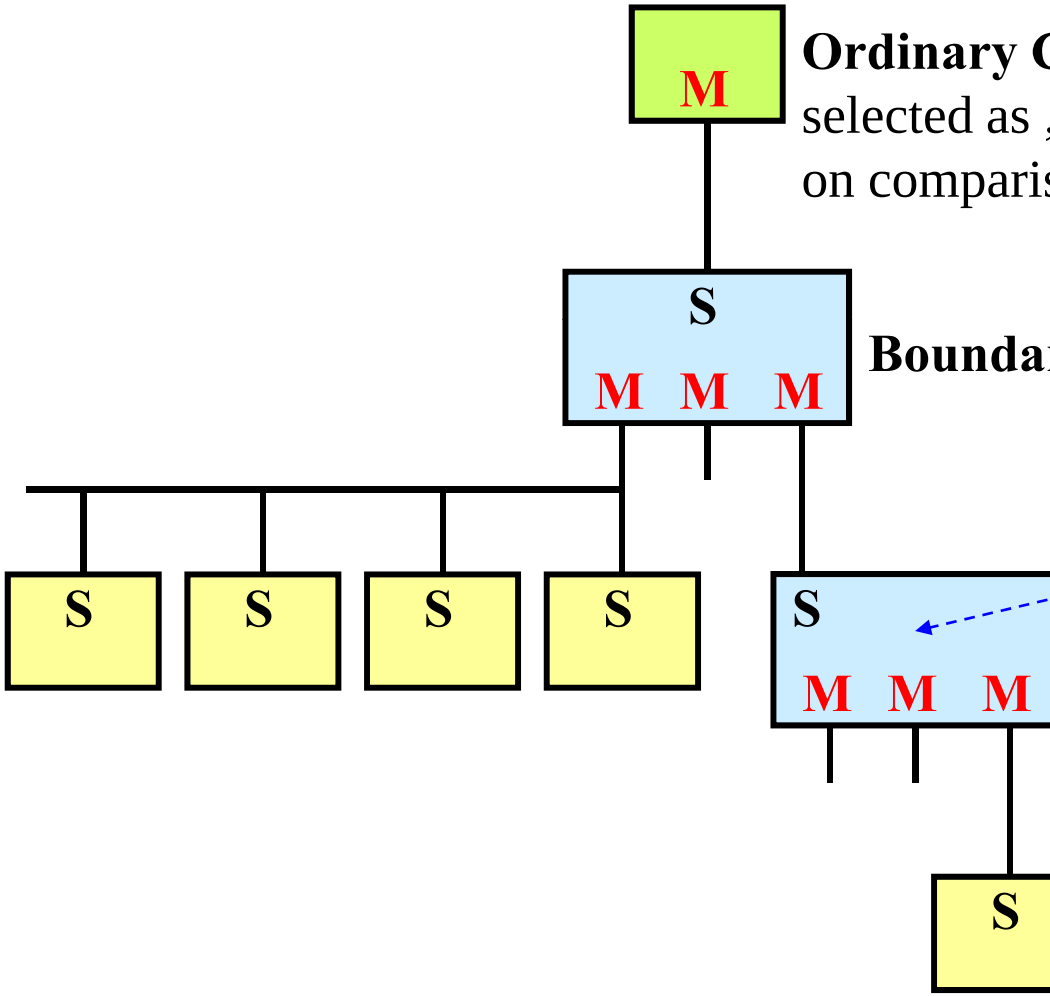
Topology and „Best Master Clock“



Ordinary Clock, Grandmaster: clock selected as „best Master“ (selection based on comparison of clock descriptors)

Boundary Clock, e.g. Ethernet switch

S: Port in Slave State
M: Port in Master State

Ordinary Clock

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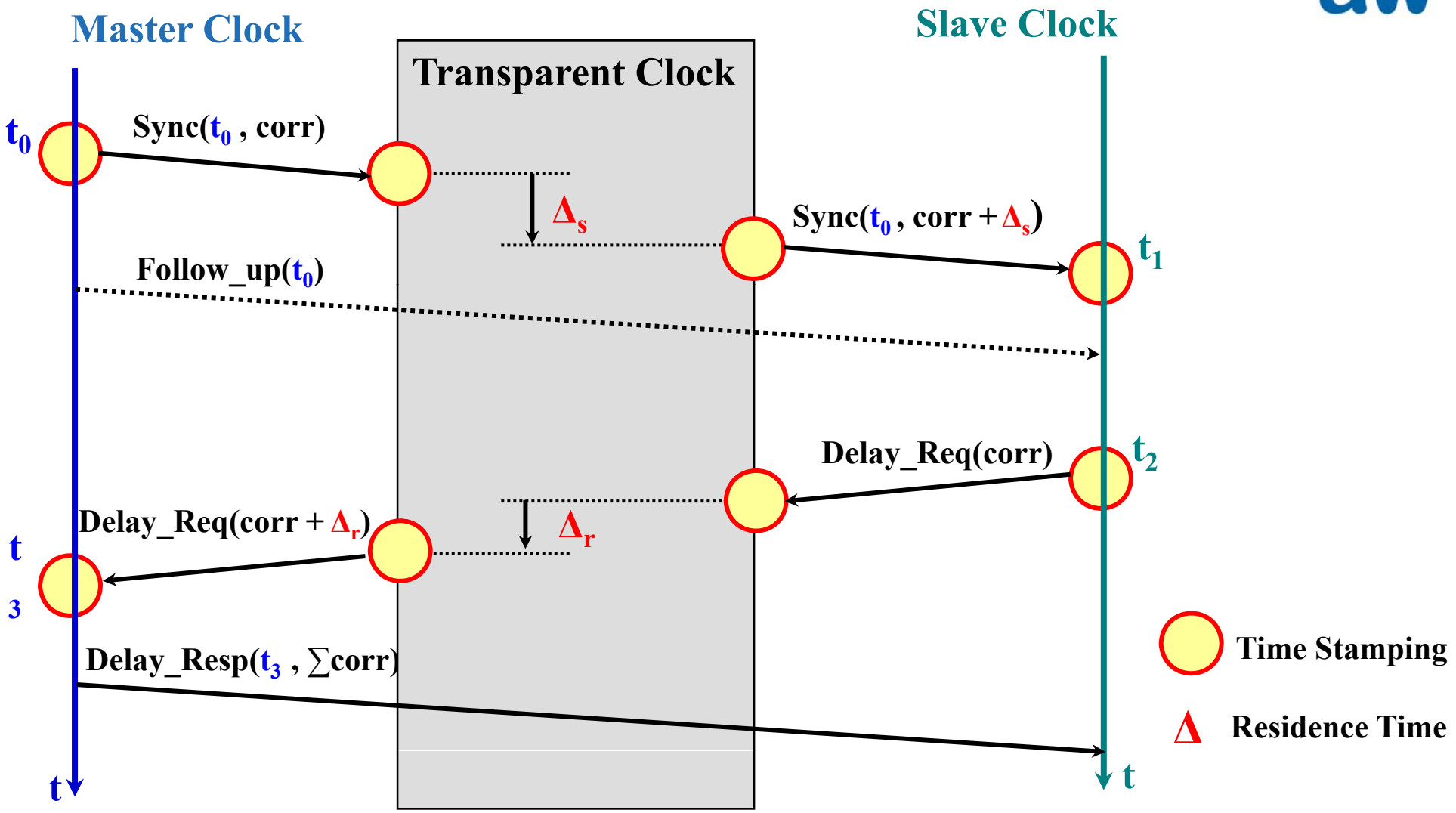
Transparent Clock



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Transparent Clock – End-to-End Delay Measurement

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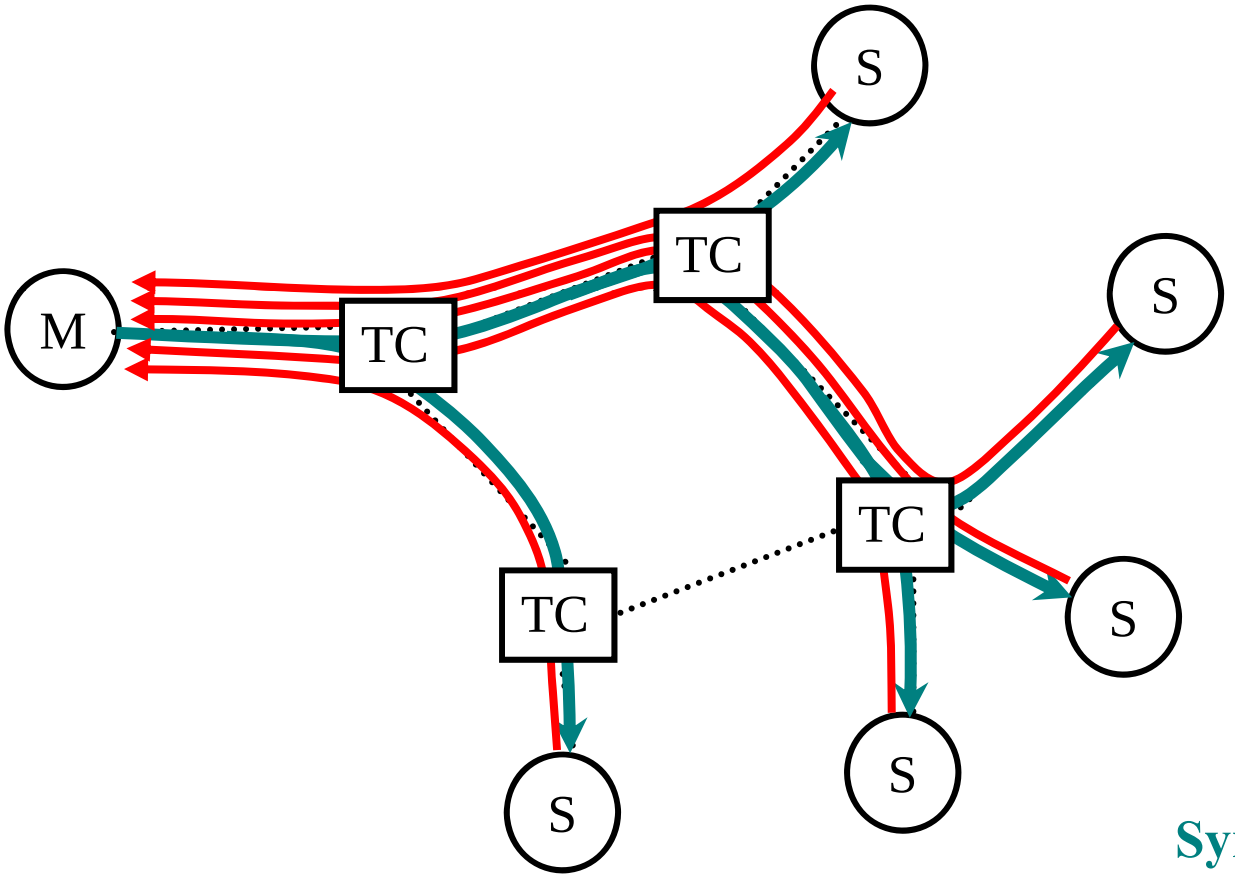

Sync Stream

e2e Delay Measurement

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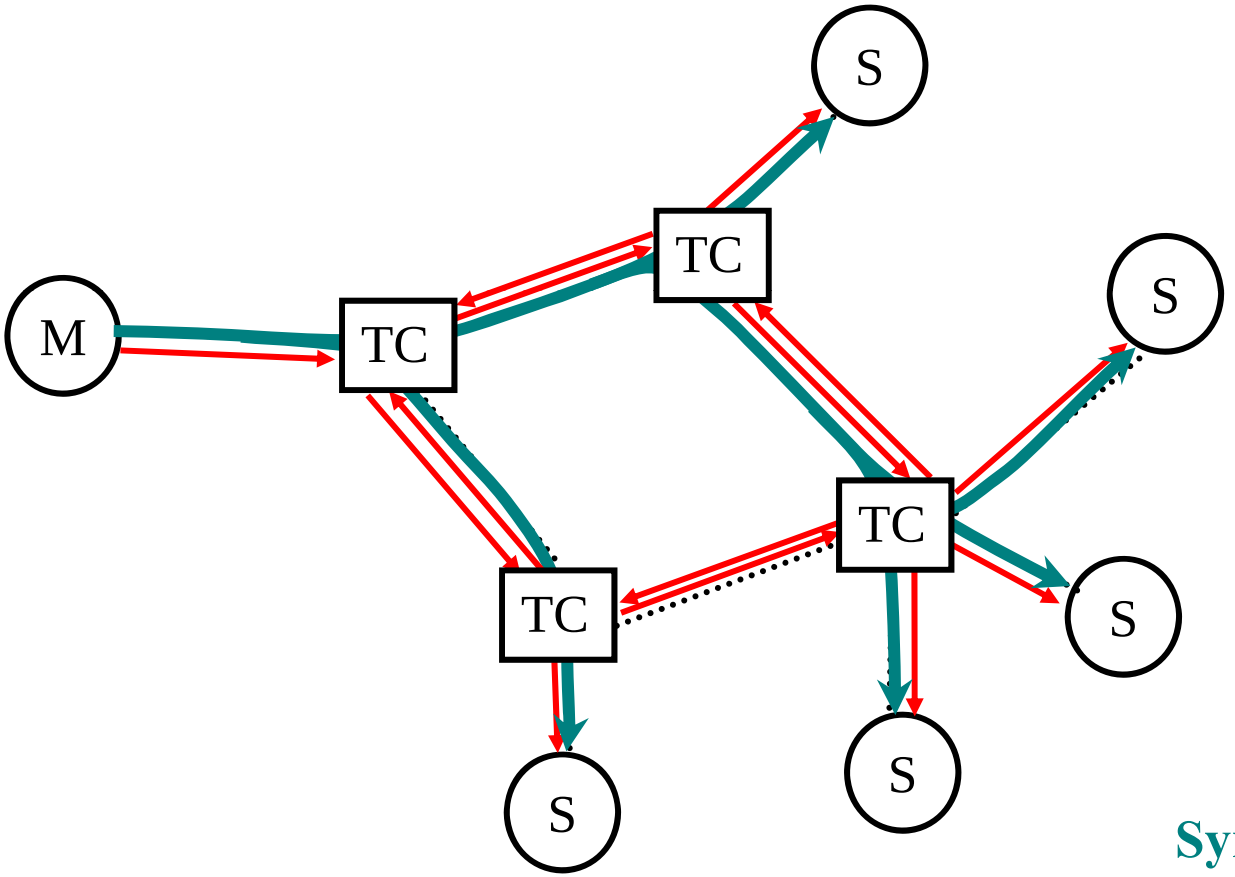
Transparent Clock – Peer-to-Peer Delay Measurement



Sync Stream

p2p Delay Measurement

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Limits

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- Timestamp quantization effects
- Accuracy of Start-of-Frame Detection
- Unknown portion of data path asymmetries in cables and transceivers
- Jitter in the data path (PHY chips, network elements)
- Environmental conditions
- Oscillator instabilities
- Implementation specific effects (e.g. phase between different asynchronous clock domains of all involved functional building blocks)
- Note: Uncertainty due to limited observation capabilities (e.g. the PPS output is subject of quantization effects as well)

→ Stochastic effects can be filtered out with statistical methods

→ Systematic errors remain

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Industry Relevance

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- PTP is or will be applied in application areas such as
  - Test and Measurement (LXI: LAN eXtensions for Instrumentation)
  - Automation and control systems (various flavors of real-time Ethernets)
  - Audio/Video Bridge (AVB according to IEEE 802.1as)
  - Telecommunications
- Silicon vendors and IP providers offer
  - Protocol software
  - Hardware assistance IPs
  - PHYs with hardware assistance logic
  - IEEE-1588 enabled microcontrollers
  - Switching cores with IEEE-1588 support

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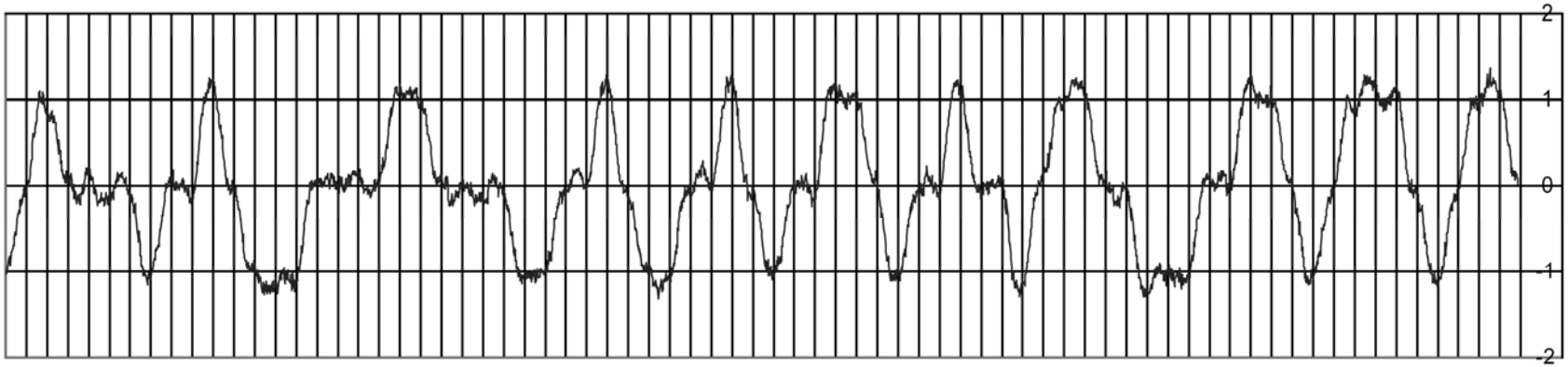
Synchronous Ethernet



Synchronous Ethernet

Physical Layer Timing in Legacy Ethernet

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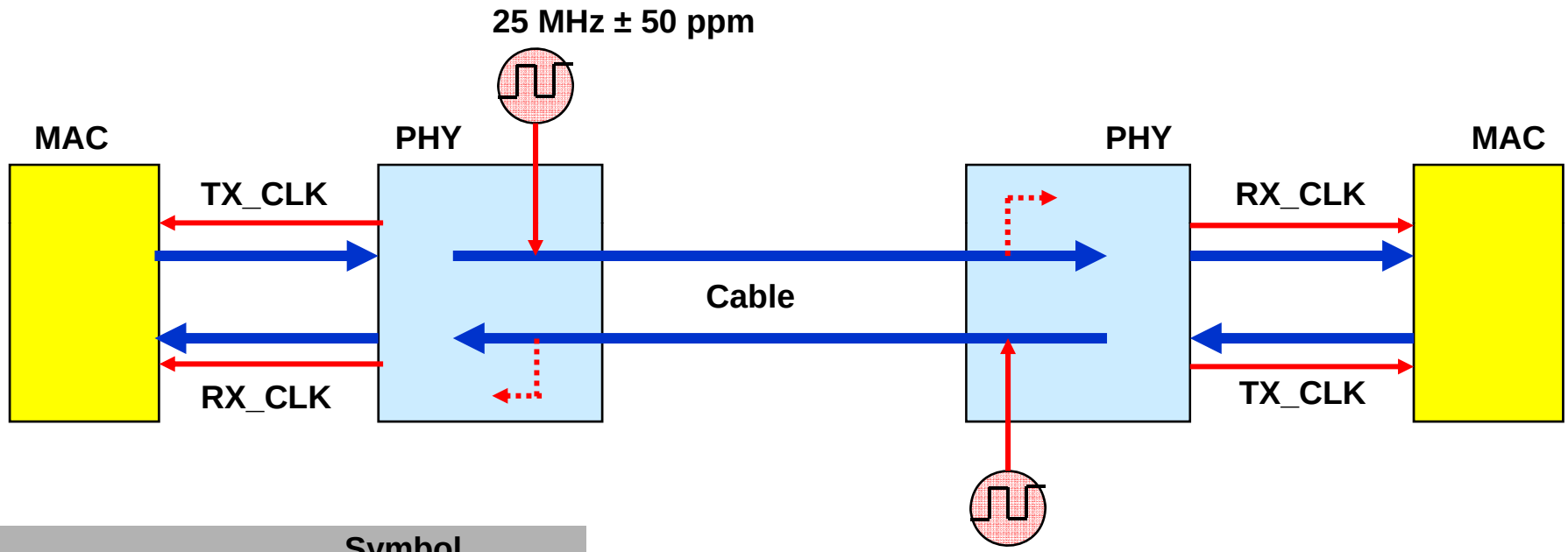
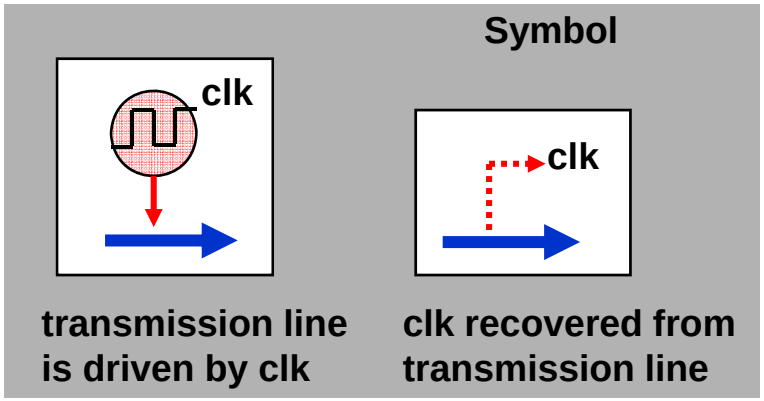
- **Ethernet works perfectly well with relatively inaccurate clocks**
- **Each Ethernet link may use its own clock**
  - **nominal clock rate is the same, but deviations of ± 50 ppm are allowed (dimensioning such that physical layer buffers do not underflow or overflow)**
- **Details differ according to transmission technology**
  - **where the two directions of a link use different media (i.e. separate wire pairs or separate fibers), both directions may have independent clocks**
  - **GBE over twisted pair uses all wire pairs simultaneously in both directions → signal processing (echo compensation technique) requires same clock on both directions of a link → one PHY acts as the master, the other as slave**

Synchronous Ethernet

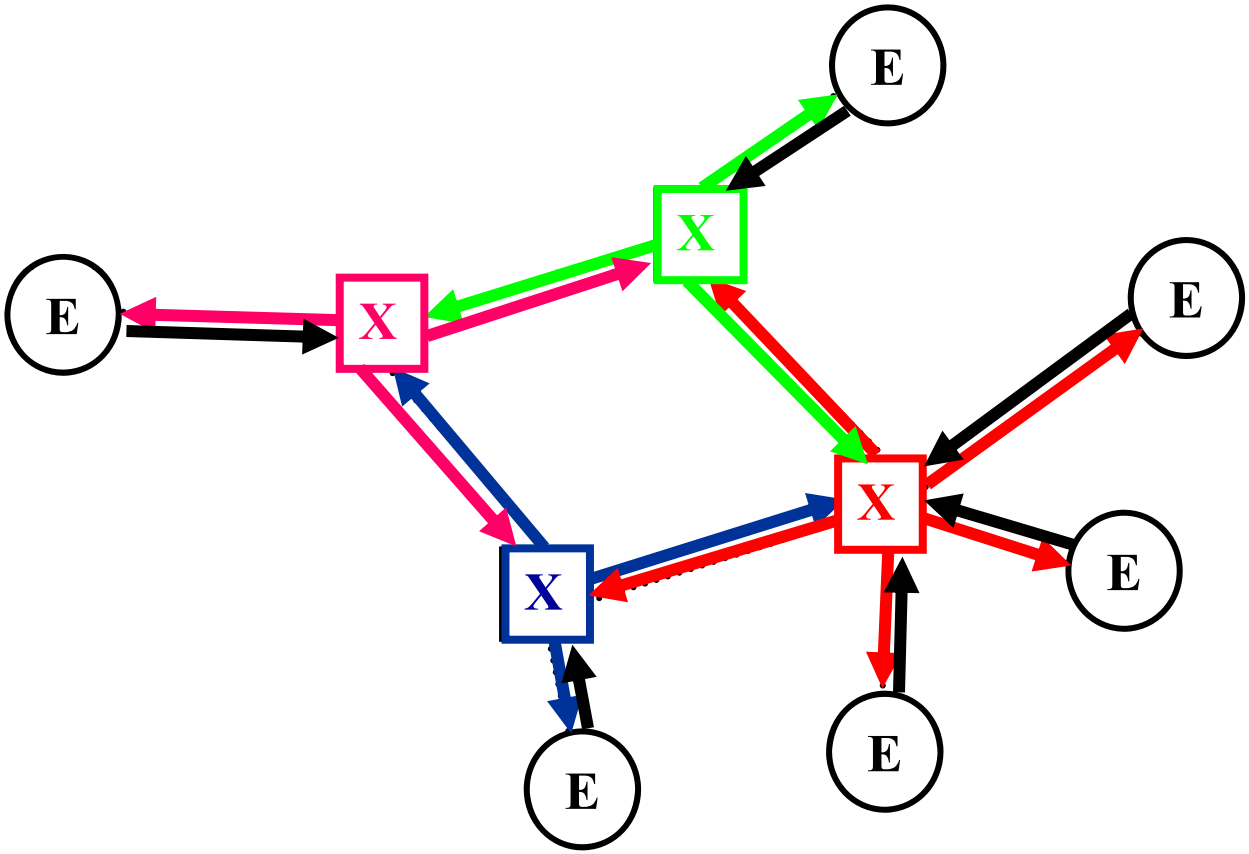
Timing of a Fast Ethernet Link (100 Base-TX)





Synchronous Ethernet

Physical Layer Timing in Legacy Ethernet



Synchronous Ethernet

Timing of a Gigabit Ethernet Link (1000 Base-T)

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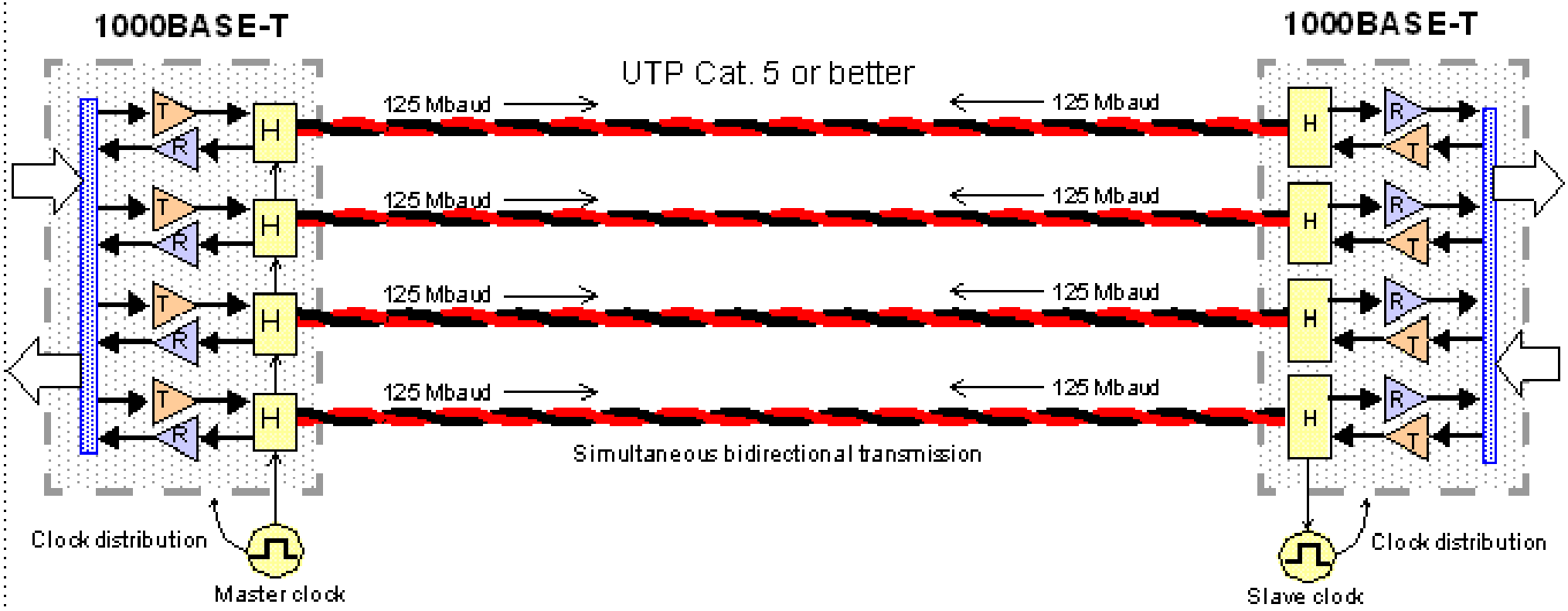
- 1000 Base-T transmission is split on 4 wire pairs operation simultaneously in both directions
  - transmitter and receiver are coupled via a hybrid
  - echo compensation is applied
  - both directions require the same clock
- A 1000 Base-T PHY can operate as a master or slave.
- Master/slave role selection is part of the auto-negotiation procedure.
- A prioritization scheme determines which device will be the master and which will be slave.
- The supplement to Std 802.3ab, 1999 Edition defines a resolution function to handle any conflicts:
  - multiport devices have higher priority to become master than single port devices.
  - if both devices are multiport devices, the one with higher seed bits becomes the master.

Synchronous Ethernet

1000 Base-T uses 4 pairs simultaneously in both directions



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1000 Base-T Pysical Layer Signalling with Echo Compensation

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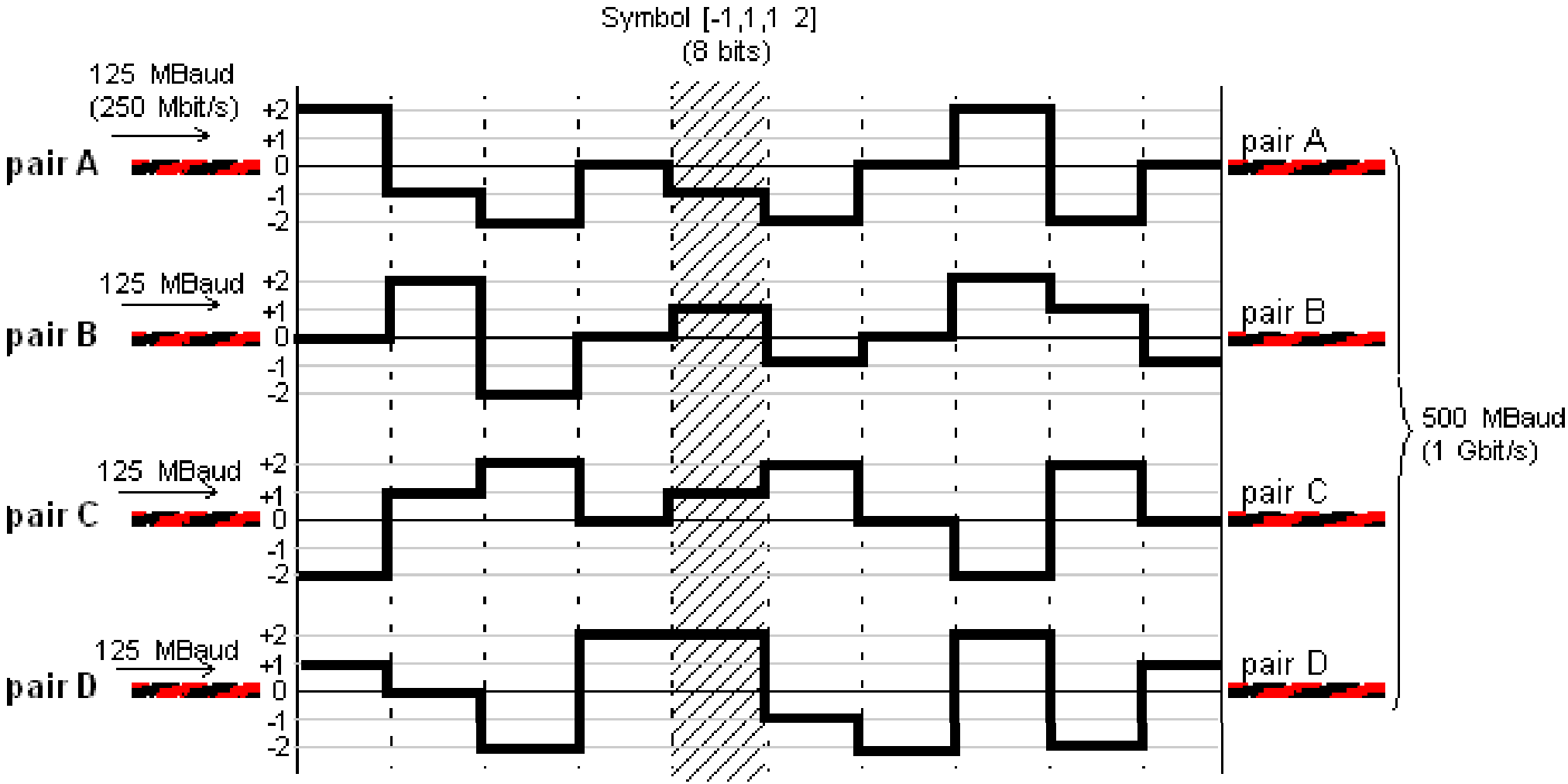
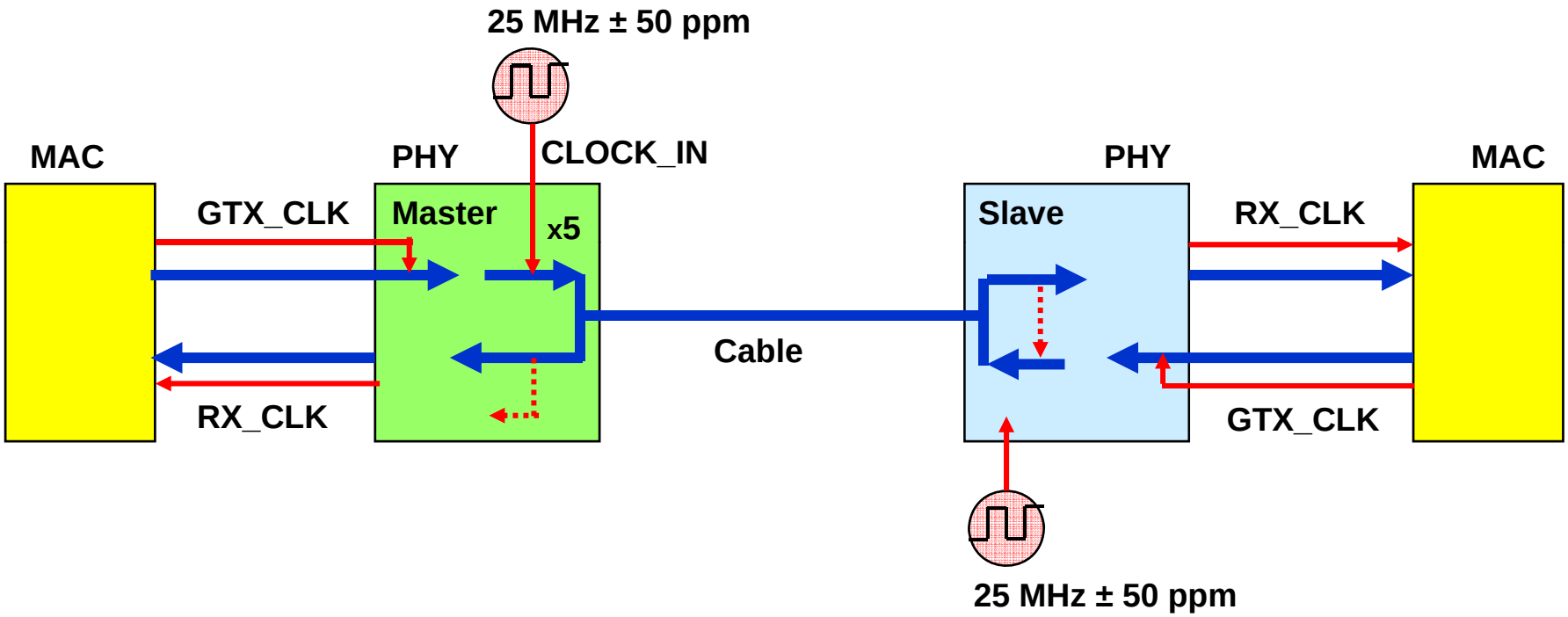


Synchronous Ethernet

Timing of a Gigabit Ethernet Link (1000Base-T)



- The Master PHY uses the internal 125 MHz clock generated from CLOCK_IN to transmit data on the 4 wire pairs.
- The Slave PHY uses the clock recovered from the opposite PHY as the transmit clock.

Synchronous Ethernet
Concept - 1

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- Concept has been proposed, elaborated, and standardized by the Telco community in ITU-T by transferring the traditional SDH clock distribution concept to Ethernet networks
- The Primary Reference Clock (PRC) frequency is distributed on the physical layer
  - a receiver can lock to the transmitter‘s frequency
  - a switch selects the best available clock
  - this results in a hierarchical clock distribution tree
- OAM messages (Synchronization Status Messages) are used to signal clock quality and sync failure conditions of the upstream switch
  - to allow selection of the best available timing source (stratum of upstream source)
  - to avoid timing loops

Synchronous Ethernet
Concept - 2

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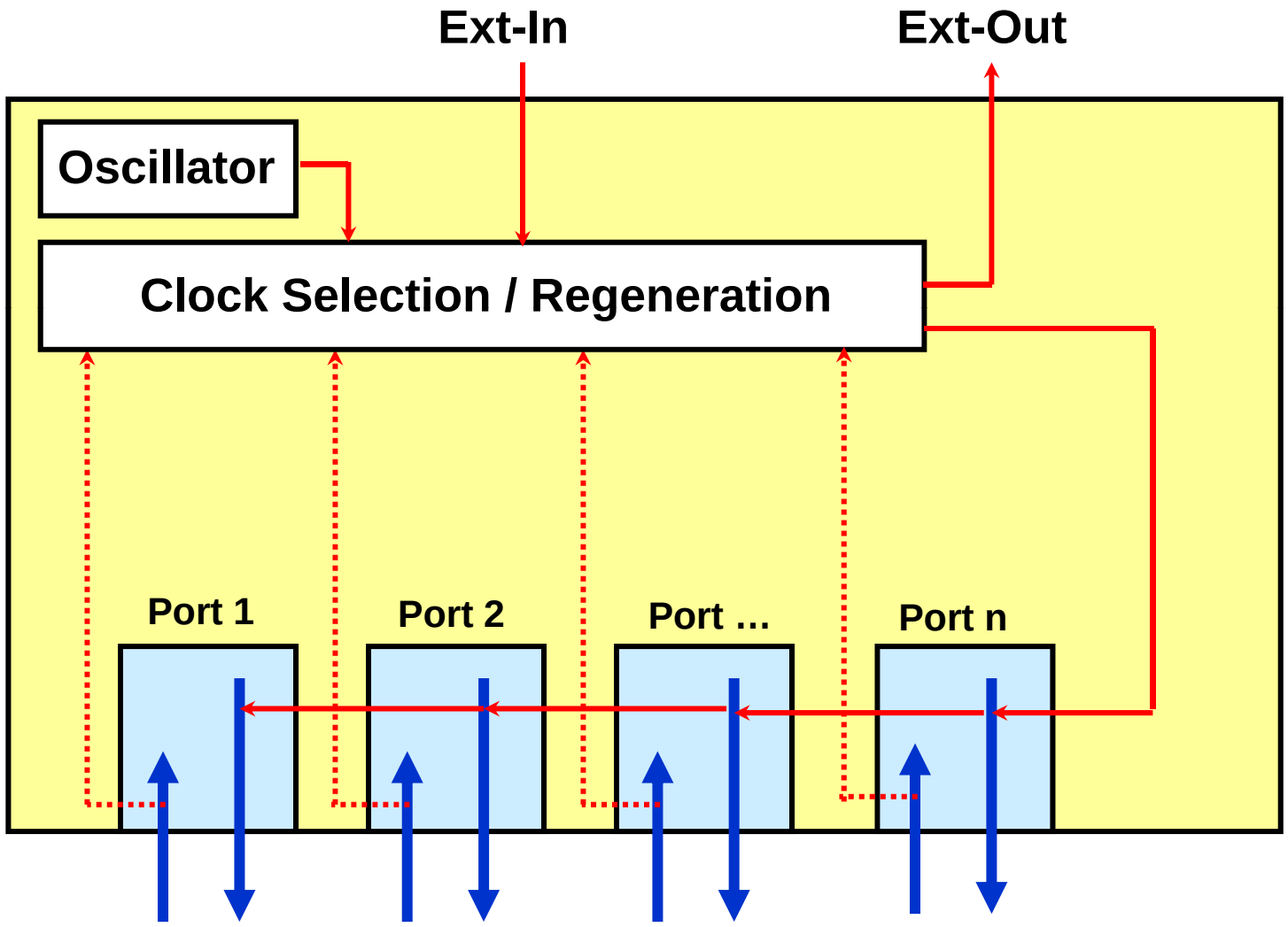
- Active layer 2 data forwarding topology (as established by spanning tree protocol) and clock distribution tree are independent (i.e. a blocked port can deliver the clock to its neighboring switch)
- Design rules (topology restrictions, priorities for source selection) guarantee clock quality
- Clocking of Ethernet devices is changed in a way that is fully conforming with IEEE 802.3 standards
- Standard PHY chips can be used as long as a few conditions are met, e.g.
  - PHY provides the recovered receive clock to the external world
  - GBE PHY allows master/slave role to be set by software (no automatic selection)

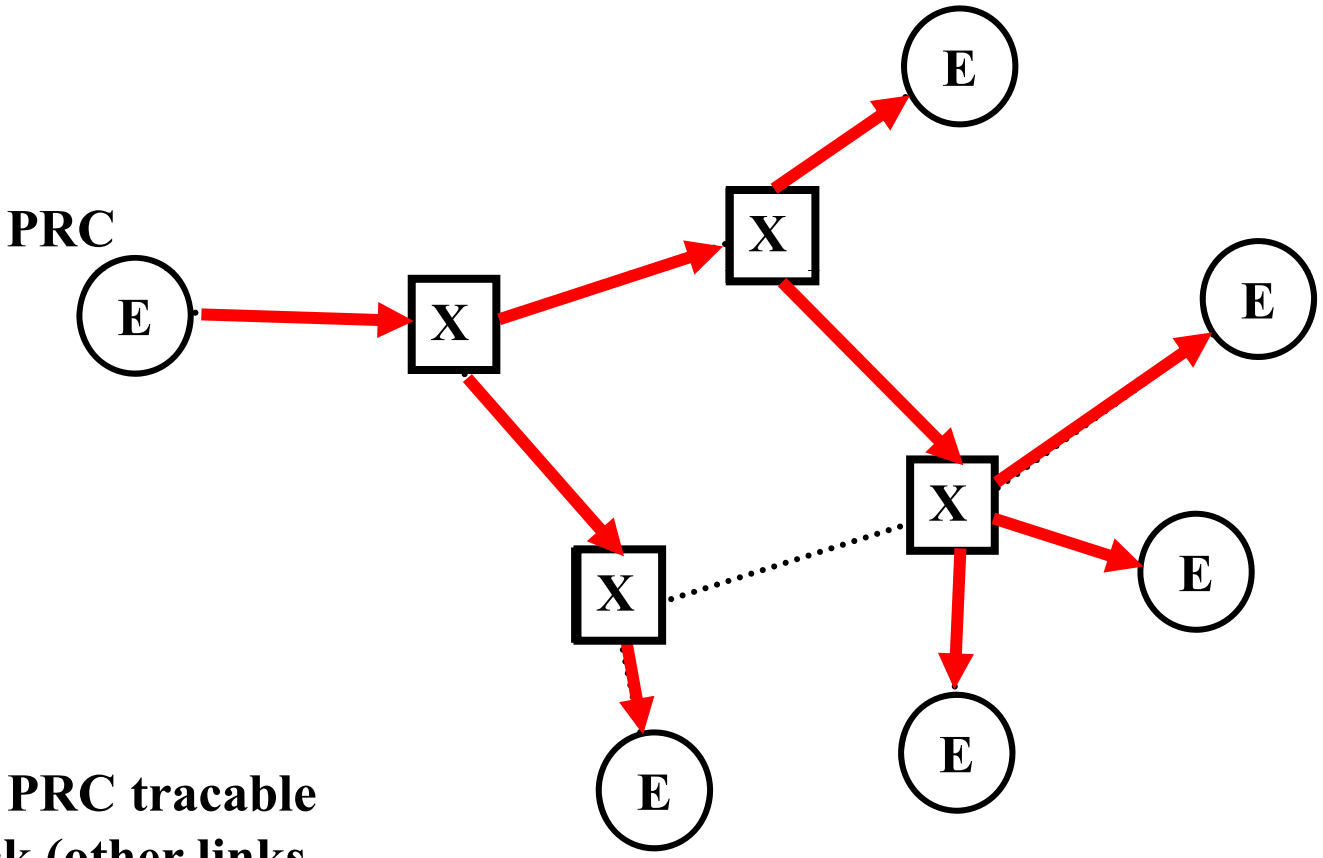
Synchronous Ethernet

Clock Sources for a Synchronous Ethernet Switch



Synchronous Ethernet

Physical Layer Timing in Synchronous Ethernet



PRC tracable clock (other links and directions are free running)

Synchronous Ethernet
Compared with IEEE 1588

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Synchronous Ethernet

- Clock distribution based on Ethernet's physical layer
- Provides frequency only
- Performance is independent of data traffic

IEEE 1588

- Application layer protocol with hardware assistance
- Provides frequency and time of day
- May be susceptible to specific data traffic patterns

Complementary technologies, can be used in combination:

Syncronous Ethernet delivers accurate and stable frequency to all nodes while IEEE 1588 can deliver time of day, where required.

Synchronous Ethernet
Industry Relevance

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- Telco equipment manufacturers rely on both technologies
- Synchronous Ethernet operation will certainly be an important feature in future carrier grade products
- Synchronous Ethernet's role in corporate and industrial communication application is not yet forseeable
- Silicon vendors and IP providers offer
  - Synchronous Ethernet compatible PHYs
  - ICs for clock monitoring, selection, and processing

Many thanks for your attention!

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