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3D integration activities at Bonn/CPPM

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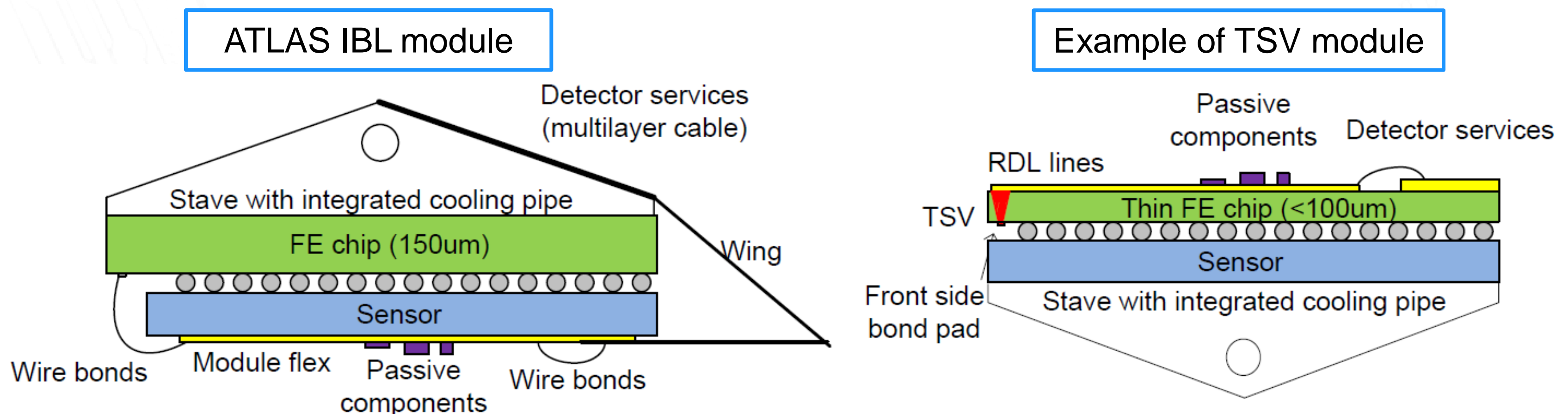
Bonn/CPPM project

- The goal of the project is to develop modules for ATLAS pixel detector at the HL-LHC using a via last TSV process
  - Post-processing technology applicable on existing FE electronics
  - Dead area at the chip periphery can be reduced

→ Compact, low mass hybrid pixel modules with minimal modification to the FE layout and using standard CMOS technology

→ Potential for 4 side abuttable modules using dedicated sensor layout

- Modules with TSV can be used for the outermost detector layers at the HL-LHC to provide full detector coverage over the large area



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Current via last TSV project

- Long term relationship between UBonn and IZM Berlin
  - IZM is the main bump bonding vendor for the ATLAS pixel detector & IBL
  - Many developments for future module concepts have been addressed: MCM-D, thin chip modules, low cost assemblies, …

- Two via last TSV processes from IZM have been demonstrated on monitor wafers: tapered side wall and straight side wall TSV → both processes work
- IZM integrates the TSV process into the bump bonding process (make TSV first and afterwards do BB)
- We profit from ultra thin (< 100µm) flip chipping (developed for bumped FE-I4 chips for the ATLAS IBL)

- The tapered side walls TSV process selected for prototyping with the ATLAS pixel FE electronics

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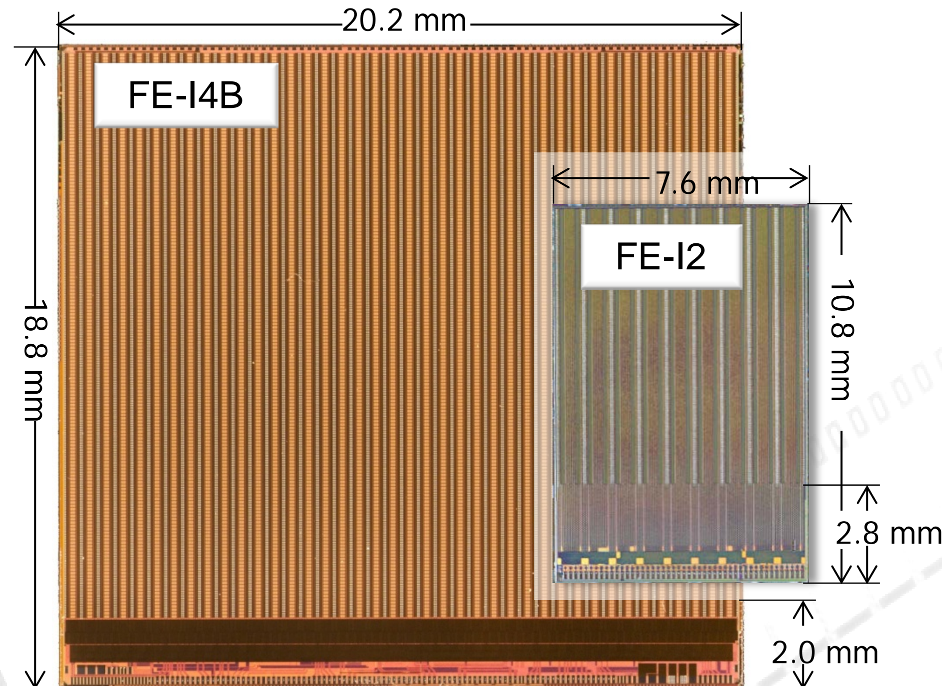
Status

- A batch of 2 FE-I2 wafers has been fully processed
  - FE-I2 is the prototype ATLAS pixel FE chip in 250nm CMOS technology
  - Demonstrator modules with TSV successfully tested
- A batch of 3 FE-I4B wafers currently processed at IZM to prototype TSV modules with the FE technology designed for the ATLAS pixel upgrade
  - FE-I4B is the IBL pixel FE chip in 130nm CMOS technology

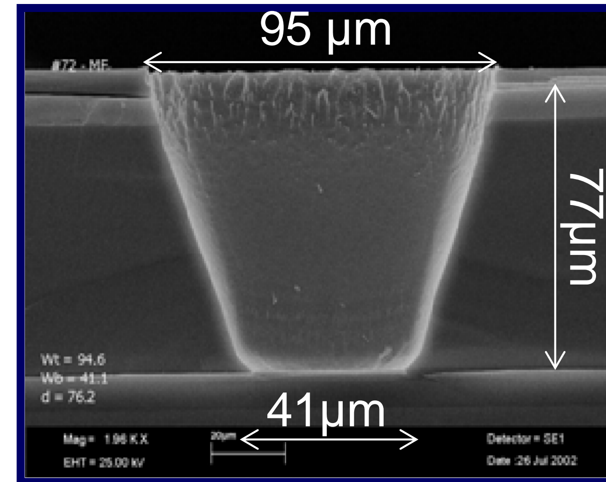


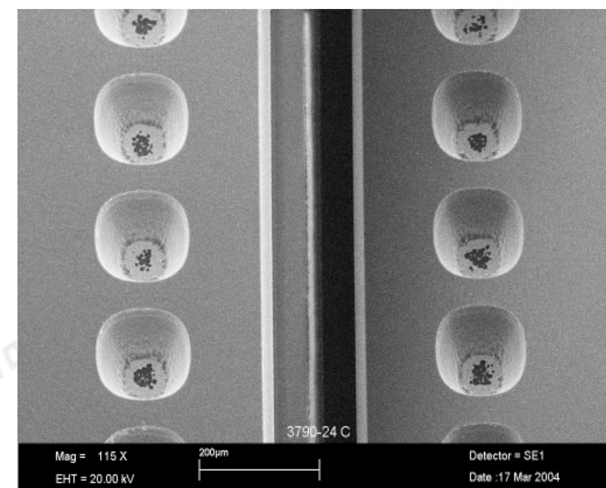
TSV etching with Tapered Side Walls

- Tapered Side Wall TSV
  - Vias are etched in one step and oxide is deposited after etching
  - Simpler deposition process of isolation layer using thin film polymers

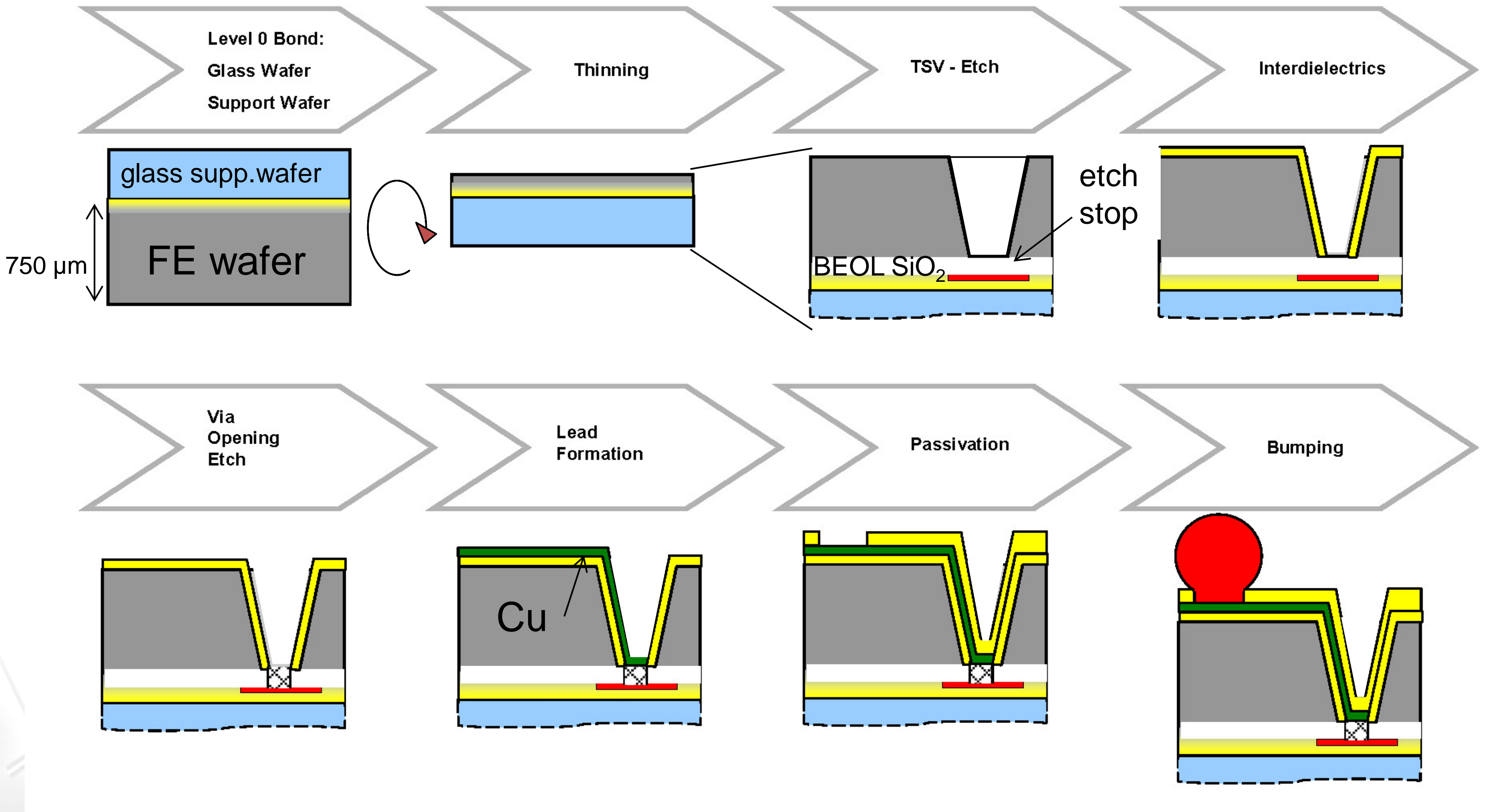
- Tapered walls
  - Side angle 72°
  - In this example
    - Via diameter on the bottom: 41μm
    - Via diameter on the top: 95μm
    - Si thickness: 77μm

Tapered Side Wall TSV on monitor wafer

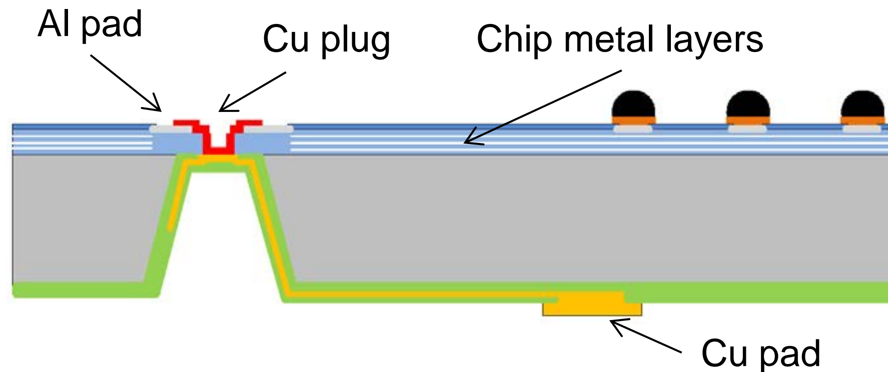


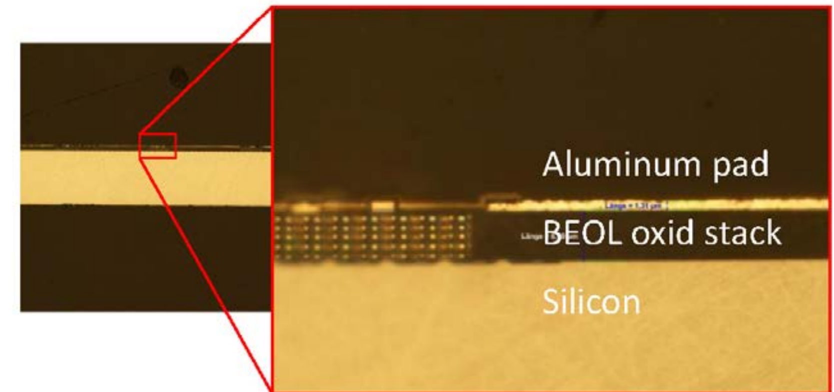


TSV: Main proces flow



Tapered TSV process for ATLAS Pixel FE-I2/3



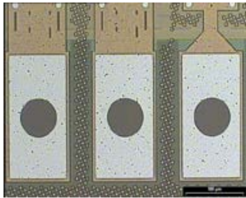


- TSV formed in the peripheral bond pad
  - Pad size of 150µm → Max Si thickness: 100µm
- TSV formation is a back side processing
  - Backside thinning to 90µm
  - TSV etched from the back side until the BEOL SiO_2 stack
- Front side processing to connect TSV bottom to Al pad → Cu plug
  - No metal layers in the pad
  - ~9µm thick BEOL SiO_2 stack technically difficult to etch from the back side through the TSV opening on the bottom

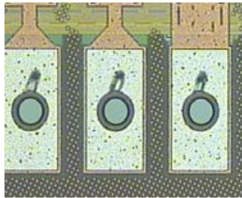
Tapered TSV processing on ATLAS FE-I2/3

Front side processing

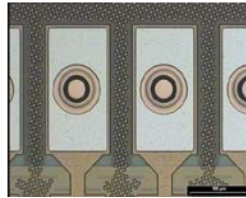
Al pad opening by wet etching



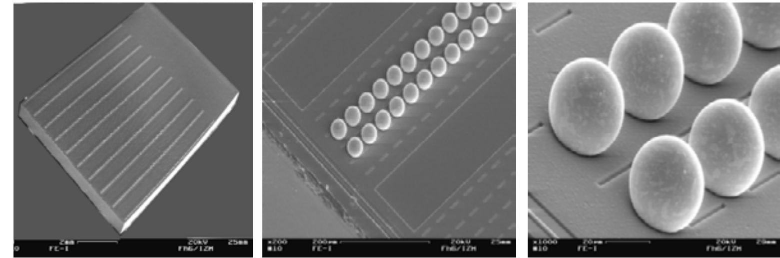
BEOL SiO_2 stack etching



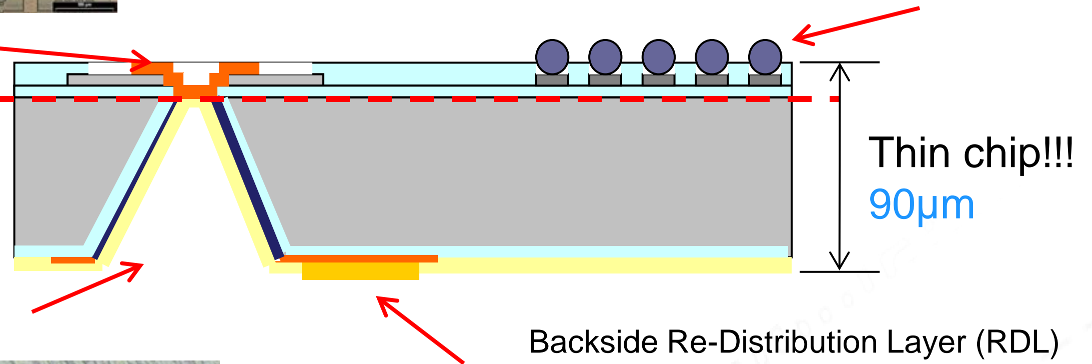
Cu electroplating – interconnection plug to Al pad



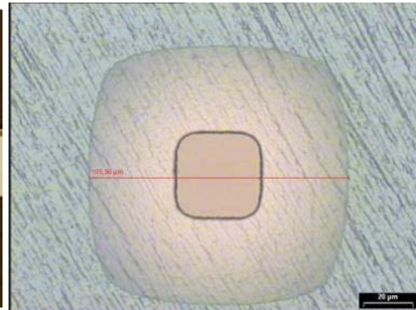
Bump deposition and dicing



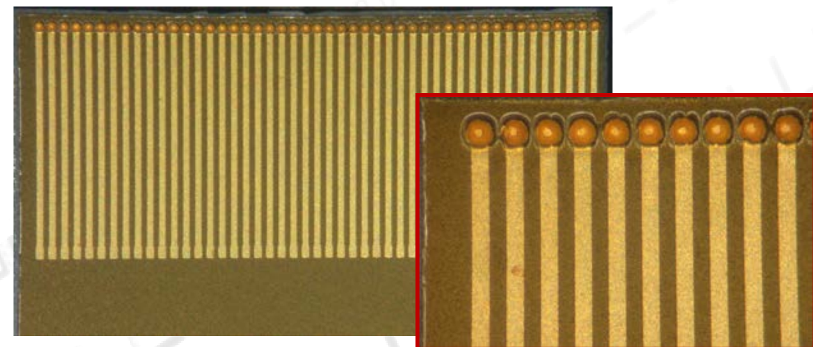
Back side processing



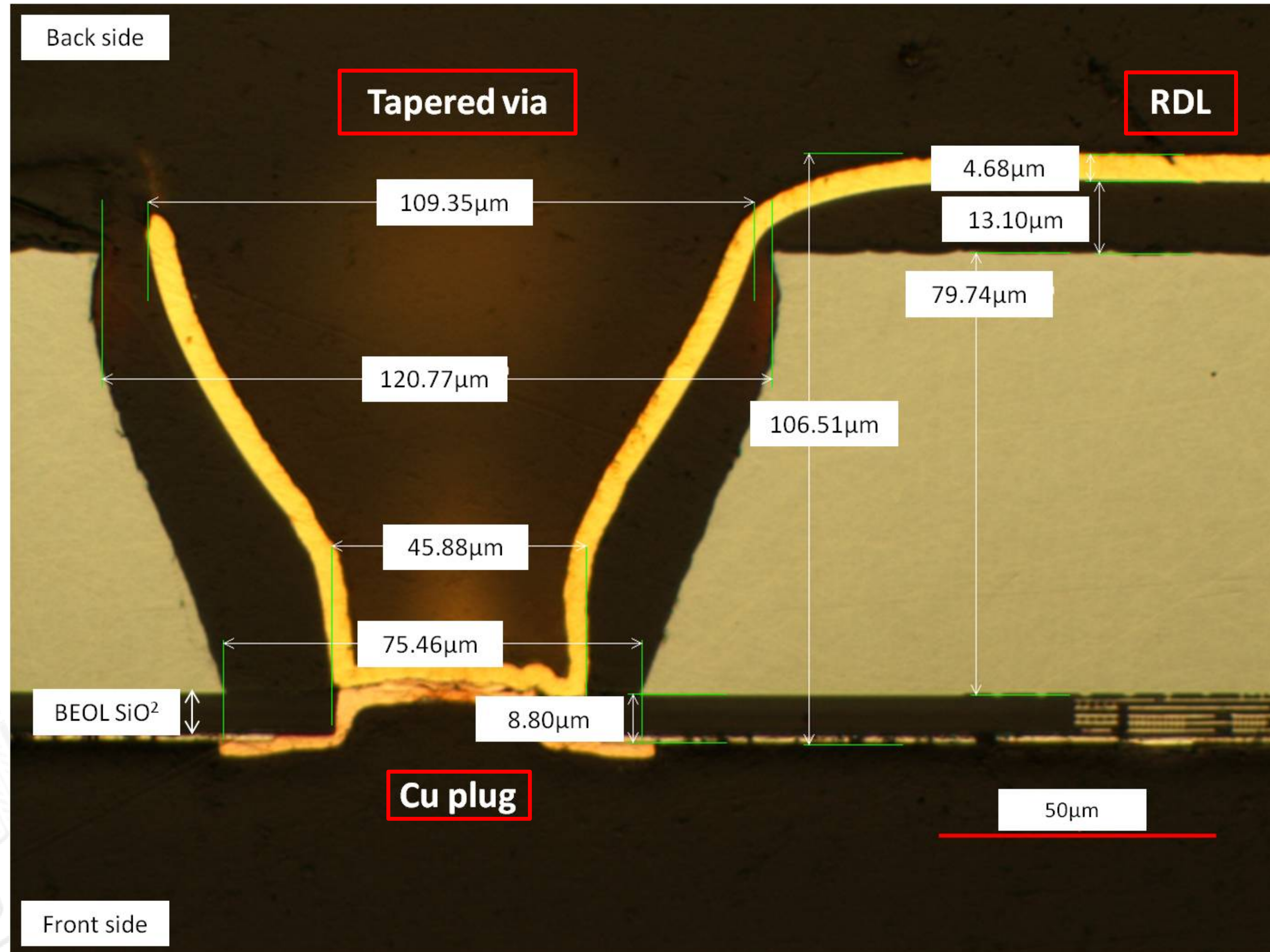
Tapered side walls TSV



Backside Re-Distribution Layer (RDL)



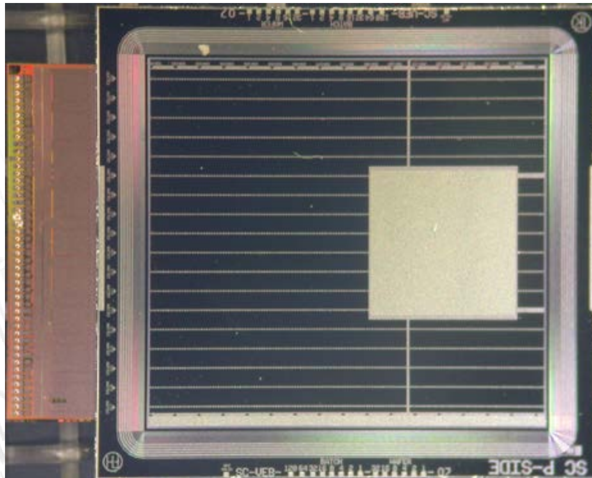
Tapered TSV on ATLAS FE-I2 wafers



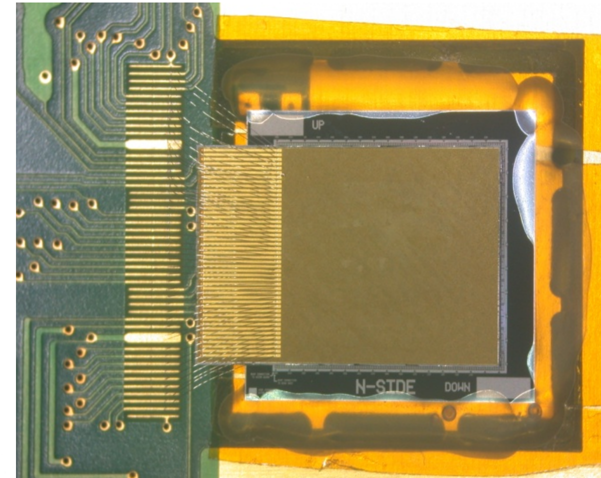
FE-I2 modules with TSV

- Single chip modules build with
  - FE-I2 ATLAS pixel readout chip 90μm thin, with tapered profile TSV and RDL
  - Planar n-in-n sensor
  - Standard flip chip process (no handle wafer for thin chip handling used, unconnected pixels expected along the chip perimeter)
- No loss in performance wrt modules without TSV
- Work published at: http://iopscience.iop.org/1748-0221/7/08/P08008/

Module front side



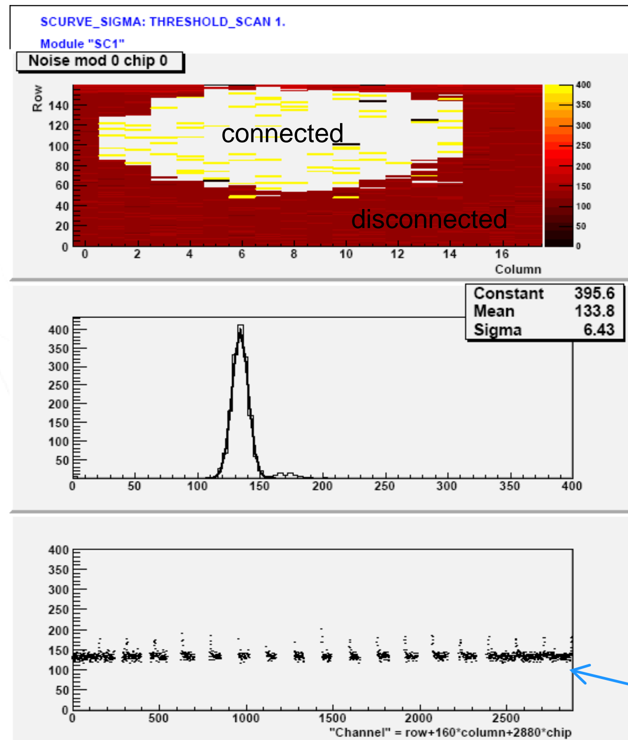
Module on board



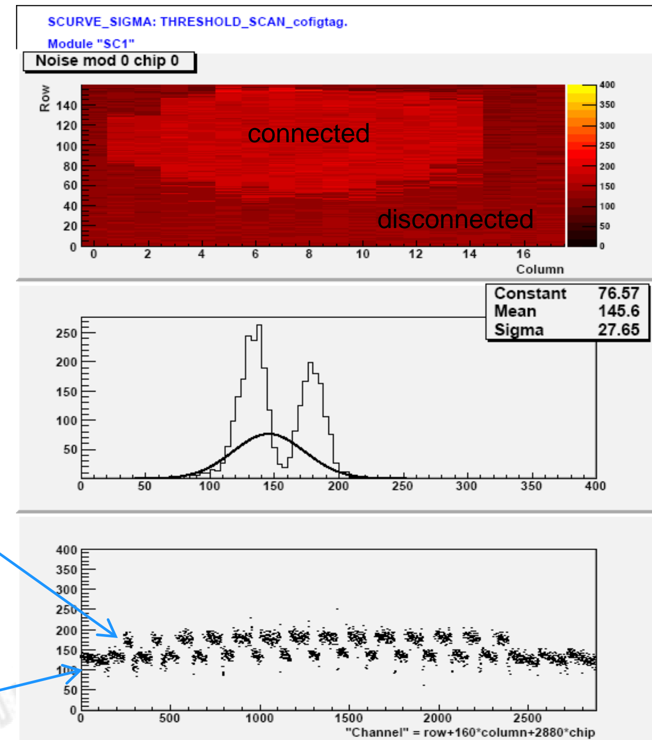
Tests: TSV module: wire bonds on backside (i.e. TSVs used for operation)

- Noise measurement with and without HV shows disconnected pixels
  - For disconnected pixels the noise stays the same indep. of HV
- ENC ~180e- → Module works fine, no indication of extra noise

Noise map, No HV



Noise map, HV = -80V

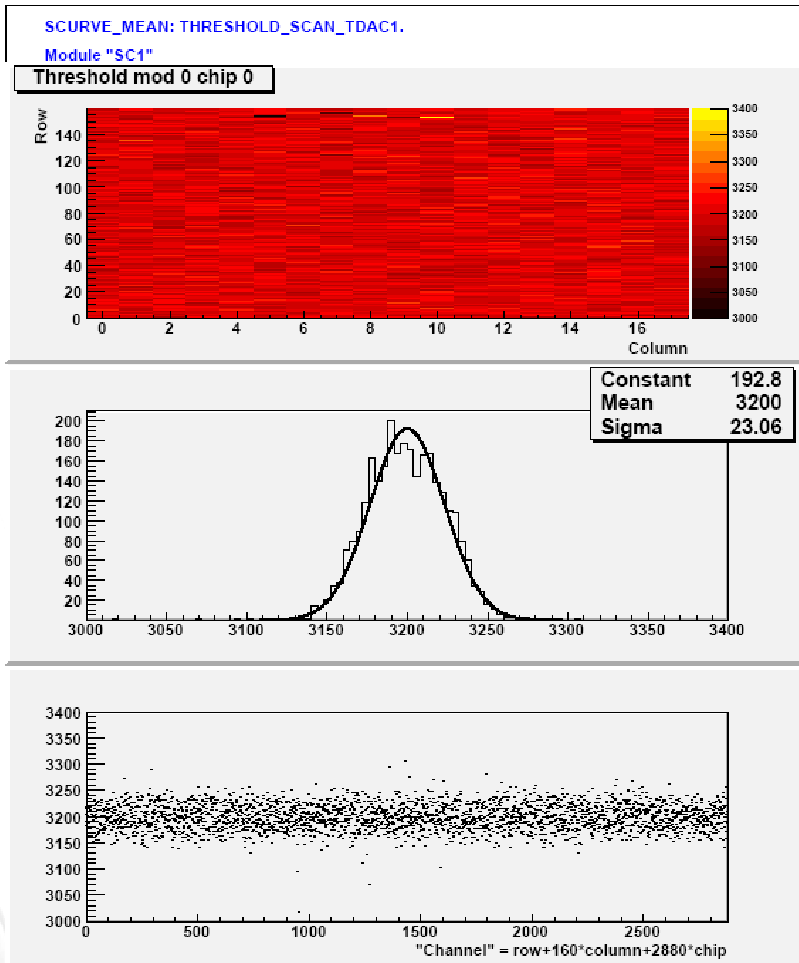


Connected pixels: ~180e

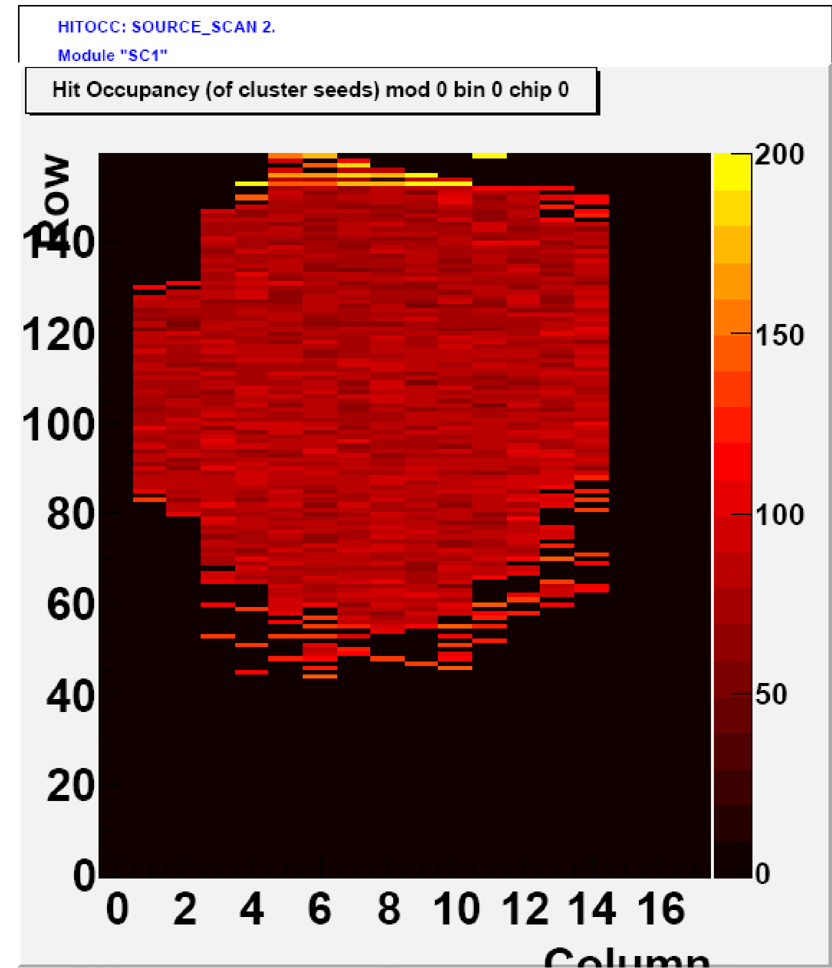
Disconnected pixels: ~130e

Tests: TSV module: wire bonds on backside (i.e. TSVs used for operation)

- Threshold tuning to 3200e

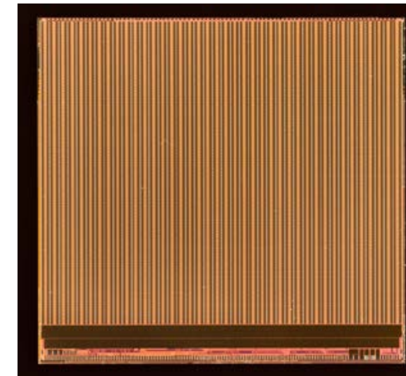


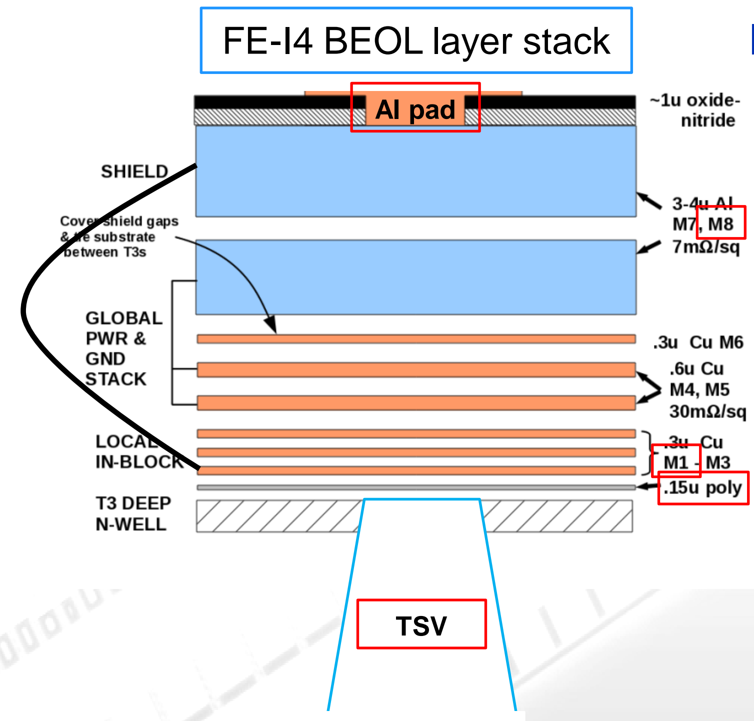
- Source scan with an Am-241 source



Next step: FE-I4B modules with TSV

- 2 FE-I4B wafers at IZM for tapered TSV processing
  - Mask in preparation
  - Approx. 6 months process time at IZM, including bump bonding to sensors
- No front side processing needed
  - Metal layers in the pad
  - M8 connected to M1
  - Between silicon and M1 thin layer of BEOL SiO_2 and poly-Si → can be etched from the back side
- Goals
  - Qualify RDL as possible flex replacement
  - Demonstrate bump bonding of thin (<100μm) FE-I4B with TSV to sensors with temporary handle wafer



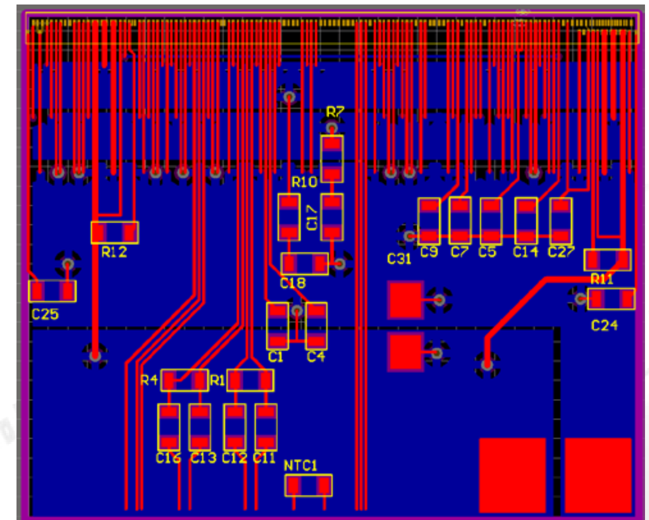


Redistribution layer

- Available RDL options
  - Multi-layer Cu redistribution layer
  - Different RDL layouts on different chips on the same wafer
  - Components can be bonded on RDL lines

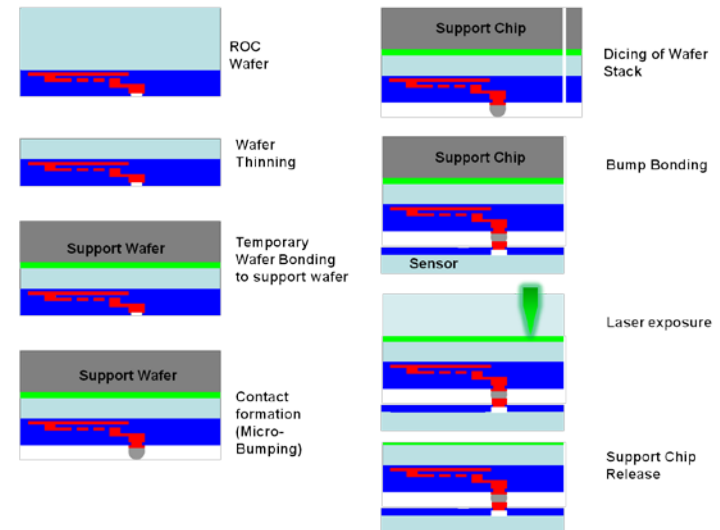
    → The flex design can implemented directly on the FE backside using the RDL

- Implement different RDL options for testing
  - Double layer RDL with bonded components
  - Double layer RDL w/o bonded components
  - Simple RDL as in FE-I2/3 run

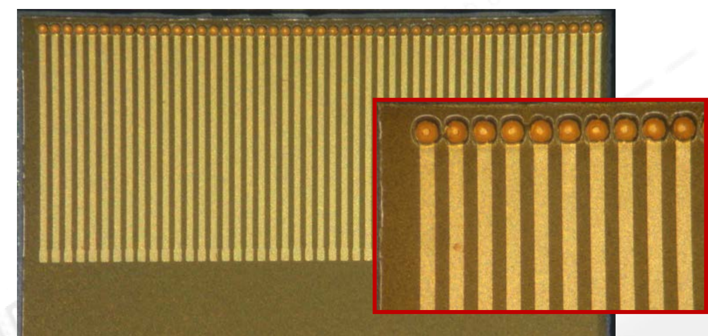


Flip chip of thin FE-I4 with TSV and RDL

- Bump bonding of thin (<100µm) FE-I4B with TSV to sensors cannot be done without handle wafer
  - FE-I4B area = ~4cm² → prohibitive bending of the FE during reflow
- IZM developed a flip chip method to bump bond 150µm FE-I4 to sensors currently used for the entire IBL module production
  - Laser releasable polymeric bonding interface
- Method needs to be demonstrated on FE-I4 wafers with TSV and RDL
  - RDL patter on backside
  - TSVs are not completely closed
  - → constraints on the polymeric glue thickness and the uniformity of the deposition



RDL on FE-I2



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Conclusion

- Bonn/CPPM are investigating the possibility of building compact, low mass modules for the upgrade of the ATLAS pixel detector at the HL-LHC using via last TSV
- The selected process is the tapered side walls TSV process from IZM
- Successful 1st demonstration of a via last TSV process on FE-I2 ATLAS FE electronics
  - Modules function well when operated with TSV + backside RDL (equivalent noise, source scan performed)
- A run with FE-I4B will start after completion of the IBL module production

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