Timepix array readout SRS

Michael Lupberger

University of Bonn

RD51 electronics school, 05.02.2014

Outline

- Front end chip
- Detector

- SRS adapter card design

- FPGA Firmware

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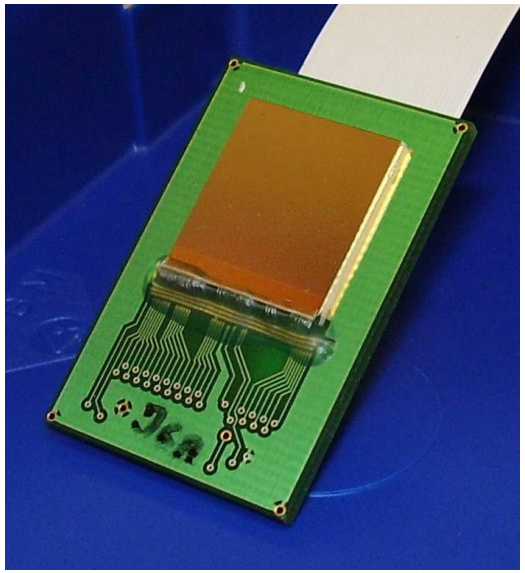
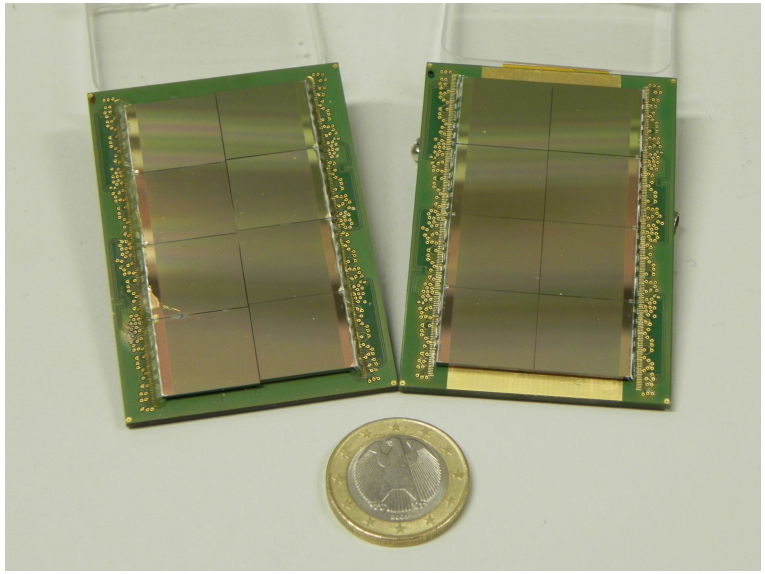
Timepix chip

- Universal readout chip
- Properties:
  - active surface: 1.4 x 1.4 cm²
  - pixel size 55 x 55 µm²
  - 256 x 256 pixel array (= 65536 channels)
  - 14 bit counter in each pixel
  - Noise threshold ~500e^- (ENC ≈ 90e^-)





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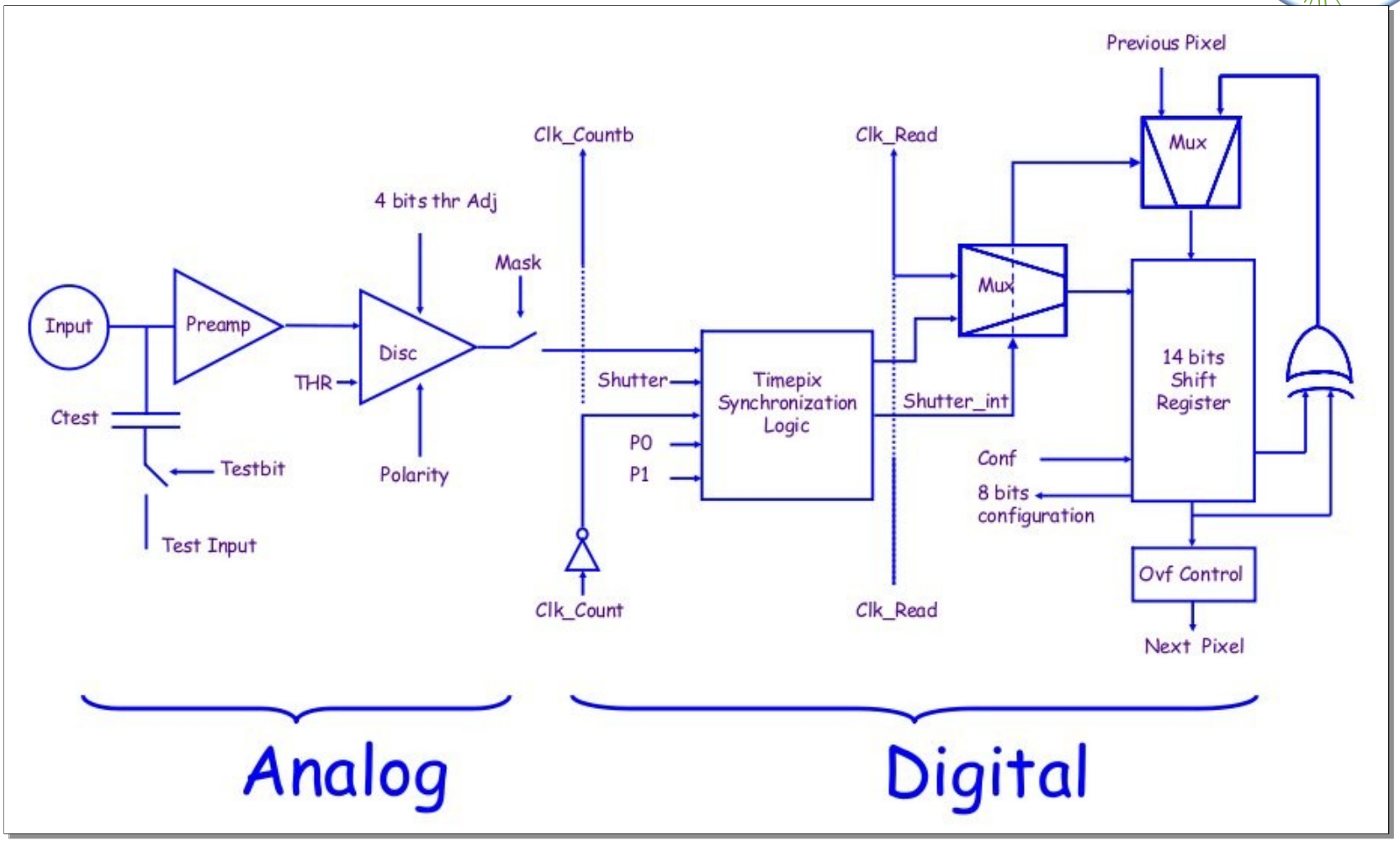
Timepix chip



Timepix chip

- 4 different modi to operate

  - Medipix:

Pixel hit how often

  - Time-over-threshold

Pixel hit how long

→ proportional to charge

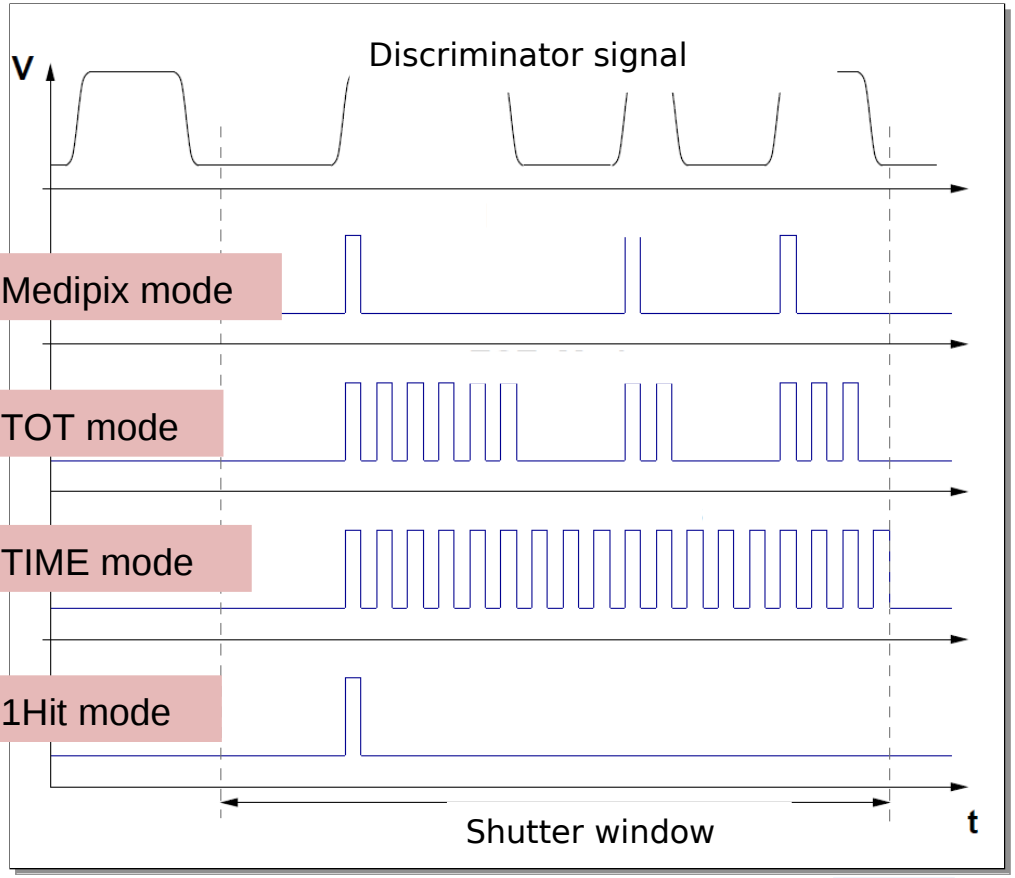
  - Time:

Pixel hit when

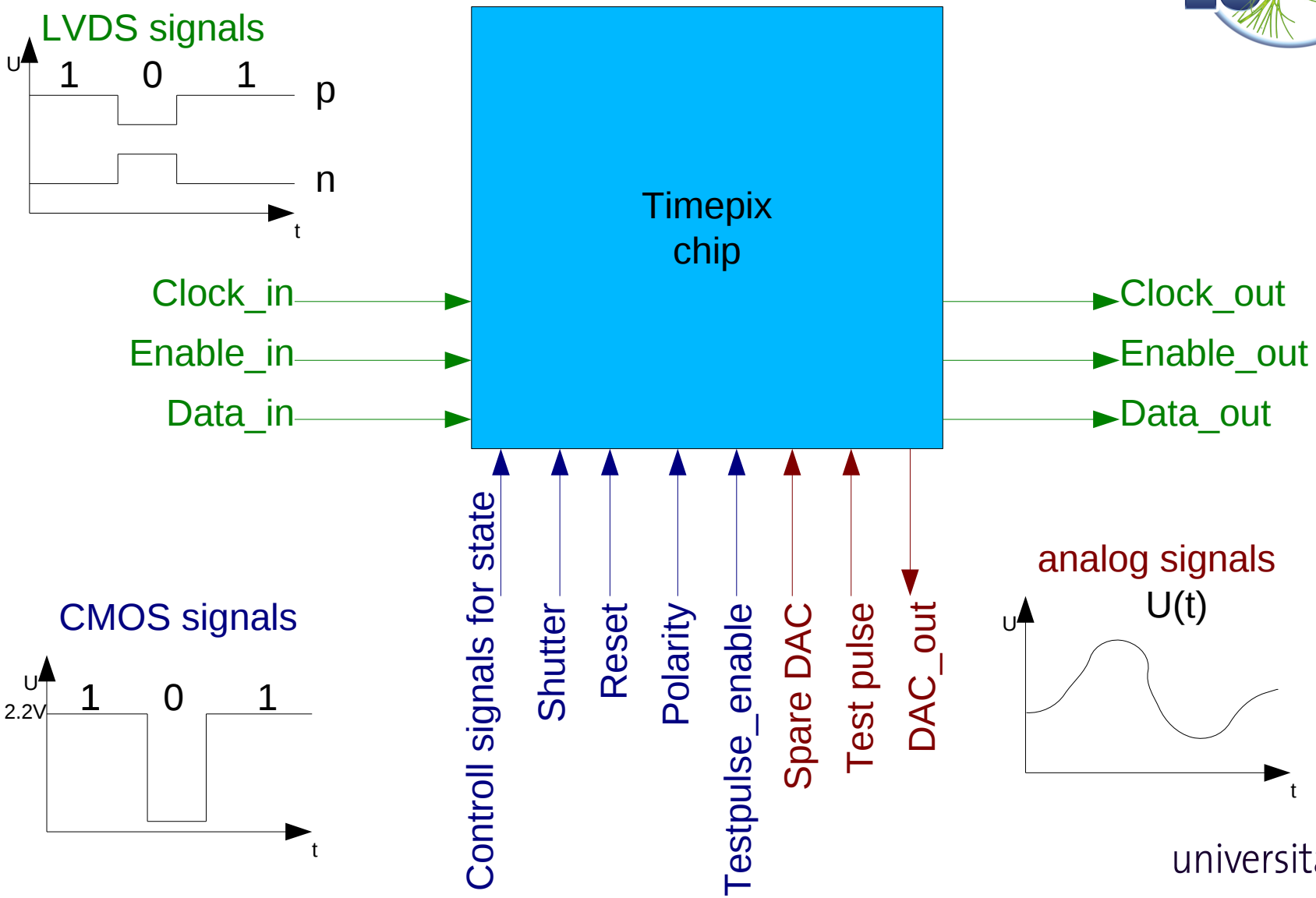
→ time of arrival

  - 1Hit:

Pixel hit in shutter window



Timepix chip



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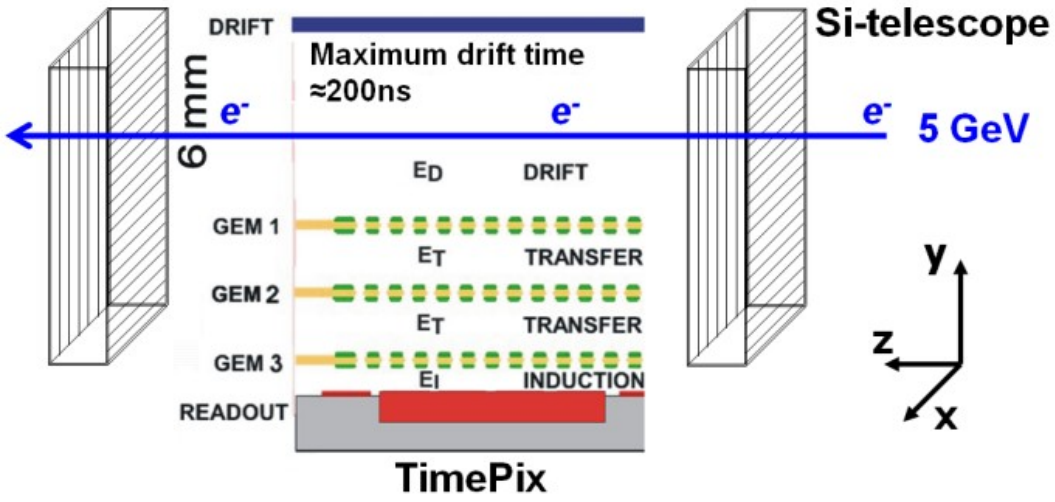
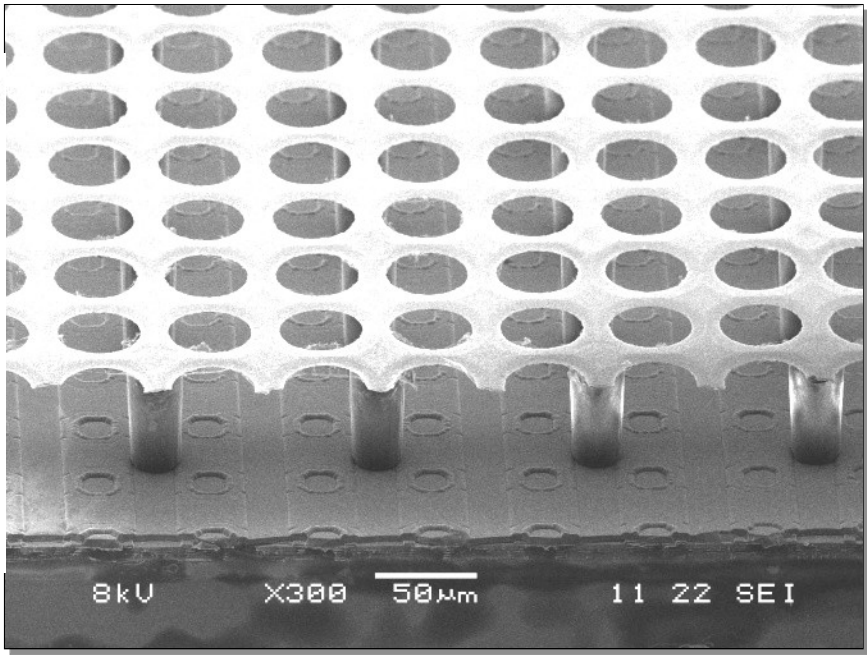
Gas amplification

- Triple GEM stack
- Micromegas: InGrid





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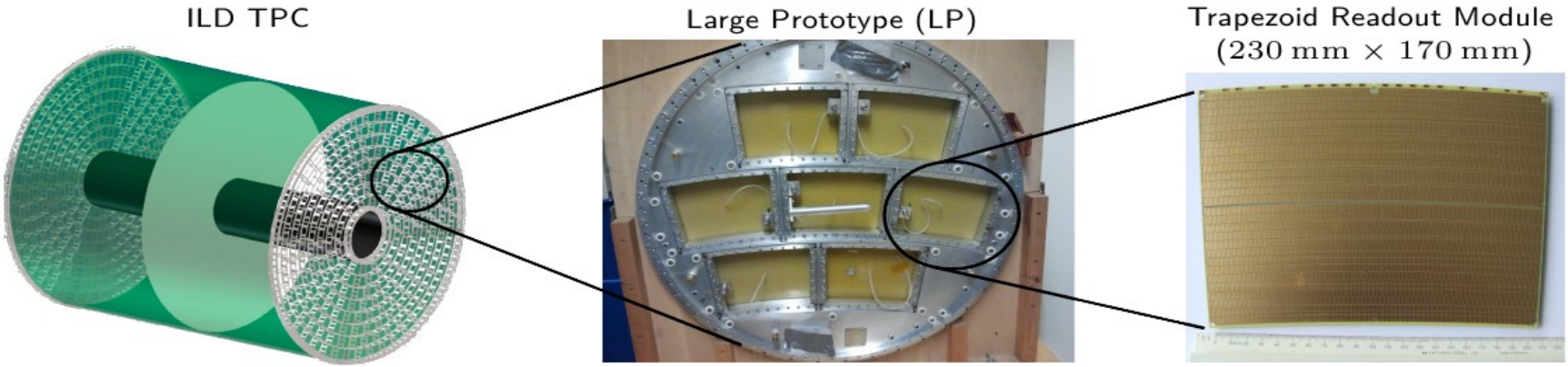
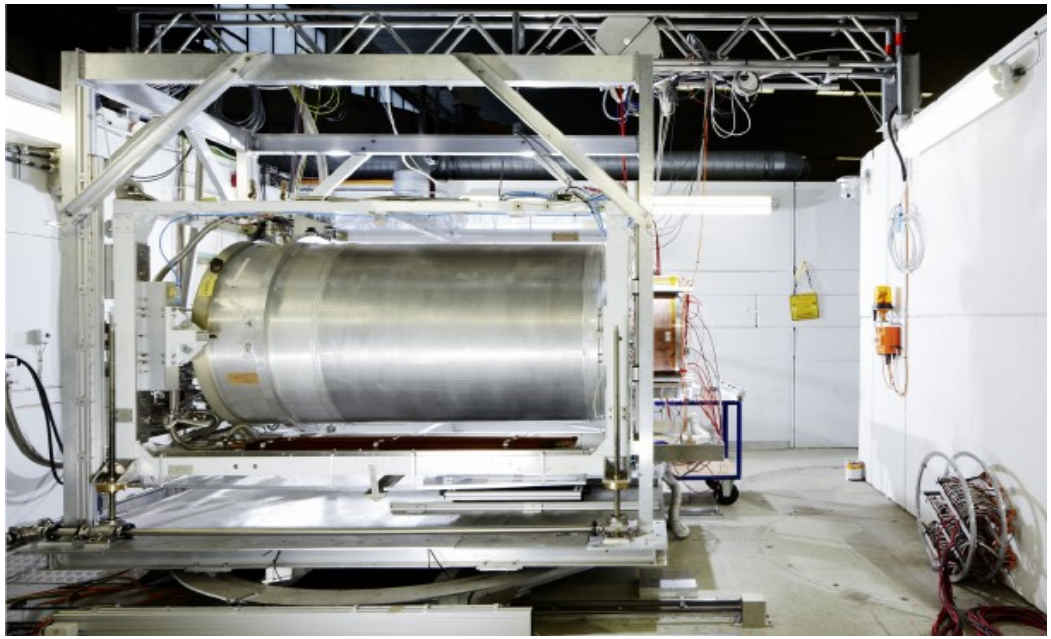
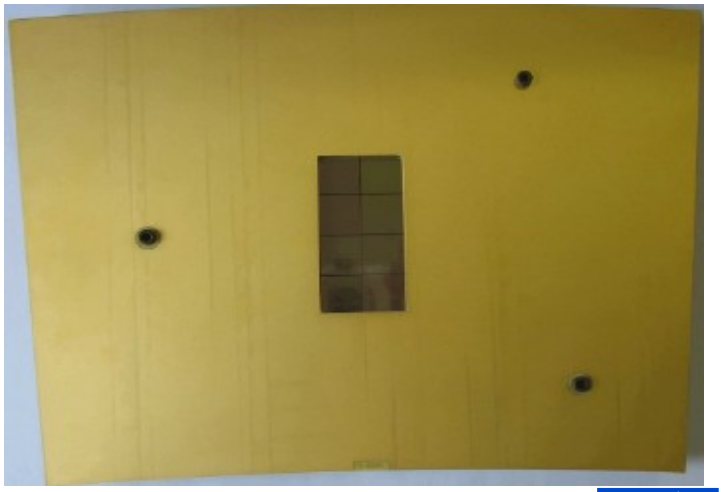
LCTPC Prototype

- Setup at DESY







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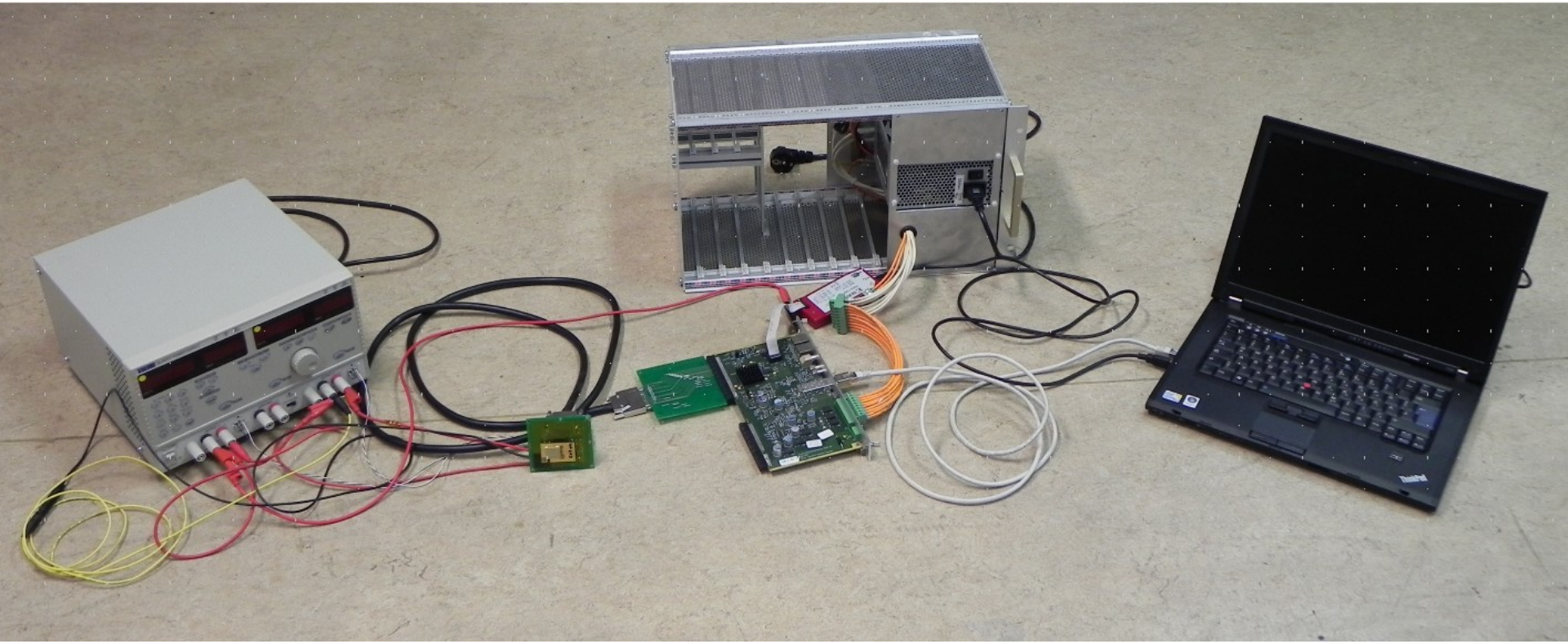
Status at Testbeam

Scalable Readout System (RD51, CERN)



Chain: Chip – Adapter card+FEC – Computer

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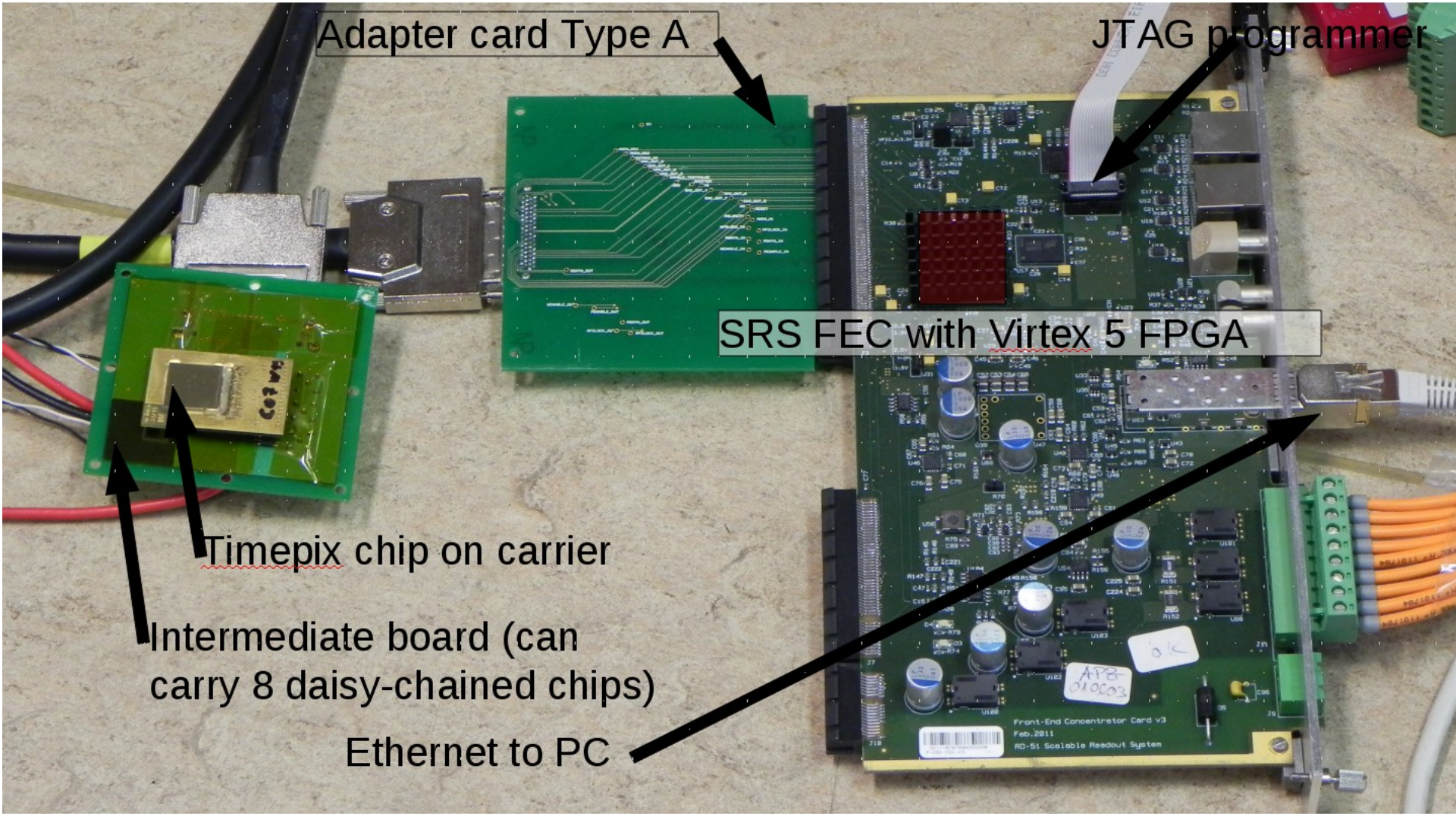
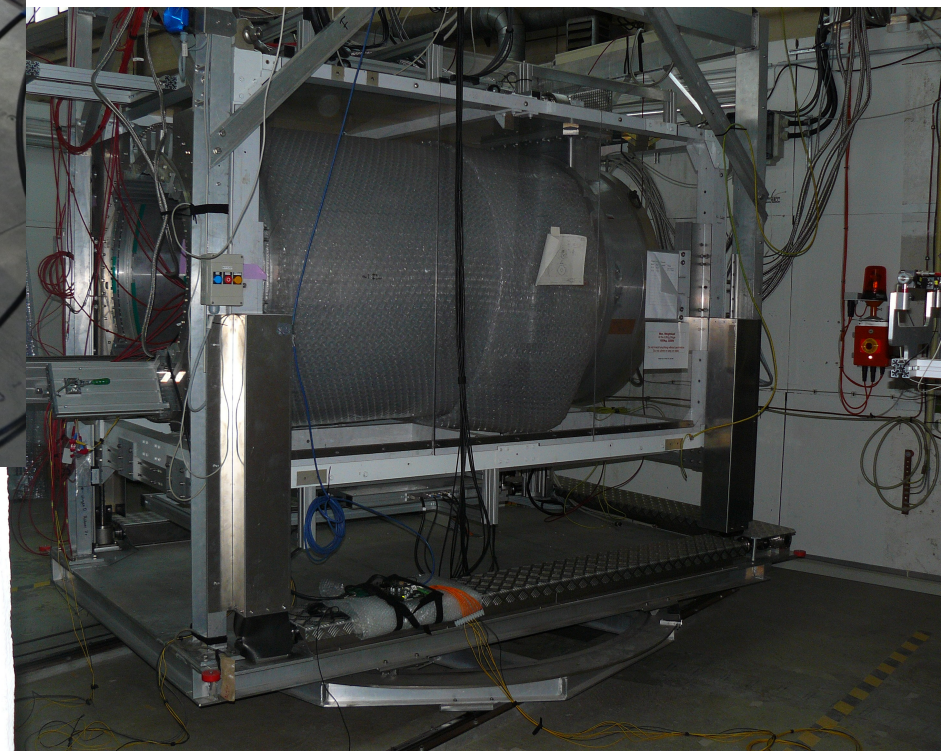
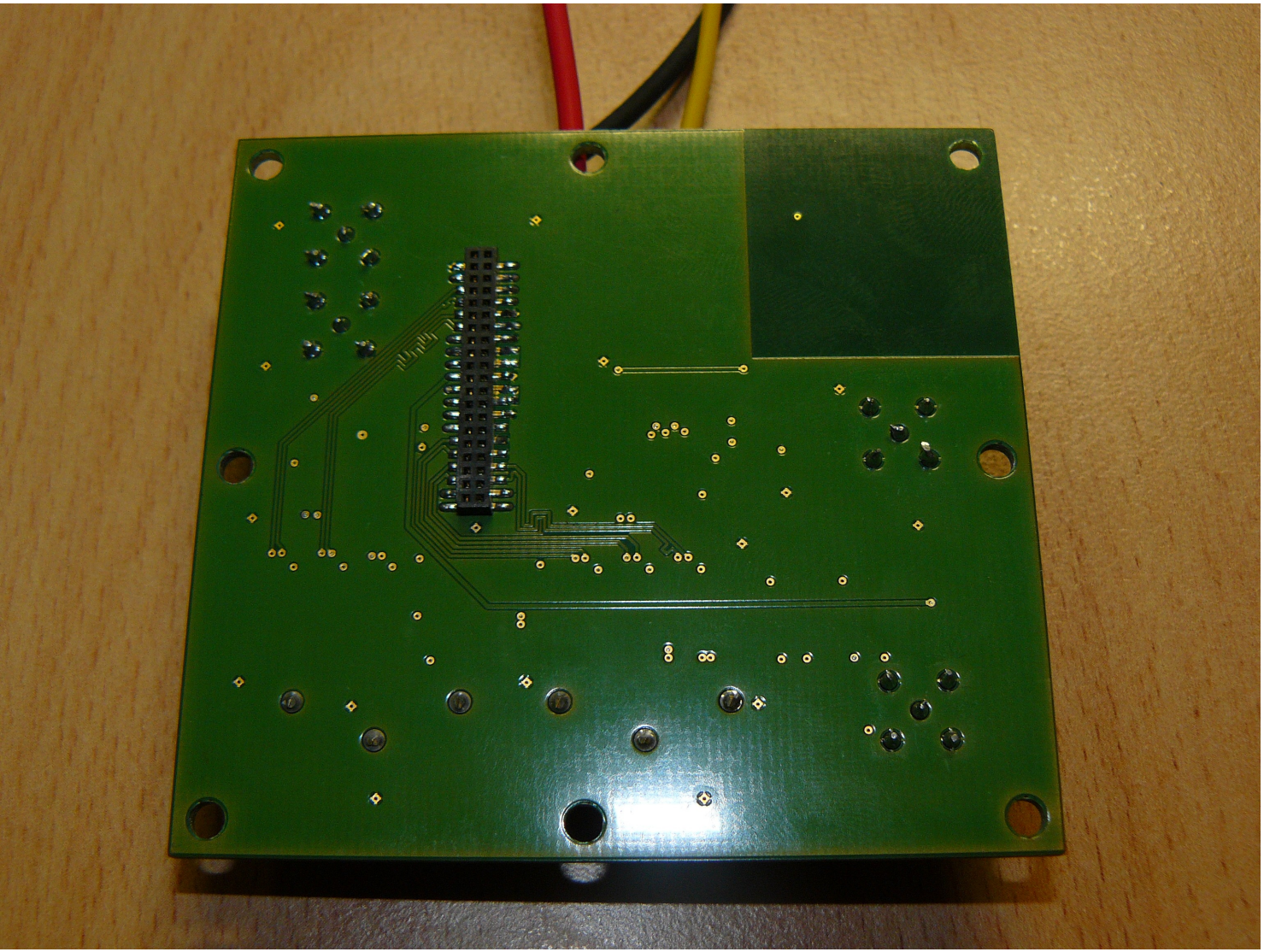
SRS with Timepix chip



Setup @ testbeam



Intermediate board



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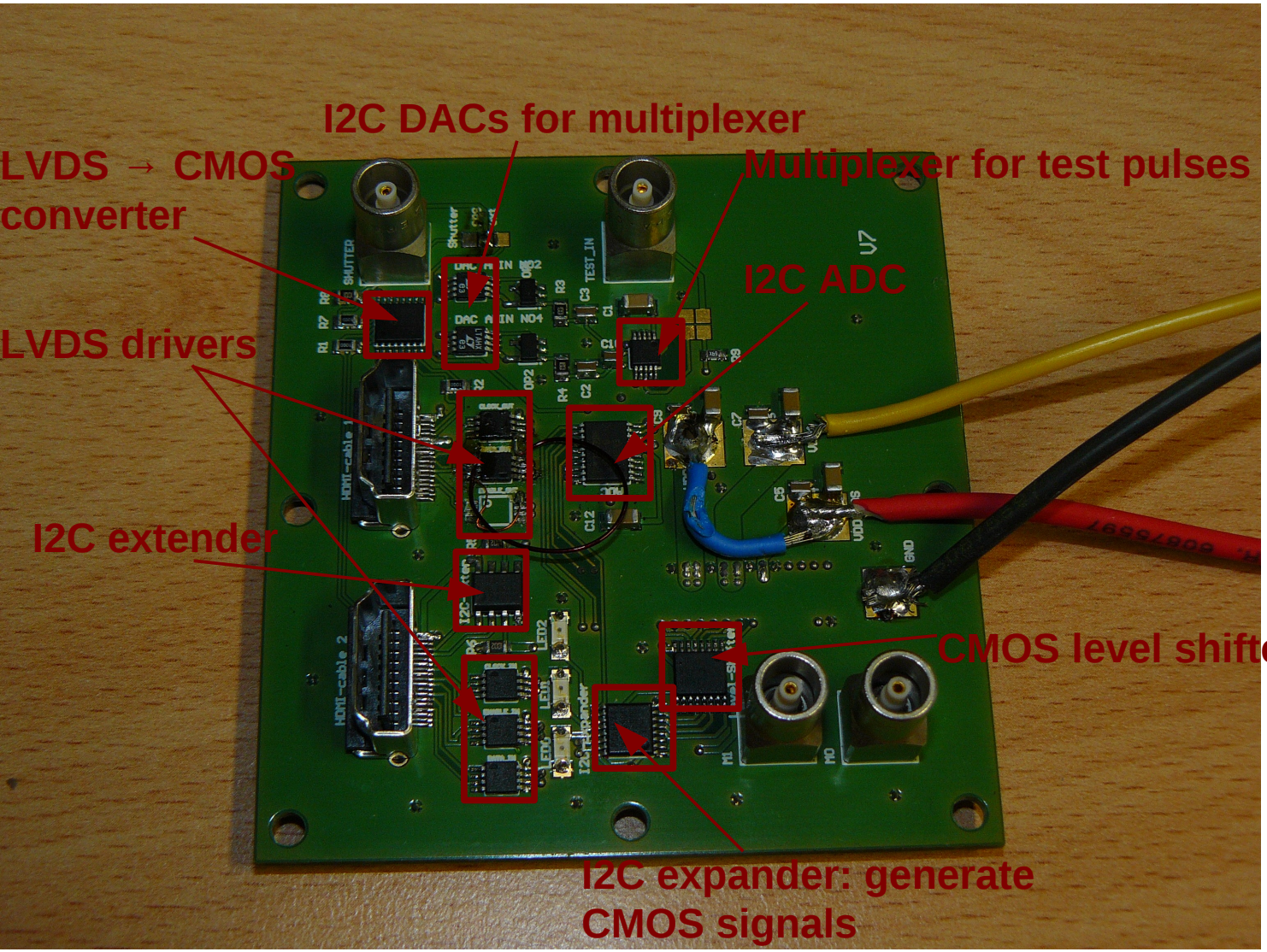
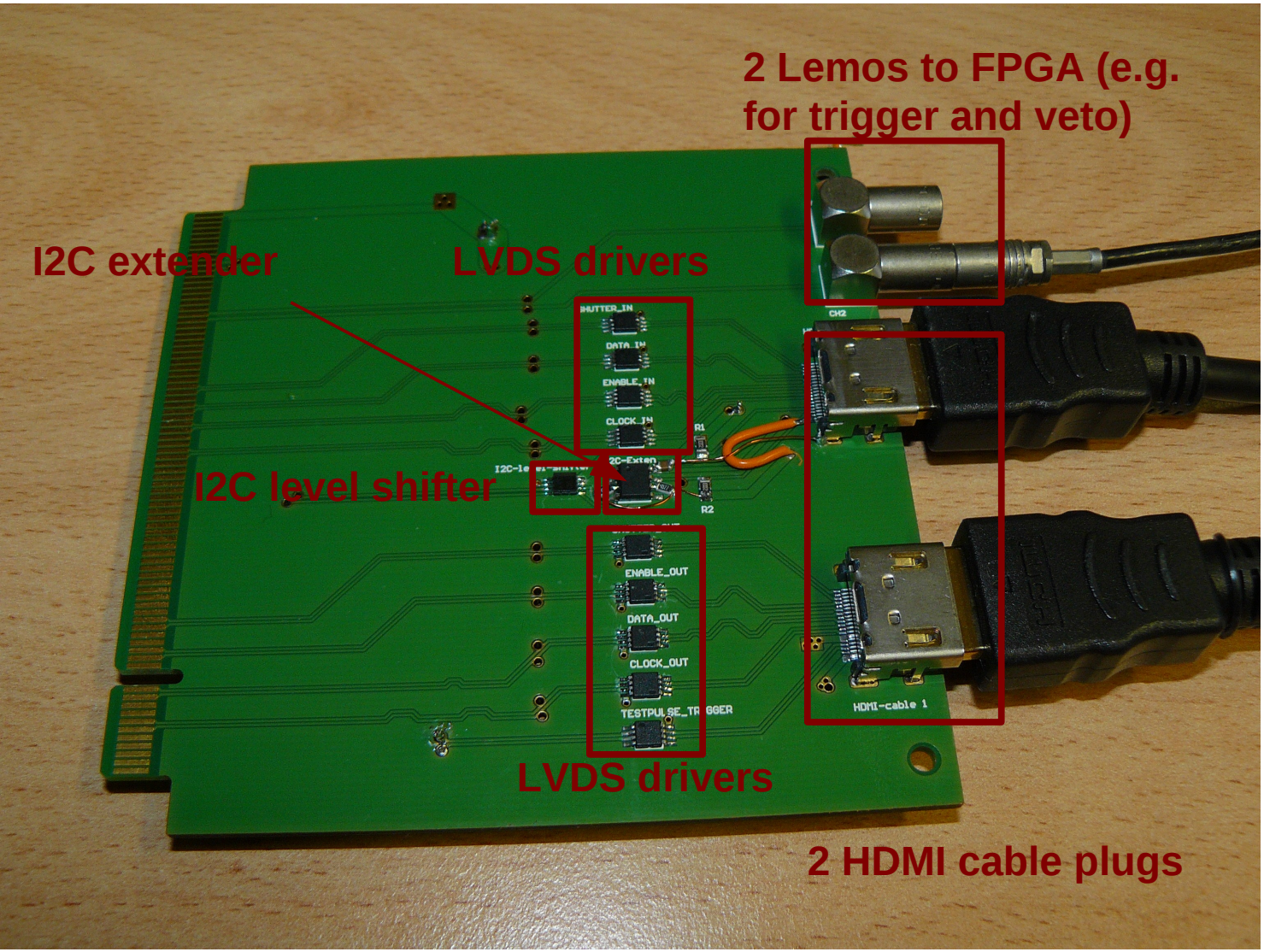
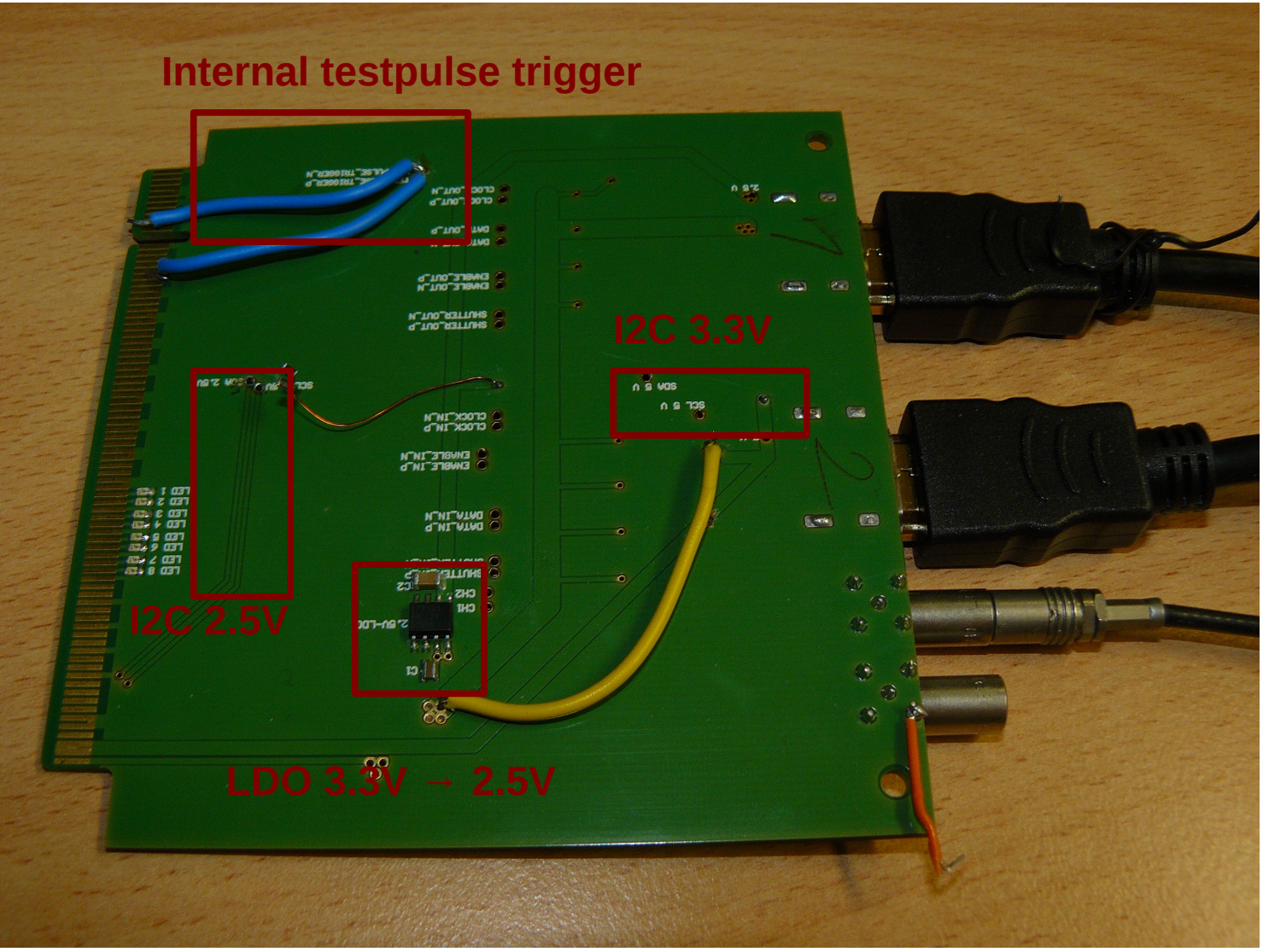


SRS A Card

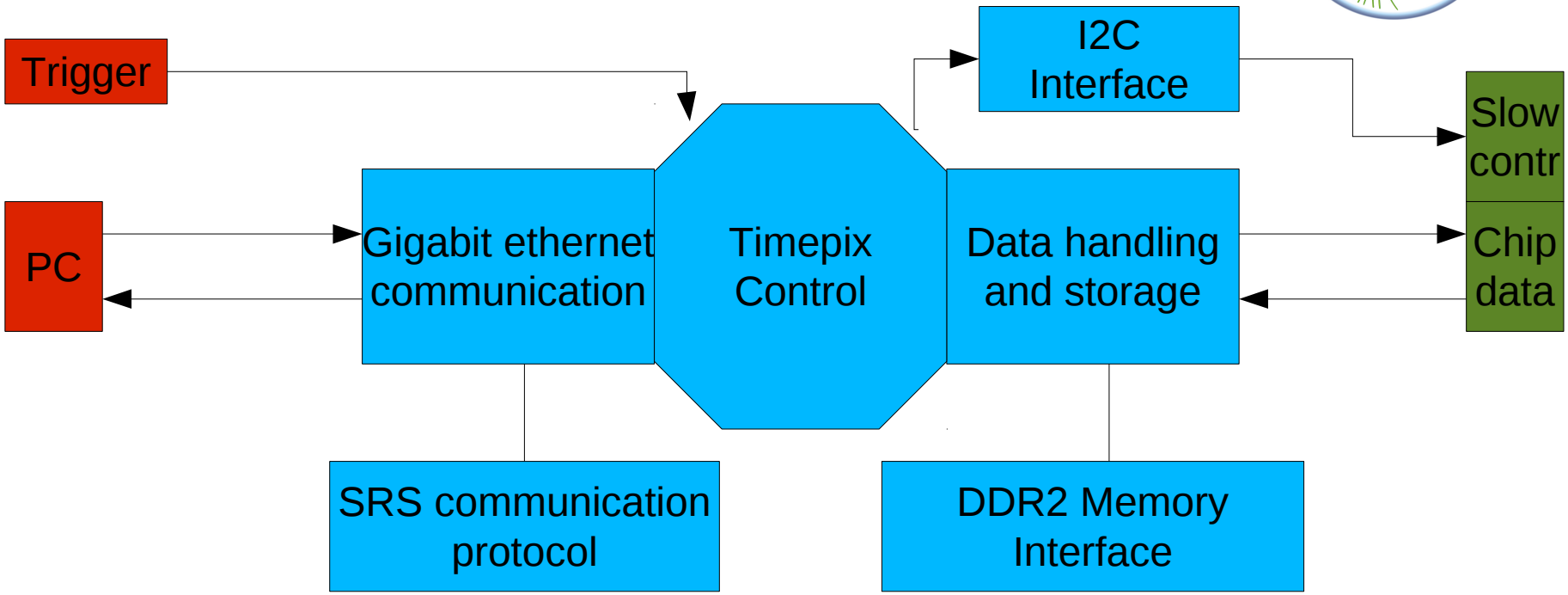


I2C: standard for small network.
Signals:
scl: clock
sda: data
Originally between PCBs next to each other.
With externs: Several meters distance.

SRS A Card



FPGA Firmware



Some features:

- ~~Multithreading~~ (read chip while sending data of last frame)
- DDR2 RAM to store data of 8 chips
- I2C for slow control

Status Timepix+SRS Readout

- A-Card and intermediate board:
  - HDMI cables
  - Signals optimised for long distance (~25 m)
  - Components on A card and intermediate board:
    - LVDS drivers for long distance
    - I2C network for CMOS signal reduction
    - Remaining CMOS signals transmitted as LVDS and converted to CMOS on intermediate board
    - I2C level shifter and extender for long distance
    - ADC to read back analog signals from Chip (DAC_out)
    - DACs to set voltages for multiplexer
- Latest new parts of FPGA Firmware:
  - I2C Interface
  - DDR2 Interface

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Status Timepix+SRS Readout

- Test of components finished
  - I2C network ok (DACs, ADC, expander work)
  - Multiplexer for test pulses ok
  - LVDS driver work => chip can be operated
- Test of FPGA Firmware:
  - DDR2 Ram ok, needs long time testing
  - I2C interface ok
- Software implementation ongoing (e.g. ADC readout, automatic calibration, ...)

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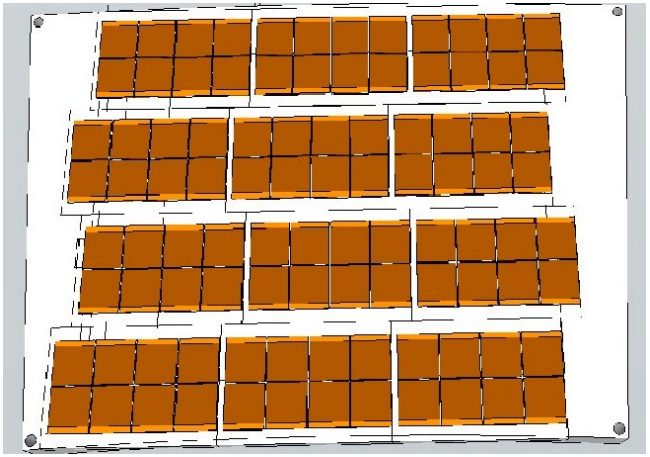
Summary and Outlook

SRS + Timepix readout system hardware components optimised for test beam and about to be finalised.

What is this all for?

Preparation of LCTPC module with ~100 chips

- Scaling up of new hardware
- Want: 3-4 Octoboards/FEC
- Power supply still unsolved



=> Demonstrator for a
pixel TPC (for ILD @ ILC)

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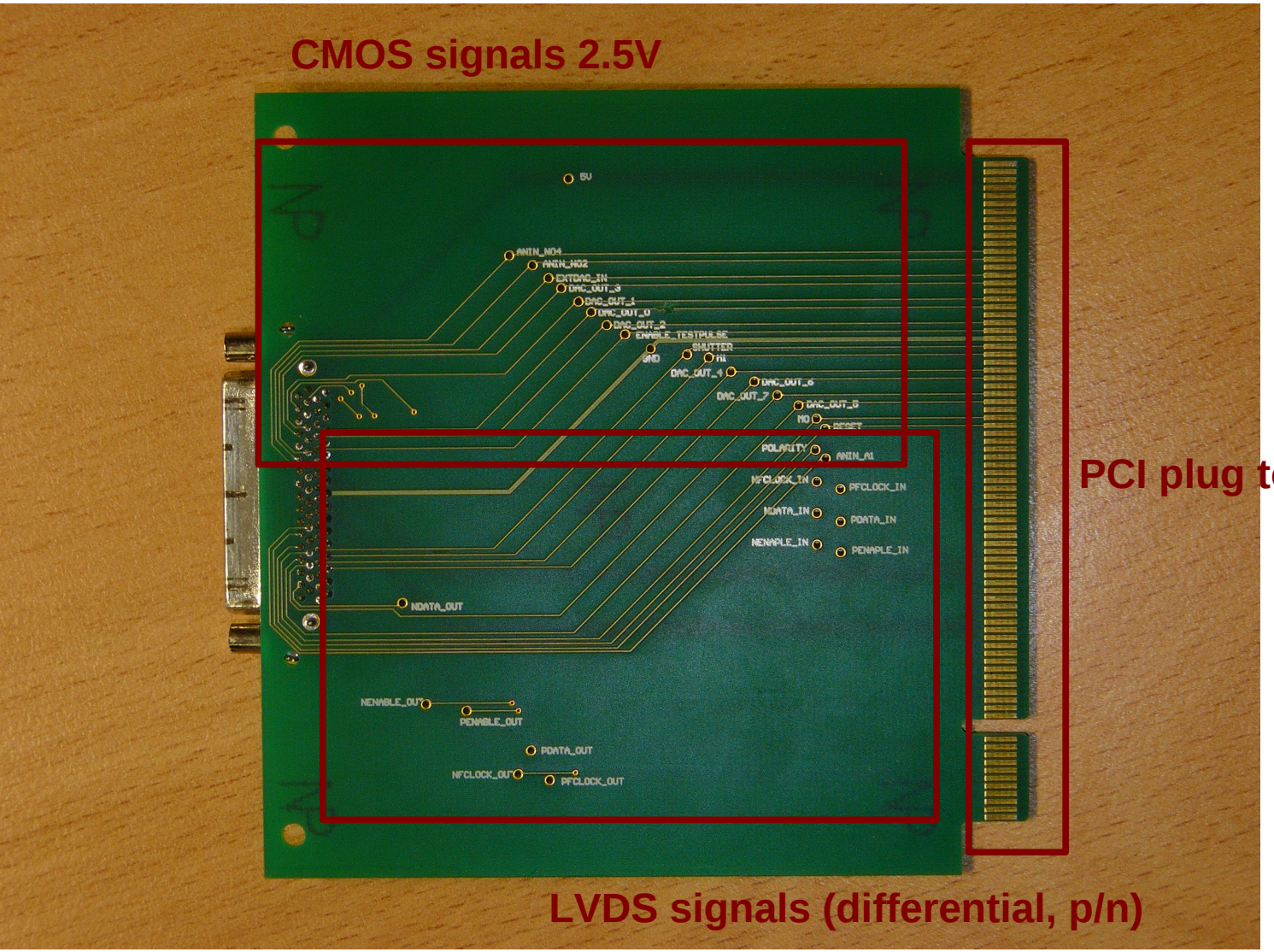
A Card



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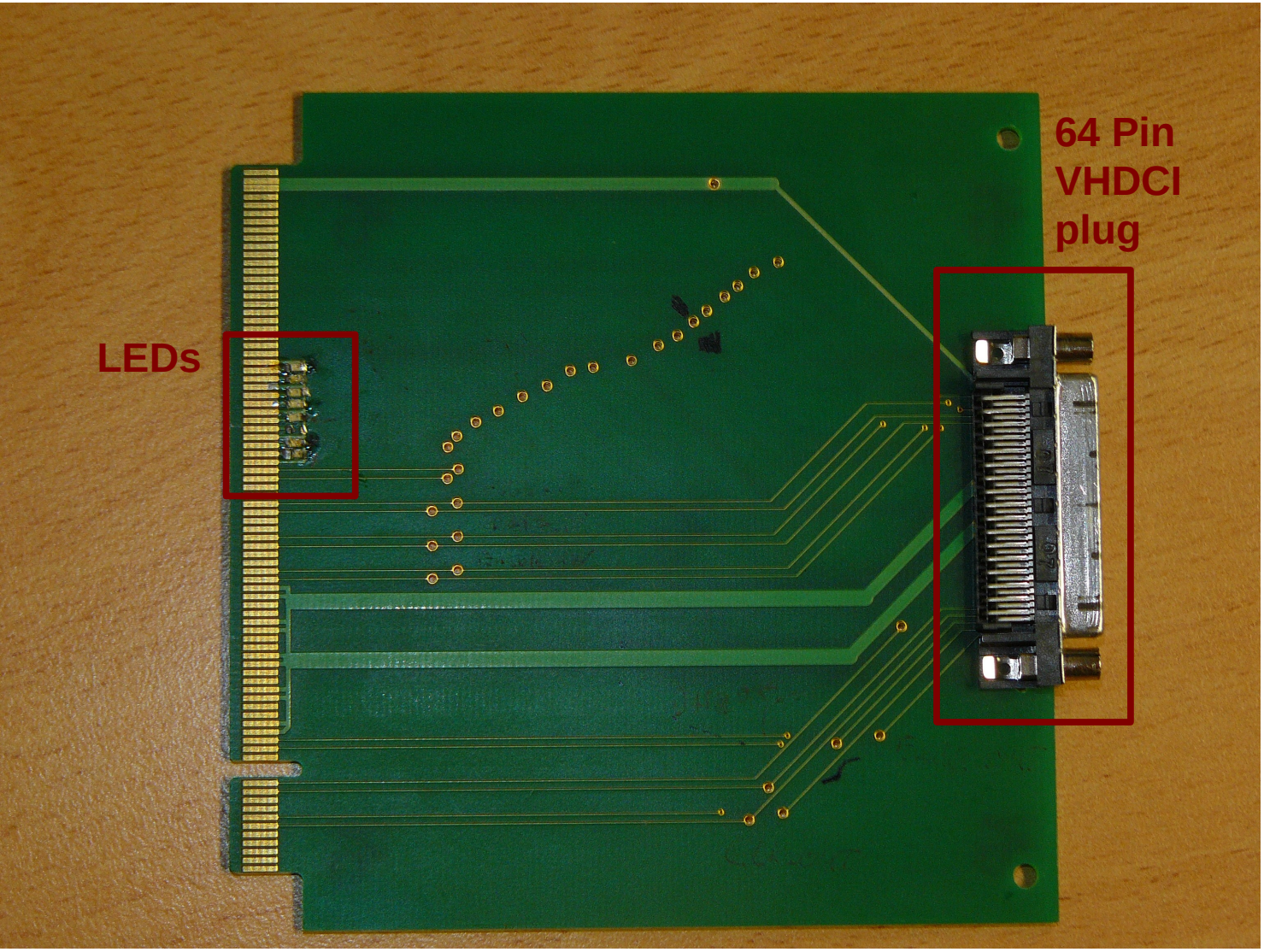
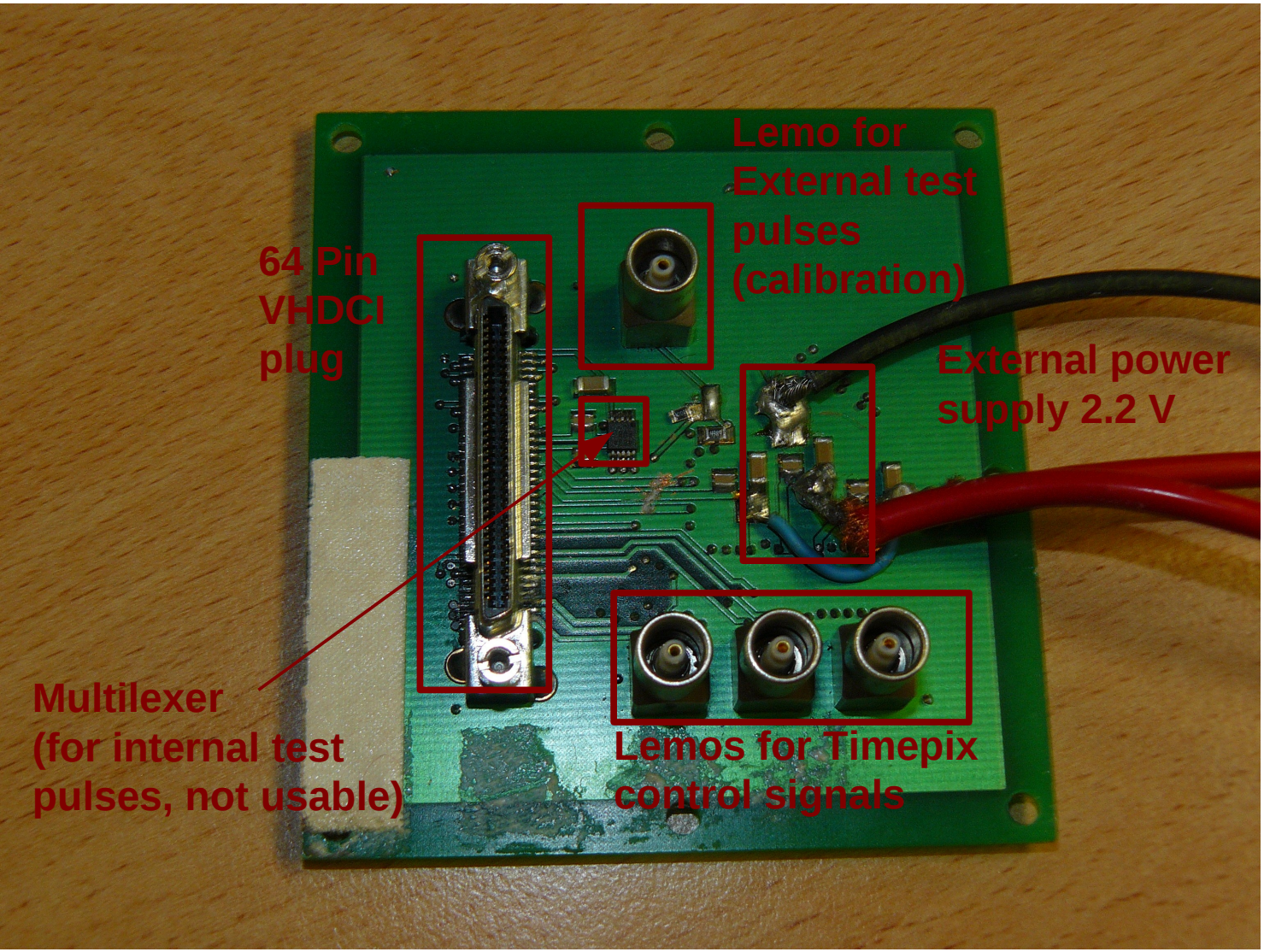
A Card



Intermediate Board



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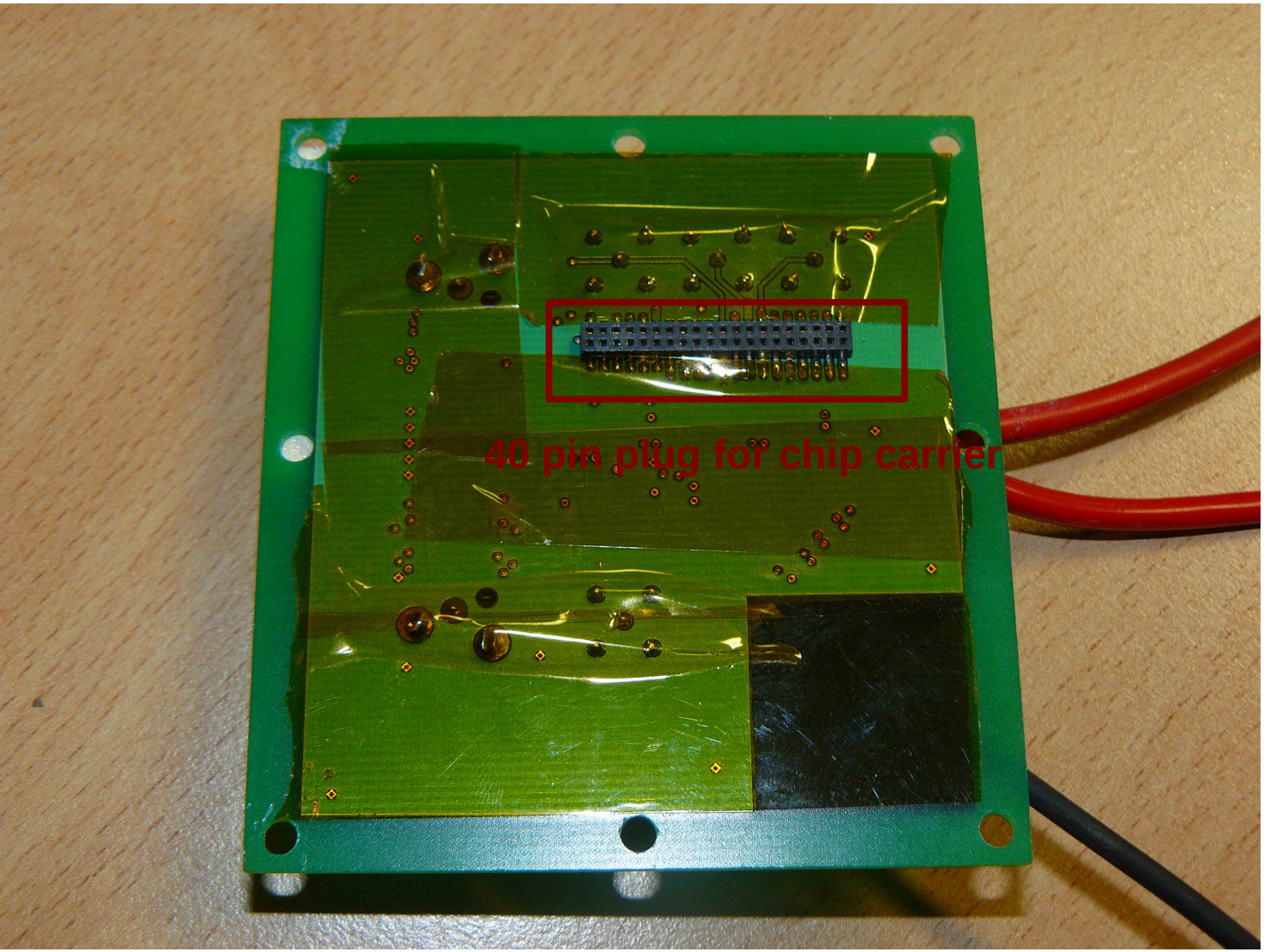

FPGA Firmware