The SiPM tracking plane in the NEXT experiment: readout with SRS

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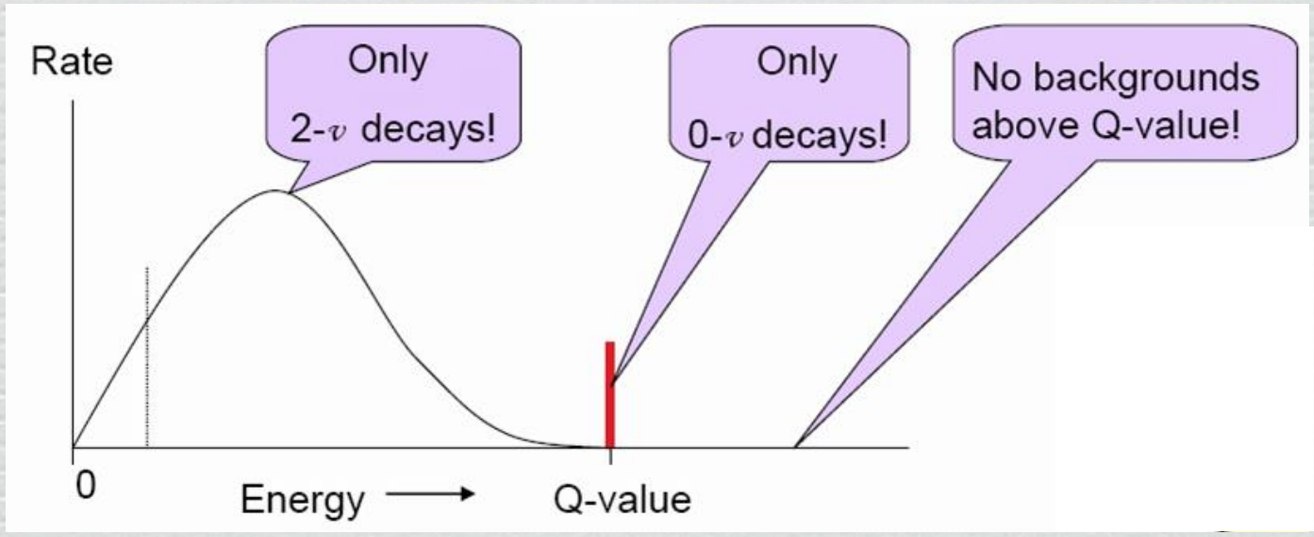
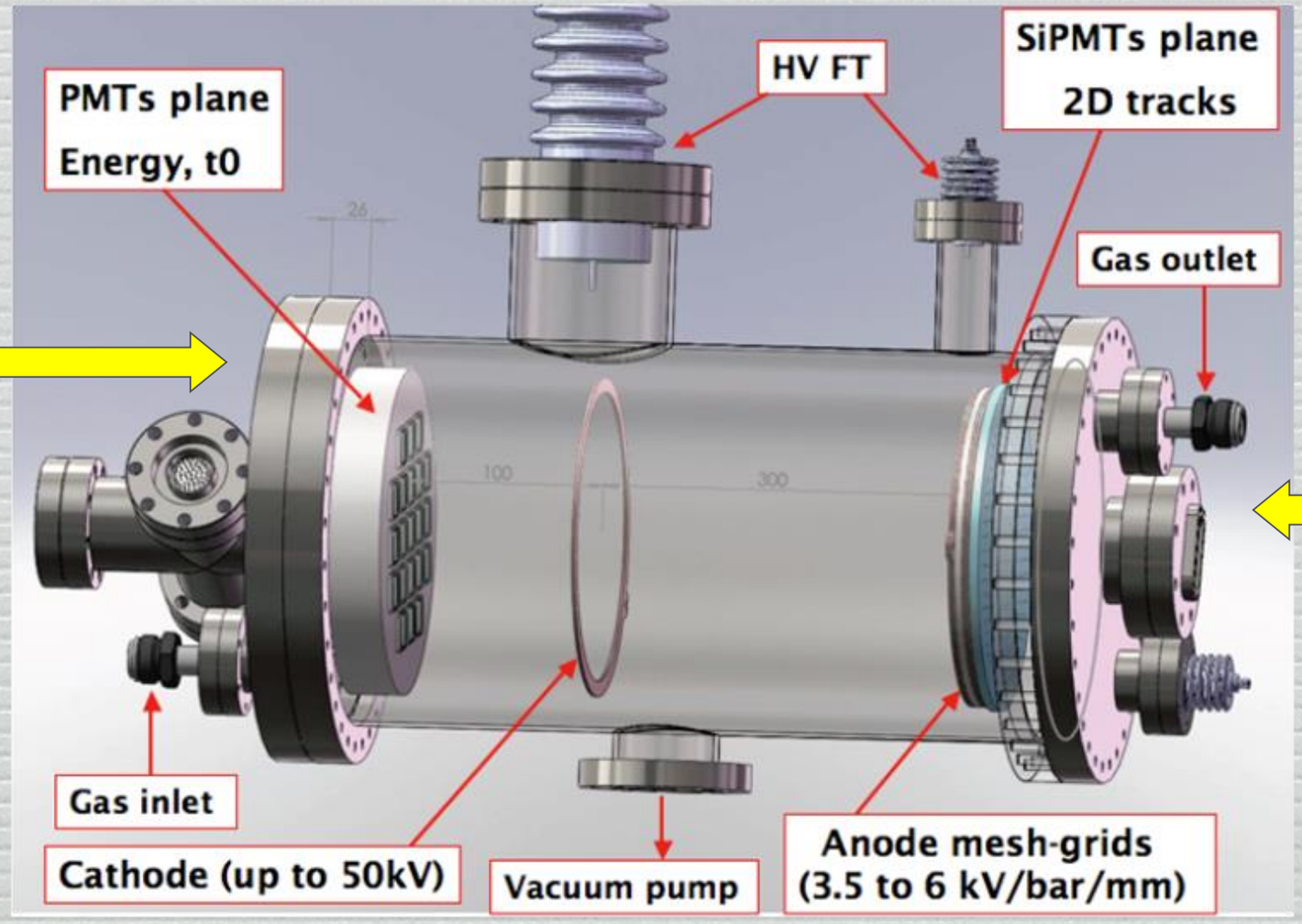
45’ to talk about…

- The NEXT experiment
- The SiPM tracking plane
- Design: the front-end
- Design: interfacing the front-end to SRS
- Design: DAQ and trigger systems based on SRS

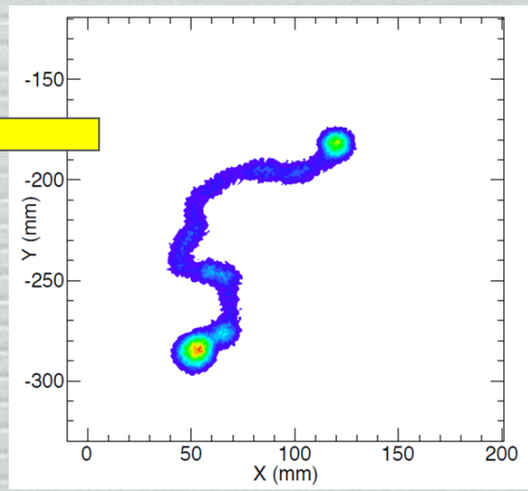
NEXT a 0ν-ββ ^{136}Xe gas TPC experiment

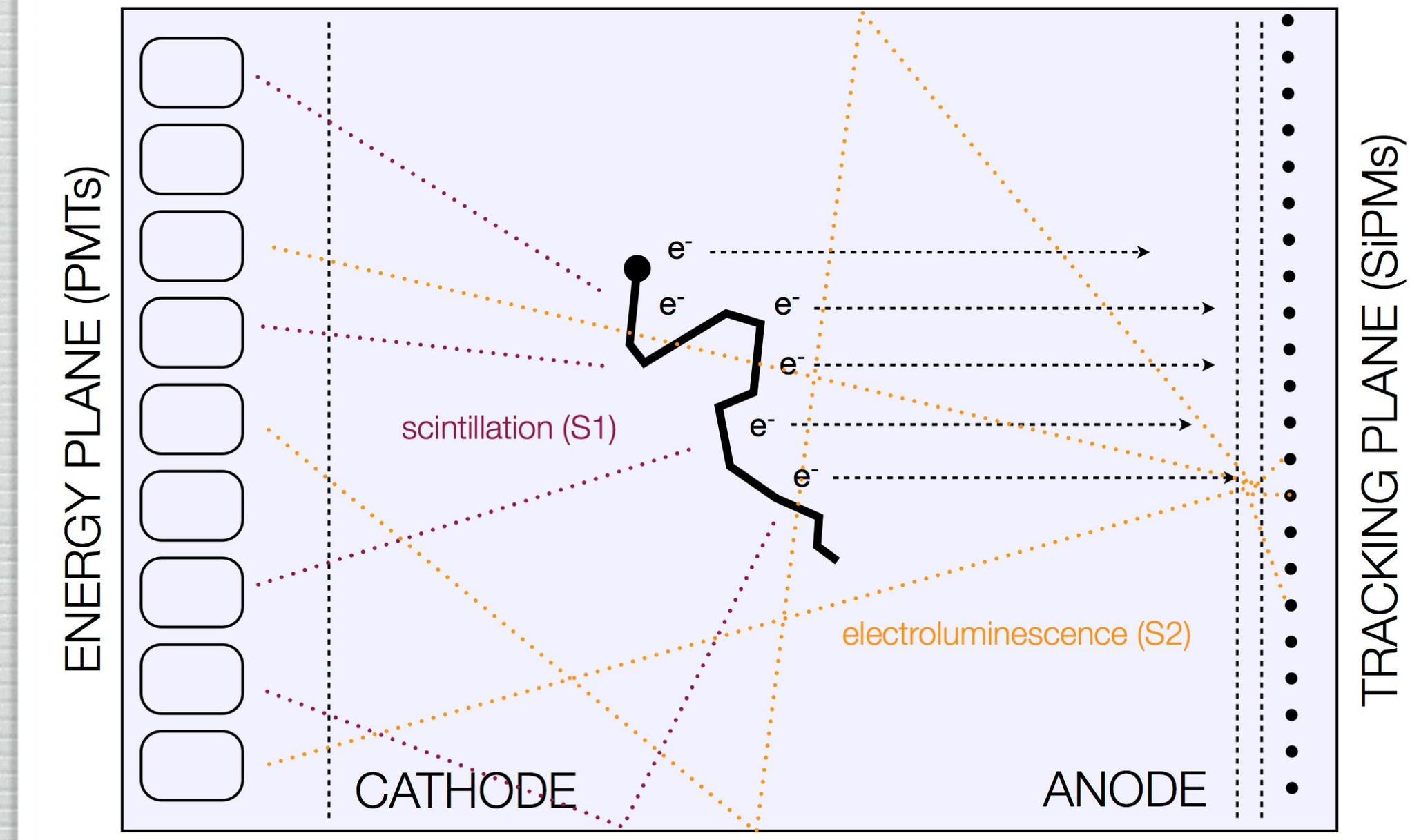


PMTs to measure E, t0 (energy plane)



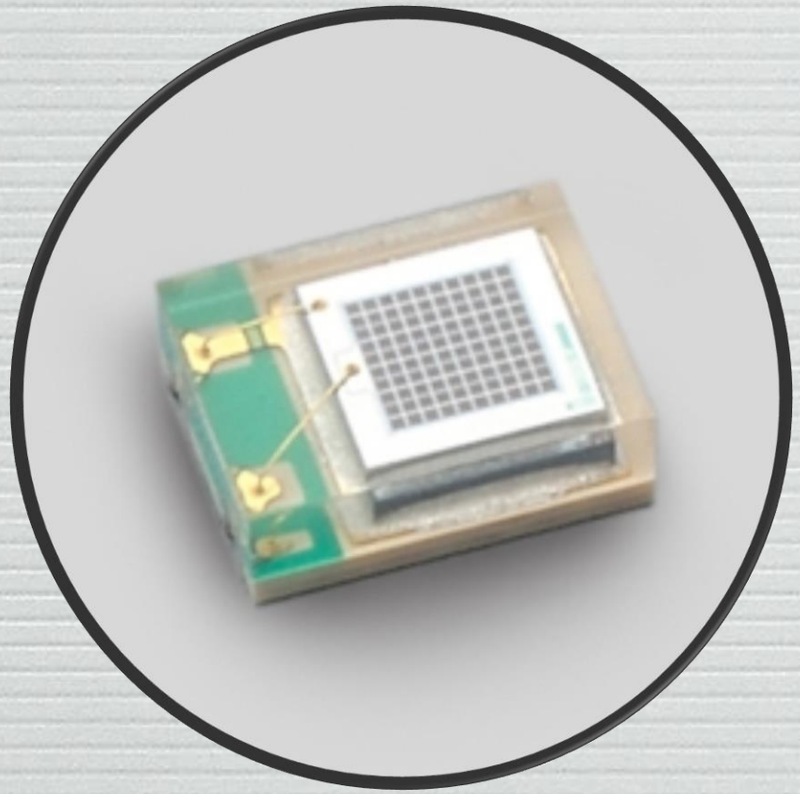
~8k SiPMs (tracking plane)





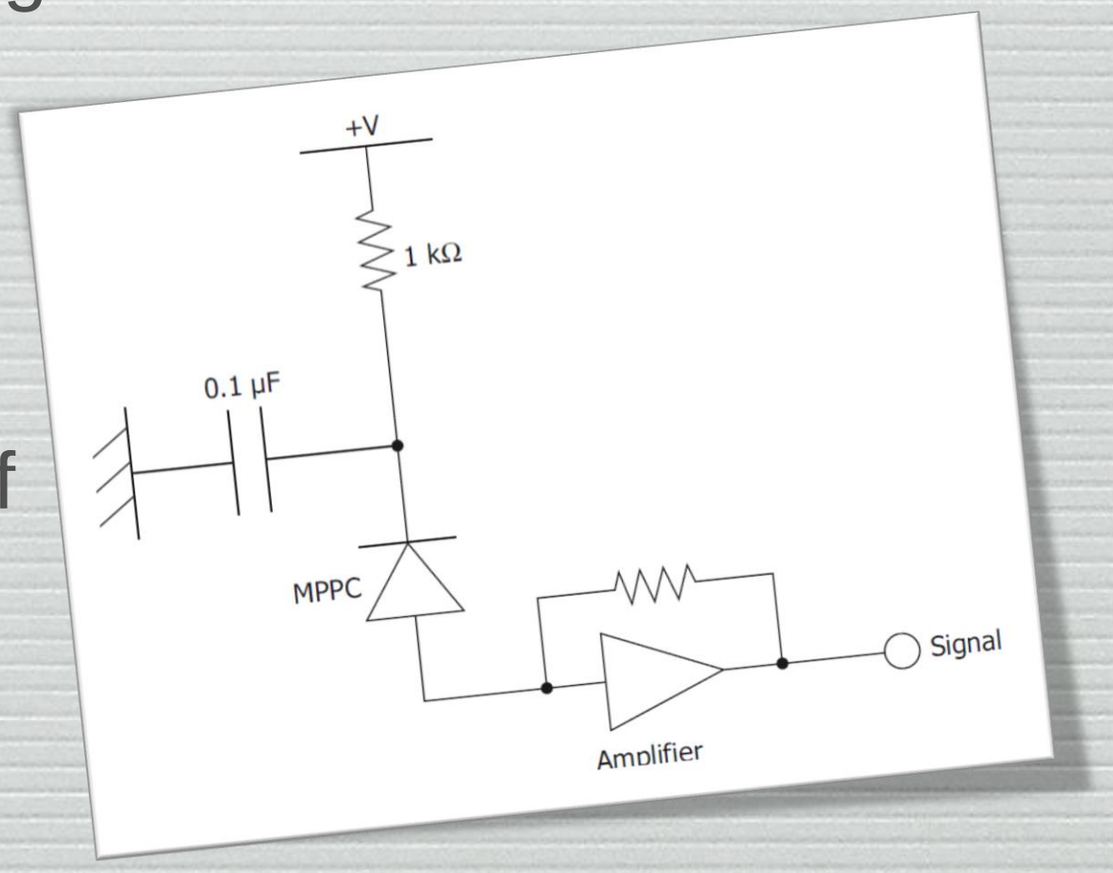
Detector concept

What's a SiPM by the way?



It's an array of avalanche photodiodes operating in Geiger mode

It's a photon counting devide with gains in the 10^5-10^6 range



The ouput from the SiPM is the sum of the current from each cell. So, the dynamic range is the number of cells

Issues: afterpulses, dark count

NEXT: a project in 3 phases

1. NEXT-DEMO ✅

2.NEW

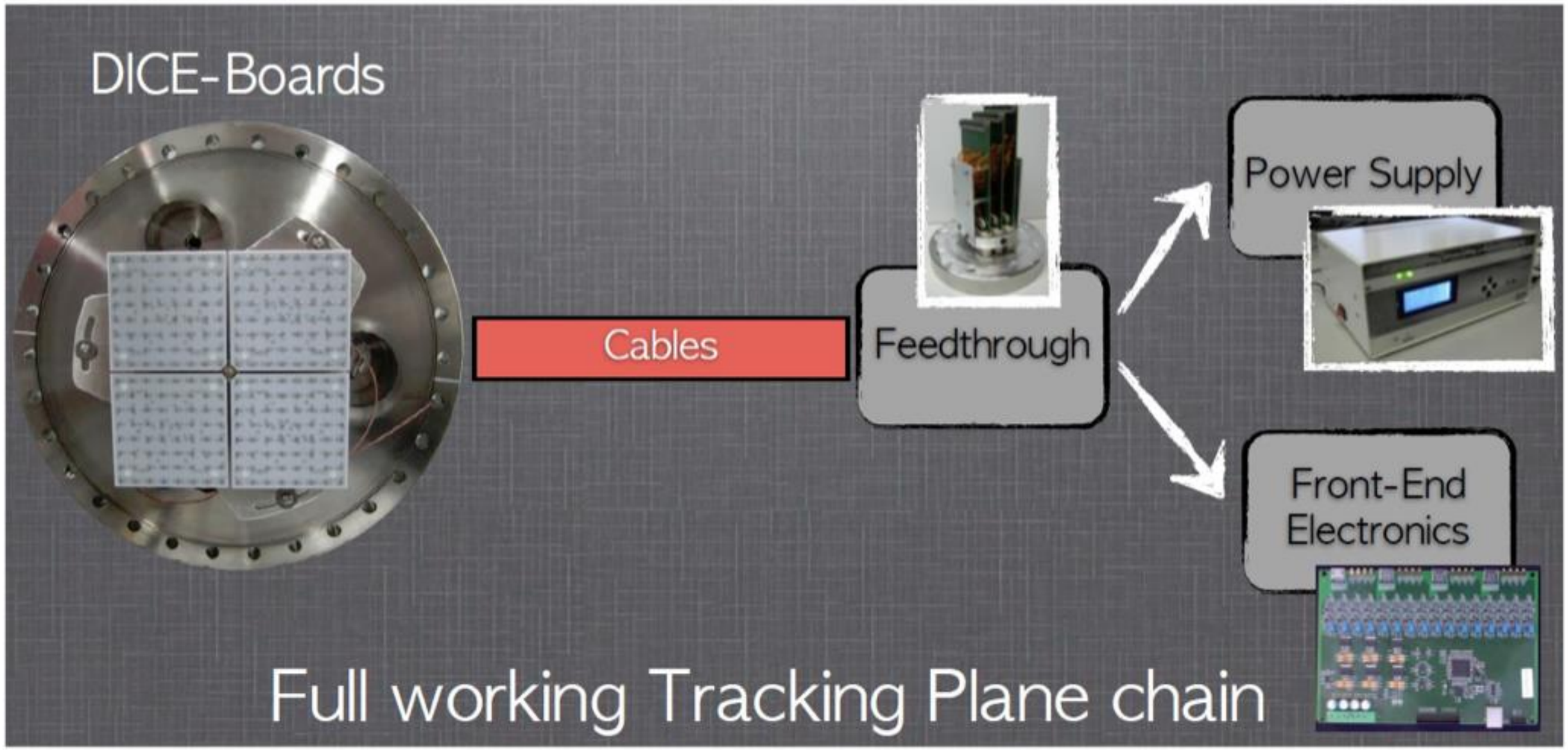
We're currently here!

3. NEXT-100

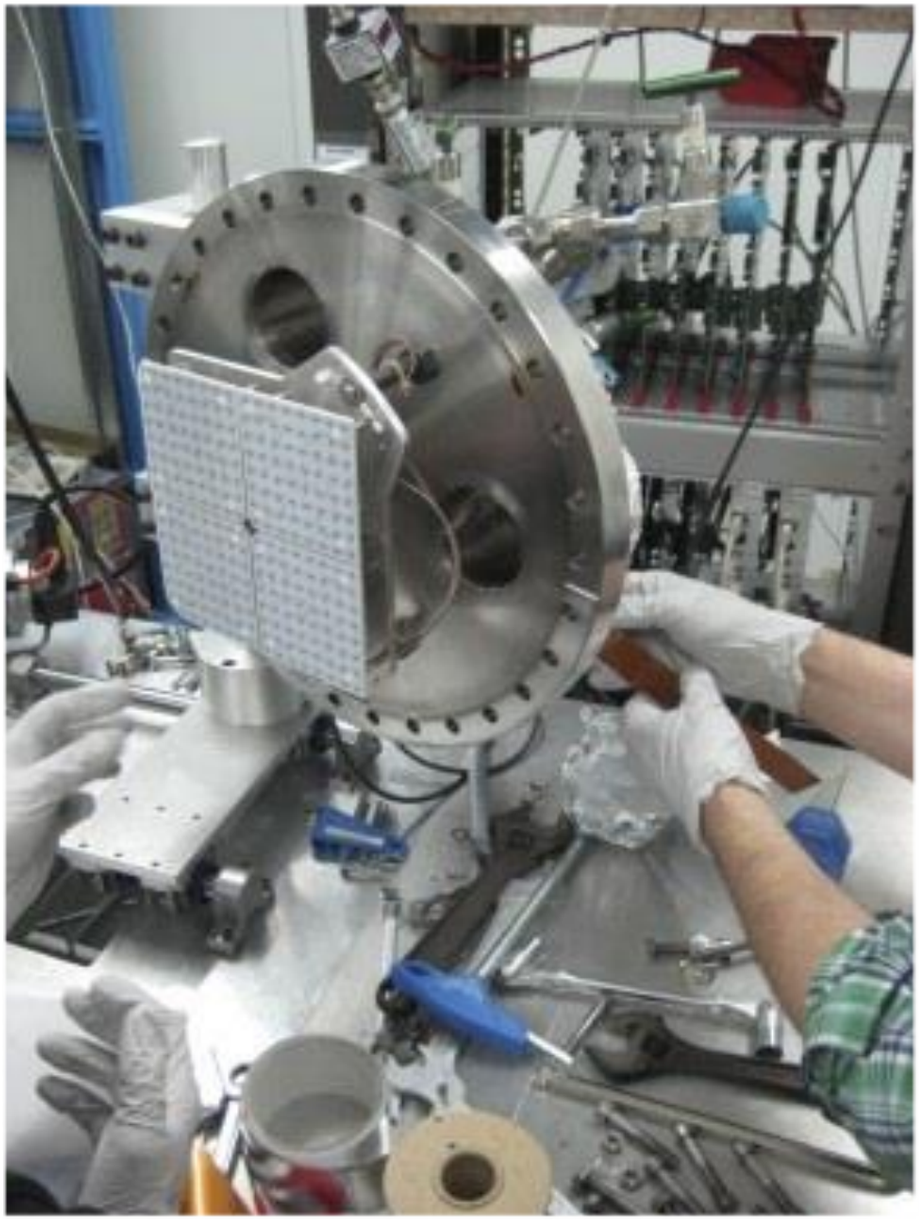
Panoramic view of NEXT-DEMO

IFIC, Valencia

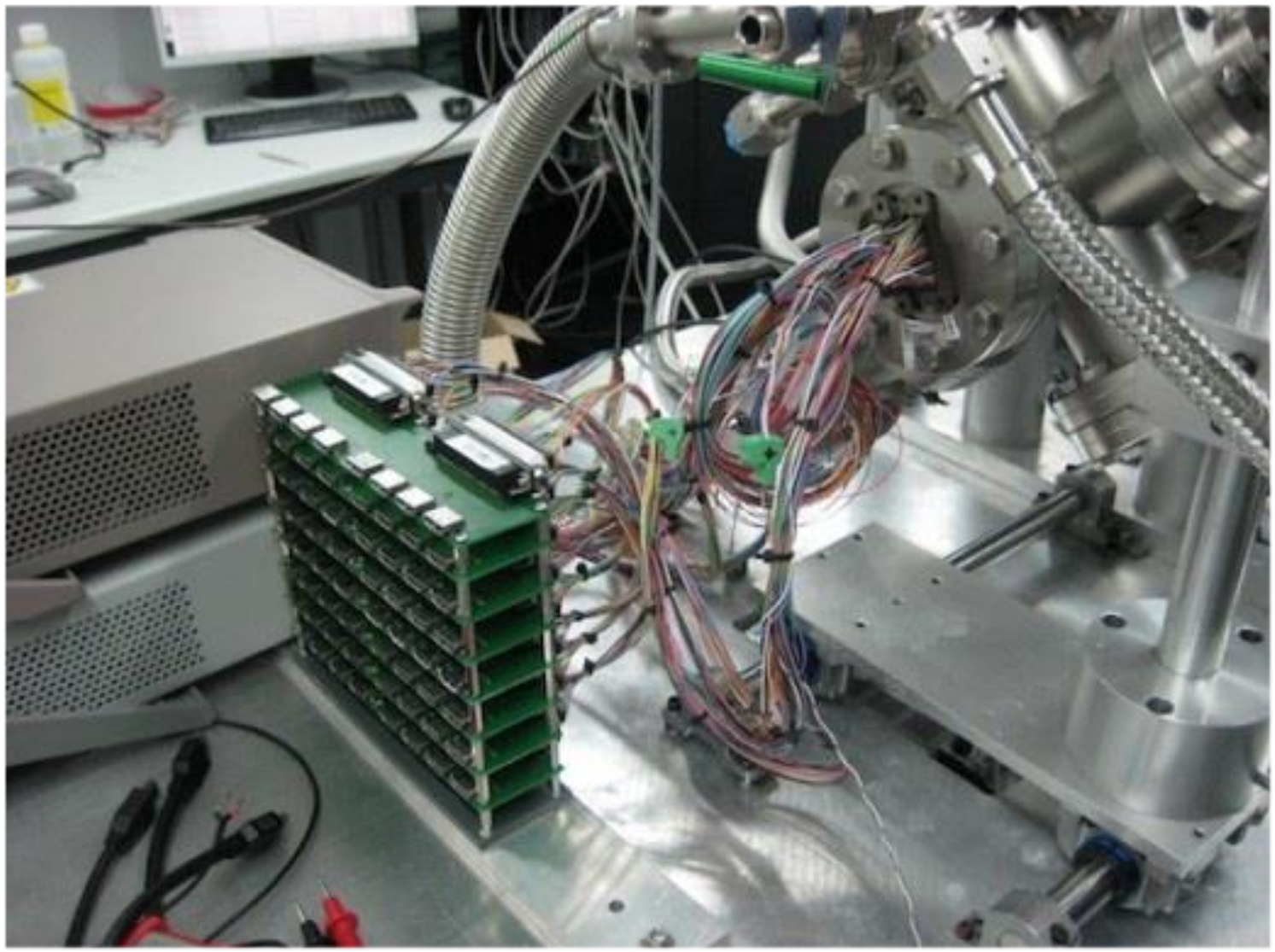
NEXT-DEMO: tracking plane



NEXT-DEMO



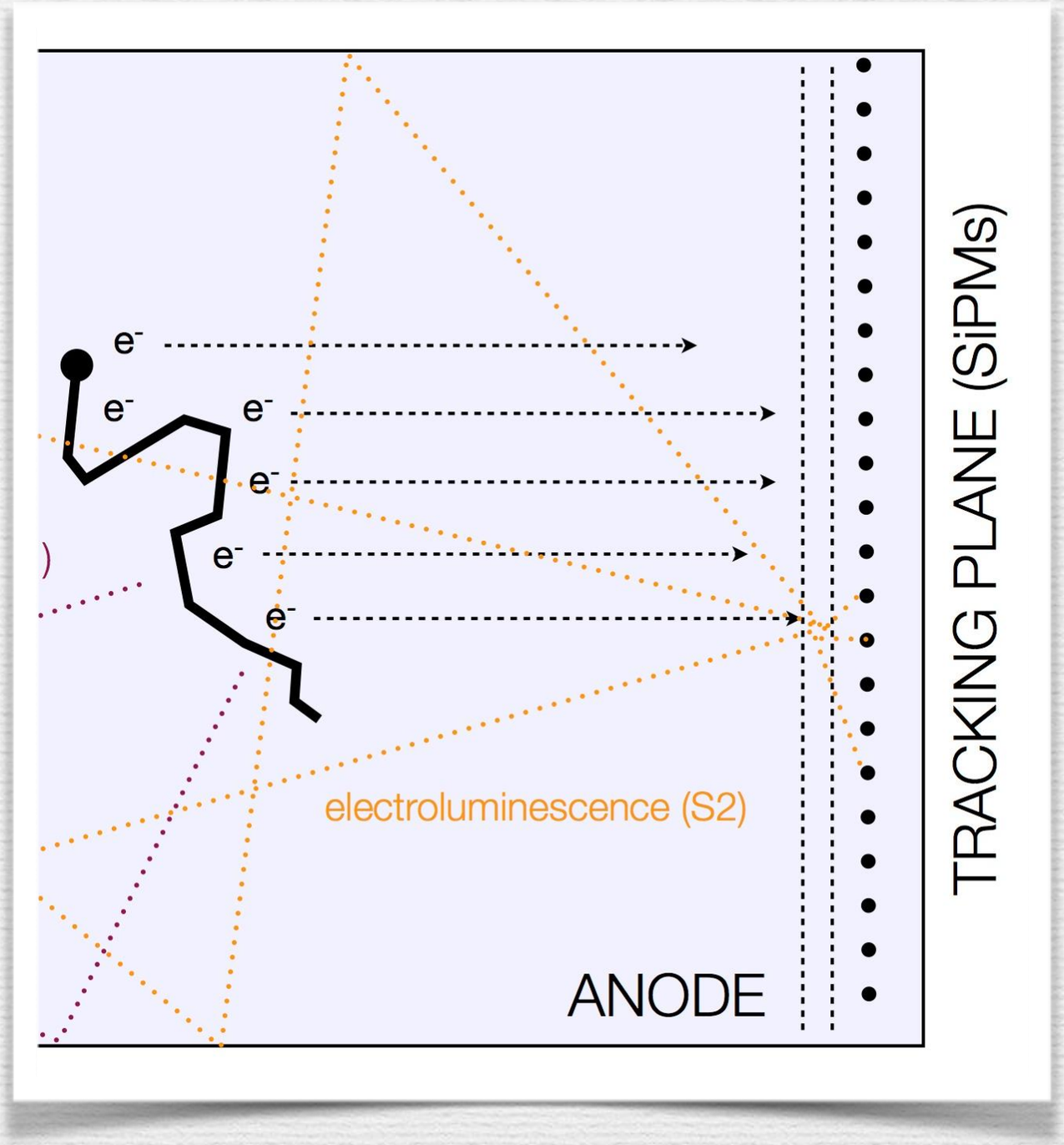
4x 64-SiPM boards (old)



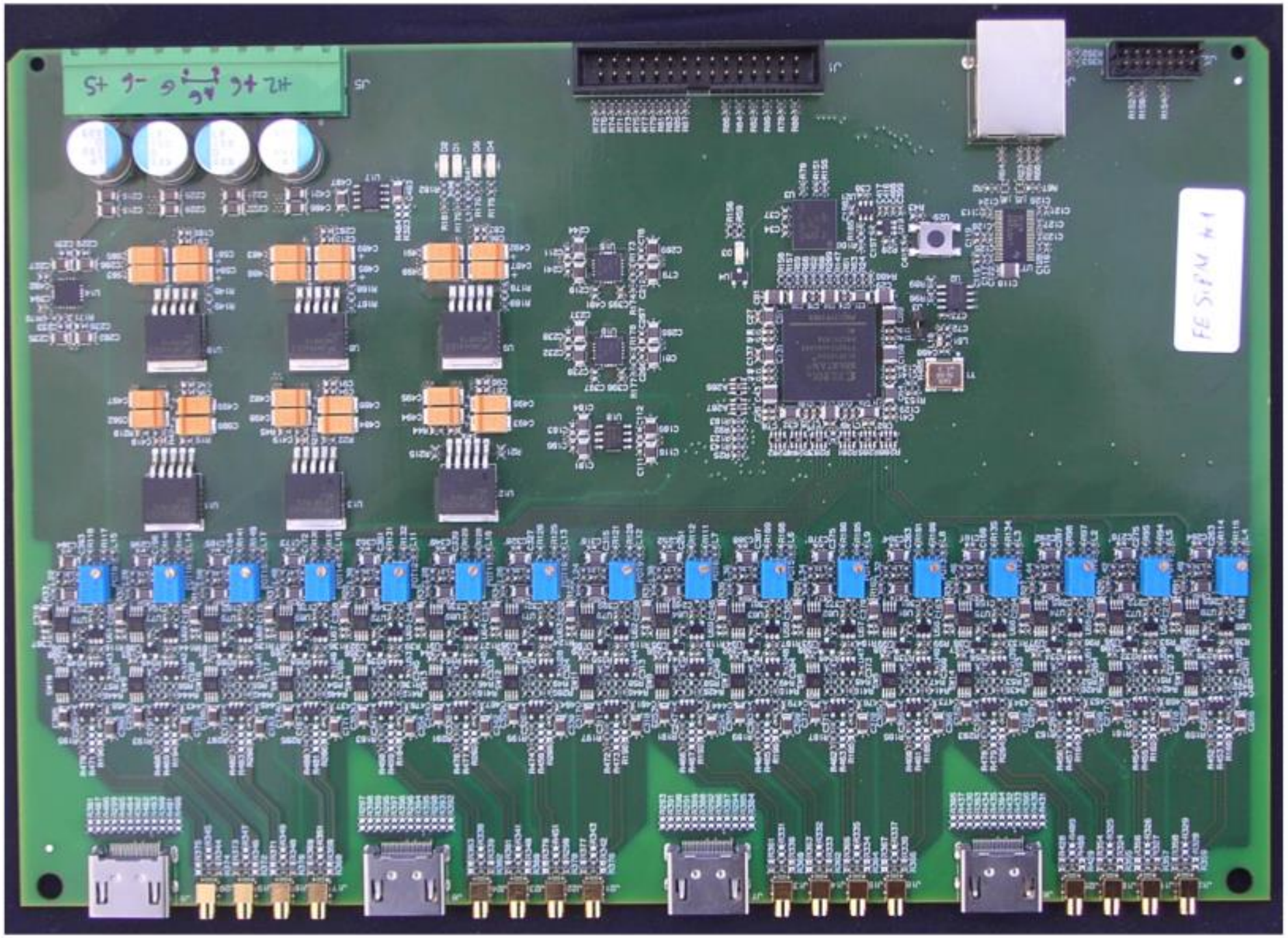
Wires coming out from the TPC and adaptation boards to HDMI

Summary of design parameters

- 256 ch (DEMO), 1.8 kch (NEW), 8 kch (NEXT-100)
- Dynamic range: up to 150 pe each μs (we use 12 bit ADCs)
- Goal: “How many photons impinge the SiPM each μs?”
- Distance from the SiPMs to the FE: 4-5 m
- Event length: from 800 us (DEMO) to 3 ms (NEXT-100)
- Trigger rate: 10 Hz



NEXT-DEMO

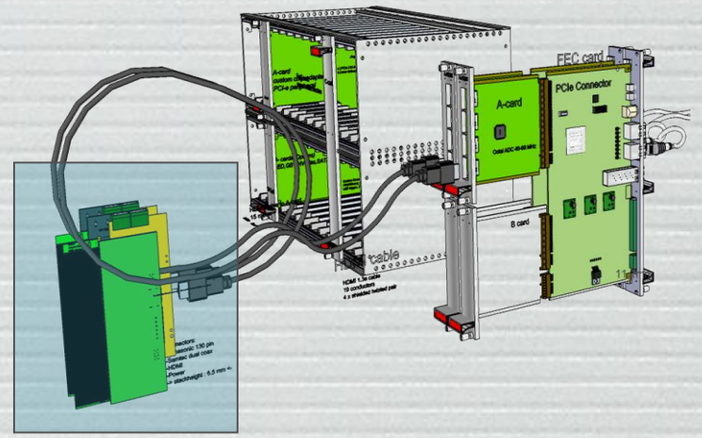


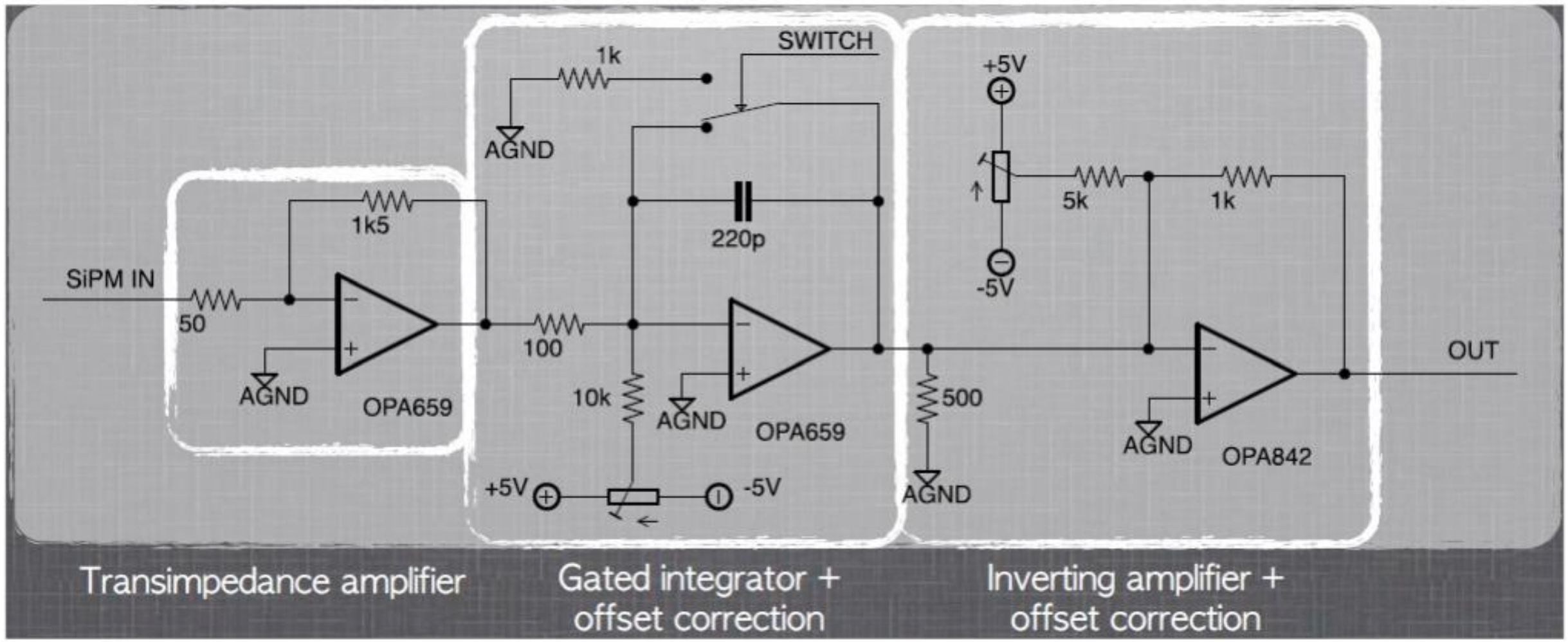
- No data buffer
- No zero-suppresion
- No trigger
- Data are pushed upstream each μs
- Clock sync with FEC
- Spartan-3AN FPGA
- RJ-45 LVDS output (DTC)

Our first FE board (16 ch, 6U)

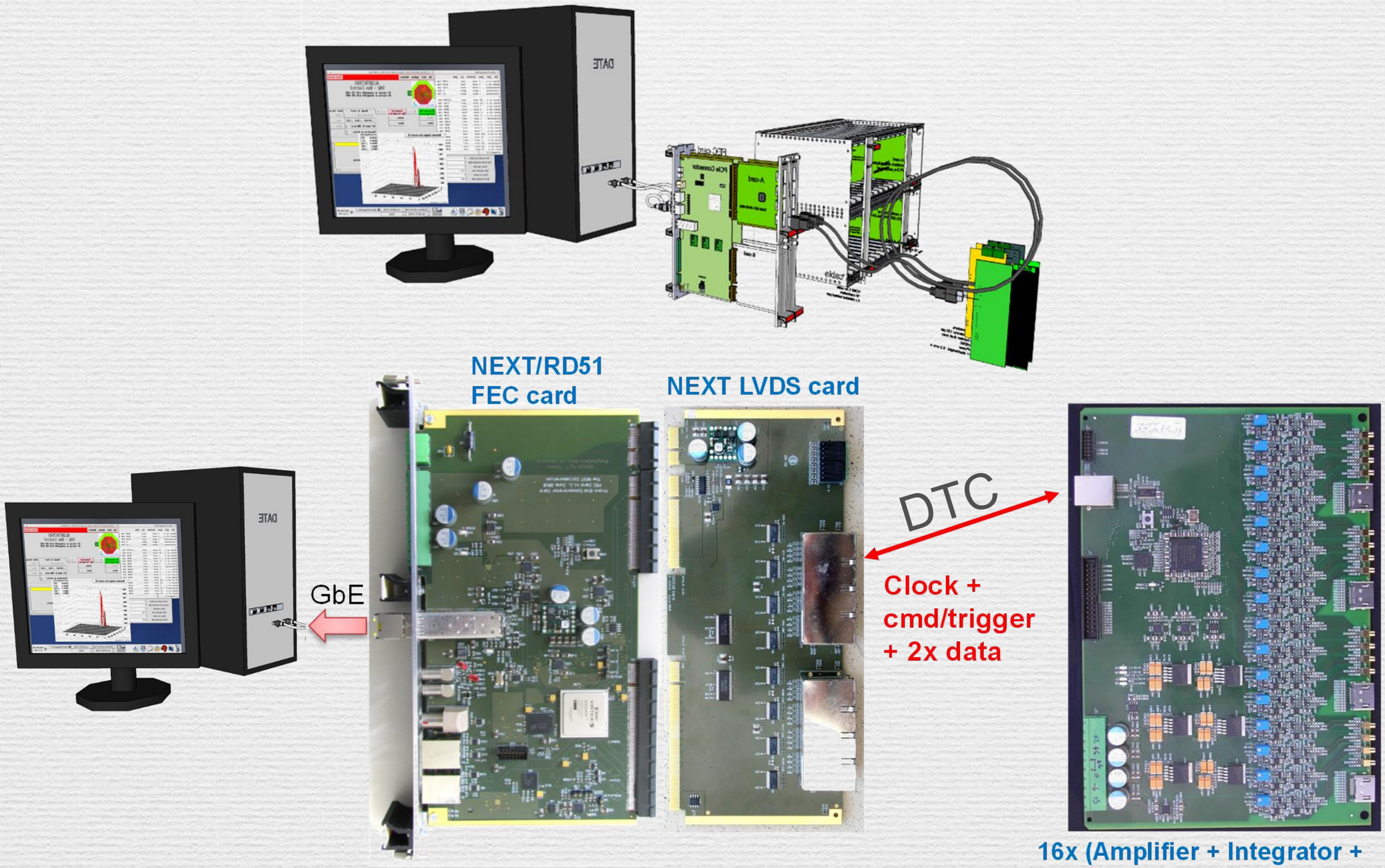
First FE design (DEMO)

Non-differential I/V amplifier + gated integrator + buffer

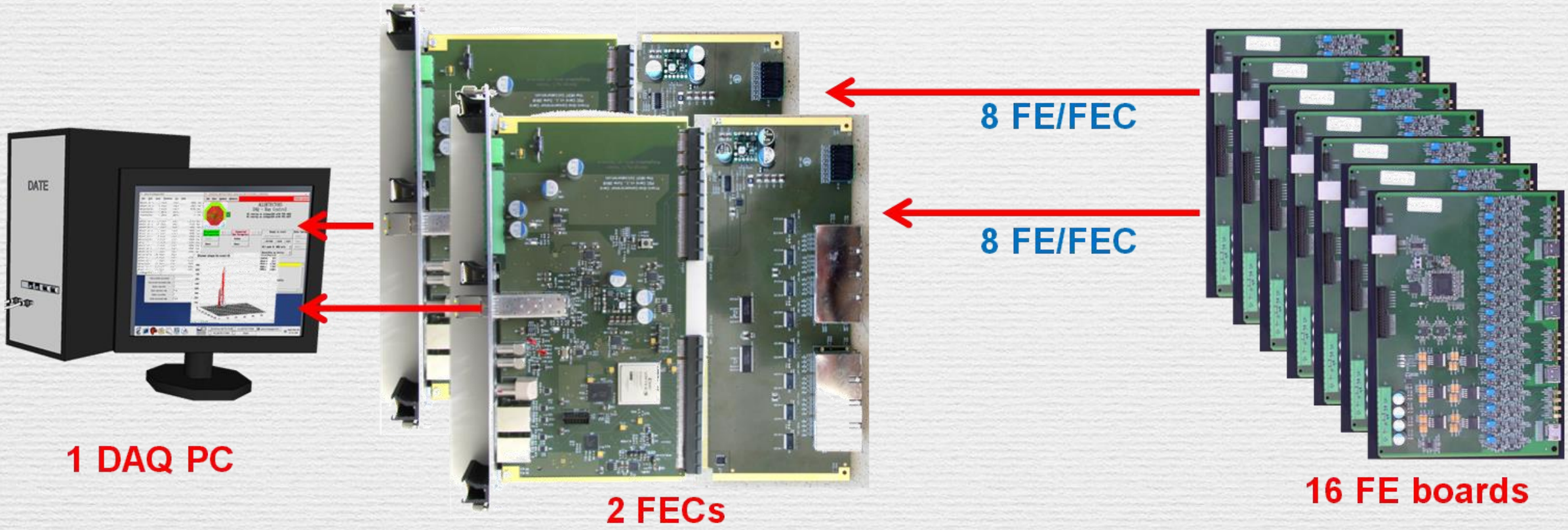




The SiPM readout chain in NEXT DEMO (simplified)

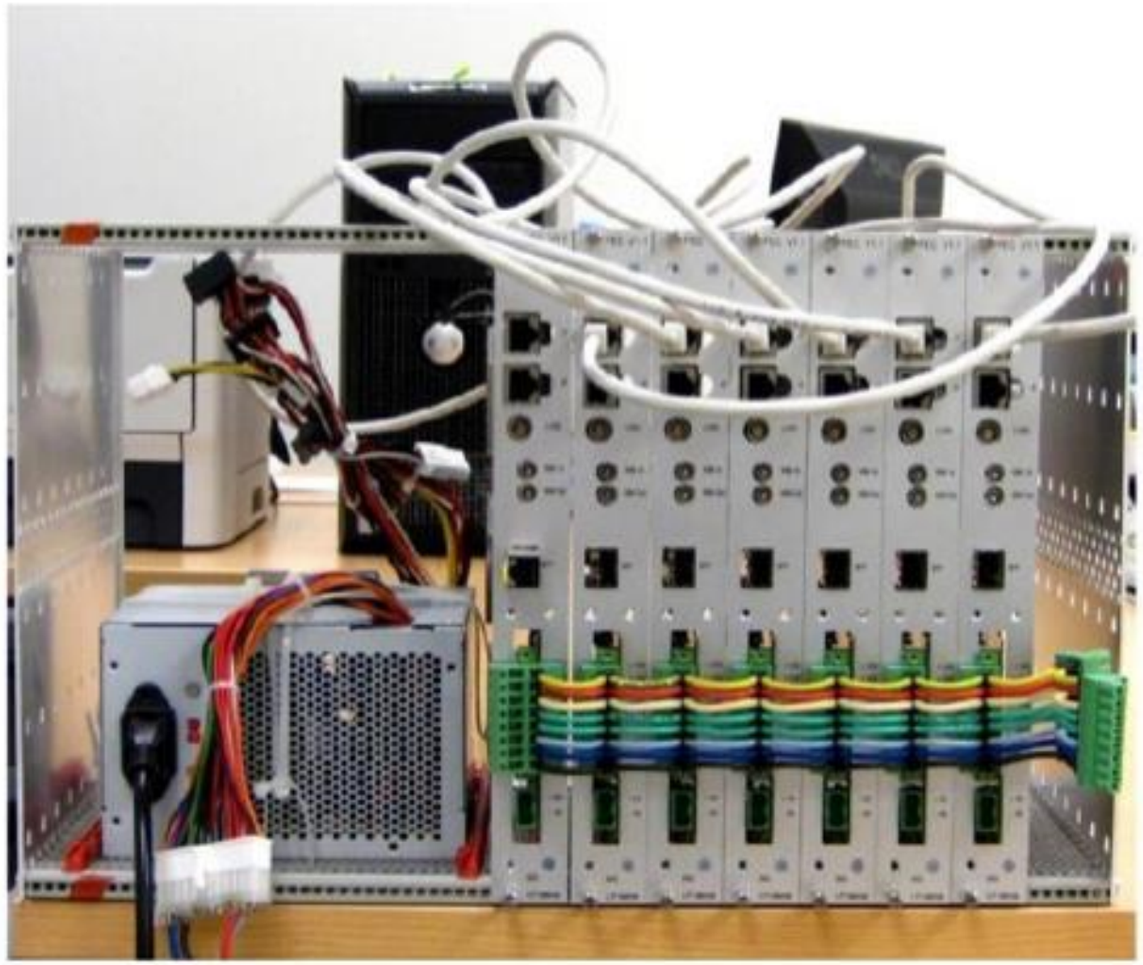


The SiPM readout chain in NEXT DEMO (complete)

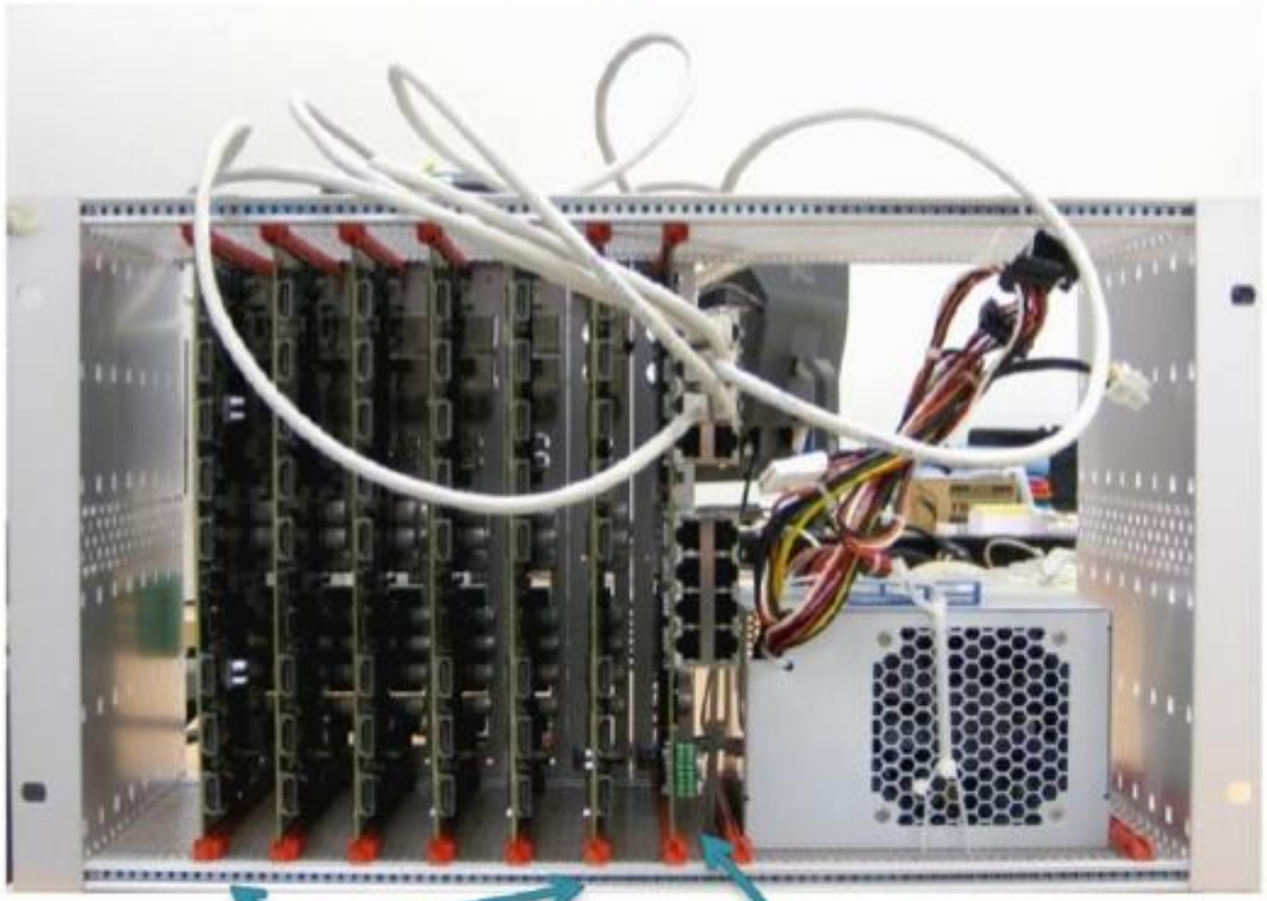


DAQ and trigger systems in NEXT-DEMO

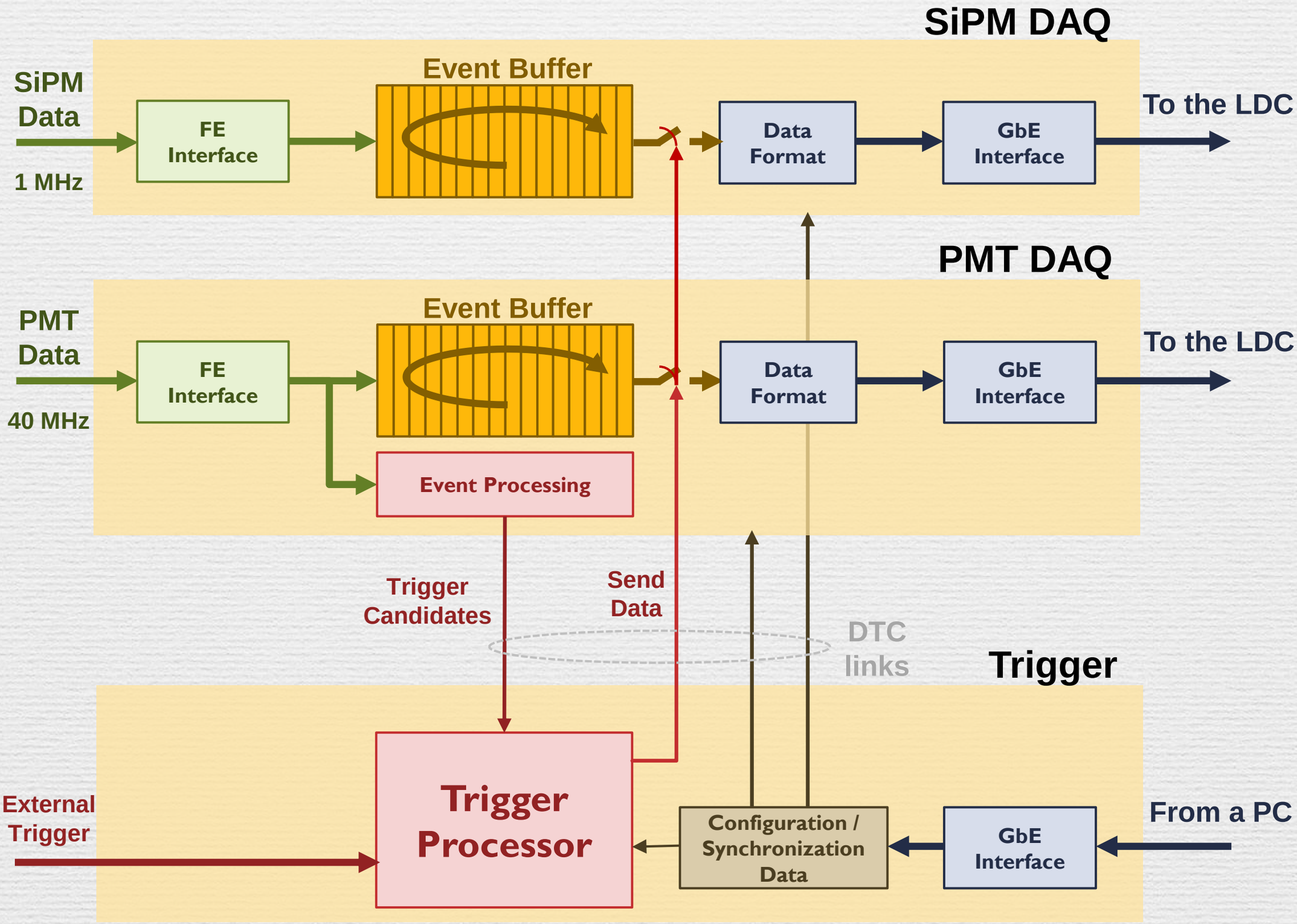
Front view



Rear view

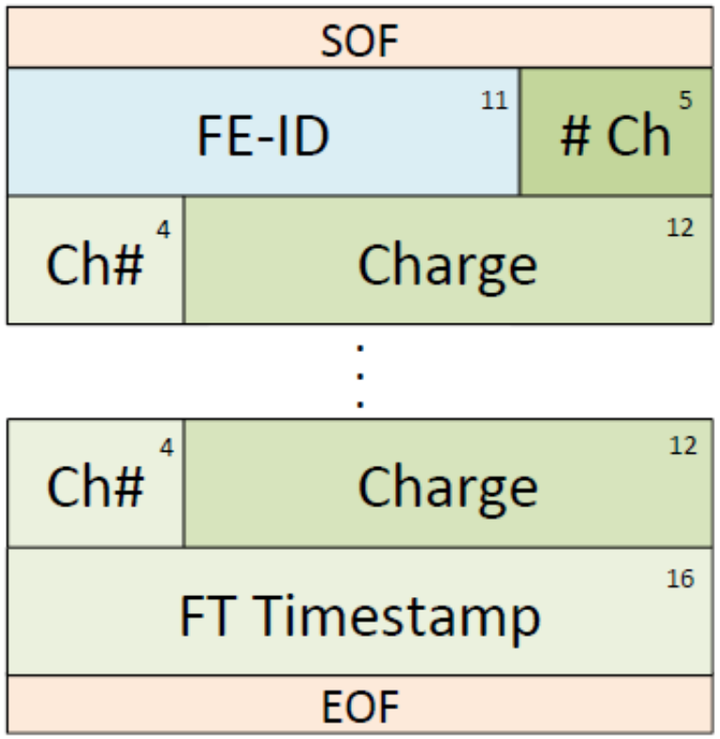


DAQ and trigger: operation



(Old) data formats in NEXT-DEMO

Upstream data frame format (max. twenty 16-bit words, one frame each us)



→ Start of frame word

→ Unique FE card ID + Number of active channels

→ Channel ID (4bit) + channel ADC count (12bit)

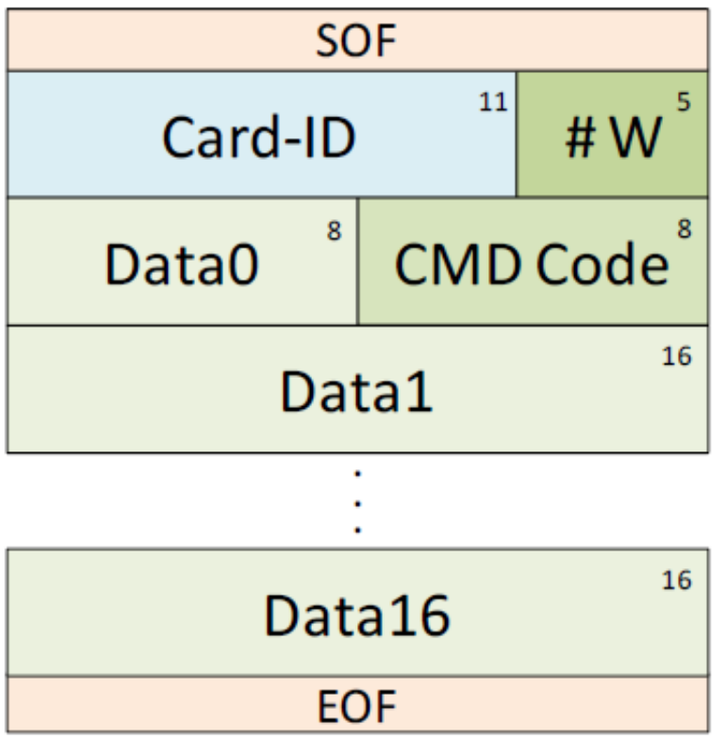
→ Timestamp + error flag

→ End of frame word

CRC just added to the data formats!

Downstream command frame

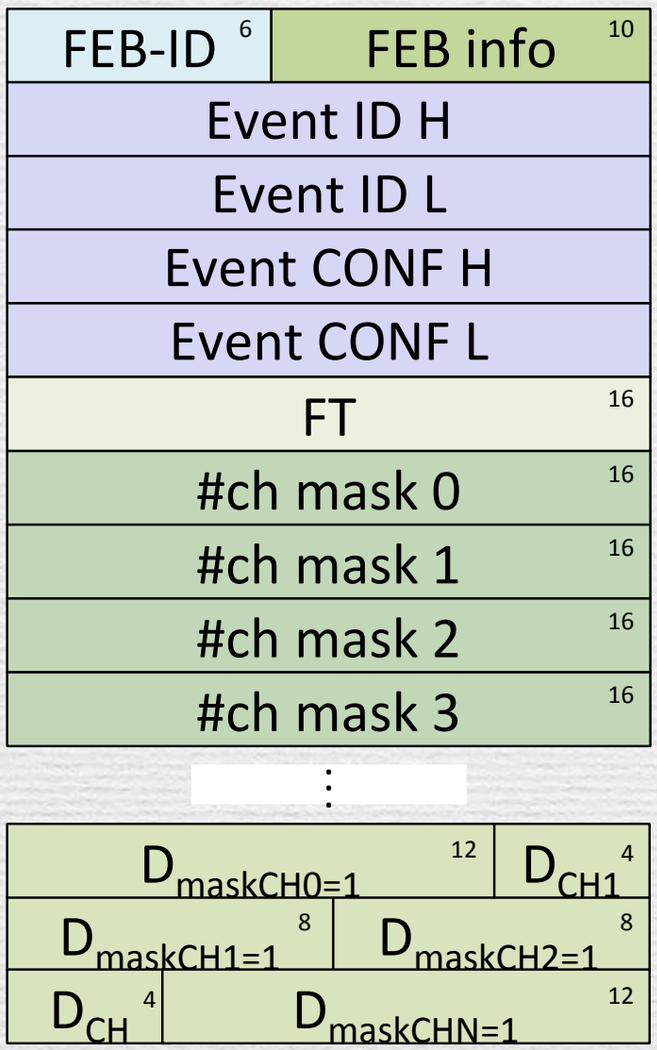
COMMANDS CODIFICATION				
CMD Code	**Command**	**Description**	**Address to**	**Source**
00h	ACQUISITION	Configuration, start/stop acquition	FEC/FE-SiPM	DATE/FEC TRG
01h	TRIGGER	Trigger command	FEC/FE-SiPM	FEC TRG
02h	WRITE REGISTER	Write configuration register	FEC/FE-SiPM	FEC
03h	READ REGISTER	Read configuration/status register	FEC/FE-SiPM	FEC
04h	STATUS	Status information (alarms, errors…)	FEC TRG	FEC
05h	SYNC	Synchronization command	FEC/FE-SiPM	FEC TRG



NEW (DTC) data formats in NEXT

Zero-suppressed data ar sent from FE to FEC ONLY when a trigger is received

Payload is encapsulated in DTC frames



→ FEB card ID + FEB info

Provided by the trigger module in the Trigger command: Trigger type and number

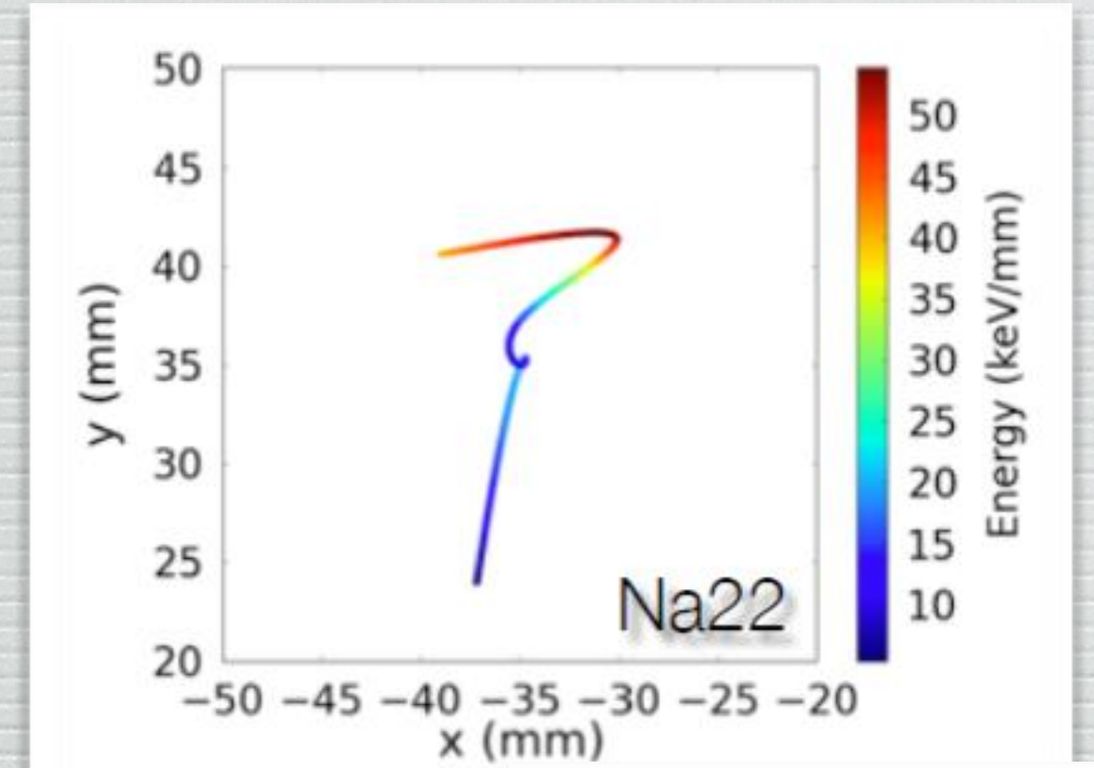
Event configuration: Total waveform length and pre-trigger

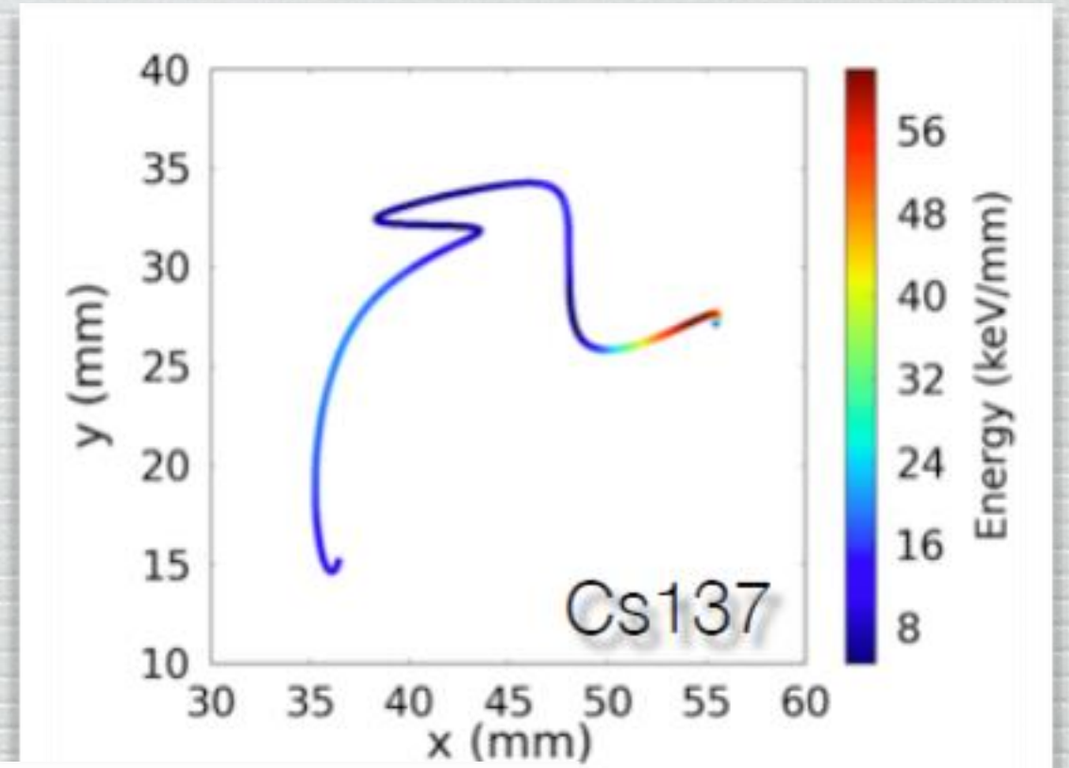
→ FT Timestamp

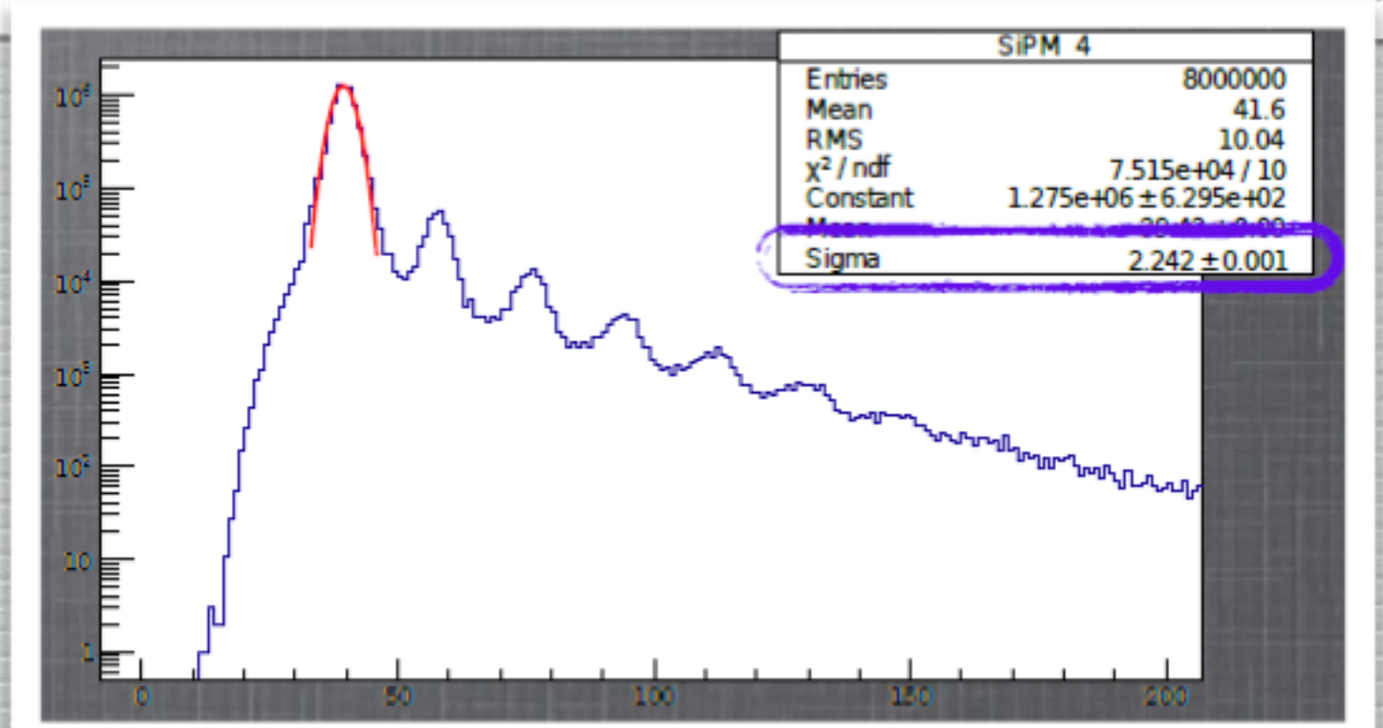
→ Data mask for 64 channels per FT

FT Block: Everytime for a given FT with data to be sent

NEXT-DEMO

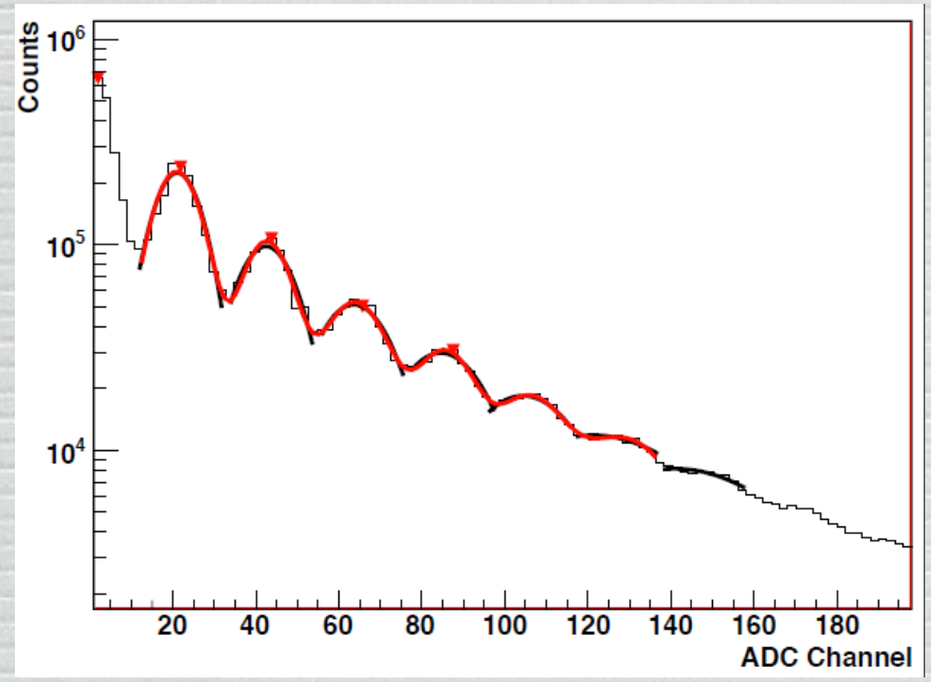






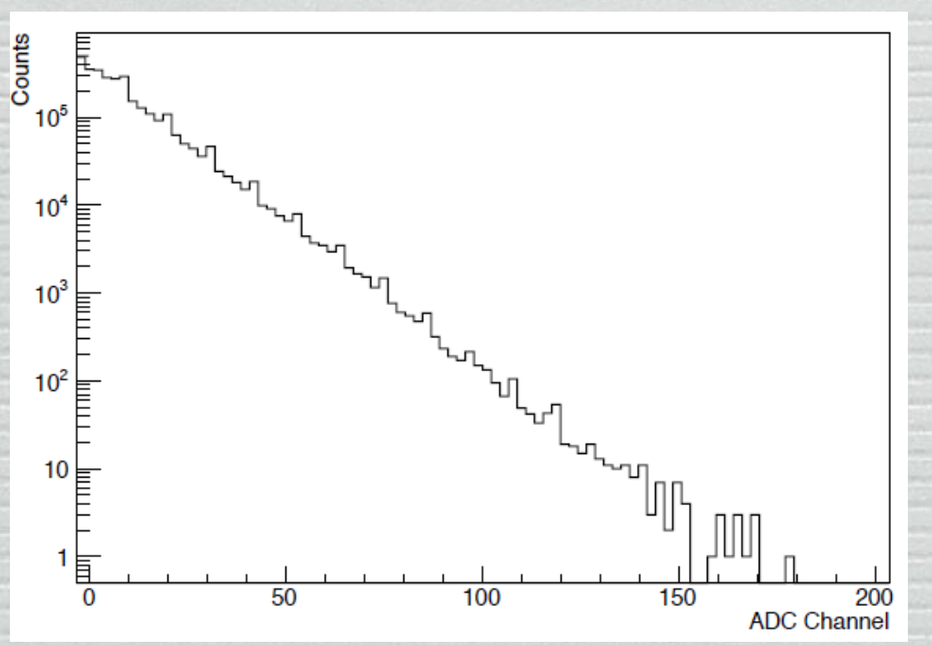
Good performance!

NEXT-DEMO



Dark current in in a SiPM channel using coax cables allows calibration base on dark count spectrum ☺

Approx. Gain is 20 ADC counts/pe



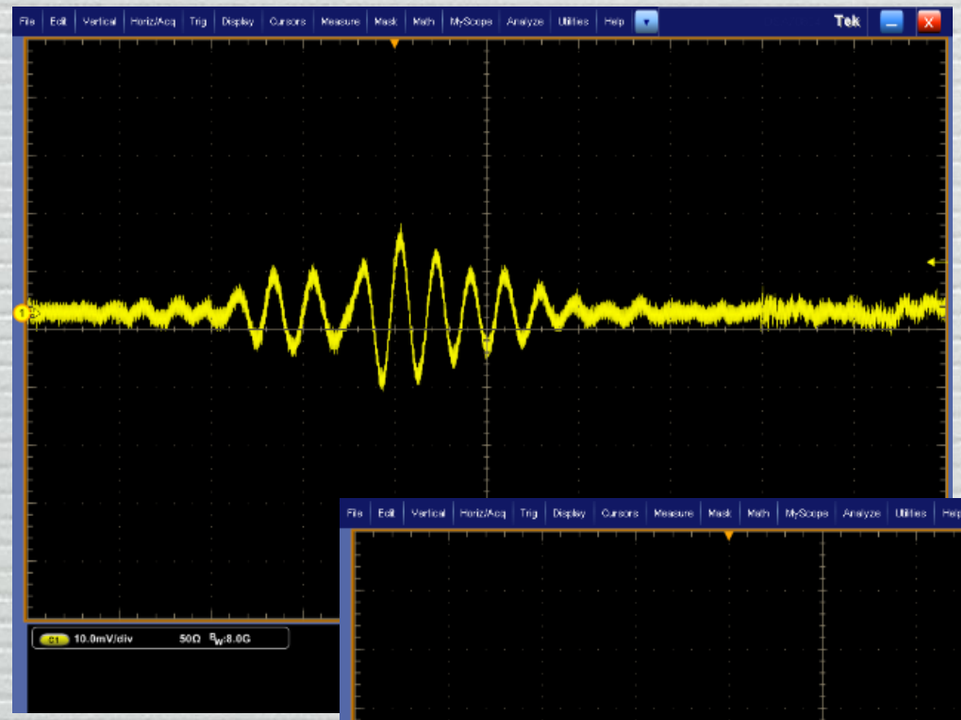
Dark current in in a SiPM channel using wires or ribbon cable ☹

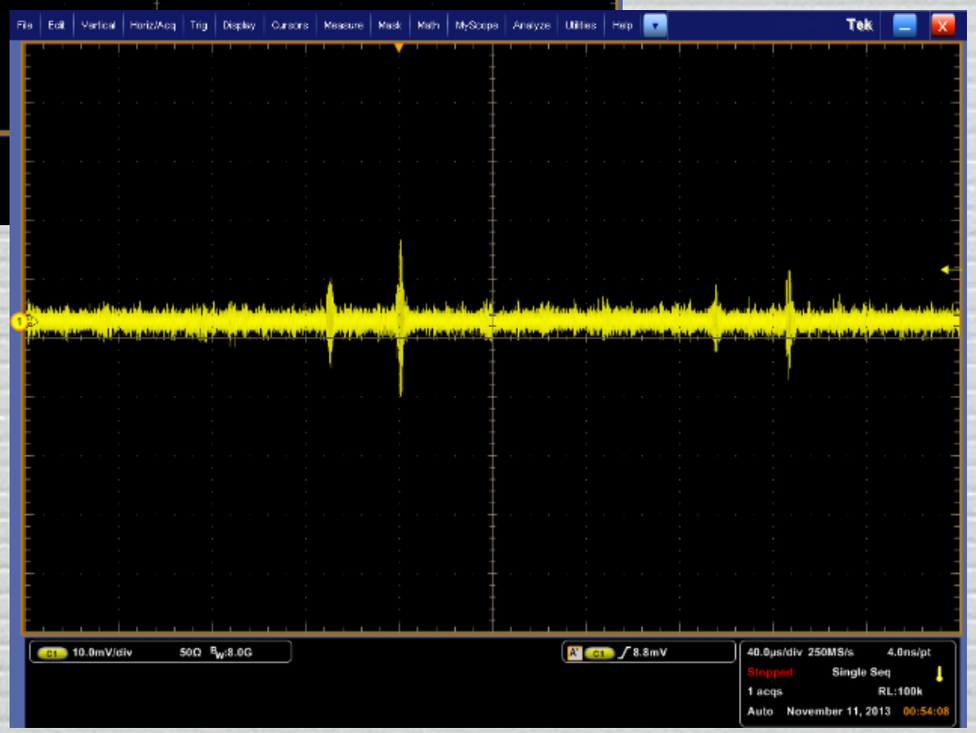
Still, we can do proper tracking, as noise is approx. 1pe in amplitude

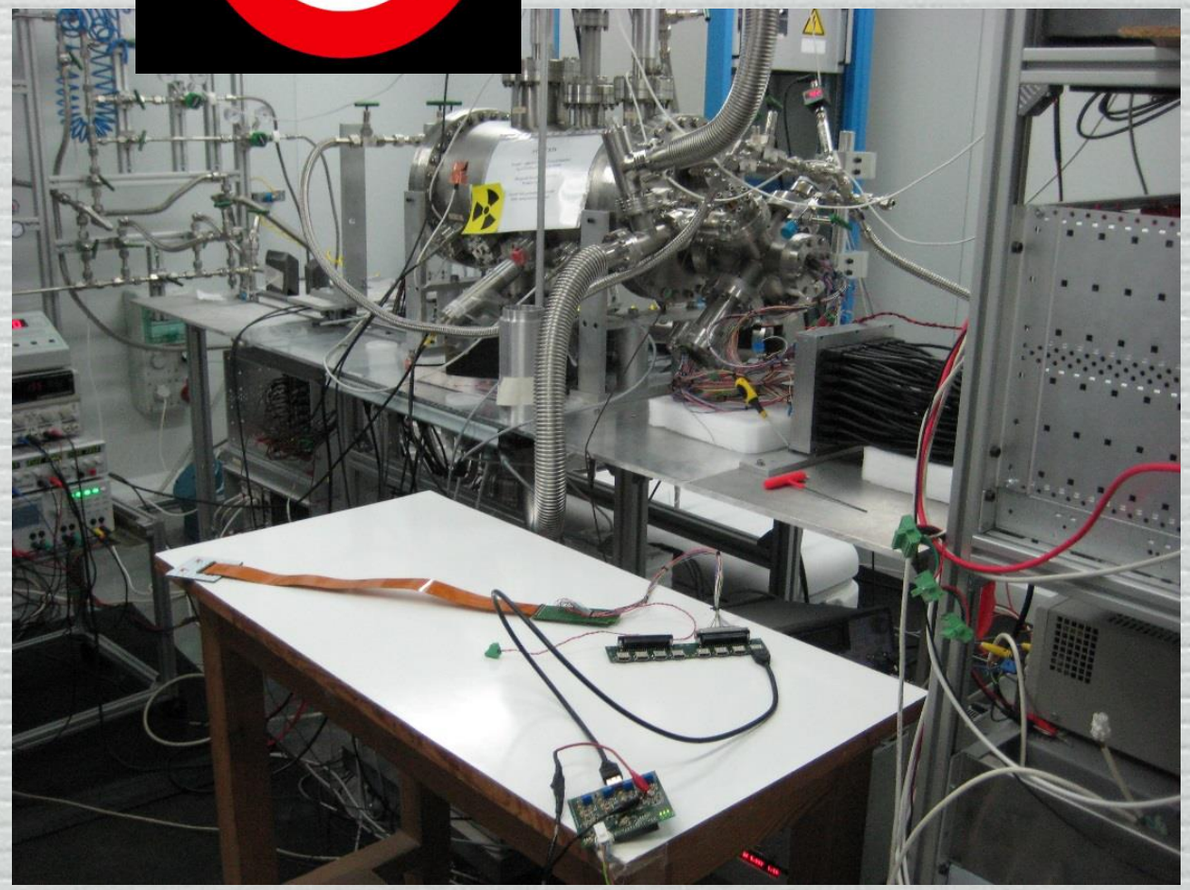
Noise is killing our calibration based on SiPM dark current…

What does our noise look like?

- It has a 2 MHz – 8 MHz bandwidth
- Consists of (non-periodic) bursts of damped 2-4 MHz tones

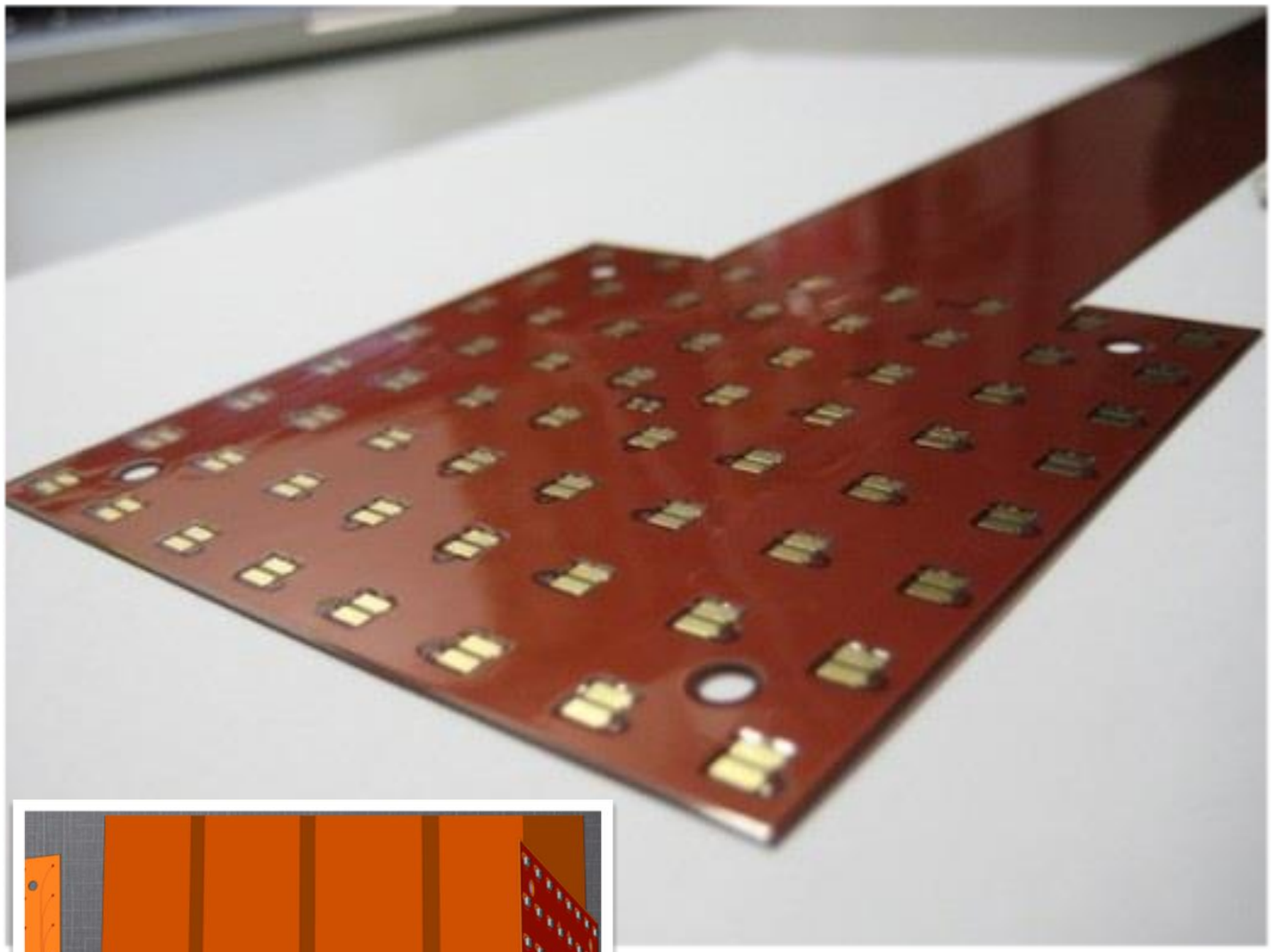


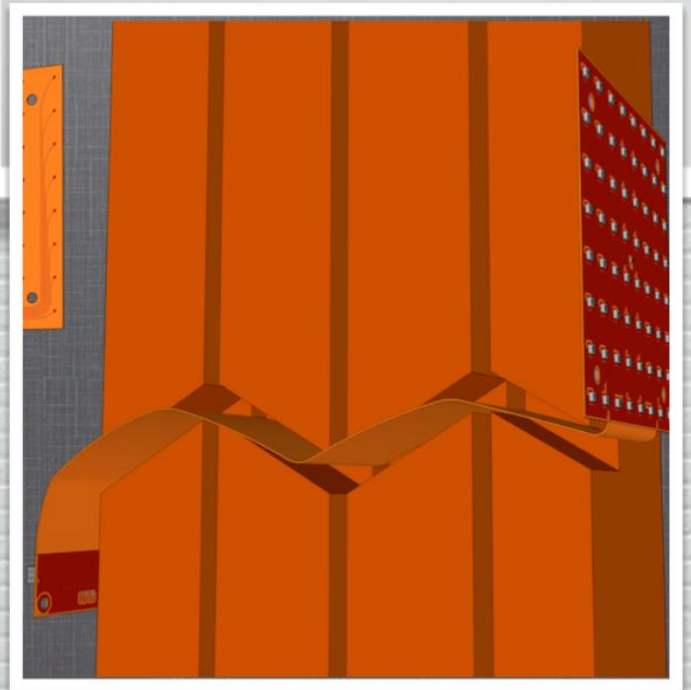




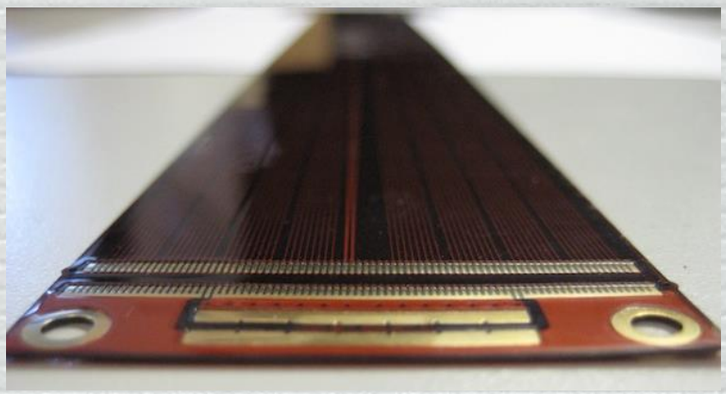
What would you do to fix the noise problem?

NEW kapton SiPM boards for NEW





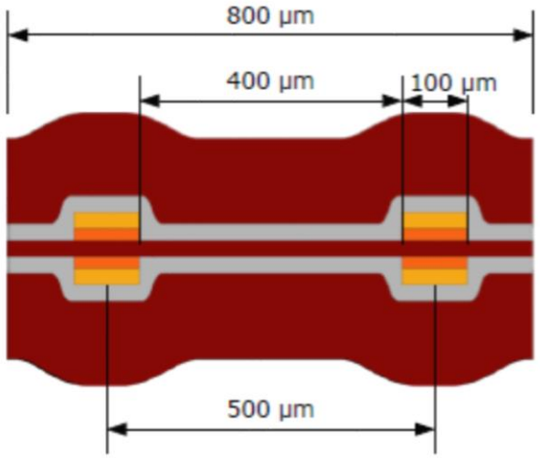
Good:



- **Radio clean**
- **SiPMs are mounted in oven**
- **Pigtail passes through copper shield**
- **Enhanced noise immunity**

Bad:

- **Only 2 copper layers to avoid adhesive (radiopurity required) prevent shielding**
- **Expensive solution**

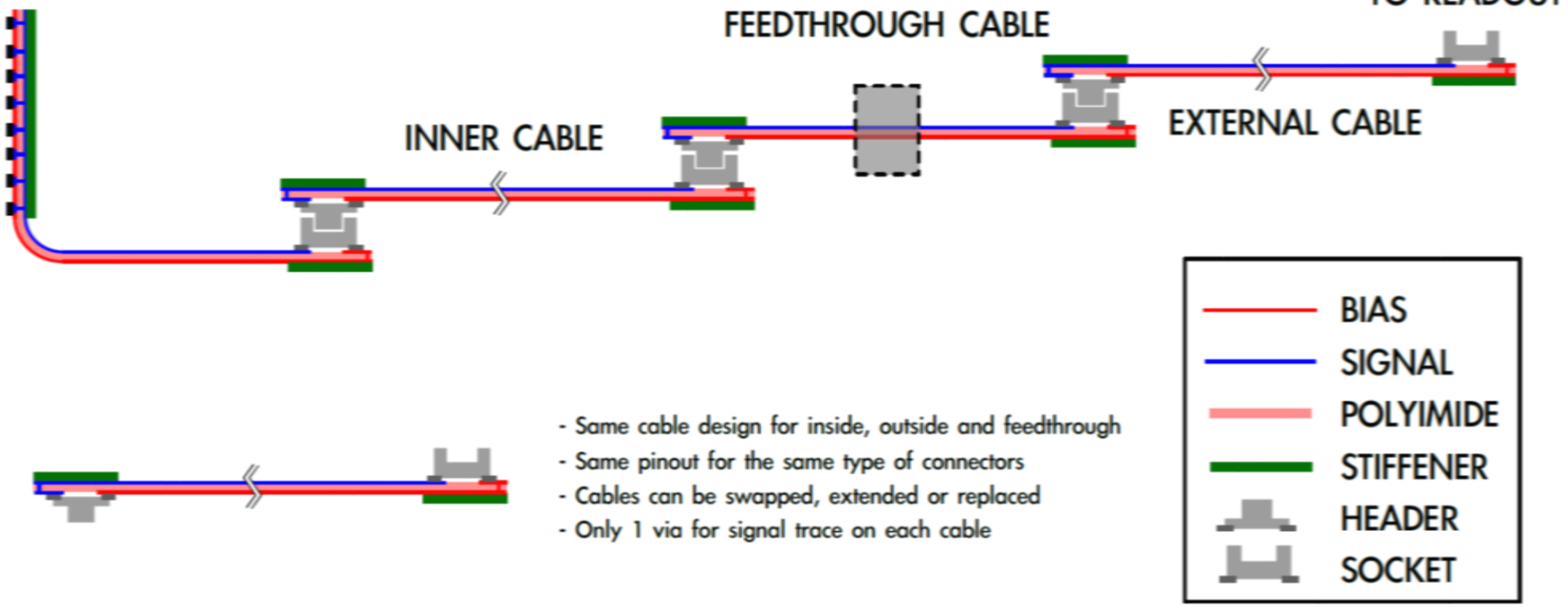


127 µm polyimide coverlay
25 µm adhesive
25 µm plating (ENIG)
18 µm copper
25 µm polyimide core
18 µm copper
25 µm plating (ENIG)
25 µm adhesive
127 µm polyimide coverlay

Broadside coupled traces

CABLE SCHEME

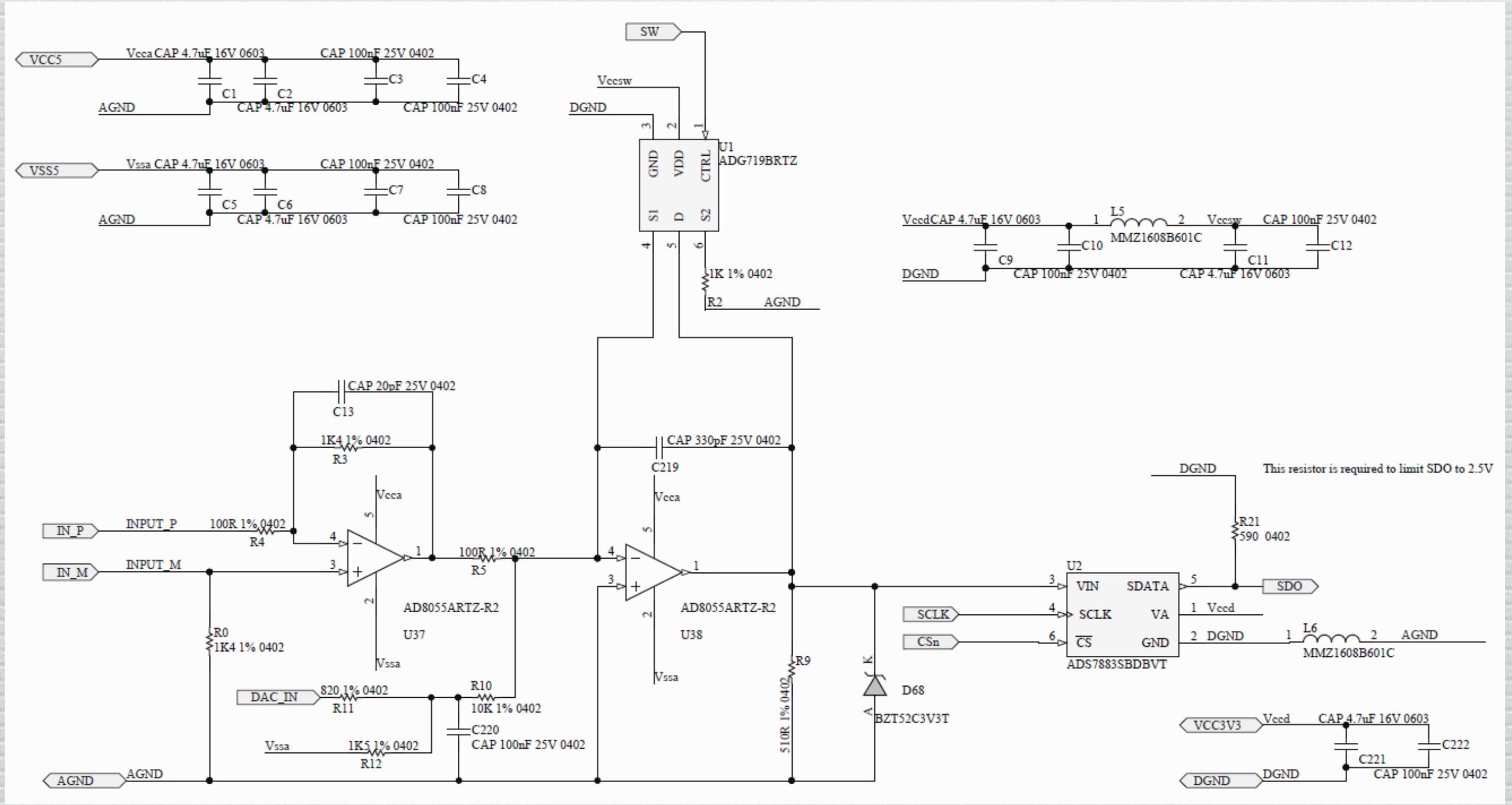
KAPTON DICE-BOARD (KDB)



- Same cable design for inside, outside and feedthrough
- Same pinout for the same type of connectors
- Cables can be swapped, extended or replaced
- Only 1 via for signal trace on each cable

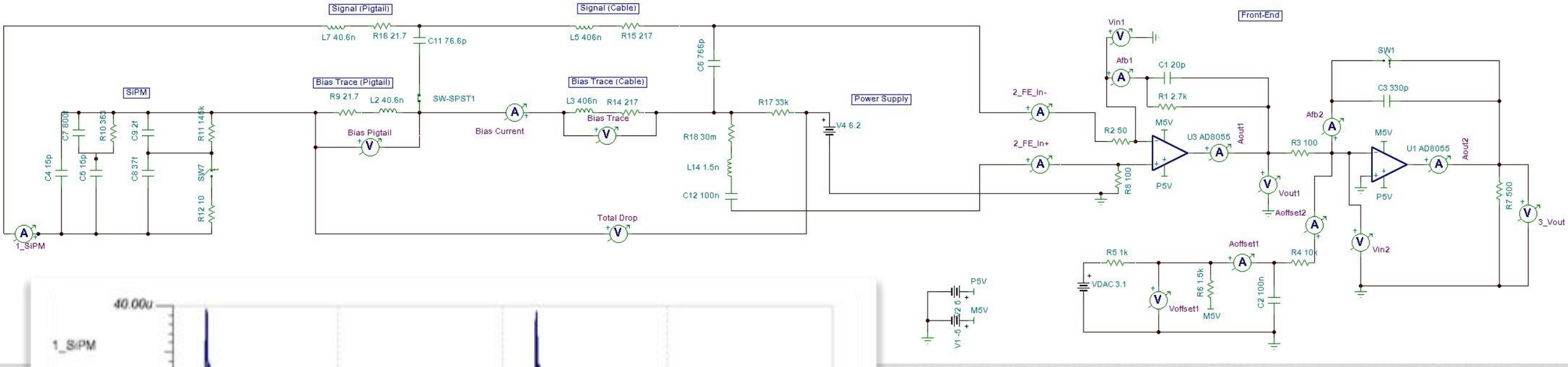
Broad-side coupled traces for better symmetry, cable bundles have basic shielding after they leave the detector

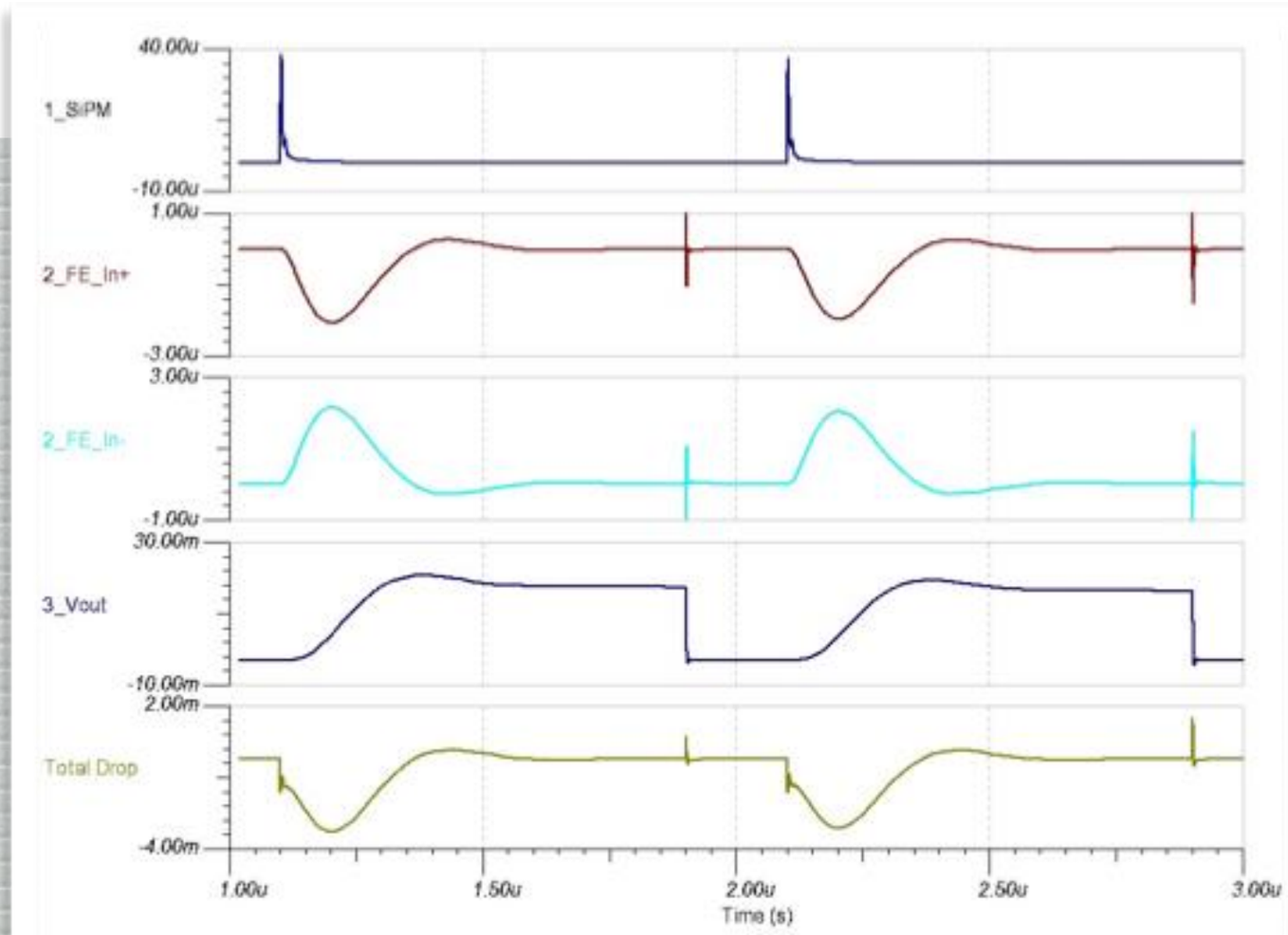
Modified front end for NEW



Differential I/V amplifier + gated integrator + automatic offset compensation + reduced power and cost

SPICE simulations for cable + FE





Is signal still ok after a 4m cable?

Our SPICE model says “yes”

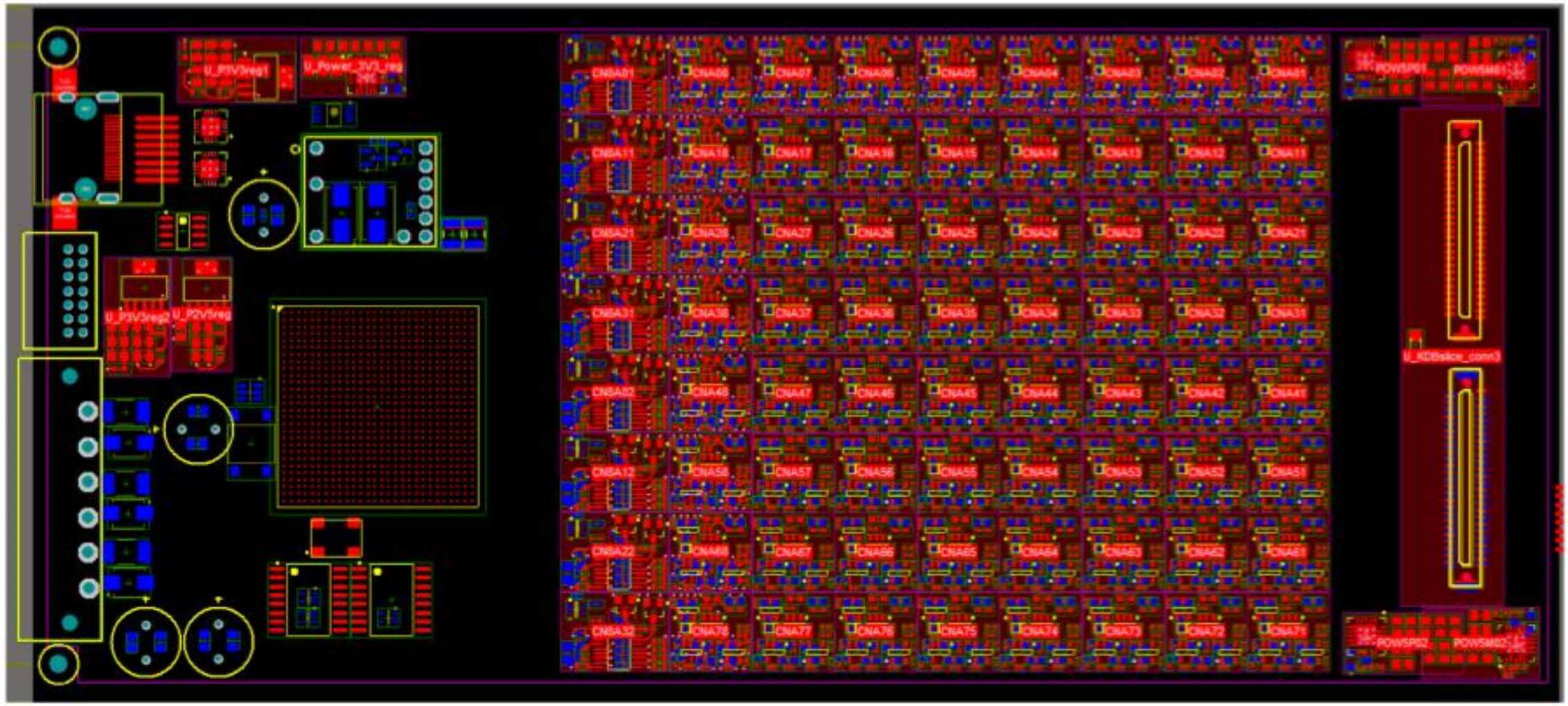
64 x ANALOG CHAINS

RJ45/HDMI

DAQ interface

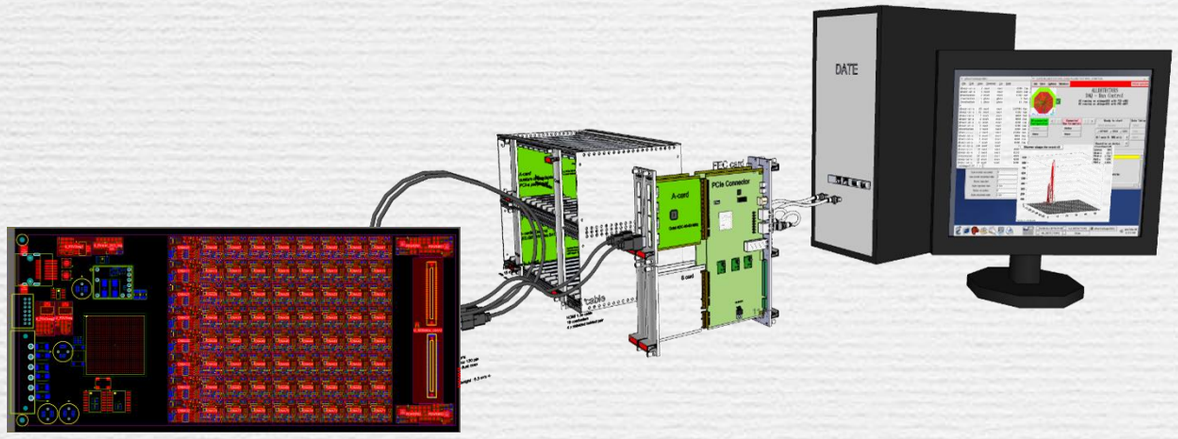
JTAG

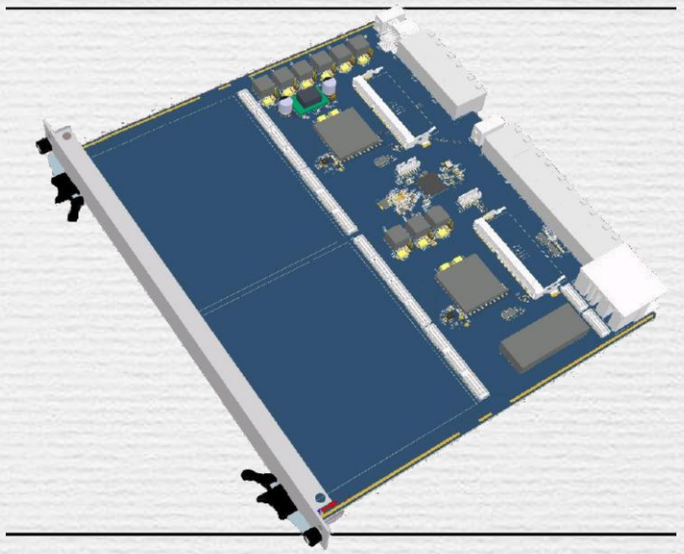
Power



Mock-up for our front-end board for NEW (64 ch, 3Ux220mm) with RJ-45/HDMI DTC link PCB design has started…

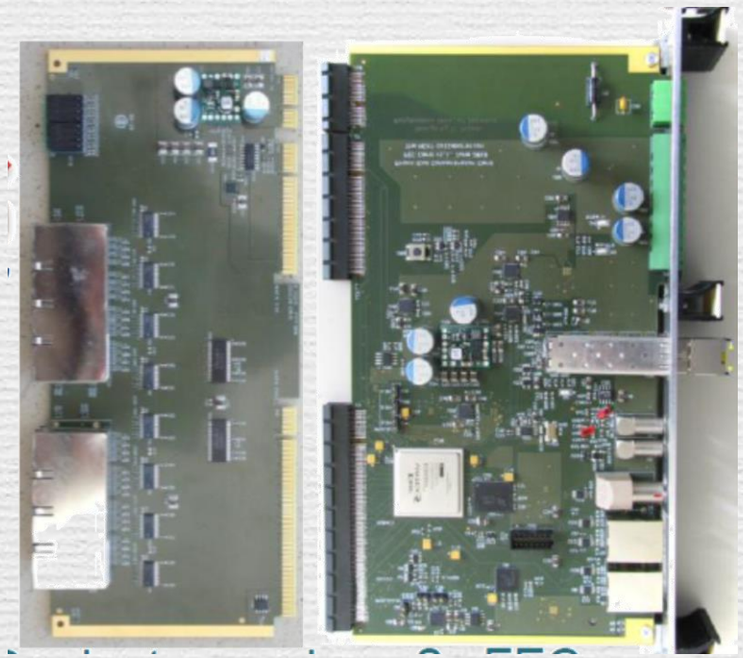
Interfacing the NEW front-end with SRS

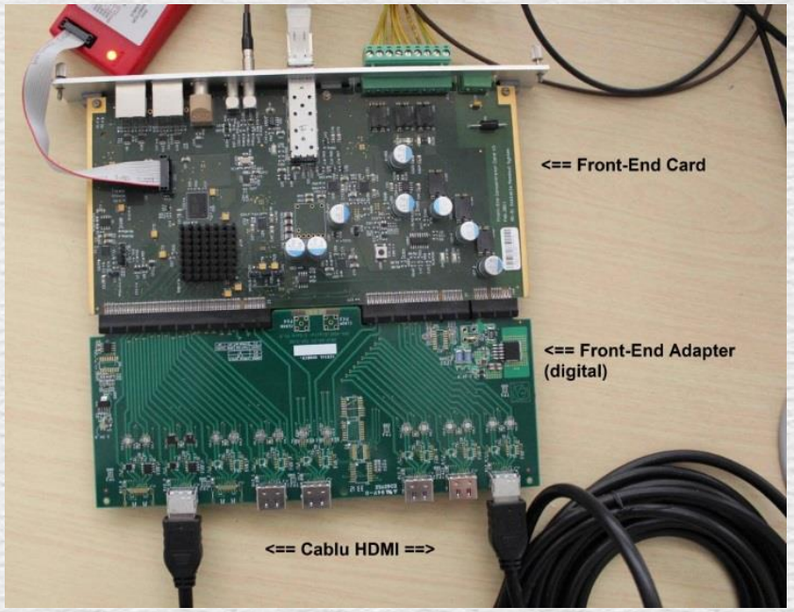




3 options

- **FEC ATCA blade + HDMI LVDS interface add-in cards**
- **FECv6 classic + RD51 digital interface add-in cards**
- **FECv6 classic + NEXT CDTC16 add-in cards**





DAQ and trigger systems in NEW

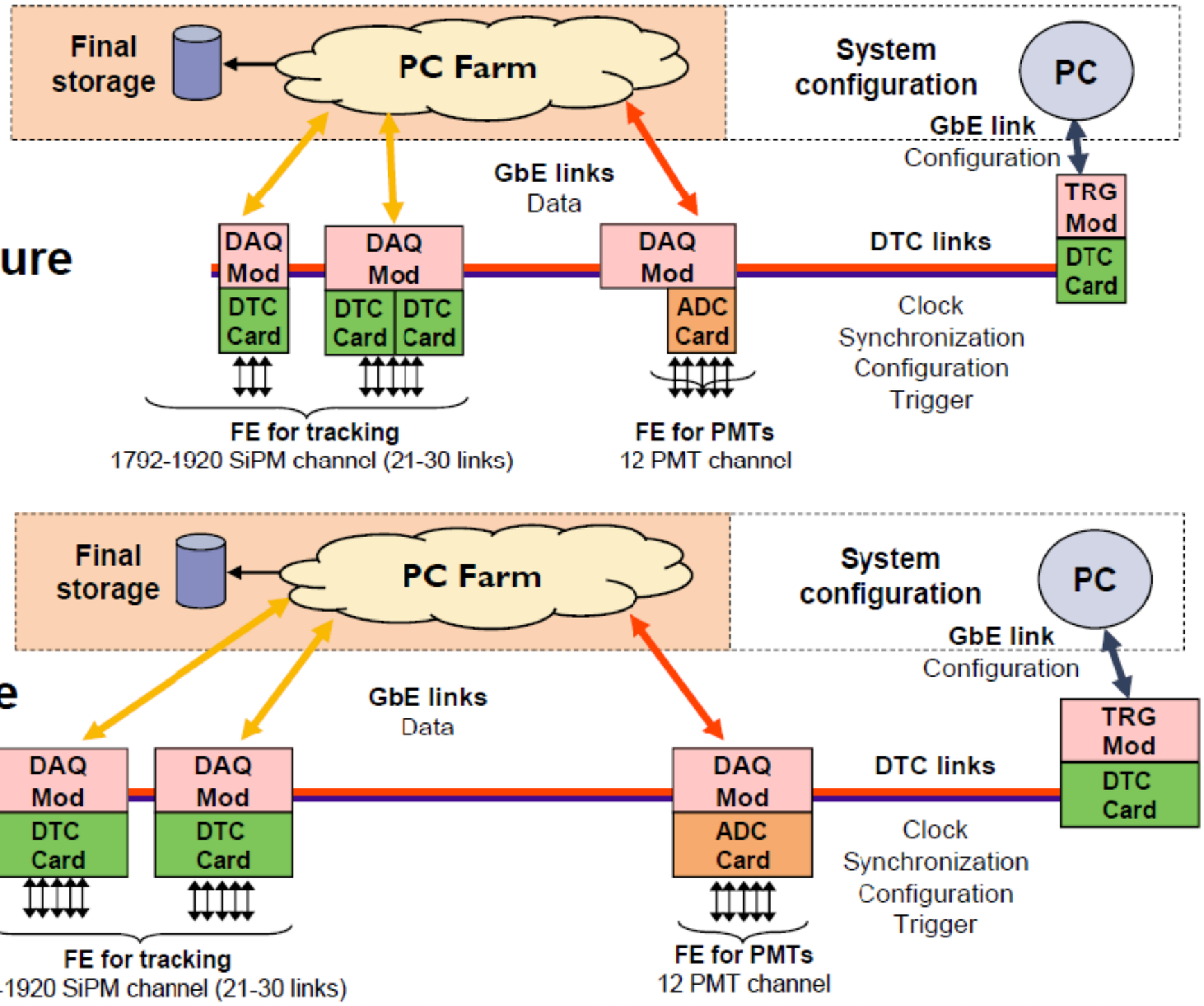
9 GbE links to DAQ PCs

4 LDCs
3 GDCs

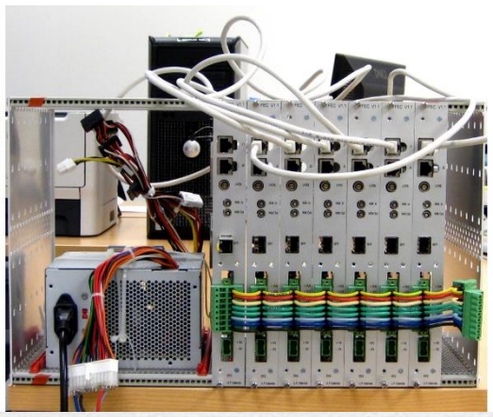
NEW DAQ
ATCA Architecture

3 LDCs
3 GDCs

7 GbE links to DAQ PCs

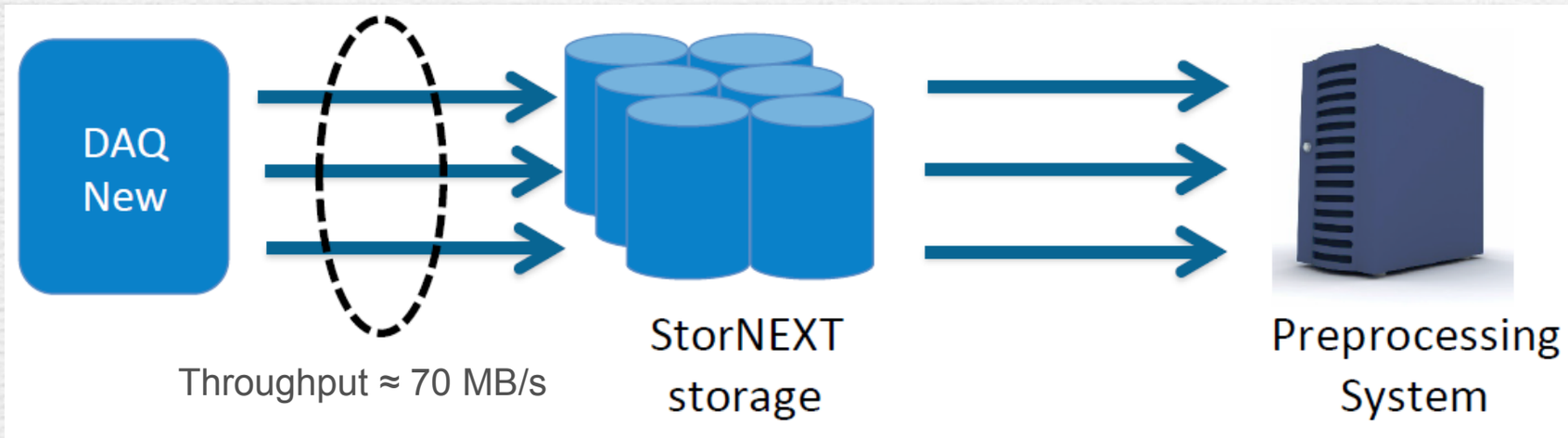


NEW DAQ
v6 Architecture



Event storage for NEW

StorNEXT-New: Requirements



Requirements

- Save (write) data at 70 MB/s from DAQ
- Read data from several processes (Pre-processing System):
  - Pre-processing
  - Monitoring
  - Compression

- Upgrade the File System: Lustre File System
  - Best Performance

DAQ_TEST

LDC status display

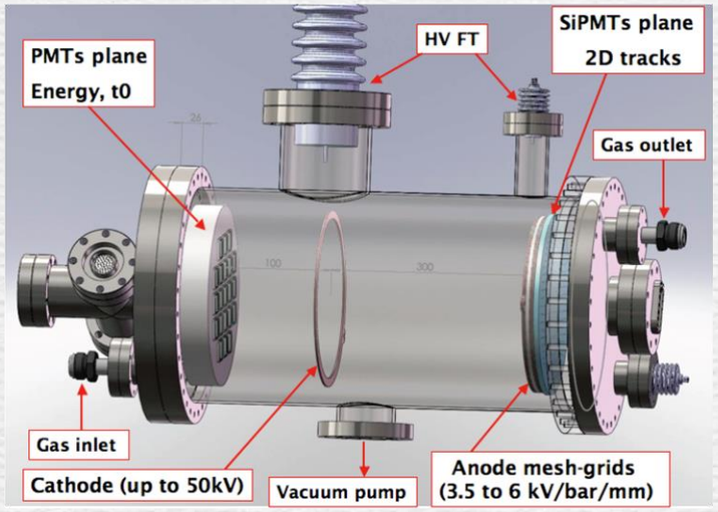
LDC name host	ldc2-LDC ldc2	ldc1-LDC ldc1
Current Trigger rate	45.600	45.600
Average Trigger rate	39.561	39.471
Number of sub-events	7477	7381
Sub-event rate	45	45
Sub-events recorded	7479	7383
Sub-event recorded rate	45	45
Bytes injected	8721890736	7616808332
Byte injected rate	53.192 MB/s	47.056 MB/s
Bytes recorded	8721890736	7616808332
Byte recorded rate	53.192 MB/s	47.056 MB/s
Nb. evts w/o HLT decision	0	0
mem allocation failed	0	0
average time bmAllocate		

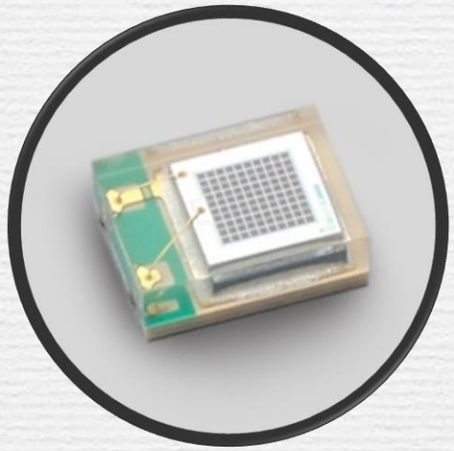
GDC status display

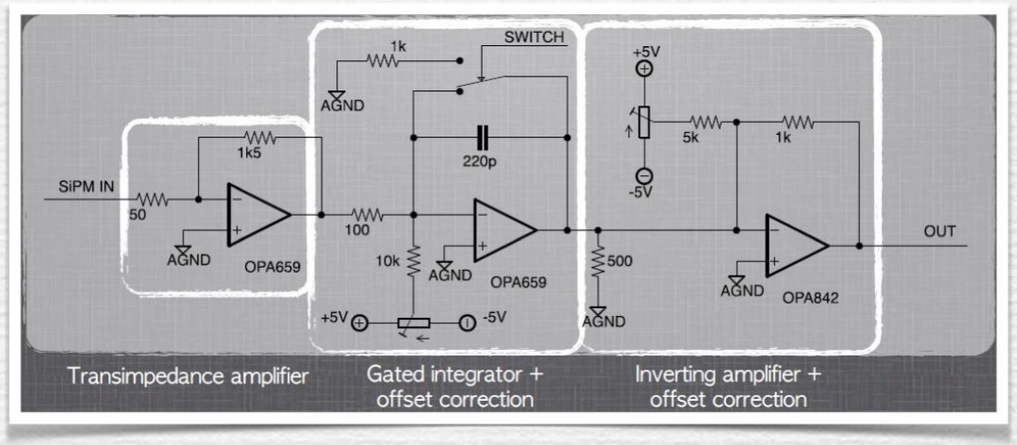
GDC name host	daqtest01-GDC gdc1	daqtest02-GDC gdc2
Number of sub-events	7388	7308
Sub-event rate	45	45
Events recorded	3696	3653
Event recorded rate	22	22
Bytes recorded	8116921648	8032210968
Byte recorded rate	50.126 MB/s	49.892 MB/s
File count	17	17
Nb. incomplete events	0	0

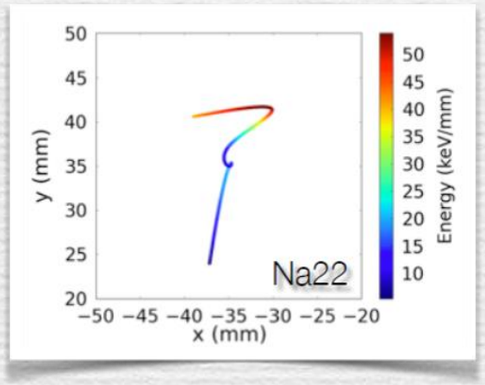
- Tests:
  - Maximum Tr. Rate = 45 Hz
  - Save data at 100 MB/s
  - Read data from 2 processes:
    - Preprocessing
    - Monitoring

Summary

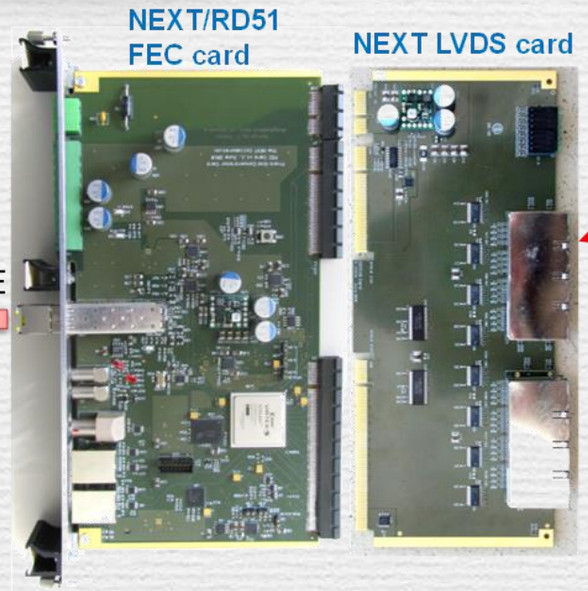

PMTs plane
Energy, t0
HV FT
SiPMTs plane
2D tracks
Gas outlet
Gas inlet
Cathode (up to 50kV)
Vacuum pump
Anode mesh-grids
(3.5 to 6 kV/bar/mm)



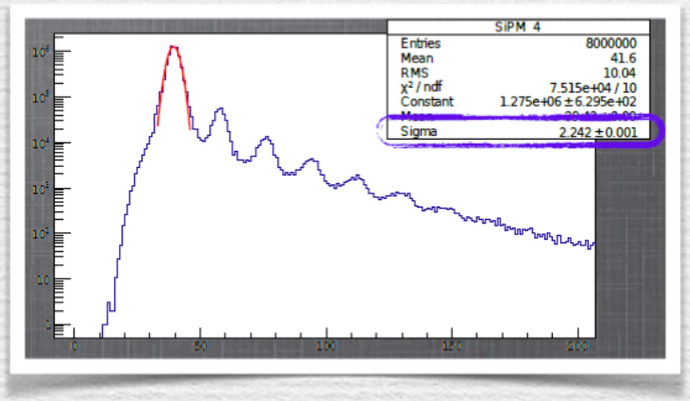

SiPM IN
50
1k5
AGND
OPA659
100
1k
AGND
SWITCH
220p
10k
AGND
OPA659
+5V
-5V
500
AGND
+5V
5k
1k
-5V
AGND
OPA842
OUT
Transimpedance amplifier
Gated integrator +
offset correction
Inverting amplifier +
offset correction

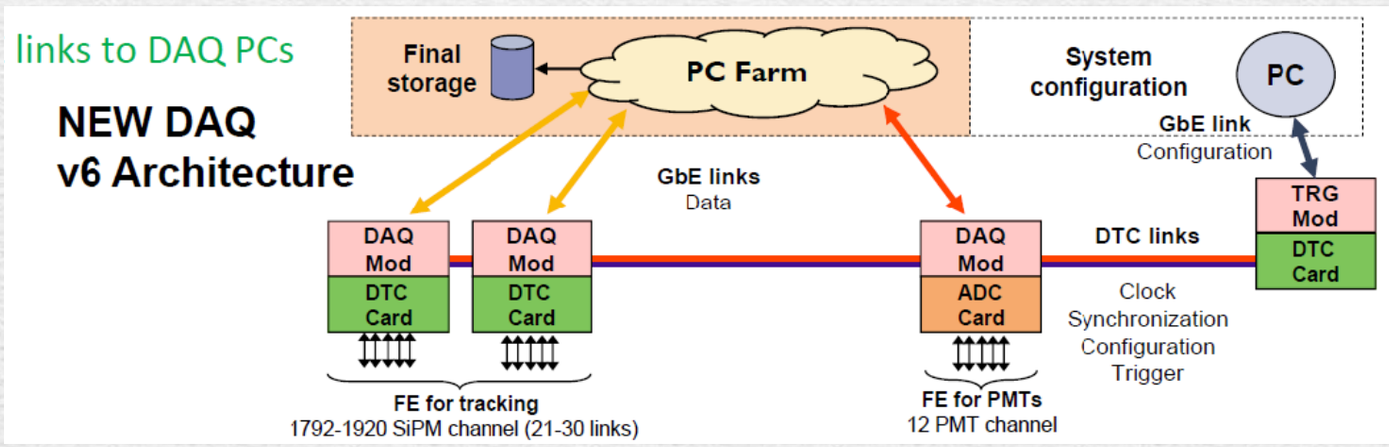

y (mm)
x (mm)
Energy (keV/mm)
Na22


GbE


NEXT/RD51
FEC card
NEXT LVDS card
DTC
Clock +
cmd/trigger
+ 2x data


16x (Amplifier + Integrator +
digitizer + data formatter)


SiPM 4
Entries 8000000
Mean 41.6
RMS 10.04
χ² / ndf 7.515e+04 / 10
Constant 1.275e+06 ± 6.295e+02
Sigma 2.242 ± 0.001


links to DAQ PCs
NEW DAQ
v6 Architecture
Final
storage
PC Farm
System
configuration
PC
GbE link
Configuration
GbE links
Data
DAQ
Mod
DTC
Card
DAQ
Mod
DTC
Card
DAQ
Mod
ADC
Card
DTC links
TRG
Mod
DTC
Card
Clock
Synchronization
Configuration
Trigger
FE for tracking
1792-1920 SiPM channel (21-30 links)
FE for PMTs
12 PMT channel

If you want to know more…

On SiPMs

- D. Renker and E. Lorenz, “Advances in solid state photon detectors,” 2009 JINST 4 P04004, DOI : 10.1088/1748-0221/4/04/P04004
- F. Corsi et al., “Current-Mode Front-End Electronics for Silicon Photo-Multiplier Detectors,” DOI 10.1109/IWASI.2007.4420025

On NEXT: http://next.ific.uv.es/next/

On the NEXT-DEMO front-end for SIPMs

- V. Herrero et al, “Readout electronics for the SiPM tracking plane in the NEXT-1 prototype,” 2012 NIM A 695, DOI: 10.1016/j.nima.2011.12.057

On the NEXT-DEMO DAQ and trigger systems

- R. Esteve et al, “The trigger system in the NEXT-DEMO detector,” 2012 NIM A 695, 2012 JINST 7 C12001, DOI:10.1088/1748-0221/7/12/C12001

On the RD51 FEC card (Virtex-5 version)

- J. Toledo et al., “The Front-End Concentrator card for the RD51 Scalable Readout System,” JINST 6 C11028 doi:10.1088/1748-0221/6/11/C11028

Thanks for your attention

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