
# Silicon Microstrip R&D at SCIPP and the University of California at Santa Cruz

**Future Linear Colliders Spanish Network**

**Universidad de Sevilla**

**10-12 February 2014**

**Bruce Schumm**

**UC Santa Cruz / SCIPP**

# The SCIPP/UCSC SiLC/SiD GROUP (Harwdare R&D Participants)

| Faculty/Senior | Students | More Students |
|---|---|---|
| Vitaliy Fadeyev | Wyatt Crockett | Vivian Tang |
| Bruce Schumm | Conor Timlin | Reyer Band |
| | Spencer Ramirez | George Courcoubetis |
| | Christopher Milke | Bryce Burgess |
| | Olivia Johnson | |

**Lead Engineer:** **Ned Spencer**

**Technical Staff:** **Max Wilder, Forest Martinez-McKinney**

All participants are mostly working on other things (ATLAS, biophysics, classes…)

Students are undergraduates from physics and engineering

# FOCUS AND MILESTONES OF SCIPP GROUP

## Activity 1: Development of long ladder and forward strip applications (THIS TALK!)

- Front-end electronics (LSTFE ASIC)
- Exploration of sensor requirements and length limitations for long ladders (NIM-A 729 p127 (2013))

## Activity 2: Development of far-forward calorimetry (NOT THIS TALK!)

- Radiation damage studies
- Detector optimization
- Physics studies

# The LSTFE ASIC

- Optimized for long (~1m) ladders but also appropriate for high-occupancy short strip application
- Uses time-over threshold analog response ➔ limited dead time without loss of resolution
- Simple re-optimization would further improve data throughput rate for high-occumpancy use
- 128-channel prototype (LSTFE-2) under testing in lab (but a bit fallow)

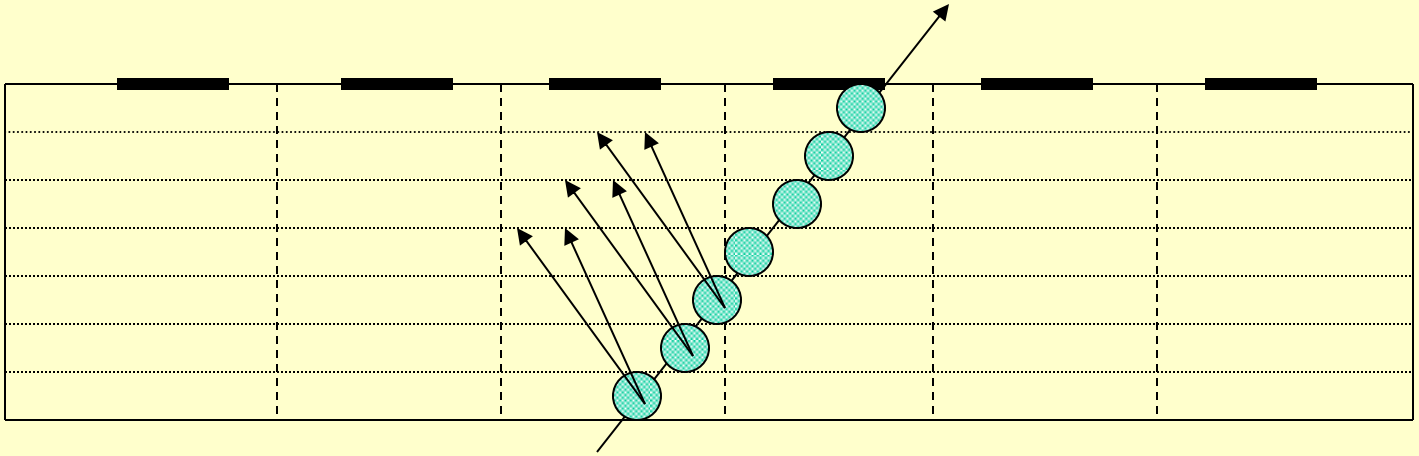
Now for the details…

# Pulse Development Simulation

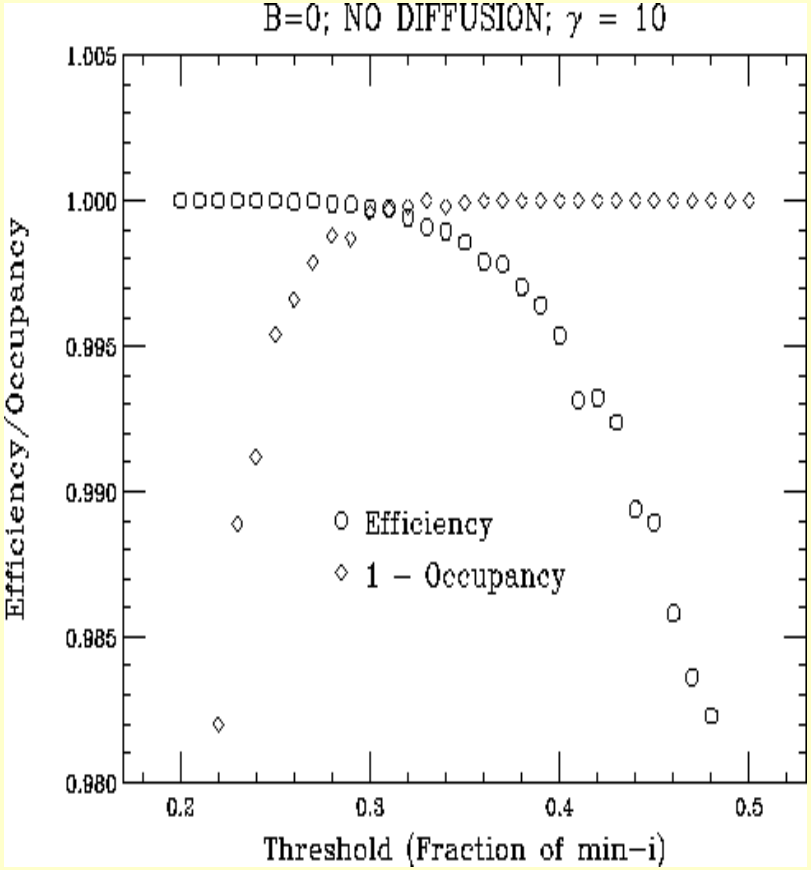
Christian Flacco & Michael Young (Grads); John Mikelich (Undergrad)

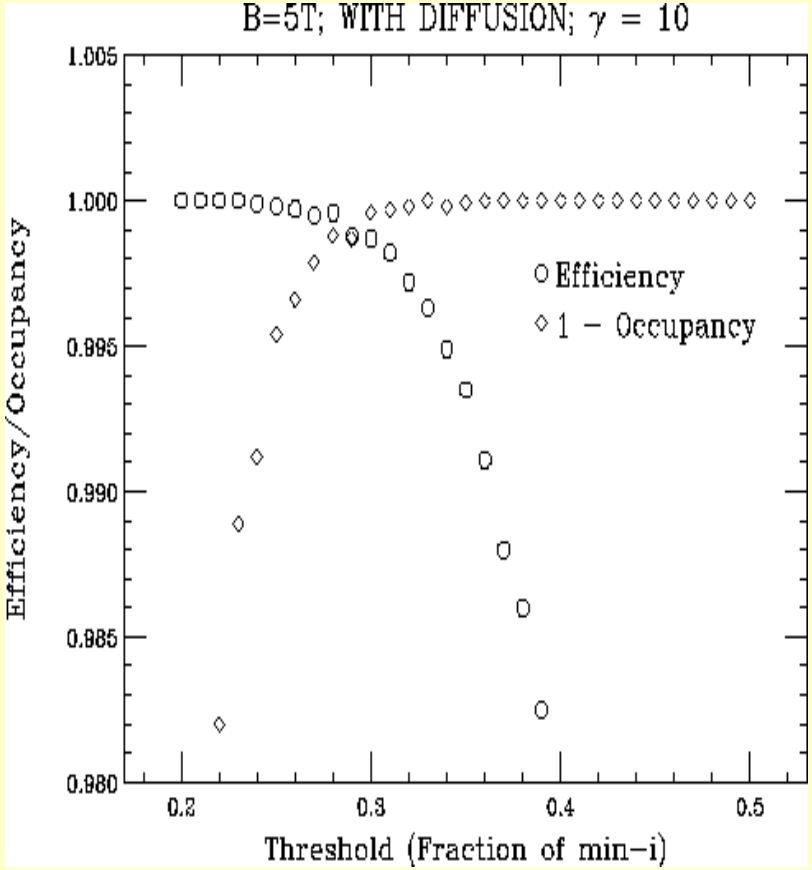
Long Shaping-Time Limit: strip sees signal if and only if hole is collected onto strip (no electrostatic coupling to neighboring strips)

Include: Landau deposition (SSSimSide; Gerry Lynch LBNL), variable geometry, Lorentz angle, carrier diffusion, electronic noise and digitization effects



# Simulation Result: S/N for 167 cm Ladder (capacitive noise only)

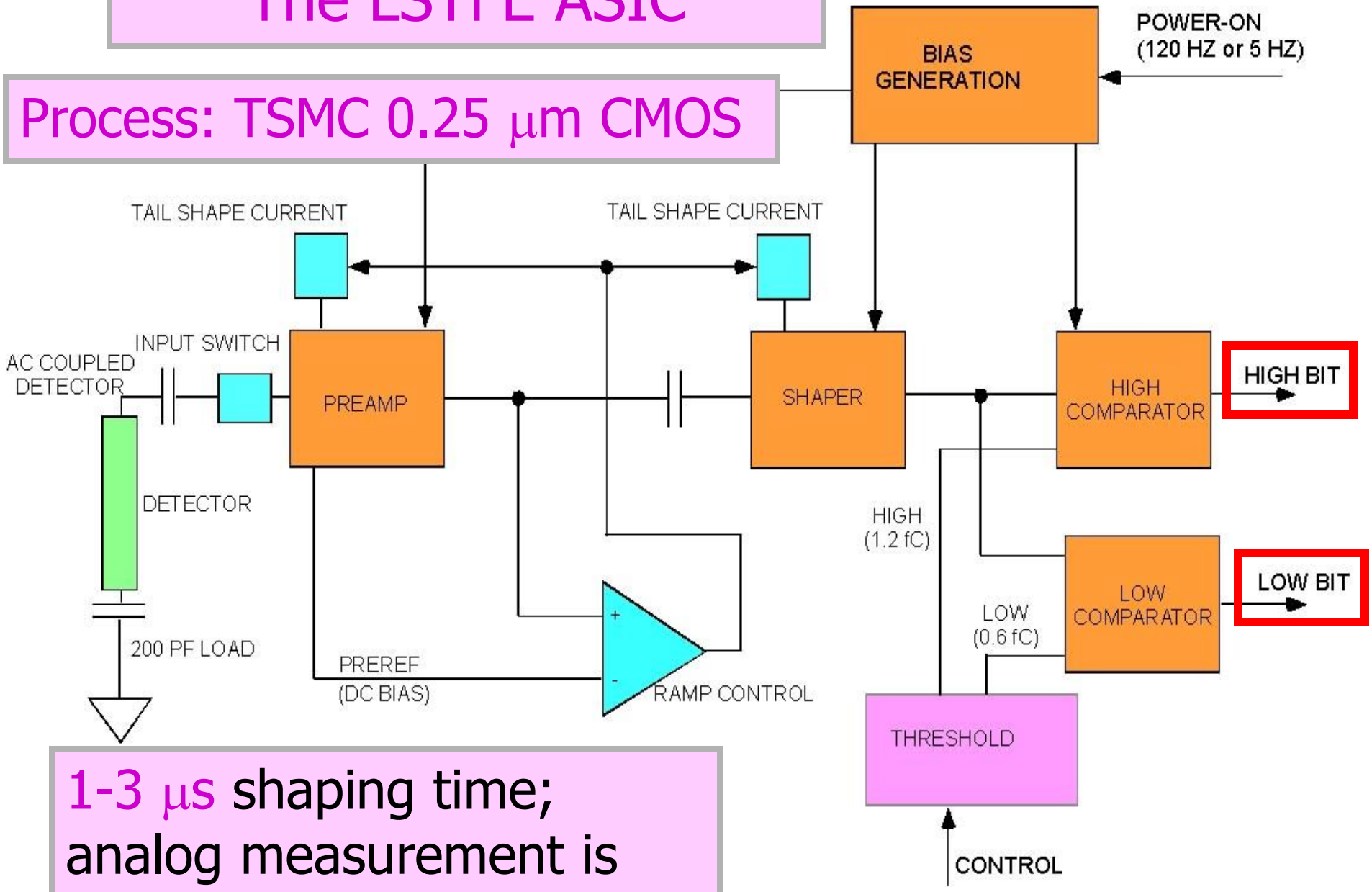



Simulation suggests that long-ladder operation is feasible

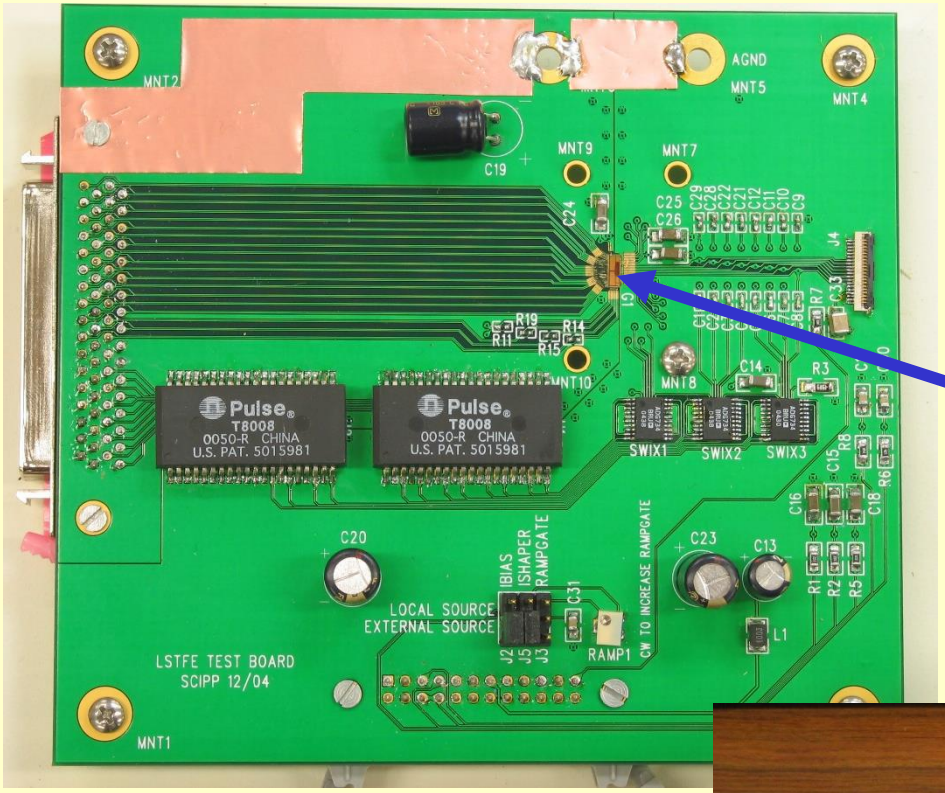
# The LSTFE ASIC

## Process: TSMC 0.25 μm CMOS

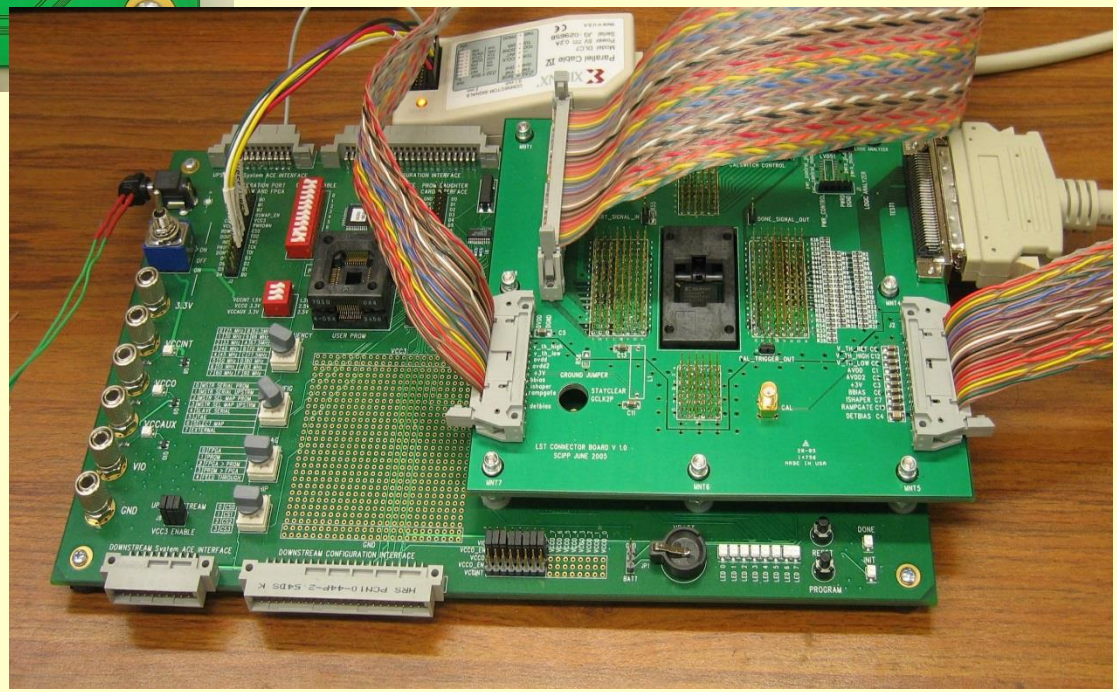



1-3 μs shaping time; analog measurement is Time-Over-Threshold

# INITIAL RESULTS




LSTFE chip mounted on readout board



FPGA-based control and data-acquisition system

# Comparator S Curves

Vary threshold for given input charge

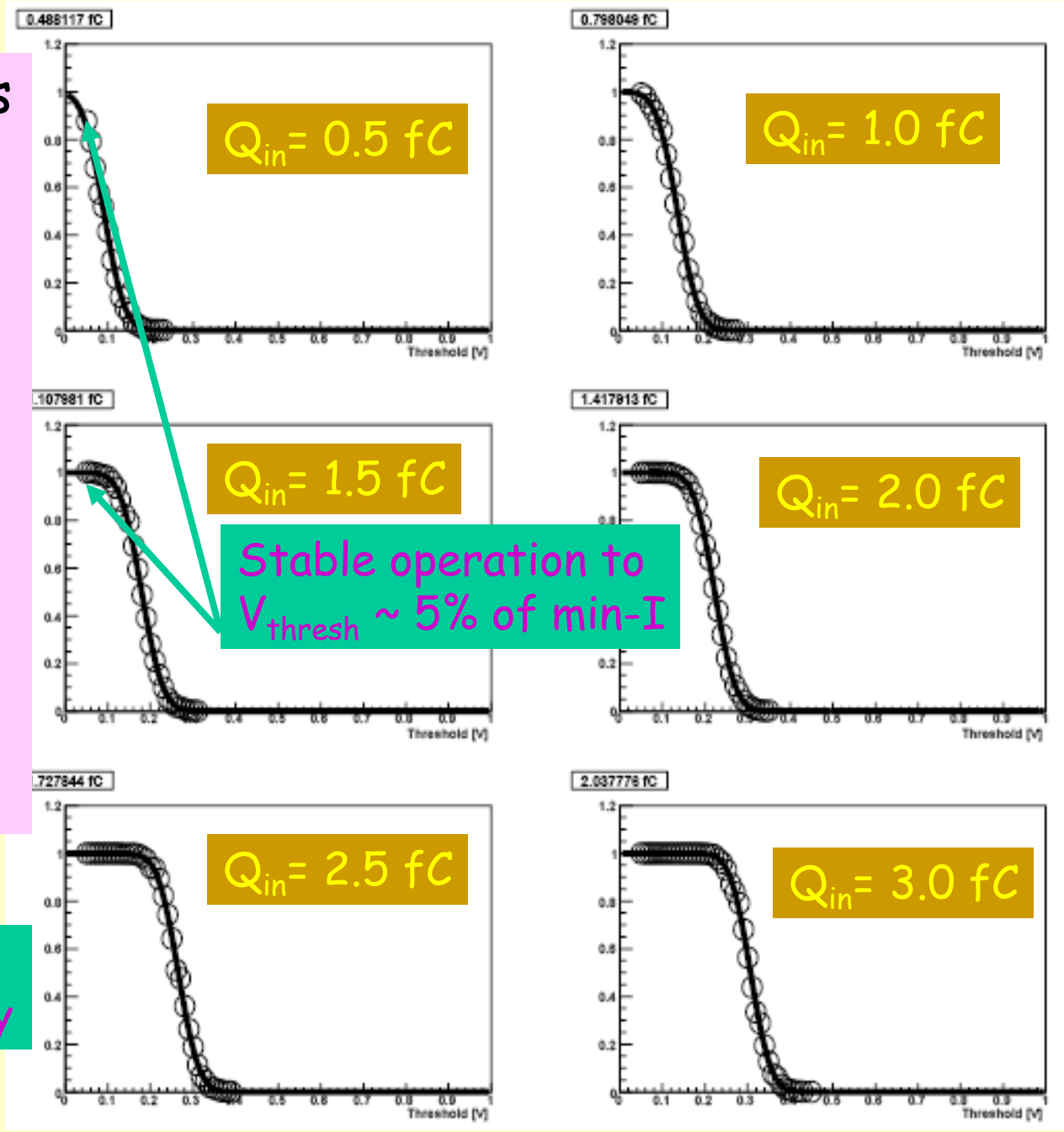
Read out system with FPG-based DAQ

Get

```
1-erf(threshold)
```

with 50% point giving response, and width giving noise

Hi/Lo comparators function independently



# EQUIVALENT CAPACITANCE STUDY

## Noise vs. Capacitance (at $\tau_{shape}$ = 1.2 $\mu$s)

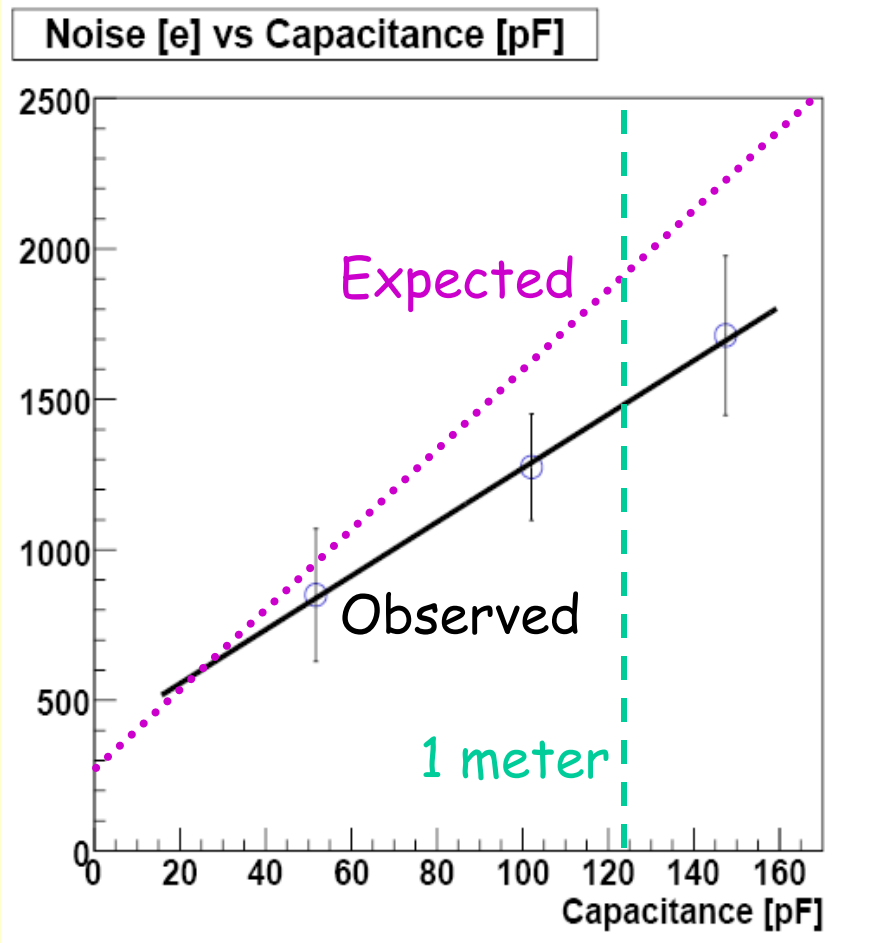
Measured dependence is roughly (noise in equivalent electrons)

$$\sigma_{noise} = 375 + 8.9*C$$

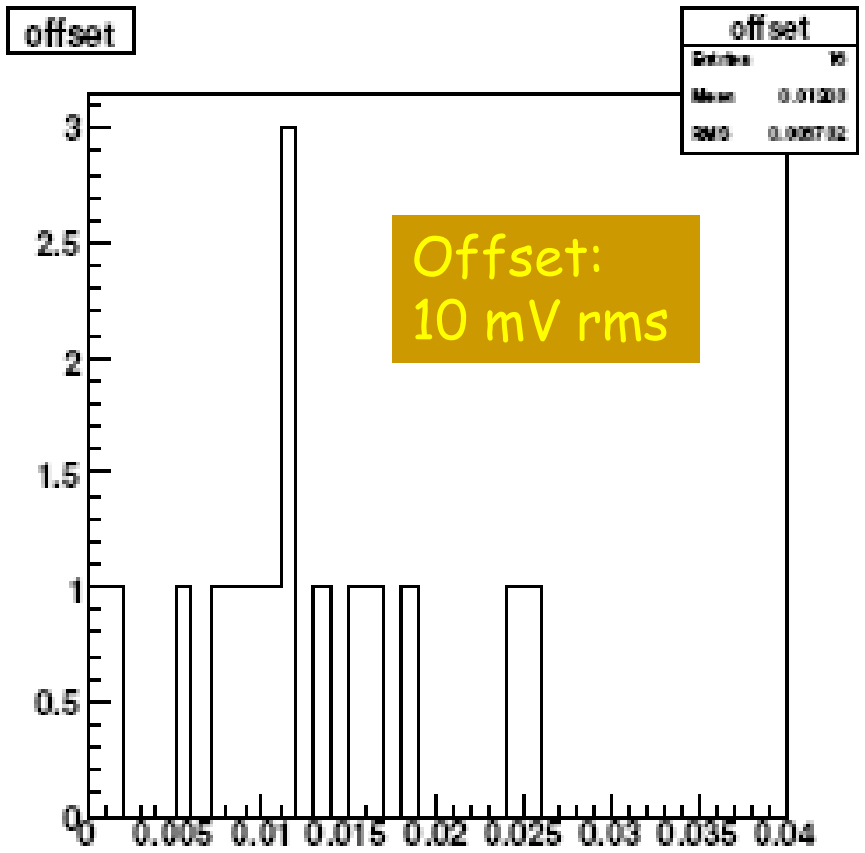
with *C* in pF.

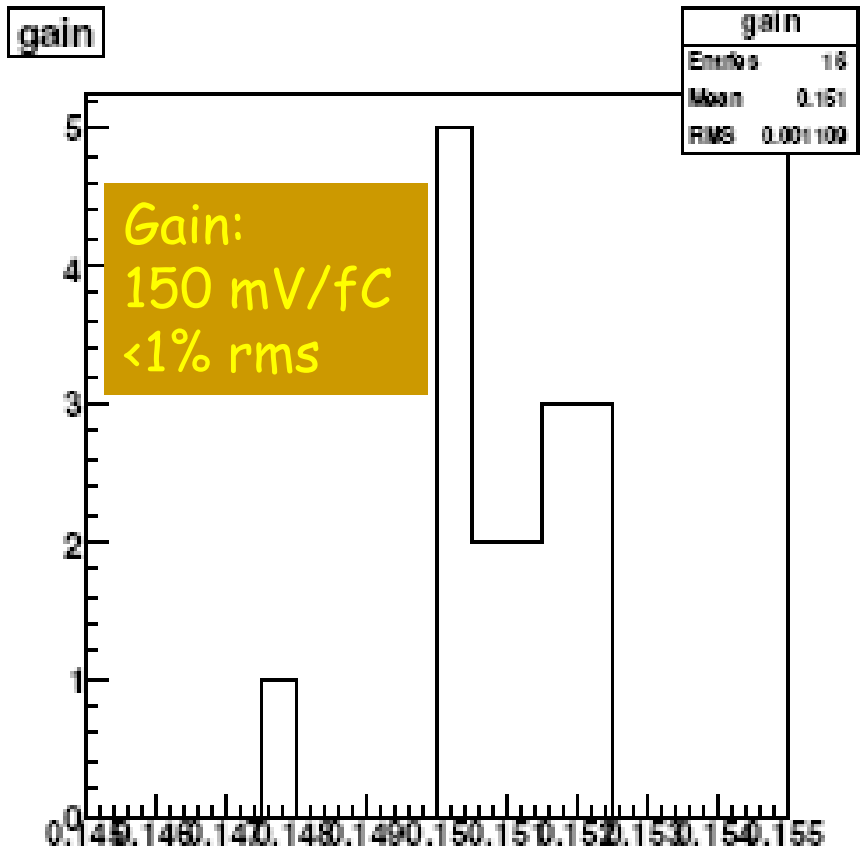
Experience at 0.5 $\mu$m had suggested that model noise parameters needed to be boosted by 20% or so; these results suggest 0.25 $\mu$m model parameters are accurate

➔ Noise performance somewhat better than anticipated.



# Channel-to-Channel Matching



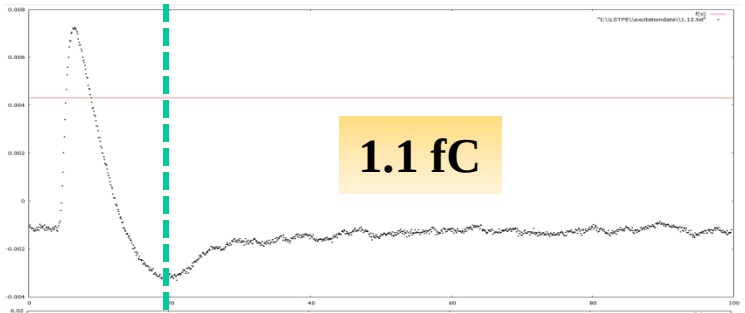



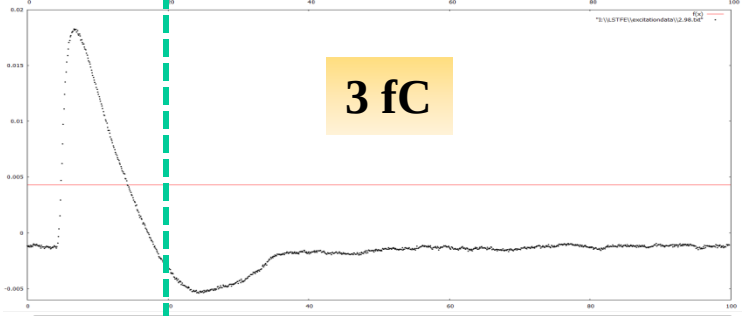

Occupancy threshold of 1.2 fC (1875 $e^-$) ➔ 180 mV

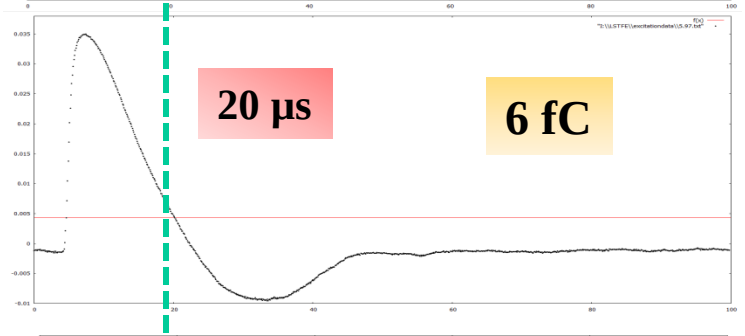
± 2 mV (20 $e^-$) from gain variation

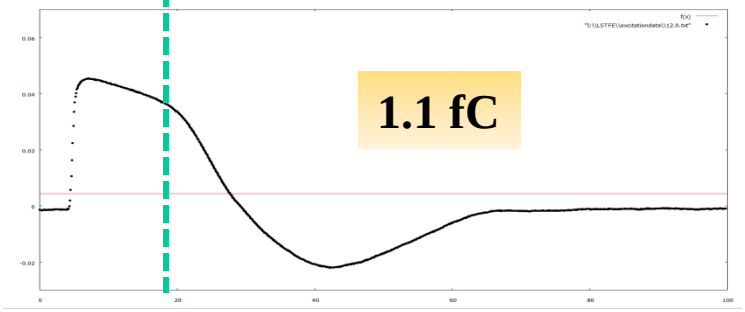
± 10 mV (100 $e^-$) from offset variation

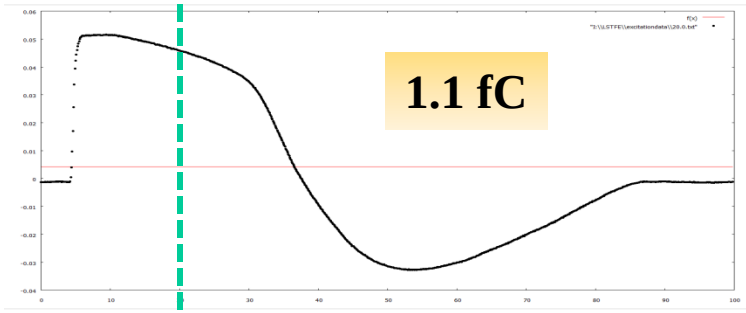
# Evolution of LSTFE response against a fixed (0.7 fC) threshold

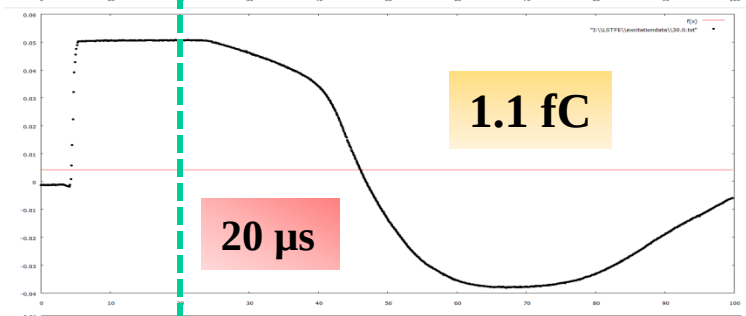


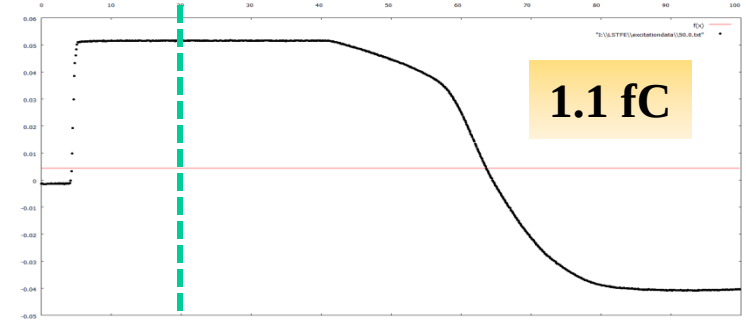



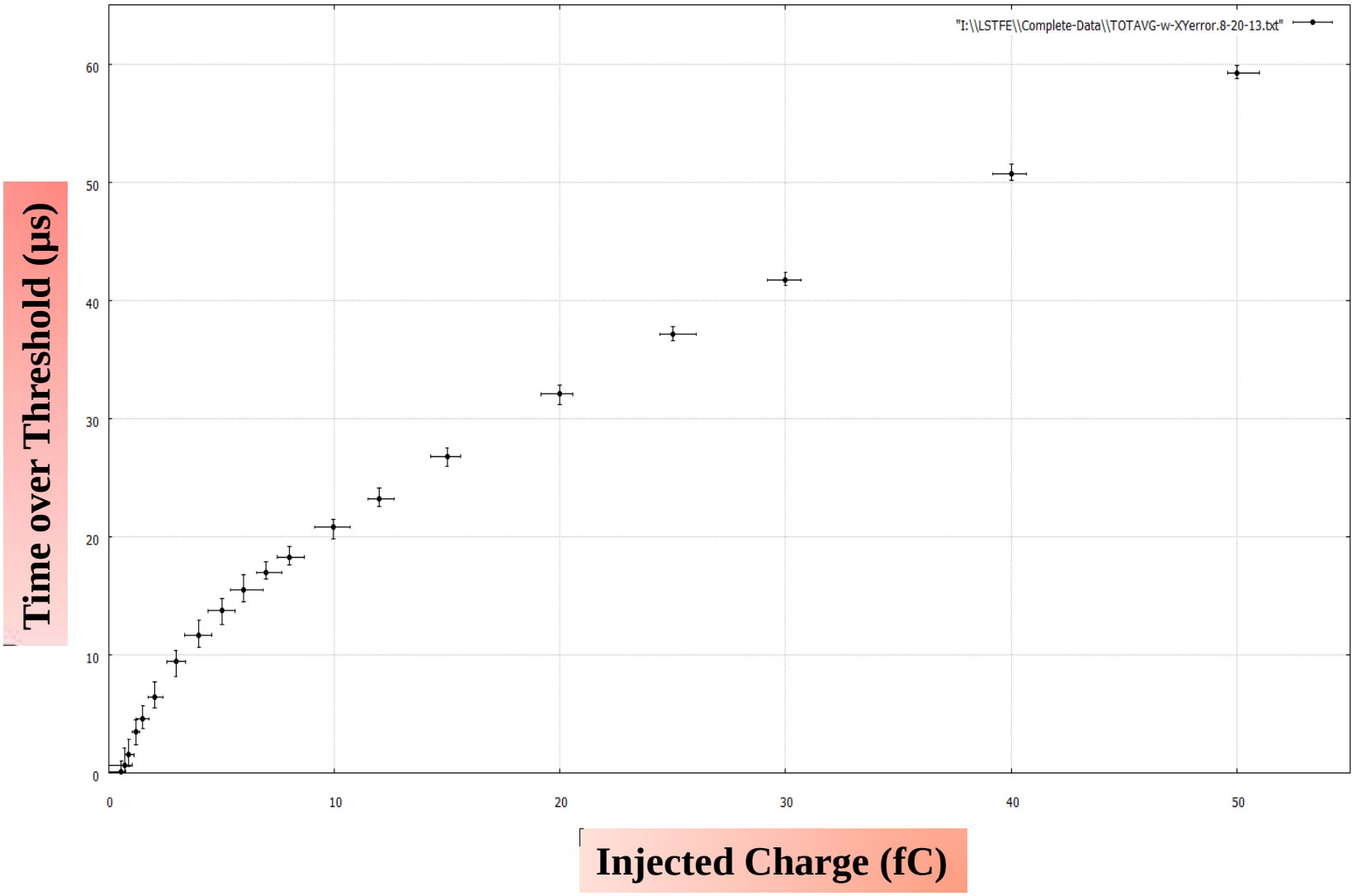



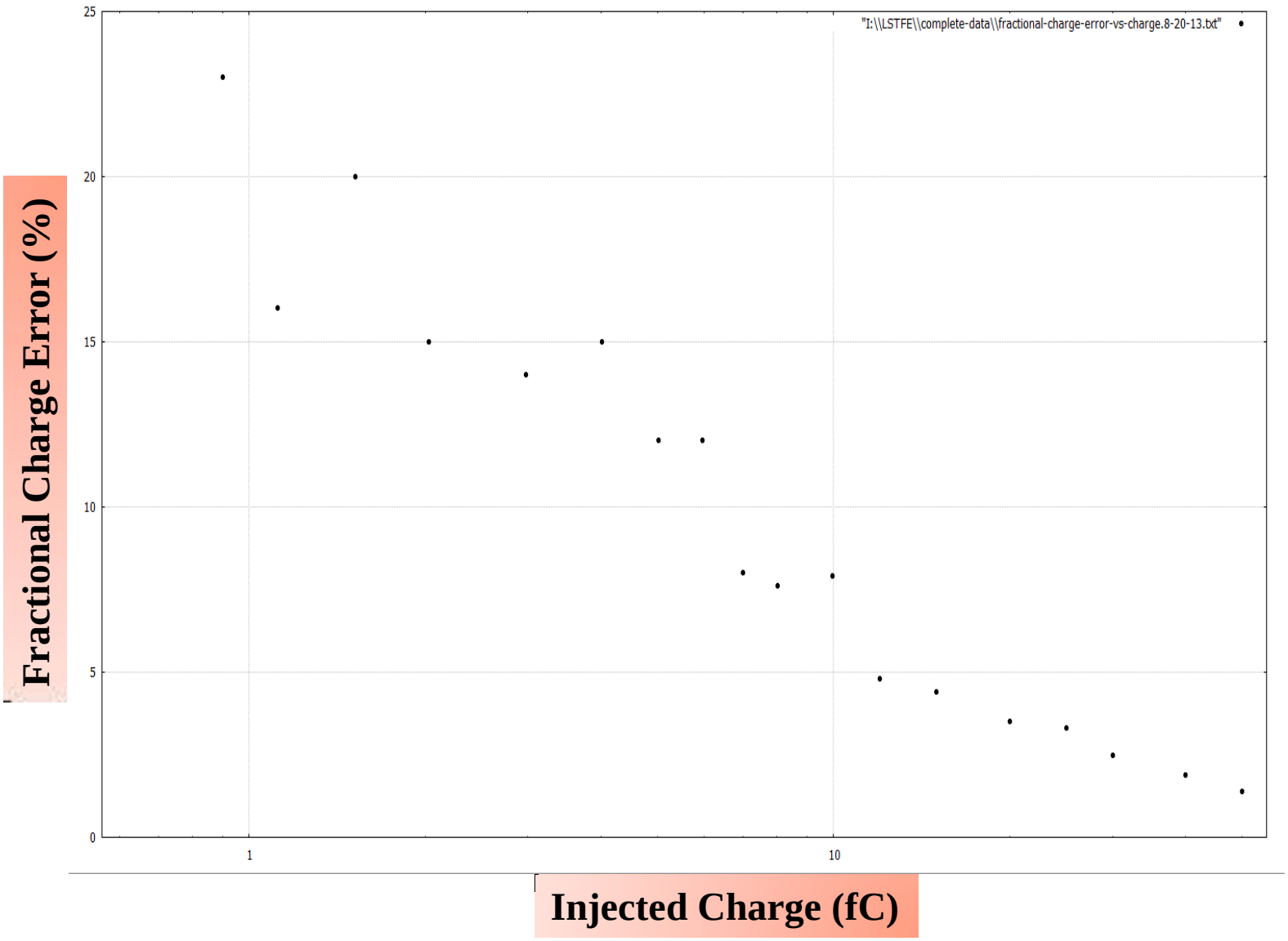




Return to baseline for typical (~3fc) pulse: 40 µs (directly related to shaping time!)

# Time Over Threshold versus Injected Charge, and RMS spread



# Resulting Fractional Charge Error



# Electronics Simulation: Resolution

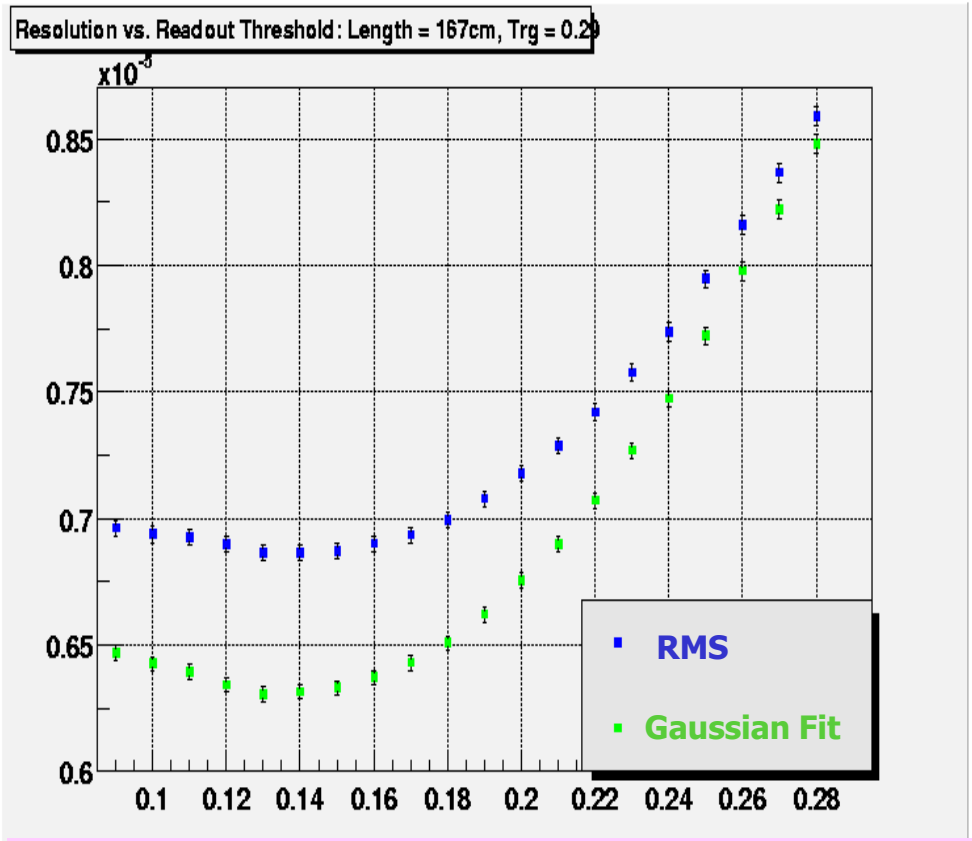
Detector Noise:

Capacitive contribution; from SPICE simulation normalized to bench tests with GLAST electronics

Analog Measurement:

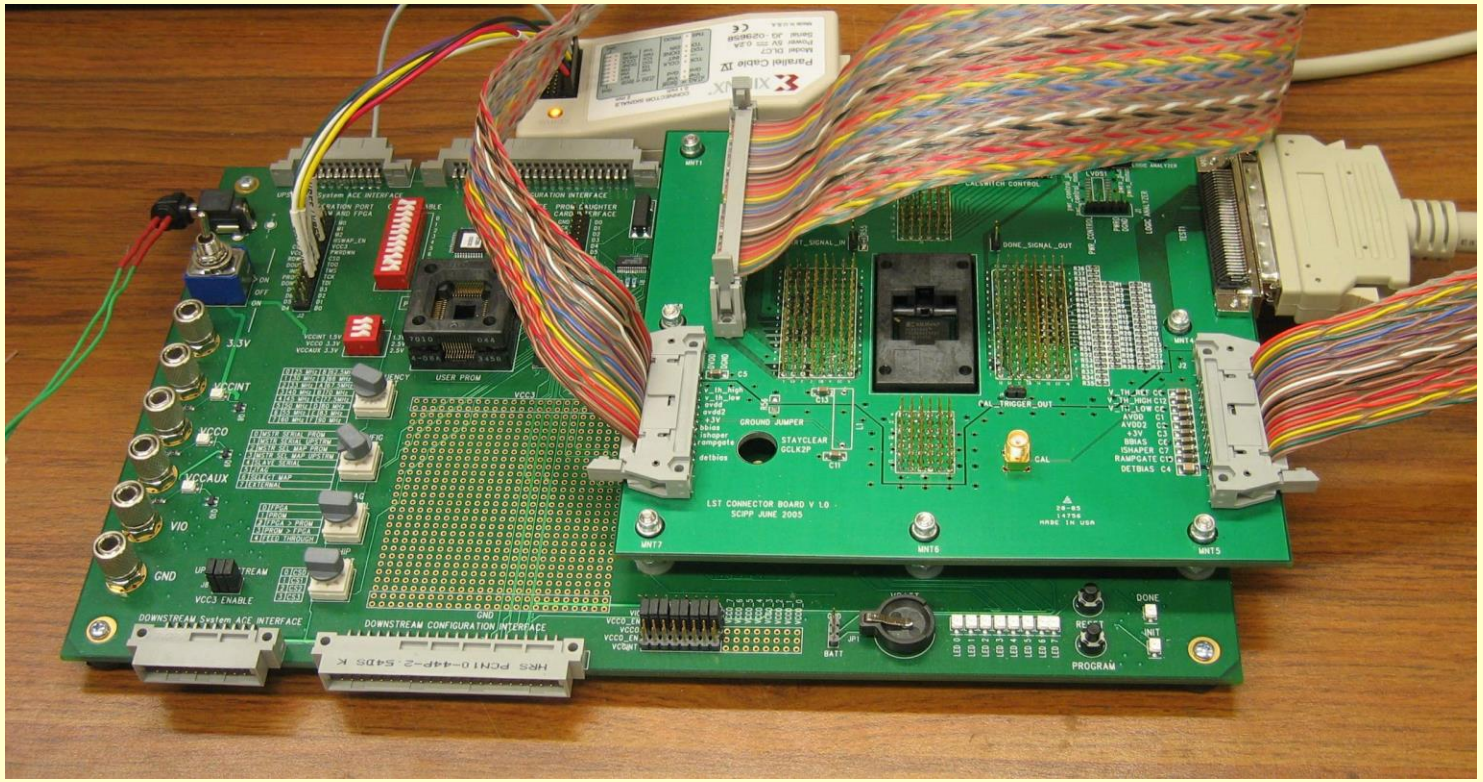
Provided by time-over-threshold; lookup table provides conversions back into analog pulse height (as for actual data)

Detector Resolution (units of 10μm)



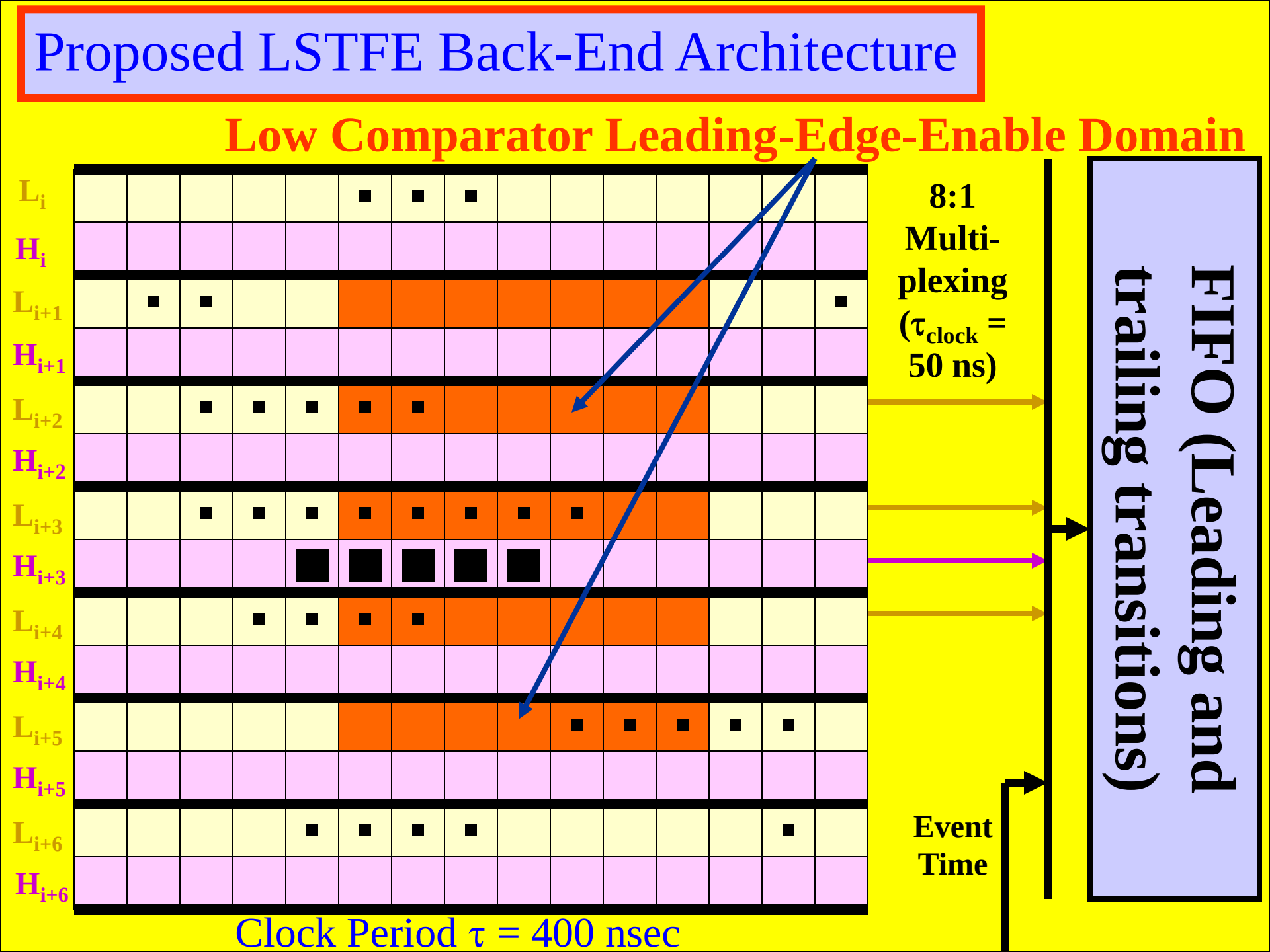

Lower (read) threshold in fraction of min-i
(High threshold is at 0.29 times min-i)

# DIGITAL ARCHITECTURE: FPGA DEVELOPMENT




Digital logic under development on FPGA (Wang, Kroseberg), will be included on front-end ASIC after performance verified on test bench and in test beam.

# Proposed LSTFE Back-End Architecture



# Note on LSTFE Digital Architecture

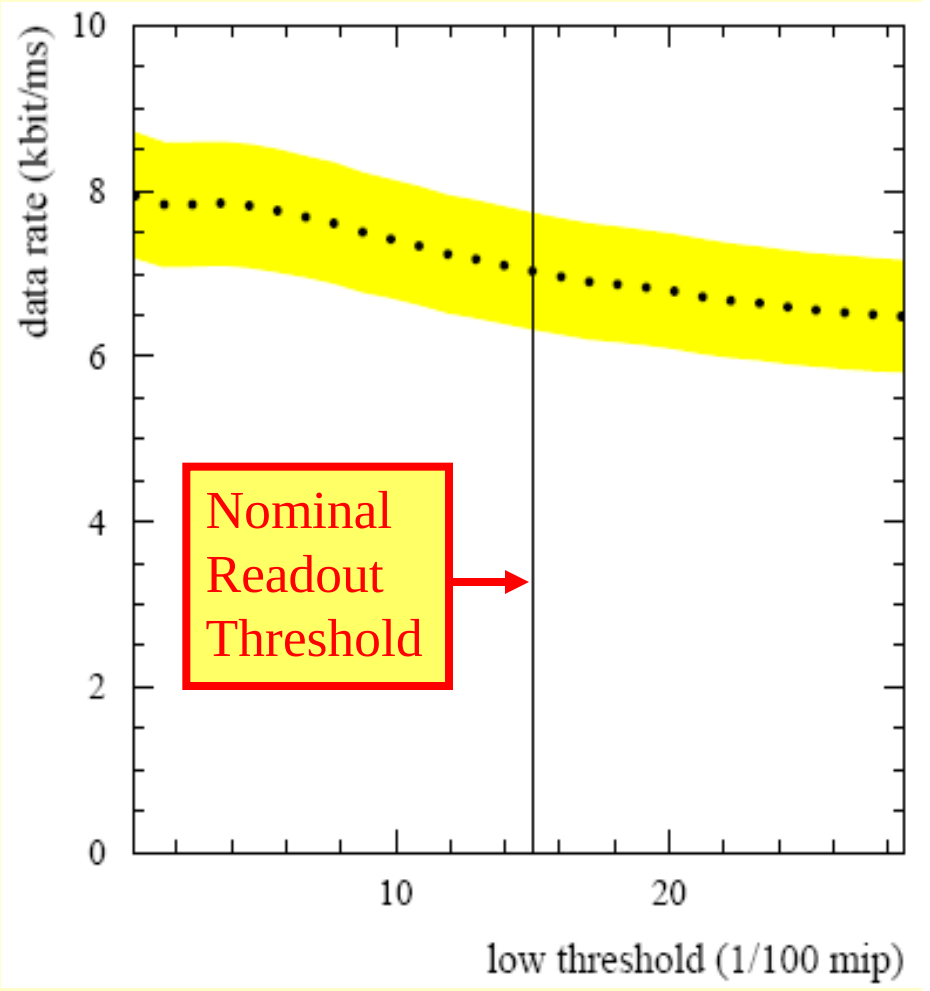
Use of time-over-threshold (vs. analog-to-digital conversion) permits real-time storage of pulse-height information.

➔ No concern about buffering

➔ LSTFE system can operate in arbitrarily high-rate environment; is ideal for (short ladder) forward tracking systems as well as long-ladder central tracking applications.

# DIGITAL ARCHITECTURE SIMULATION

ModelSim package permits realistic simulation of FPGA code (signal propagation not yet simulated)




Simulate detector background (innermost SiD layer) and noise rates for 500 GeV running, as a function of read-out threshold.

Per 128 channel chip ~ 7 kbit per spill ➔ 35 kbit/second

For entire SiD tracker ~ 0.5-5 GHz data rate, depending on ladder length (x100 data rate suppression)


# Limitations on Microstrip Ladder Length

**International Workshop on Future Linear Colliders**
**University of Tokyo, 11-15 November 2013**

**Bruce Schumm**
**Santa Cruz Institute for Particle Physics**

Study involved:

- Measurements of readout noise vs. strip load
- SPICE-level simulation of readout noise, including network effects
- Pulse-development simulation to determine operating point and length limitations

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journal homepage: www.elsevier.com/locate/nima


# Microstrip electrode readout noise for load-dominated long shaping-time systems

Kelsey Collier, Taylor Cunnington, Sean Crosby, Vitaliy Fadeyev, Forest Martinez-McKinney, Khilesh Mistry, Bruce A. Schumm*, Edwin Spencer, Aaron Taylor, Max Wilder

*Santa Cruz Institute for Particle Physics and the University of California, Santa Cruz, CA 95064, United States*

# Standard Form for Readout Noise (Spieler)

Series Resistance

Parallel Resistance

$$Q^2 = F_i \tau \left( 2eI_d + \frac{4kT}{R_B} + {i_{na}}^2 \right) + \frac{F_v C^2}{\tau} \left( 4kTR_s + {e_{na}}^2 \right) + 4F_v A_f C^2$$

Amplifier Noise (parallel)

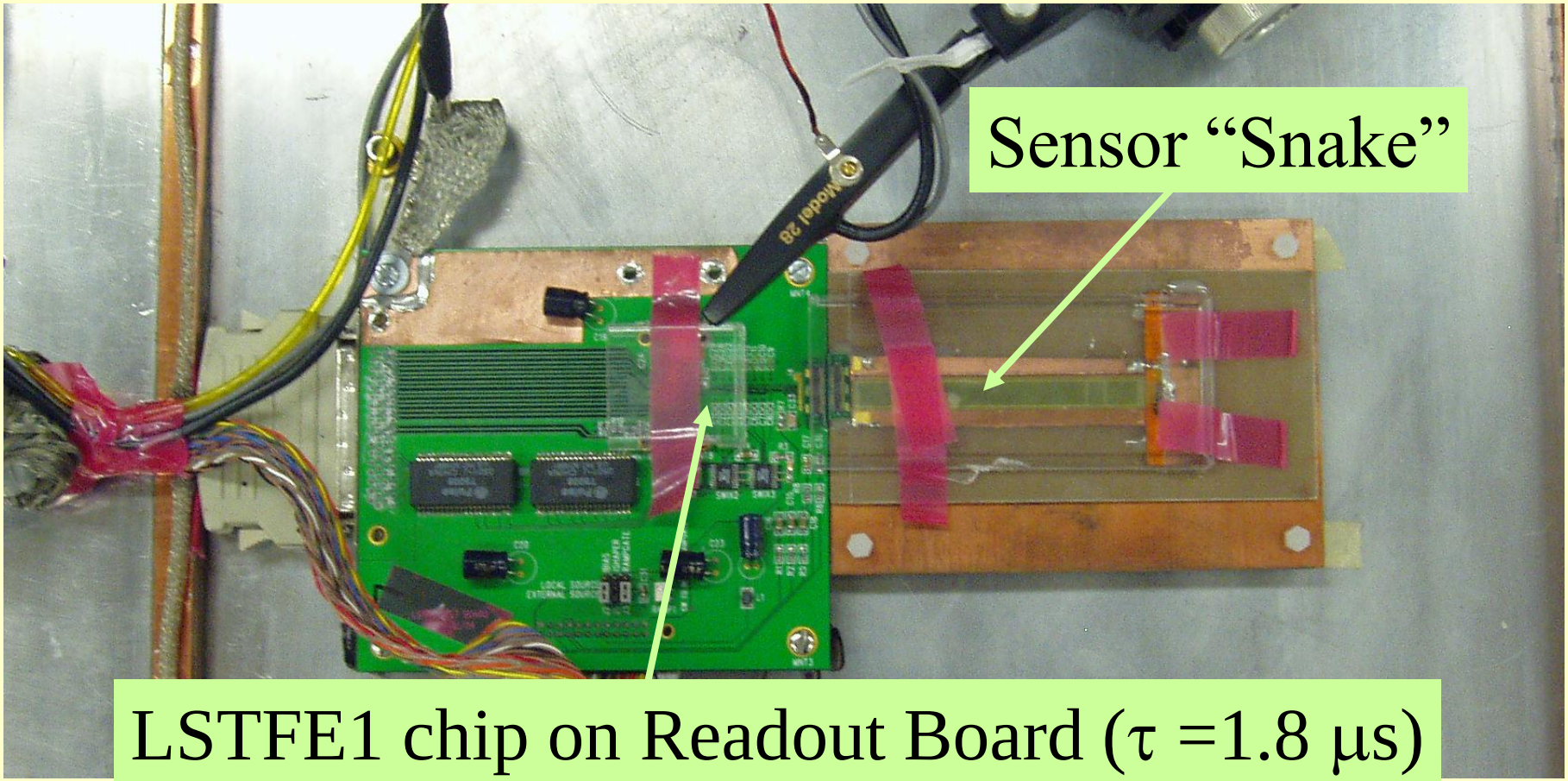
Amplifier Noise (series)

Dominant term for long ladders (grows as $L^{3/2}$)

$F_i$ , $F_v$ are signal shape parameters that can be determined from average scope traces.

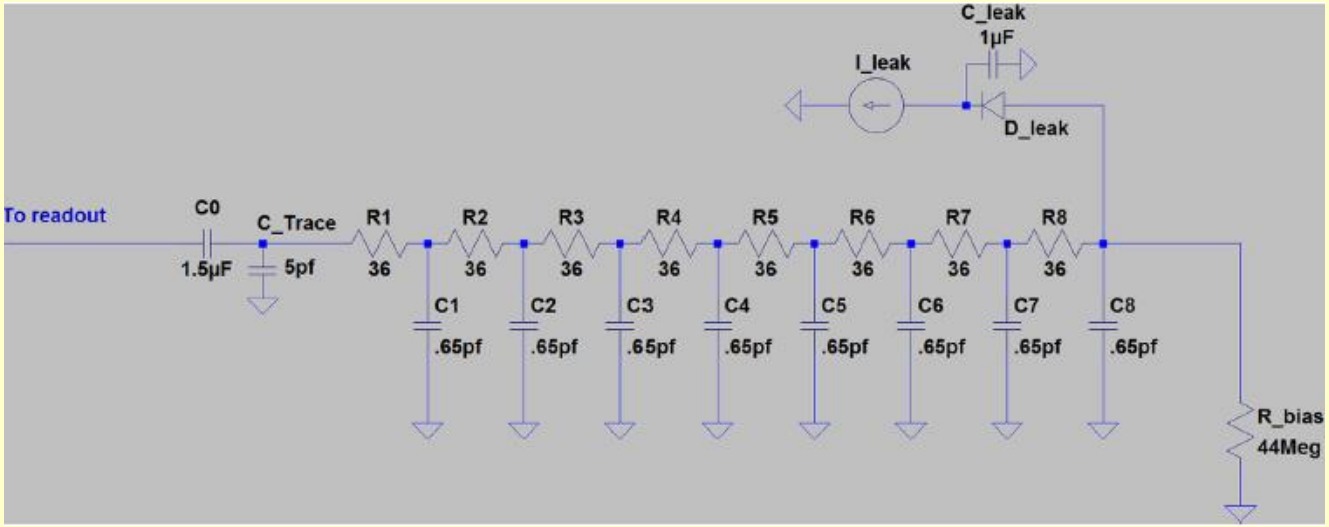
➔ Expression assumes single, lumped R, C load element; in fact, microstrip electrode is a **distributed network**

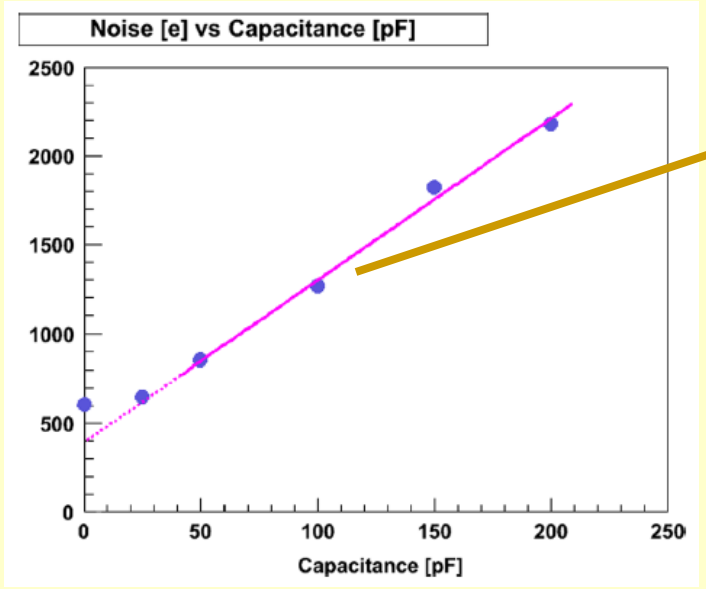
# Sensor “Snake”: Read out up to 13 daisy-chained 5cm sensors (with LSTFE-1 ASIC)

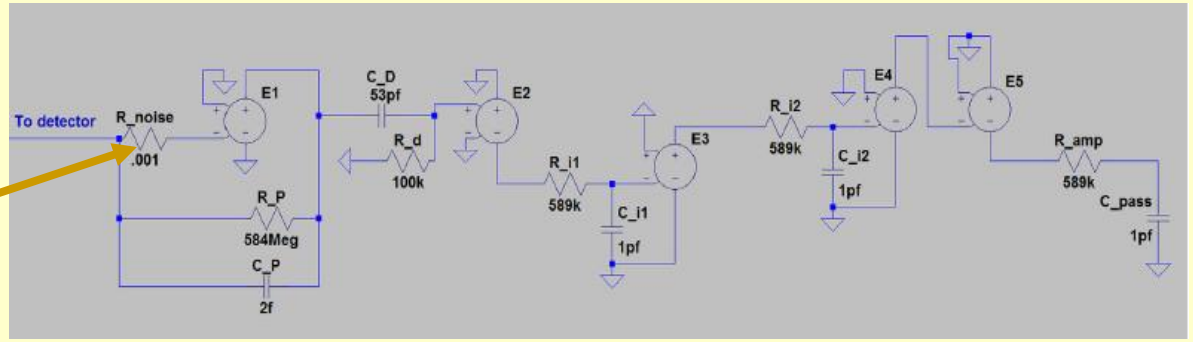



**Can read out from end, or from middle of chain (“center-tap”)**

Simulation: Each “rung” (strip) divided into 8 discrete pieces; equivalent to continuous network.

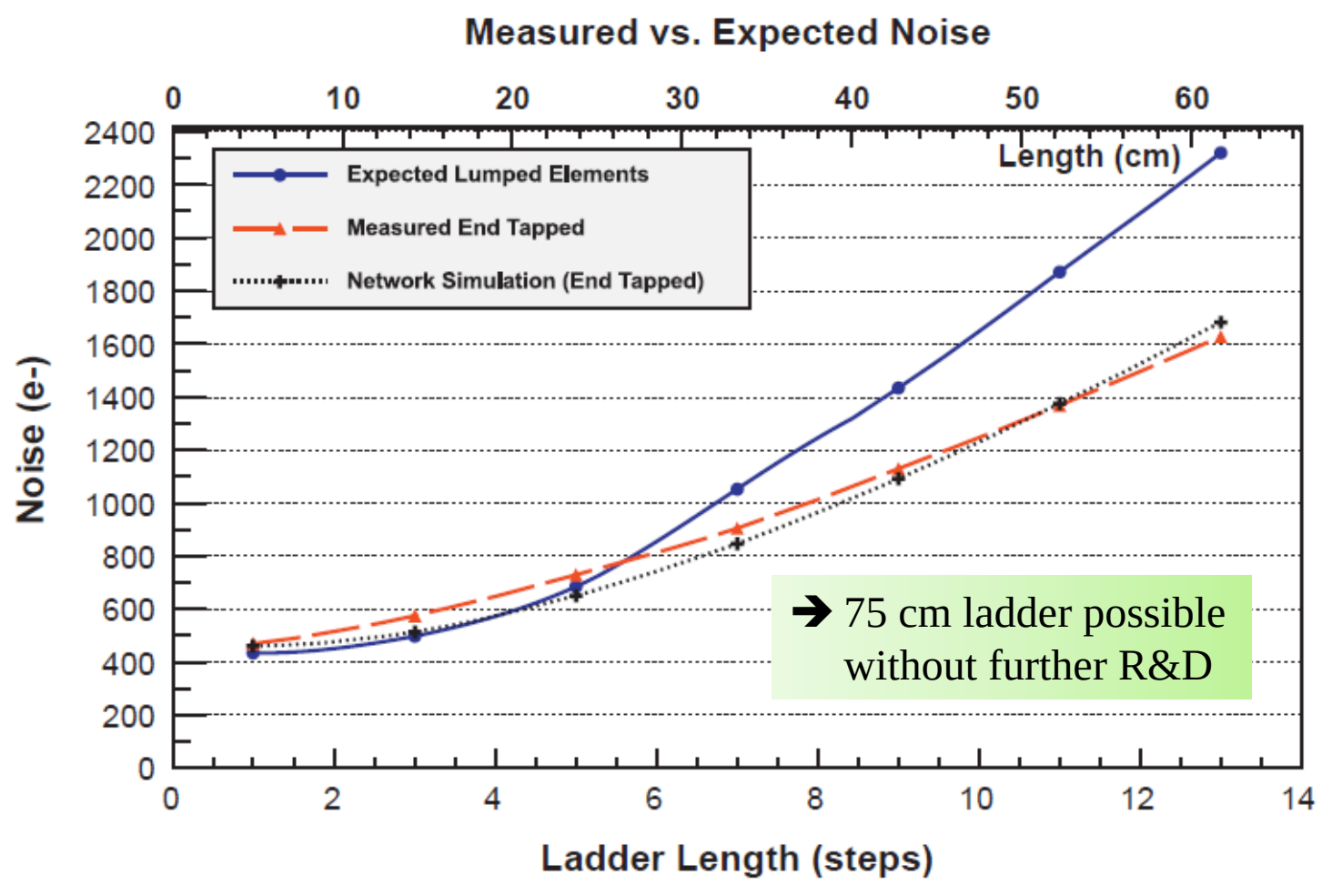


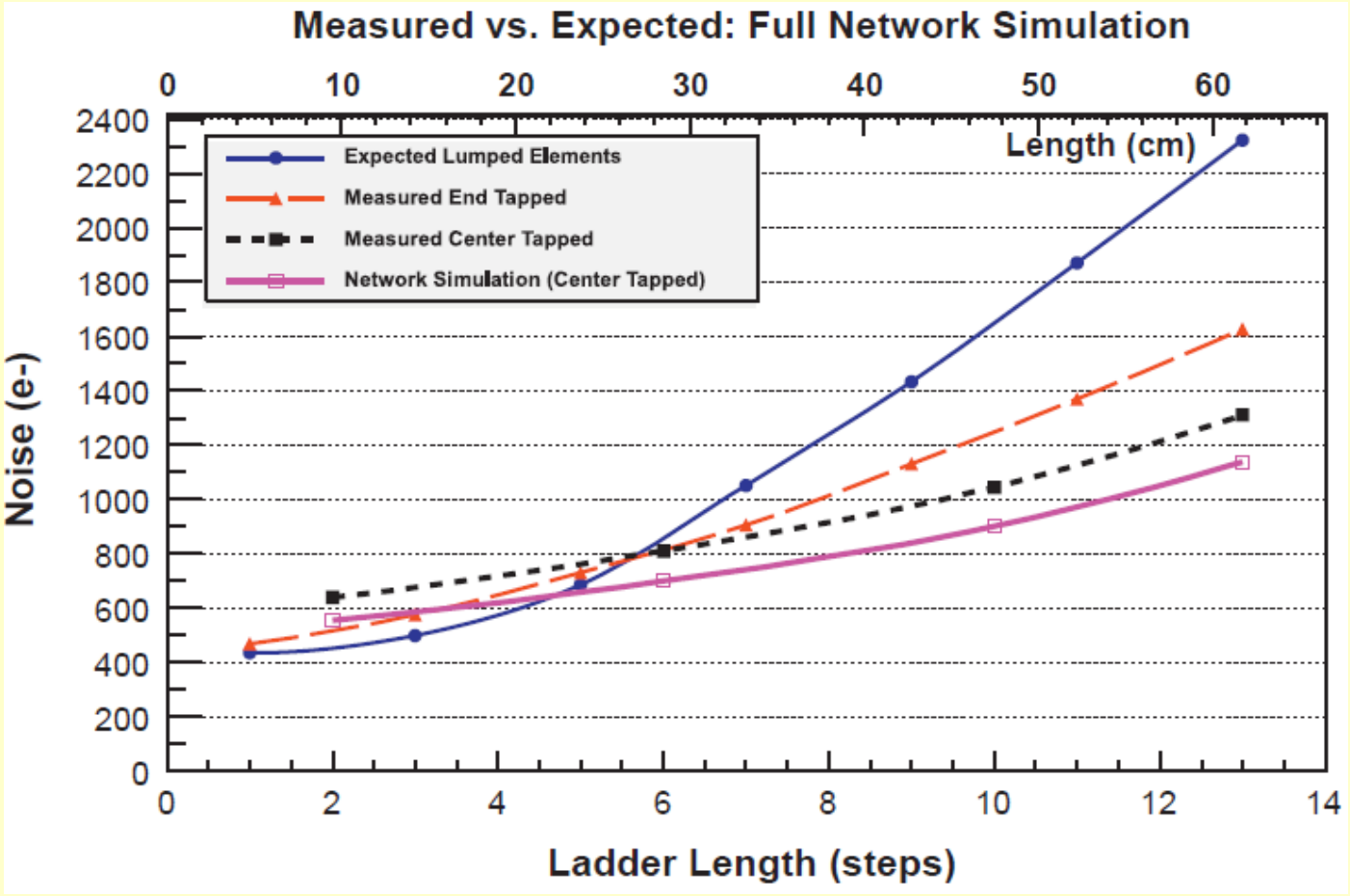

Readout (LSTFE) noise matched to noise calibration with purely capacitive load via small finite-temperature resistor

# End Read-Out Results




- Good agreement between simulation and measurement
- Significant mitigation of noise by network (good news!)

# Center Read-Out Results




- Additional mitigation of noise (more good news)
- Not quite as helpful as expected (?)

# SUMMARY

- The LSTFE ASIC is designed for generic ILC microstrip readout
- Features real-time readout via time-over-threshold
- ~20 μs recovery time can be lessened for short forward strips by reducing shaping time
- Relative simple (reliability, yield)
- Further work: implement power-cycling, develop digital back end [optimize shaping time for short strips]
- Long ladders: can reach ~1m with center readout and/or thicker, wider microstrip traces

# RANDOM BACK-UP SLIDES

# Note About LSTFE Shaping Time

Original target: $\tau_{shape}$ = 3 μsec, with some controlled variability ("ISHAPR")
➔Appropriate for long (2m) ladders

In actuality, $\tau_{shape}$ ~ 1.5 μsec; tests are done at 1.2 μsec, closer to optimum for SLAC short-ladder approach

Difference between target and actual shaping time understood in terms of simulation (full layout)

LSTFE-2 will have 3 μsec shaping time

# Power Cycling

Idea: Latch operating bias points and isolate chip from outside world.

- Per-channel power consumption reduces from ~1 mW to ~1 μW.
- Restoration to operating point should take ~ 1 msec.

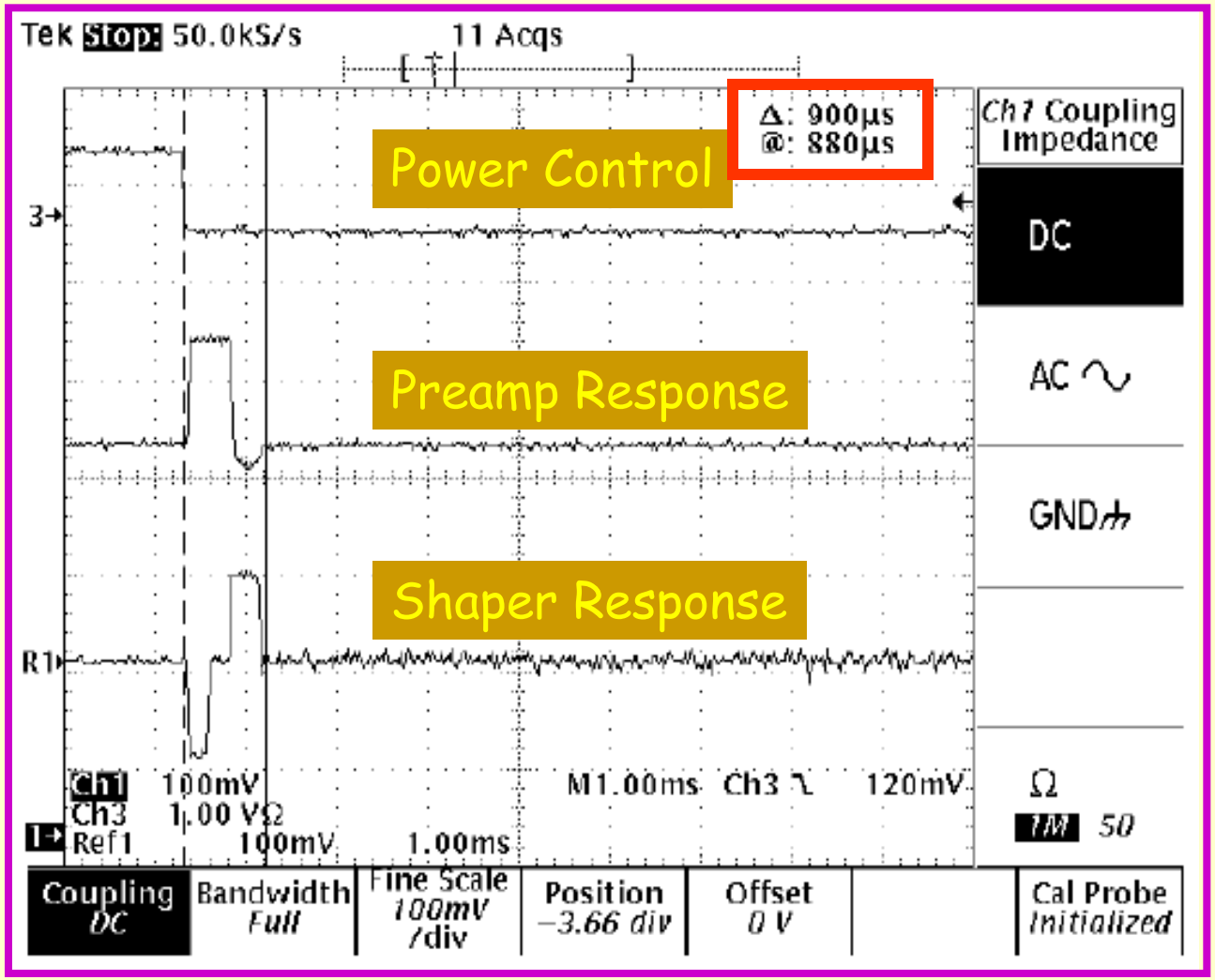
Current status:

- Internal leakage (protection diodes + ?) degrades latched operating point
- Restoration takes ~40 msec (x5 power savings)
- Injection of small current (< 1 nA) to counter leakage allows for 1 msec restoration.

Future (LSTFE-2)

- Low-current feedback will maintain bias points; solution already incorporated in LSTFE-2 design

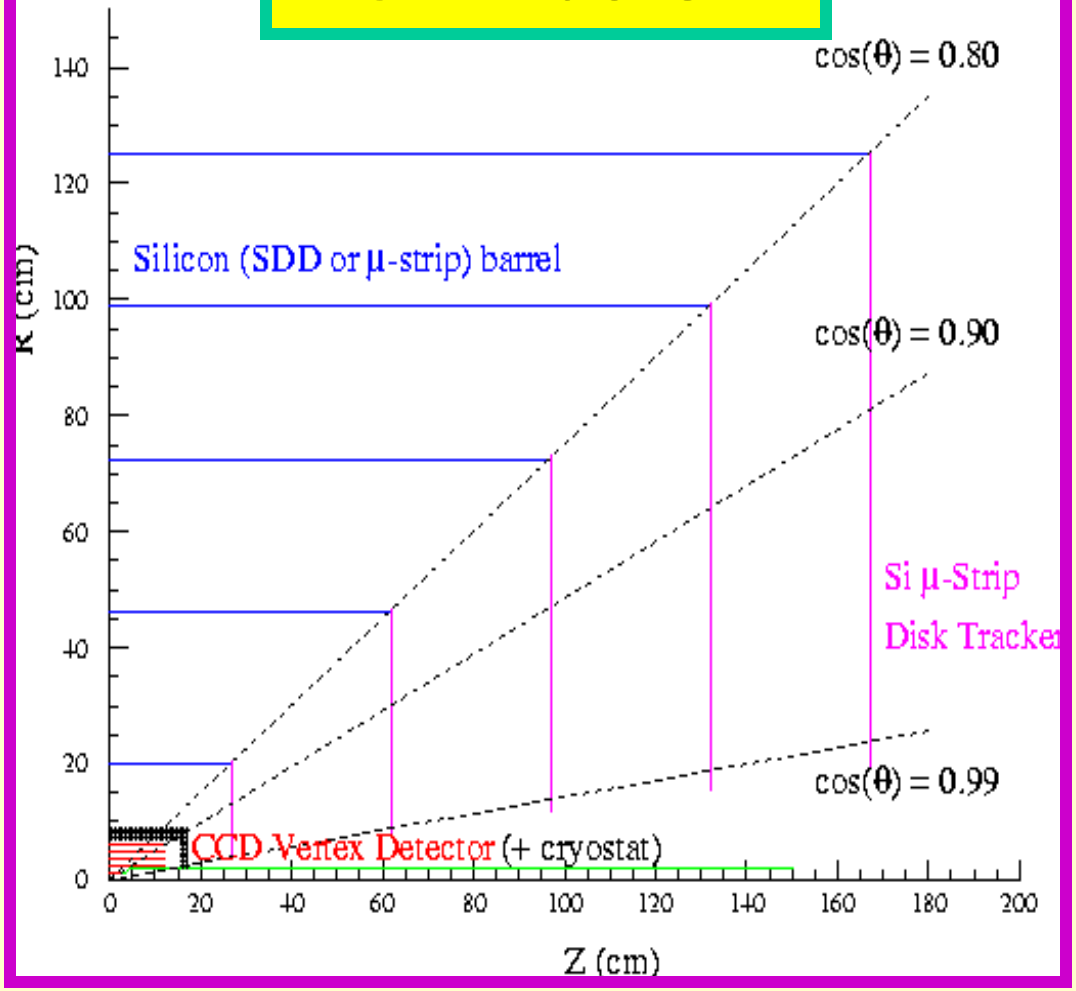
# Power Cycling with Small Injected Current




Solution in hand to maintain bias levels in "off" state with low-power feedback; will eliminate need for external trickle current

# Silicon Microstrip Readout R&D

## SiD Tracker




## Initial Motivation

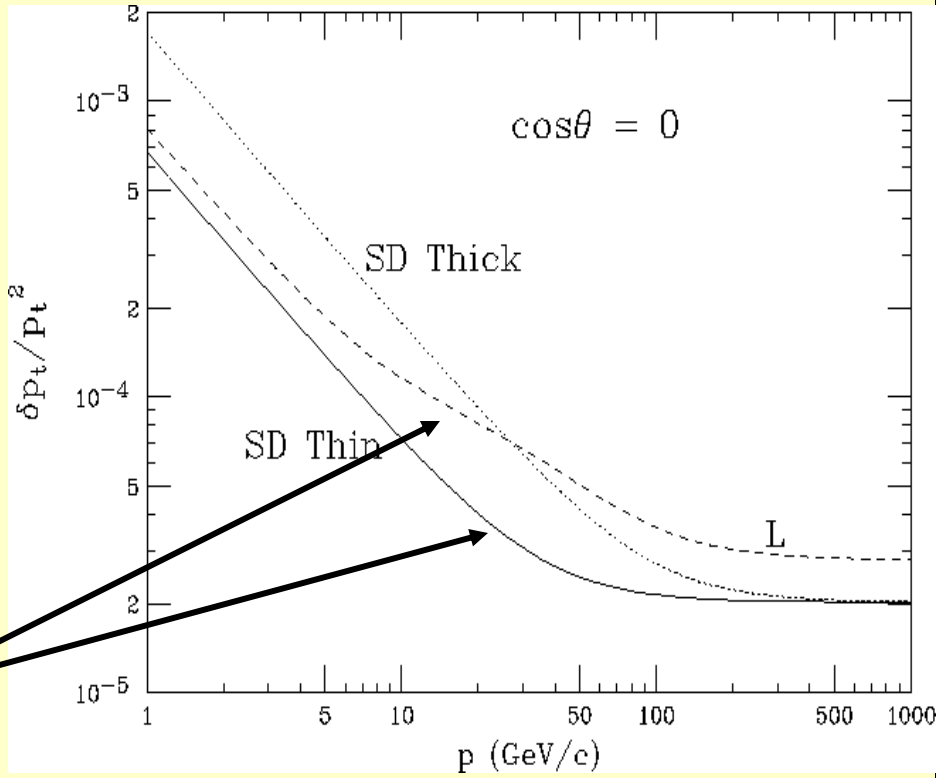
Exploit long shaping time (low noise) and power cycling to:

- Remove electronics and cabling from active area (long ladders)
- Eliminate need for active cooling

# The Gossamer Tracker

Ideas:

- Low noise readout ➔ Long ladders ➔ substantially limit electronics readout and support
- Thin inner detector layers
- Exploit duty cycle ➔ eliminate need for active cooling




Competitive with gaseous tracking over full range of momentum (also: **forward region**)

Alternative: shorter ladders, but better point resolution

# LSTFE-2 DESIGN

LSTFE-1 gain rolls off at ~10 mip; are instituting log-amp design (50 mip dynamic range)

Power cycling sol'n that cancels (on-chip) leakage currents

Improved environmental isolation

Additional amplification stage (noise, shaping time, matching

Improved control of return-to-baseline for < 4 mip signals

Multi-channel (64? 128? 256?) w/ 8:1 multiplexing of output

Must still establish pad geometry (sensor choice!)