

Status of the biasing electronics for the DHPT chip for DEPFET sensors

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SIC, Departament d'Electrònica

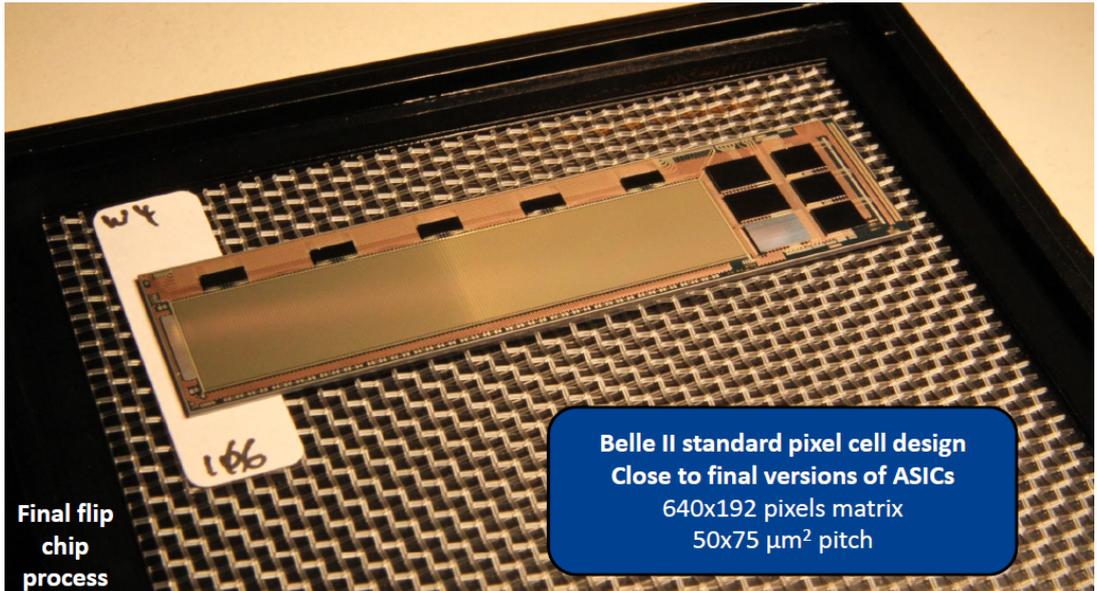
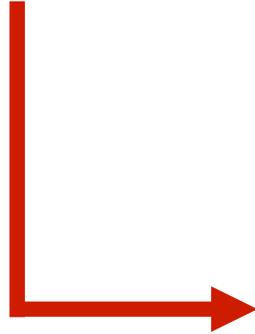
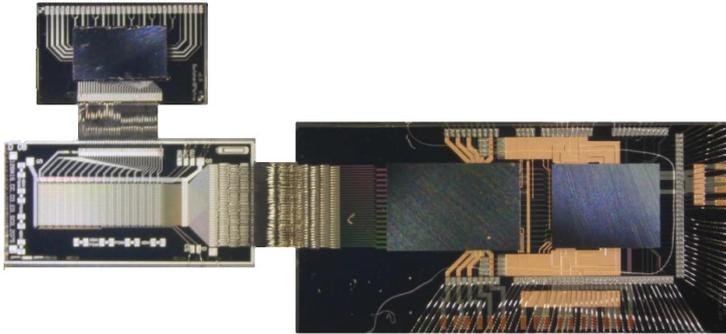
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Outline

- Resume of previous work
- DHPT 1.0 status
 - Bonn IP blocks status
 - UB analog blocks status
 - Tests and results
- Conclusions

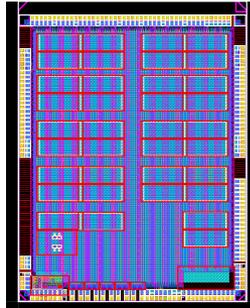
Resume of previous work



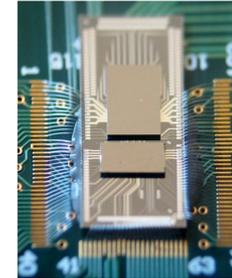
C. Mariñas, PXD/SVD Workshop, Jan. 2014

Resume of previous work

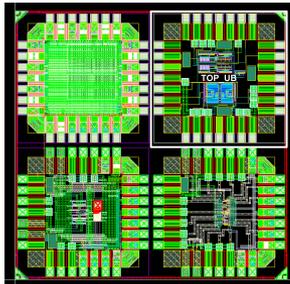
DHP 0.2



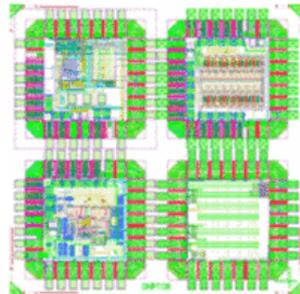
DHP 0.1



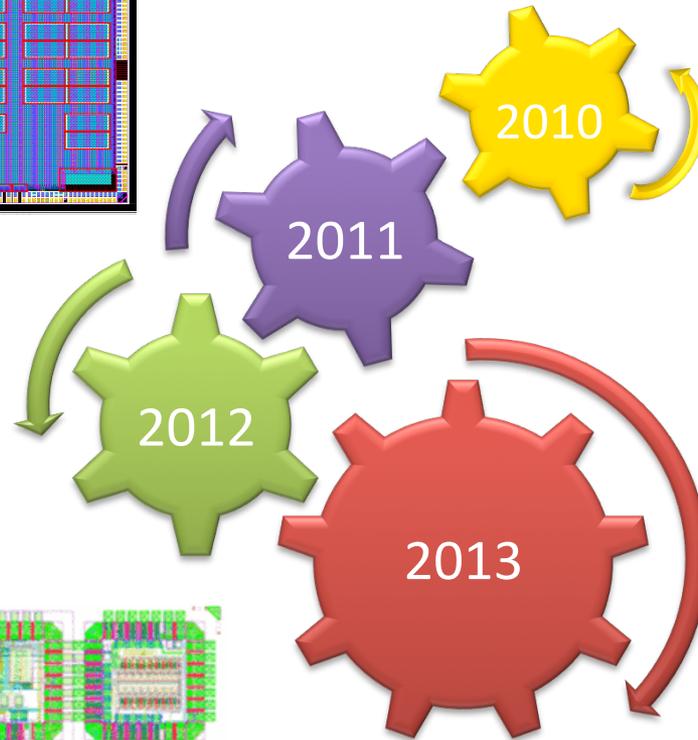
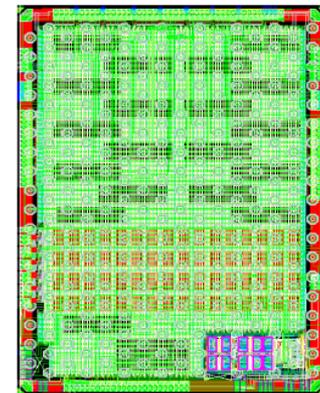
DHPT 0.1



DHPT 0.2



DHPT 1.0



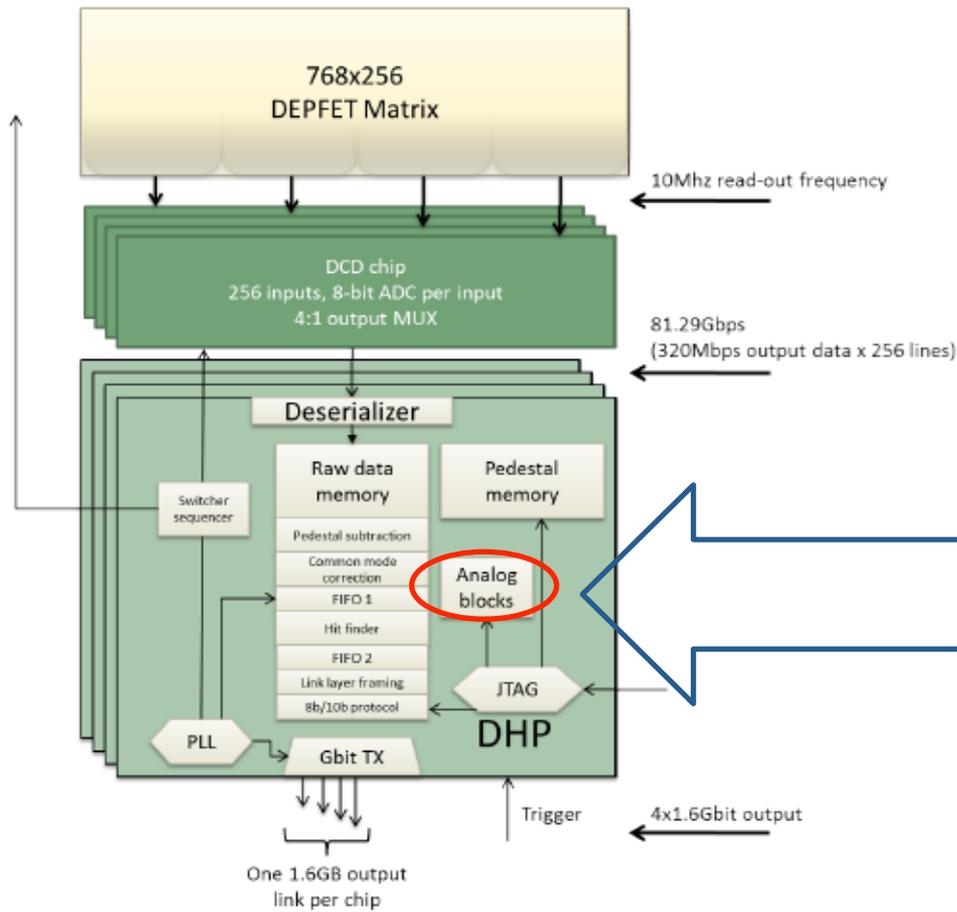
DHPT 1.0 status

	IP Block / Task	Status	Comment
Custom IP	Gbit Link Driver	✓	
	PLL / Serializer	(✓)	Works with adjusted VCC / CLK freq.
	Temperature Sensor	✓	
	LVDS IO	✓	
	Interface DHP-DCD	TBD	Need new WB adapter (LVDS DCDCLK)
	Interface DHP-Switcher	TBD	
	Bias DAC, Current reference	✓	
Data Processing	Command Interface (Manchester encoded)	✓	
	Memory Access (via JTAG)	✓	
	Data Processing: Channel Masking	TBD	
	Double Precision Common Mode Processing	TBD	
	Overflow Handling	TBD	

Wafer batch has “slow NMOS” (too high threshold) -> speed limitations

Hans Krüger, PXD/SVD Workshop, Jan. 2014

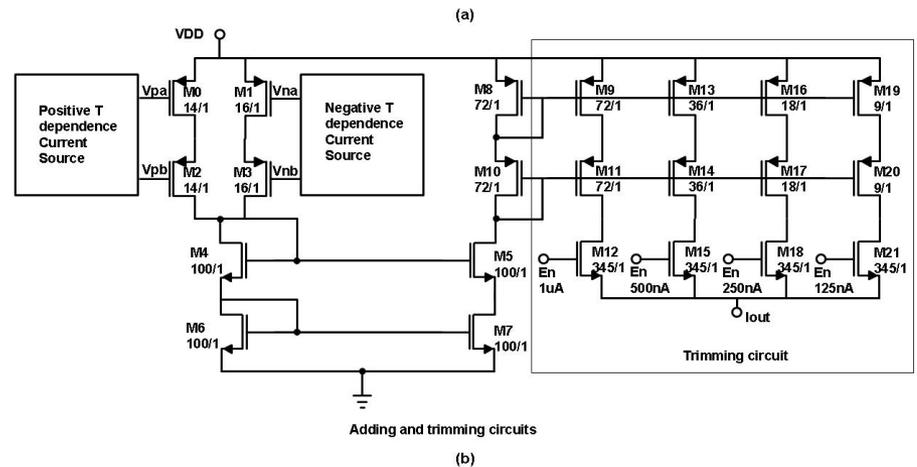
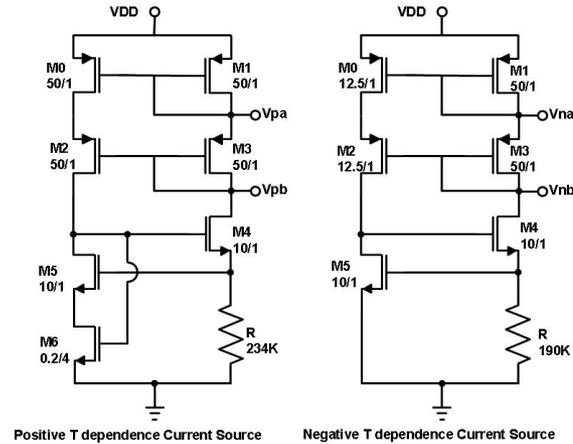
DHPT 1.0 status



- Independent temperature current source
- 10 current DACs
 - CML driver
 - LVDS driver
 - PLL
 - Test
- Temperature sensor

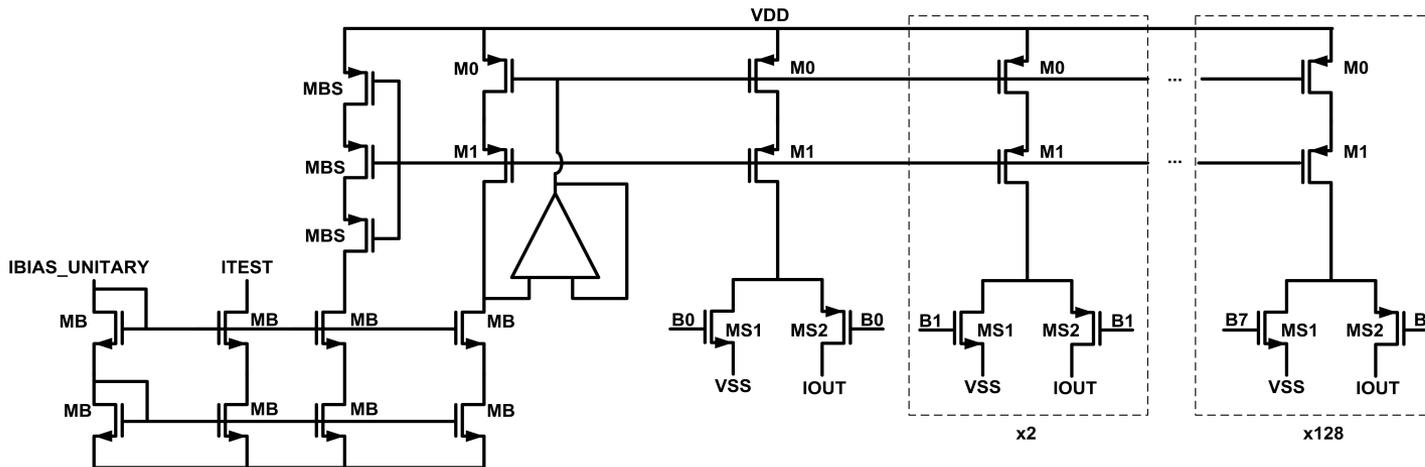
DHPT 1.0 status

- Positive T dependence current source
- Negative T dependence current source
- Trimming circuit
- Backup solution: Pad connected to lout to overdrive the output
- Power consumption (trimming 1uA) : 9 uW



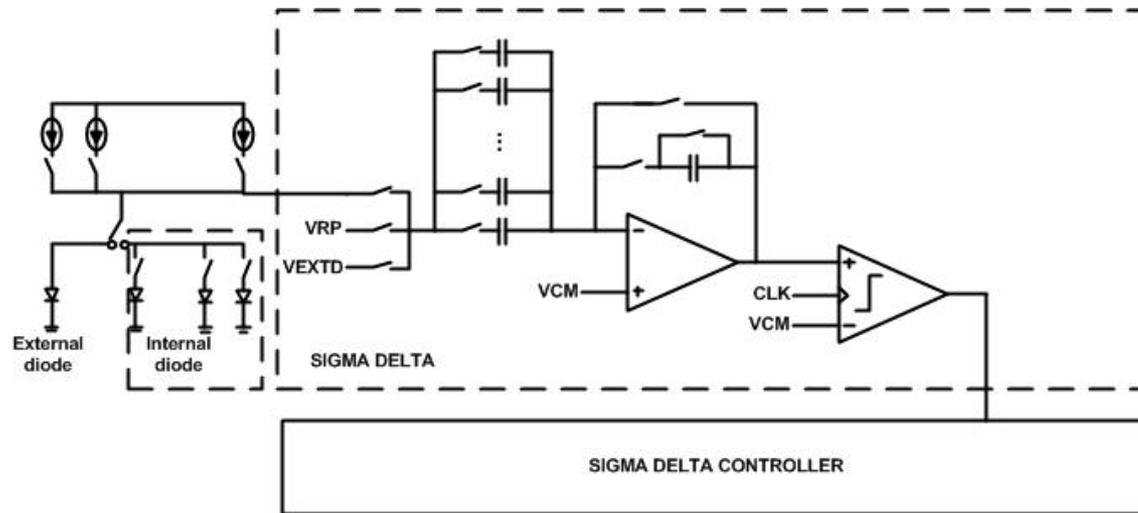
DHPT 1.0 status

- Configurable bias current
- Maximum output voltage 970 mV
- Power consumption 320 μ W (room Temp.)



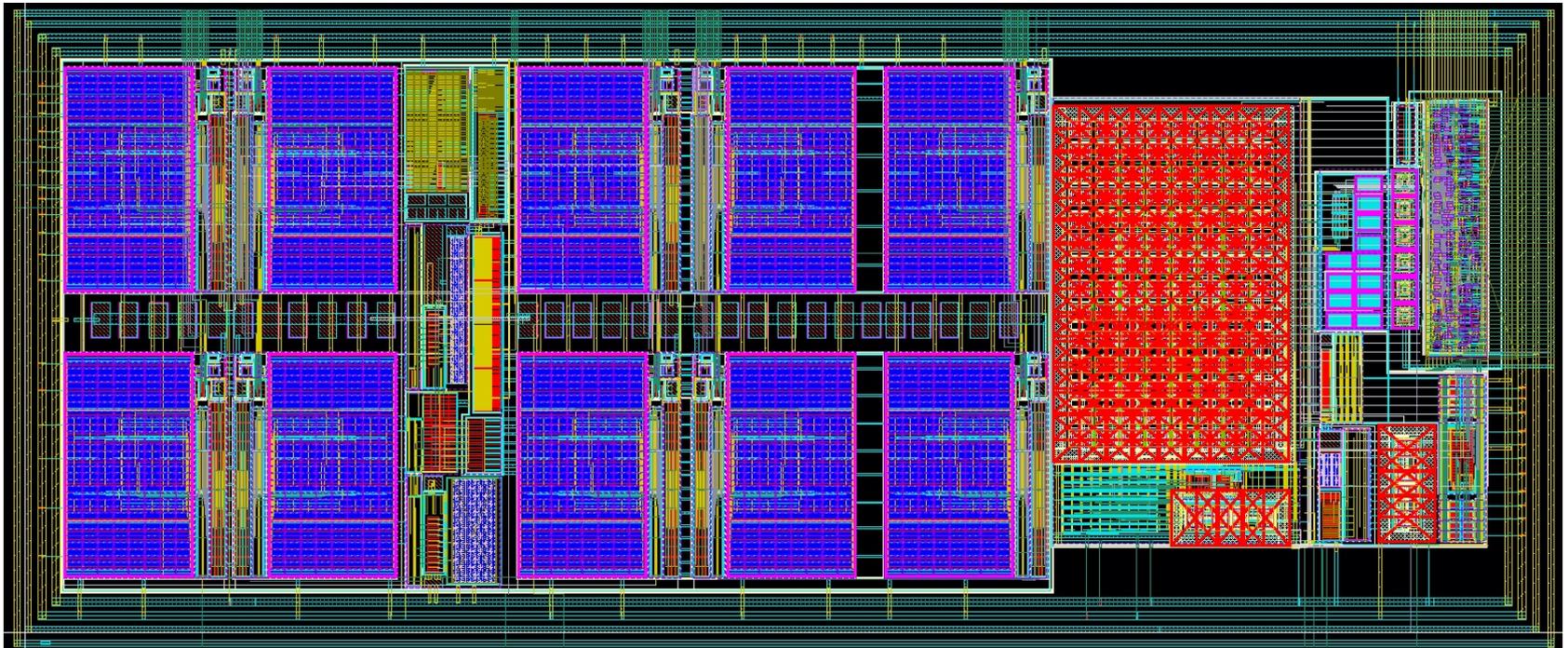
DHPT 1.0 status

- Programmable
 - Temperature range
 - Gain (1 to 20)
 - Current(1-4) and area (1-5) ratios
- Configurable incremental sigma delta converter:

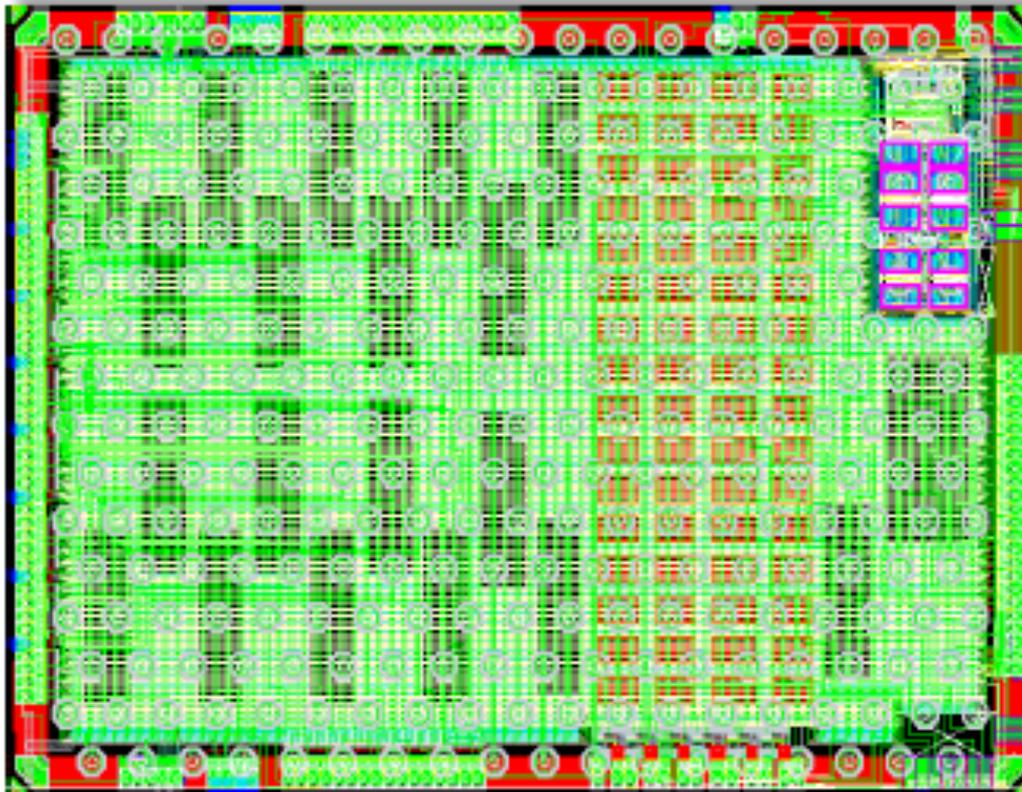


DHPT 1.0 status

- Layout
 - Area : 995 μm x 410 μm
 - 4 Guard rings (Analog and digital supplies)



DHPT 1.0 status



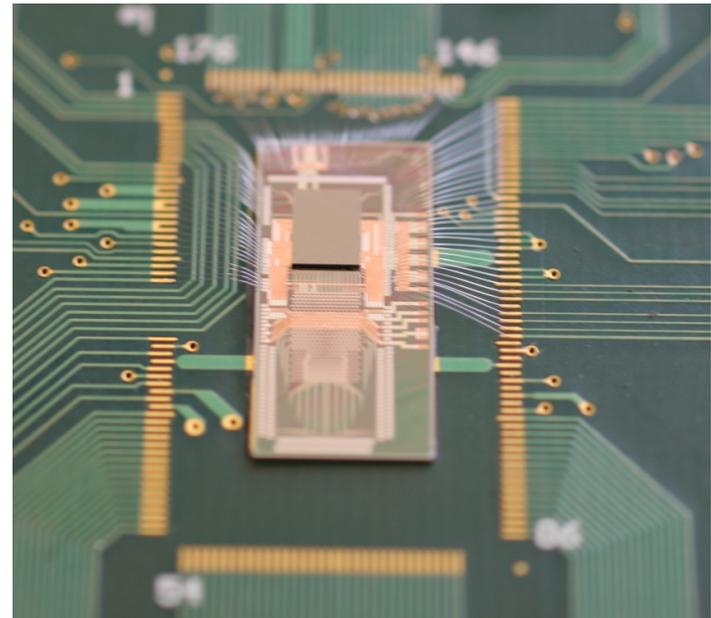
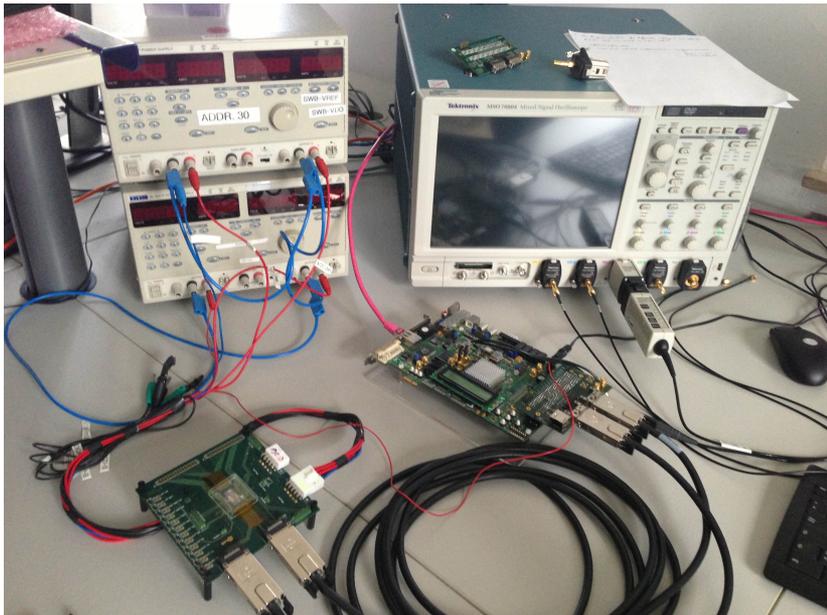
DHPT 1.0 status

Tests @Bonn:

- Current source from board #2 with different loads.
 - Current source from board #2 in the temperature chamber (temperatures from -20 to 50 C degrees)
 - IDACs from board #2 and #3.
 - Temperature sensor from board #2.
 - Temperature sensor from board #2 in the temperature chamber (temperatures from -20 to 50 °C degrees)
-
- For the temperature sensor we selected 7 different configurations, each test measurement was repeated 20 times and averaged.
 - Current measurements were repeated 10 times and averaged.

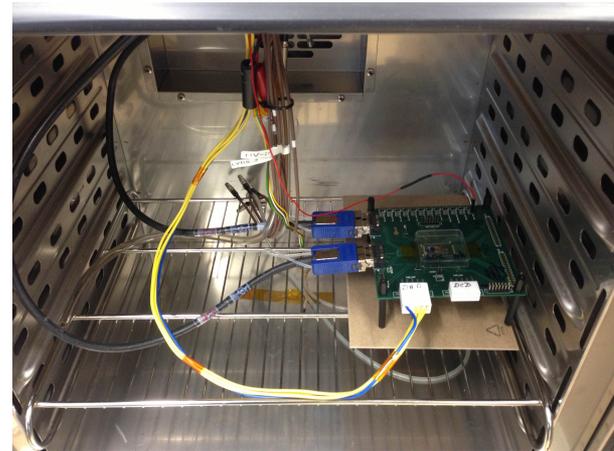
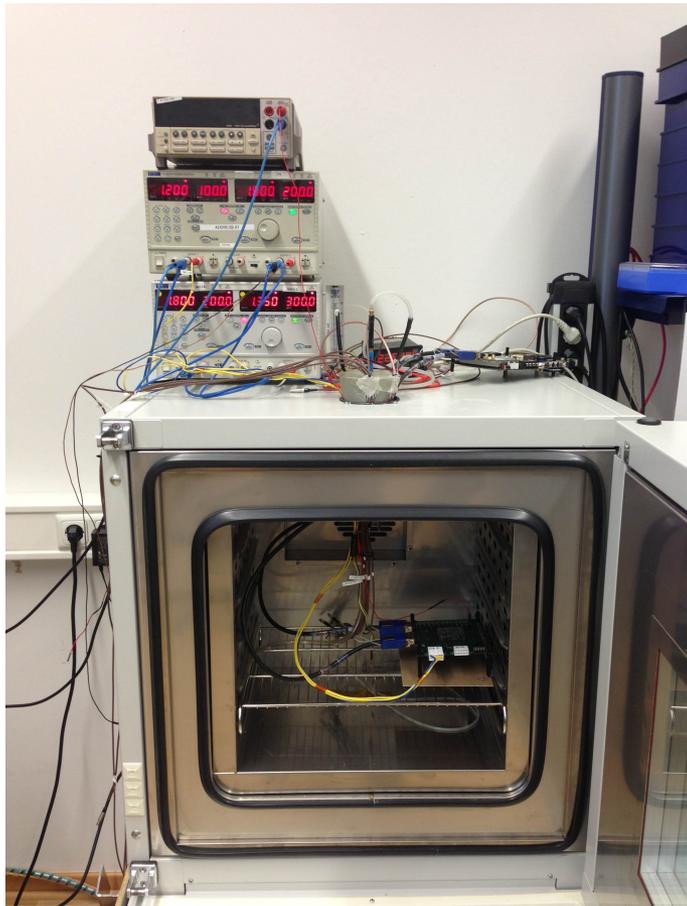
DHPT 1.0 status

First tests used to demonstrate that the Analog UB part is ok



Special thanks to Mikhail and Leo who the welcoming and the help that they gave me

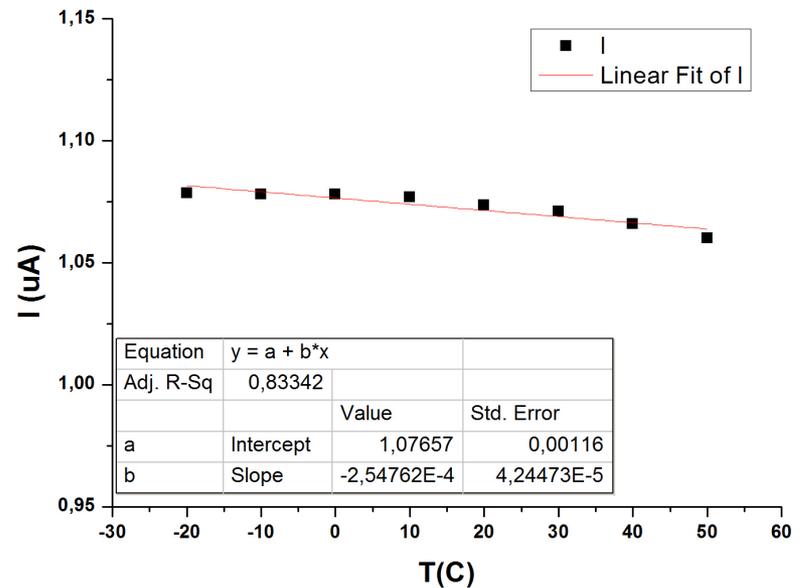
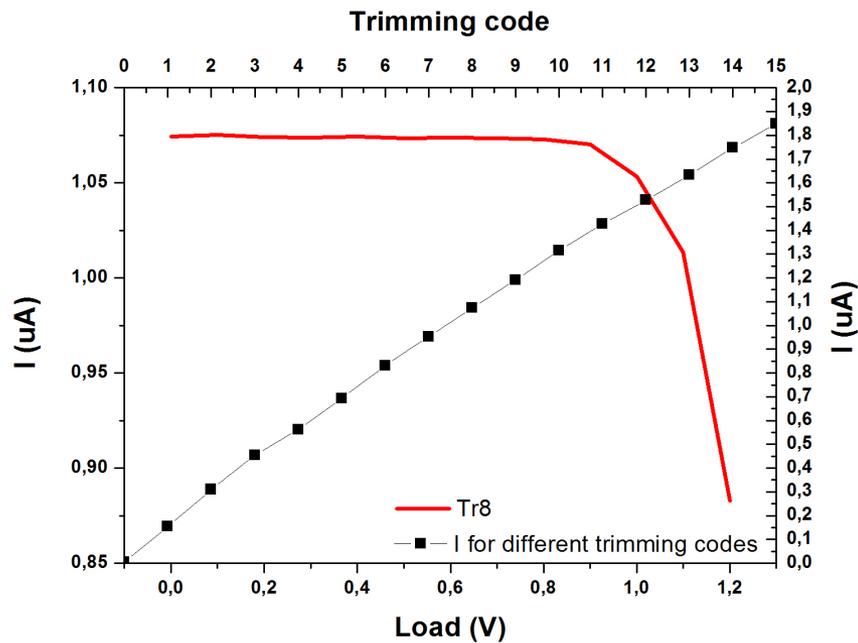
DHPT 1.0 status



DHPT 1.0 status

Temperature Independent Current Reference

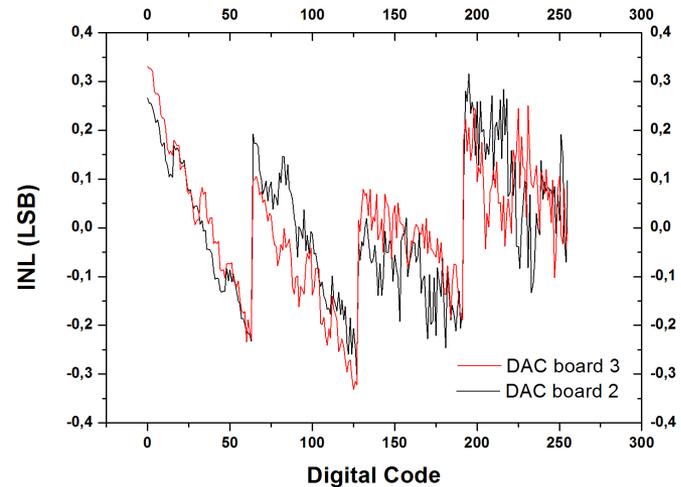
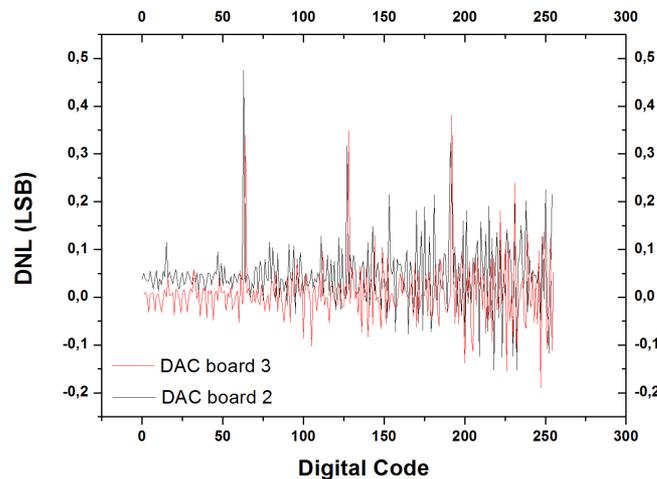
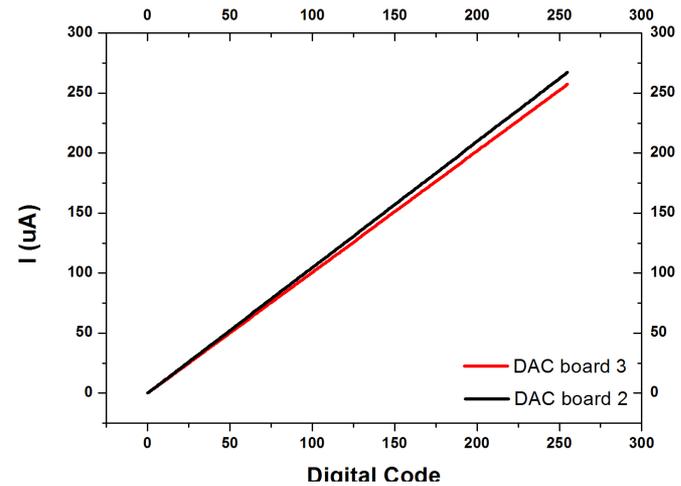
- ✓ Compliance
- ✓ Trimm. functionality
- ✓ Temperature sensitivity



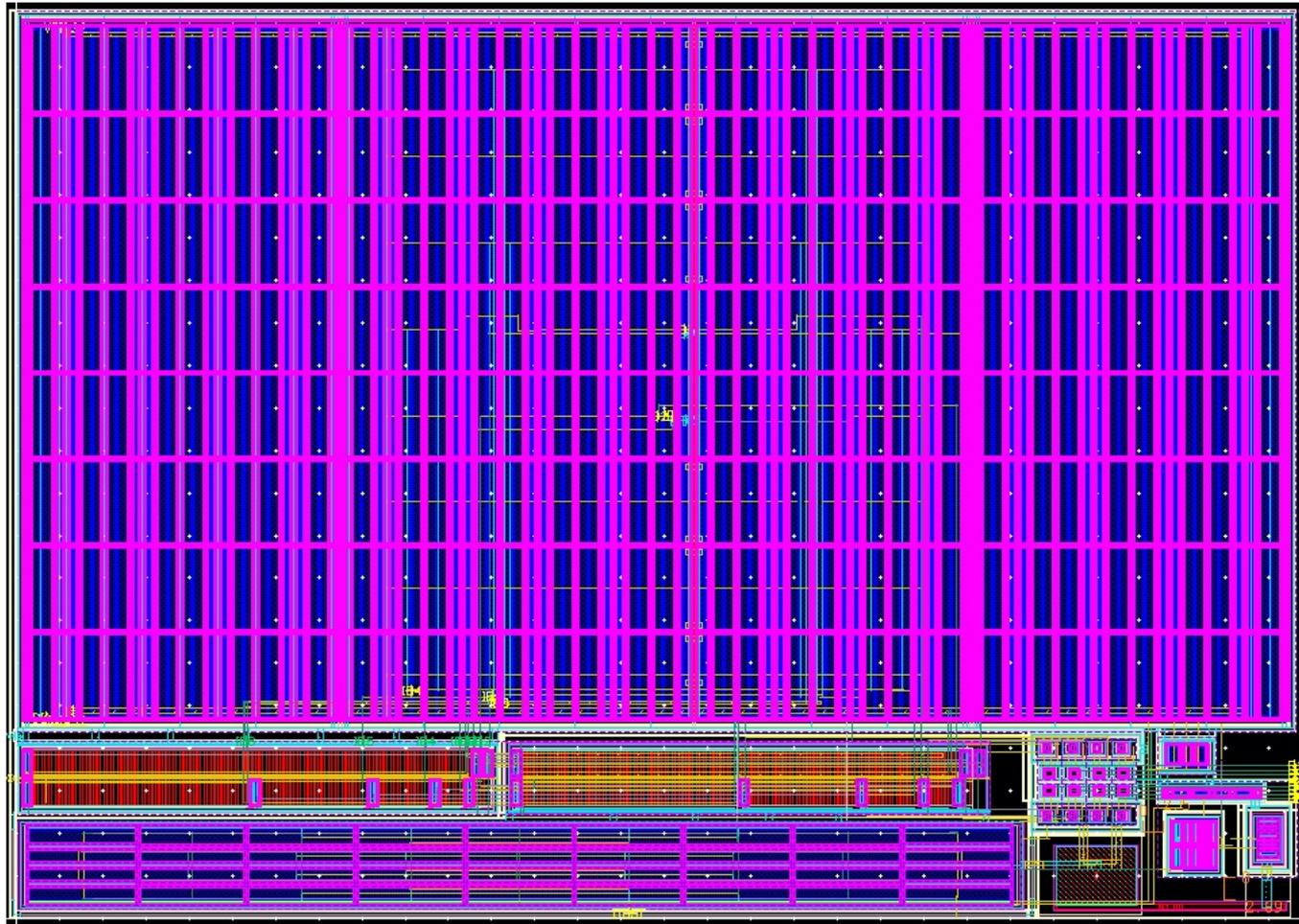
DHPT 1.0 status

8-bit DAC for bias current control

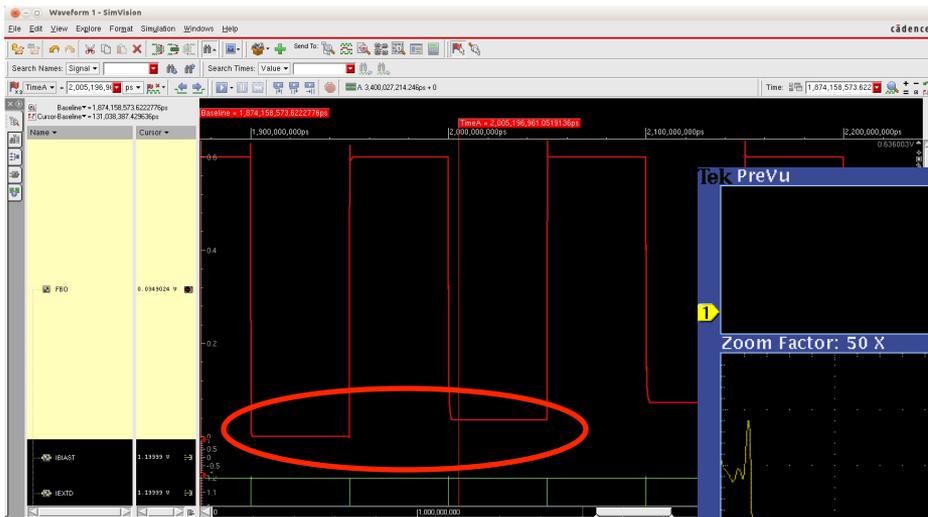
- ✓ Dynamic range
- ✓ Linearity



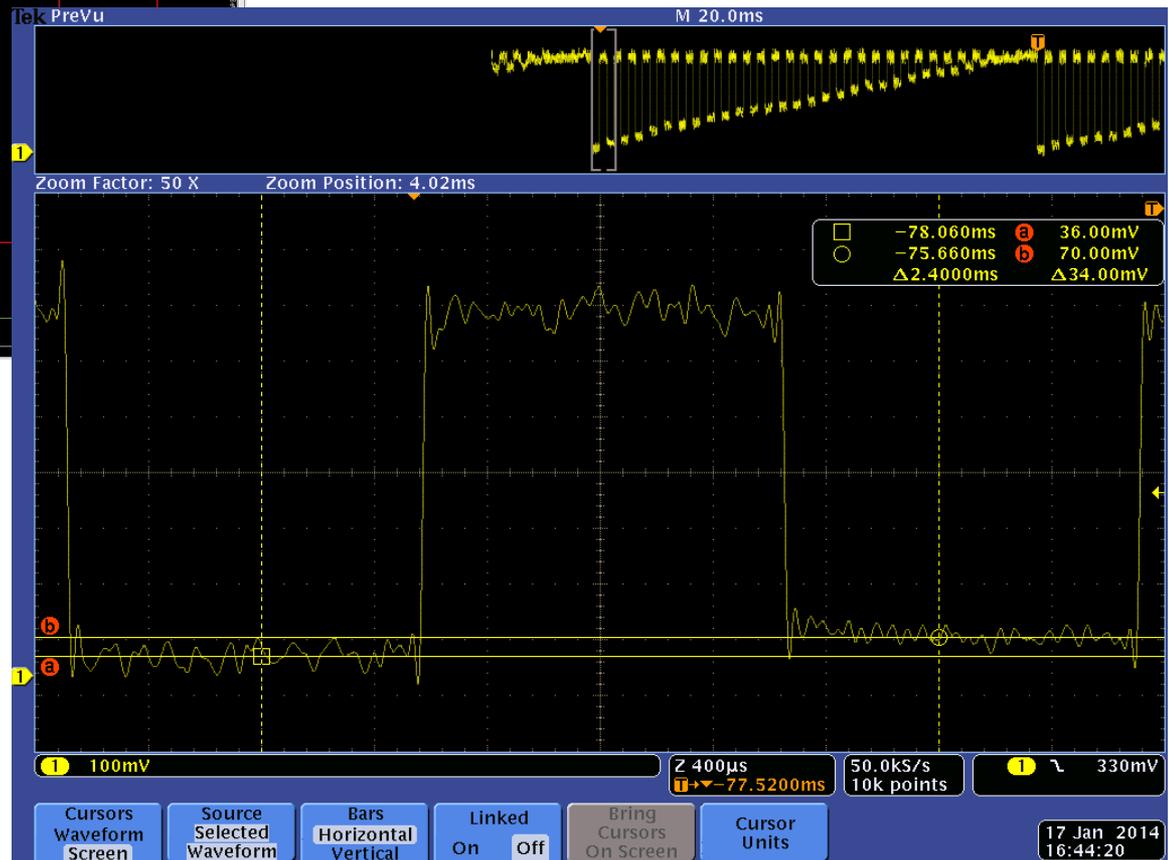
DHPT 1.0 status



DHPT 1.0 status



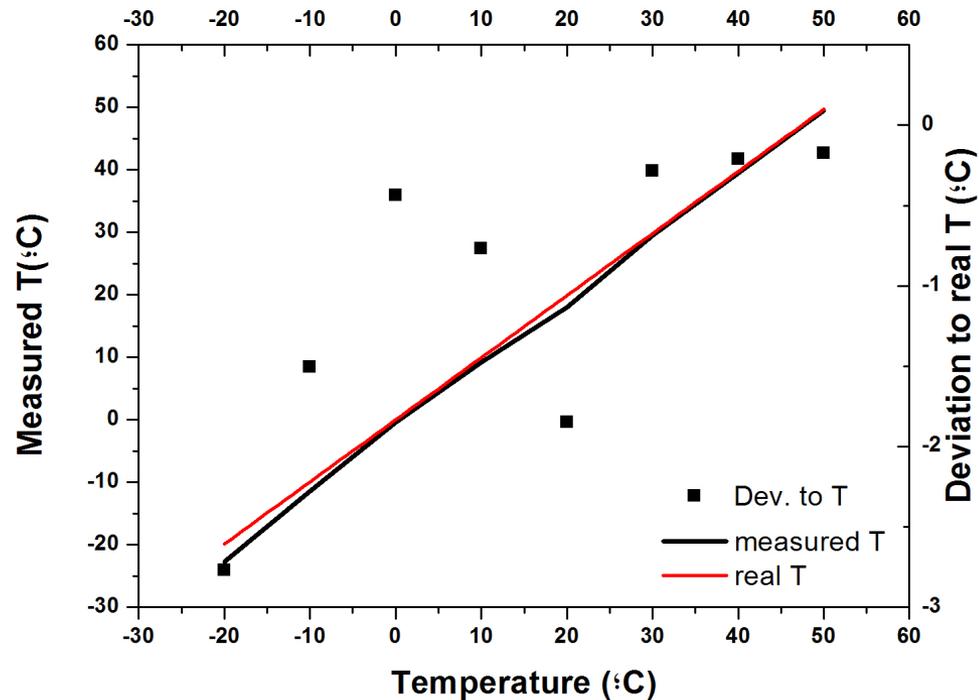
- Simulation $\Delta V \approx 35$ mV
- Measured $\Delta V \approx 34$ mV



DHPT 1.0 status

Internal or external sensing diode + 16 bit Sigma-Delta ADC

- ✓ Measurement range -20°C ... +50°C



Conclusions

- Functional verification: DHPT 1.0 mounted on PCB with WB adapter -> ongoing
 - ✓ Analog blocks & ongoing
 - ✓ Digital signal processing -> ongoing
 - Interface DCD, Switcher -> TBD
 - Serializer needs non standard operation conditions
- Next verification steps
 - Full functional coverage with current PCB test setup
 - Probe station tests -> known good die
 - System tests
- Planned re-design DHPT 1.1
 - Serializer bug fix
 - Anything else that eventually shows up ...

Conclusions

- ICS and IDAC layout re-design (deep n-well)
 - Tests reported better results than DHPT 0.1
- Improvement of T sensor:
 - Layout re-design
 - Digital controlled changes
 - Self-biasing blocks added
 - Tests reported better results than DHPT 0.2
- More tests have to be done to fully characterize the analog block
- DHPT 1.1 tentative schedule
 - Tape-out: April
 - Delivery: July
 - Tested production chips available starting from September