CIEMAT activities in Calice SDHCAL: Electronics

X Meeting of the Future Linear Colliders Spanish Network

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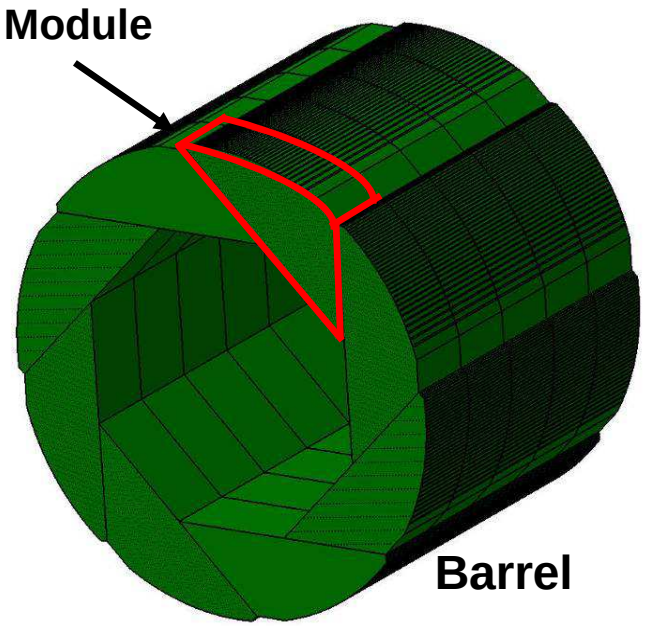
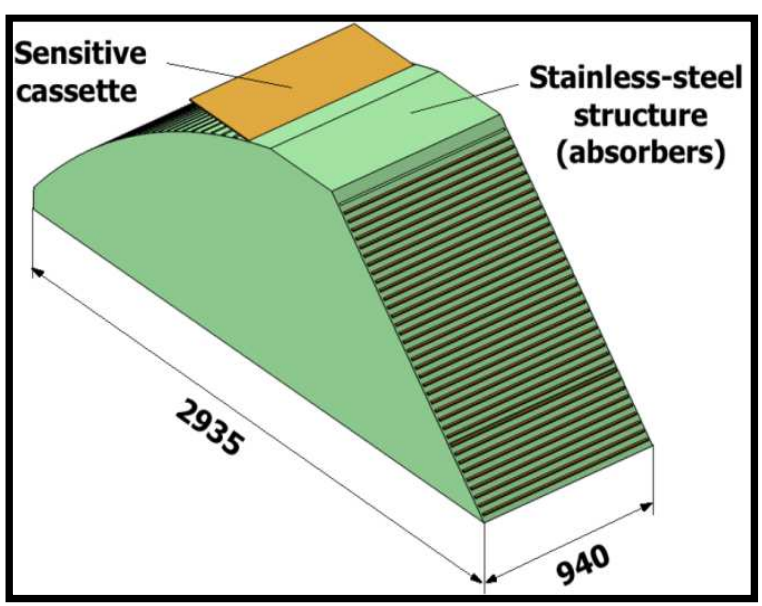
SDHCAL

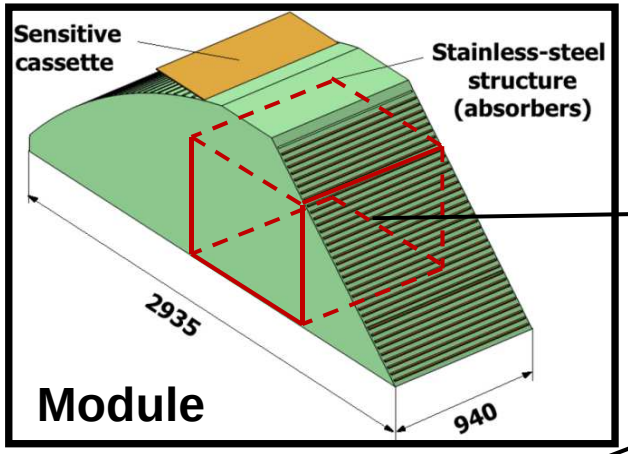
The Semi-Digital HCAL was one of the two hadronic calorimeters options proposed at the DBD for ILD.

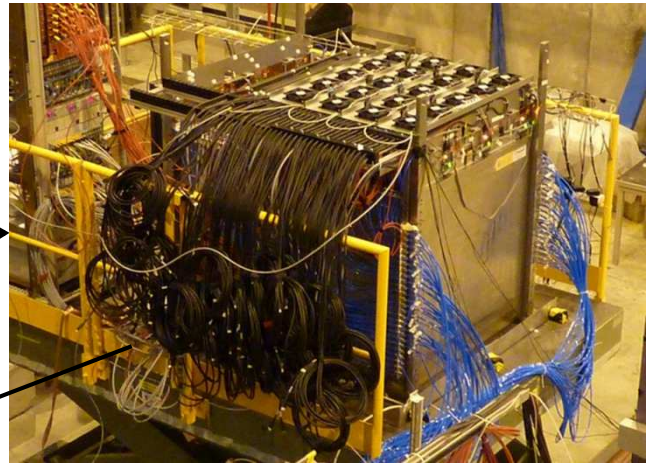




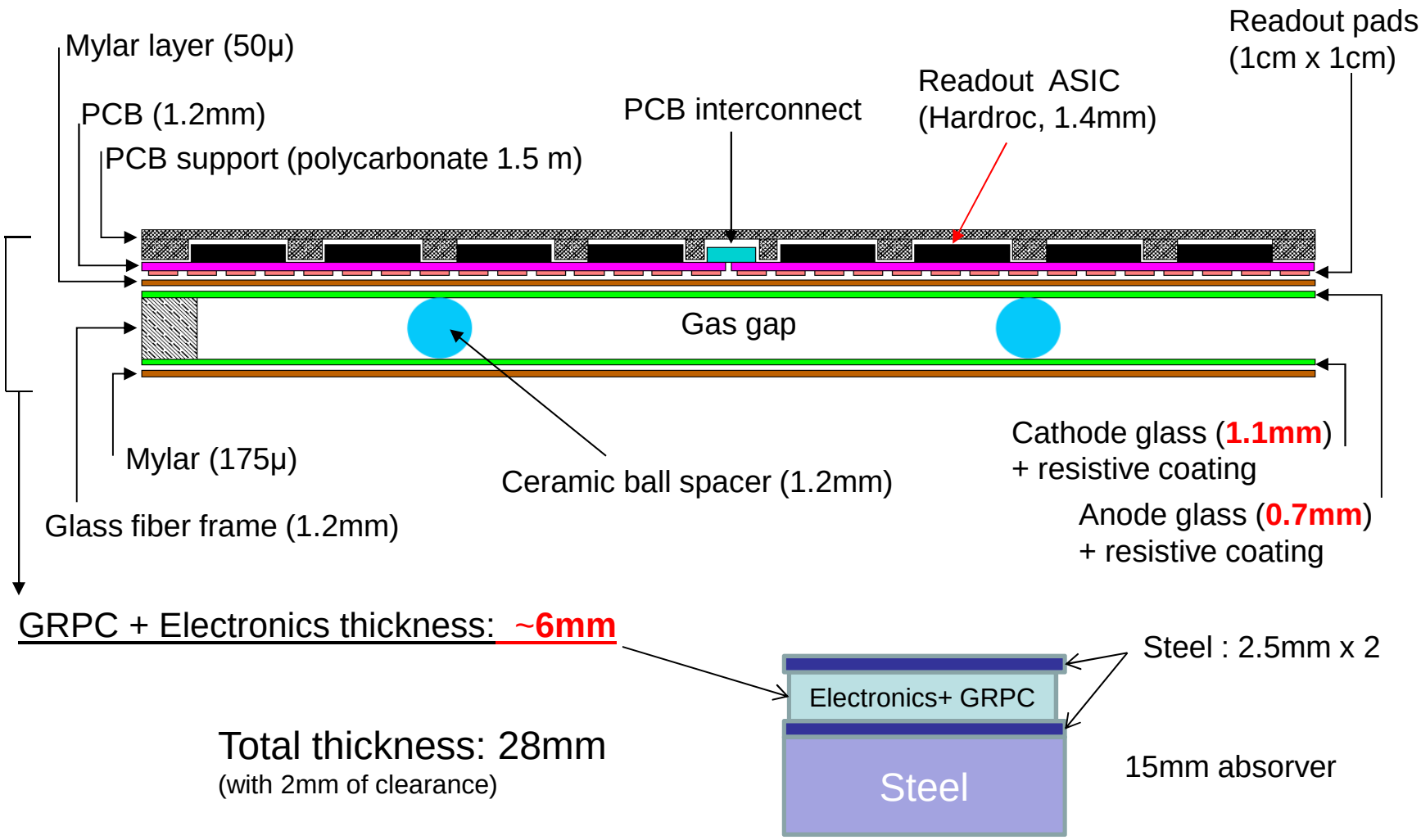
First prototype: 1m³

40 Detection planes with 9216 channels each: 368640 readout channels
Successfully built and tested in pion beams at CERN



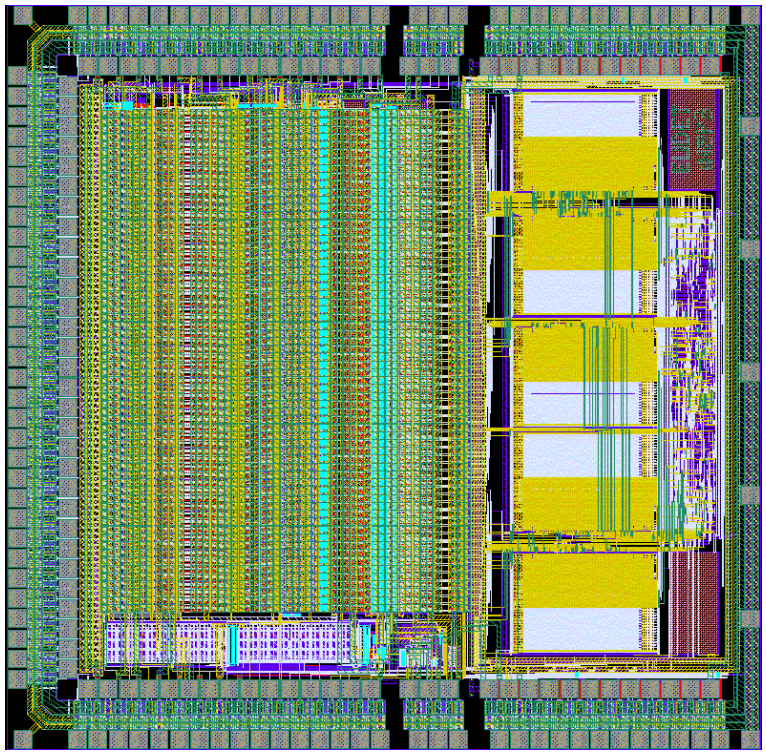


Detector cassette cross-section



HaRDROC chip for SDHCAL

Hadronic Rpc Detector Read Out Chip



- **ASICs embedded** inside the detector for compactness and **daisy chained** to minimize output lines on the detector.
- **64 inputs**, **1 serial output @ 5 MHz**
- Each input is compared with 3 (programmable) threshold levels and the results are encoded in 2 bits (SemiDigital)
- **Power pulsing capability**: Low power mode after data acquisition and readout (99% of the time). From 1mW/ch to 10µW/ch with PP
- **Digital memory for 128 events**: store all channels (2 bits/chan) and BCID (24 bits) for every hit (20 kbits total)
- New in HR3:
  - **I2C bus** for slow control
  - **Independent memory** for each input. Only is sent the memory of touched inputs.

Readout PCB: ASU

As it is not possible to produce the 1m² PCB in one piece, it was built assembling 6 smaller boards.

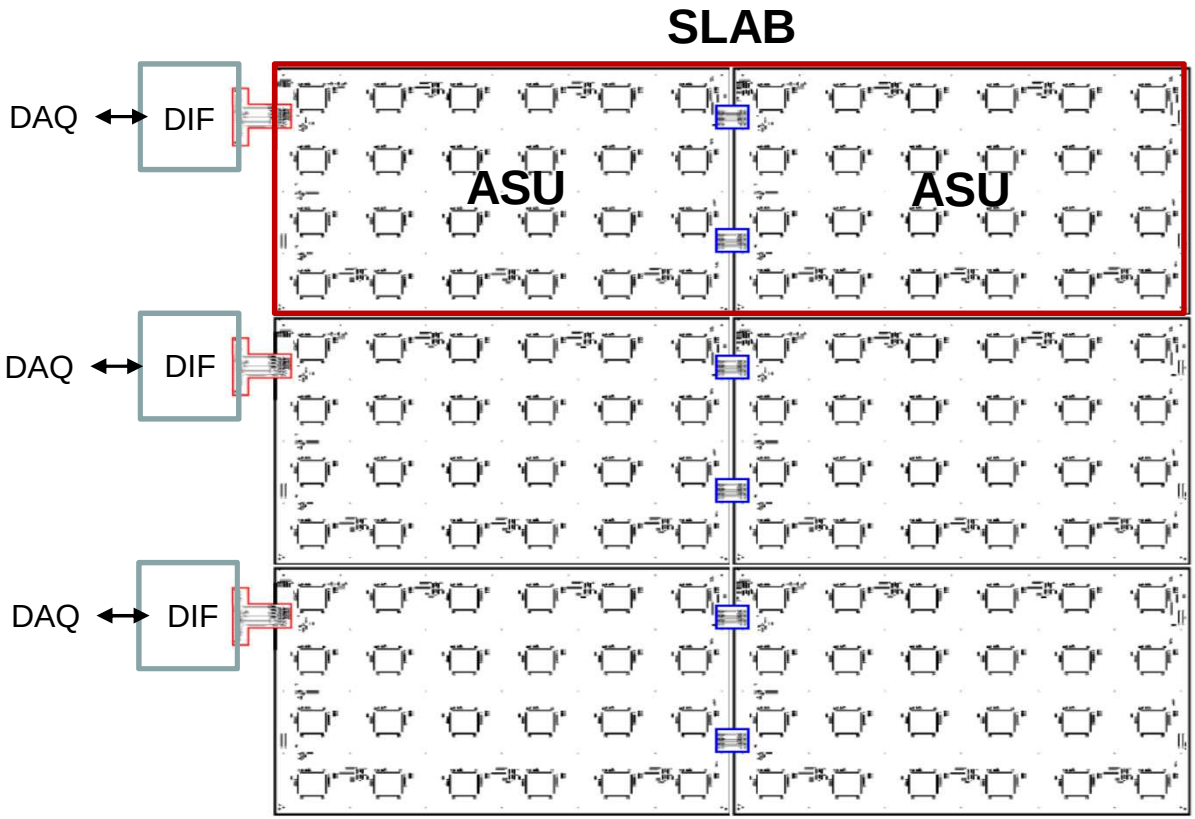
Each of these boards are called ASU (Active Sensor Unit) and they hosts the front-end electronics.

Each ASU hosts 24 HARDROC (HR) chips. So, there are 144 HR /m²

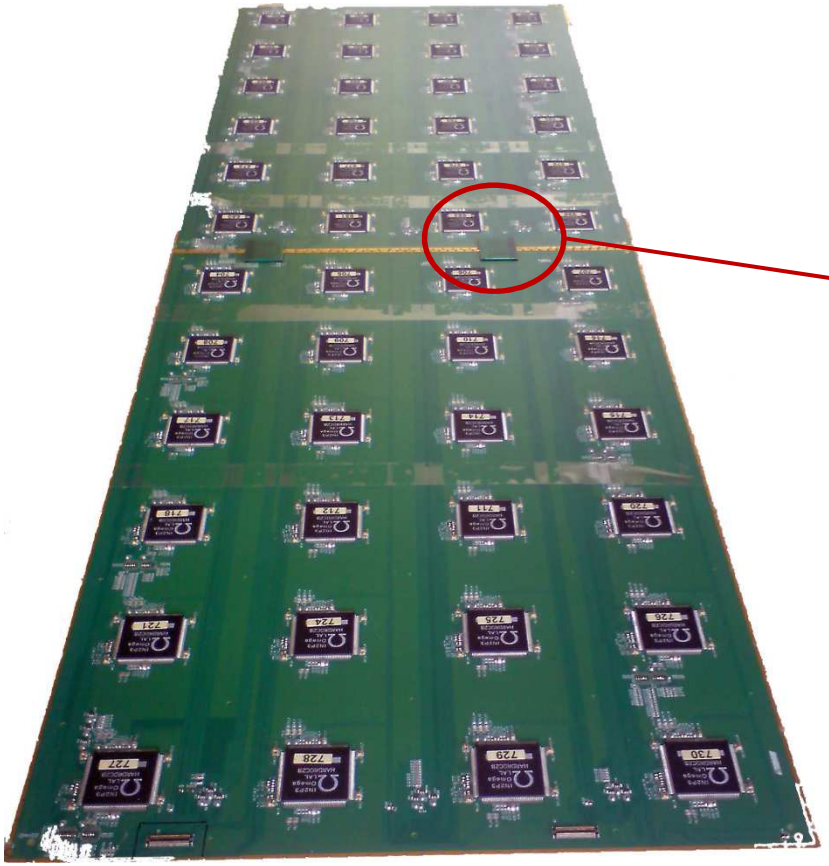
ASUs are connected two by two to form a 'slab'.

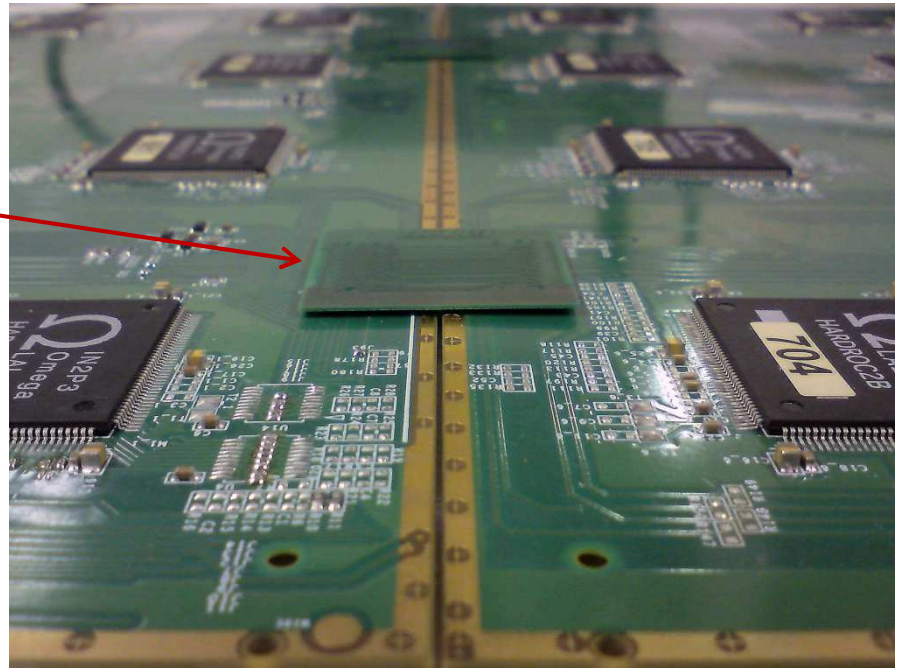
Each 'slab' is connected to a DIF (Detector Inter-Face) board

3 DIFs are needed for the 1m² plane



ASU board

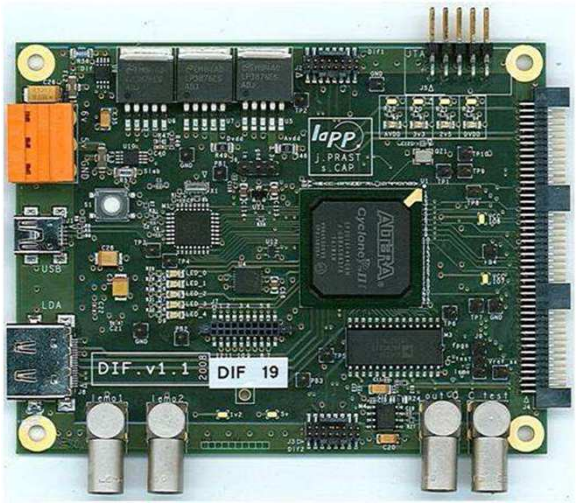




Detail of the ASU to ASU connector

DIF board

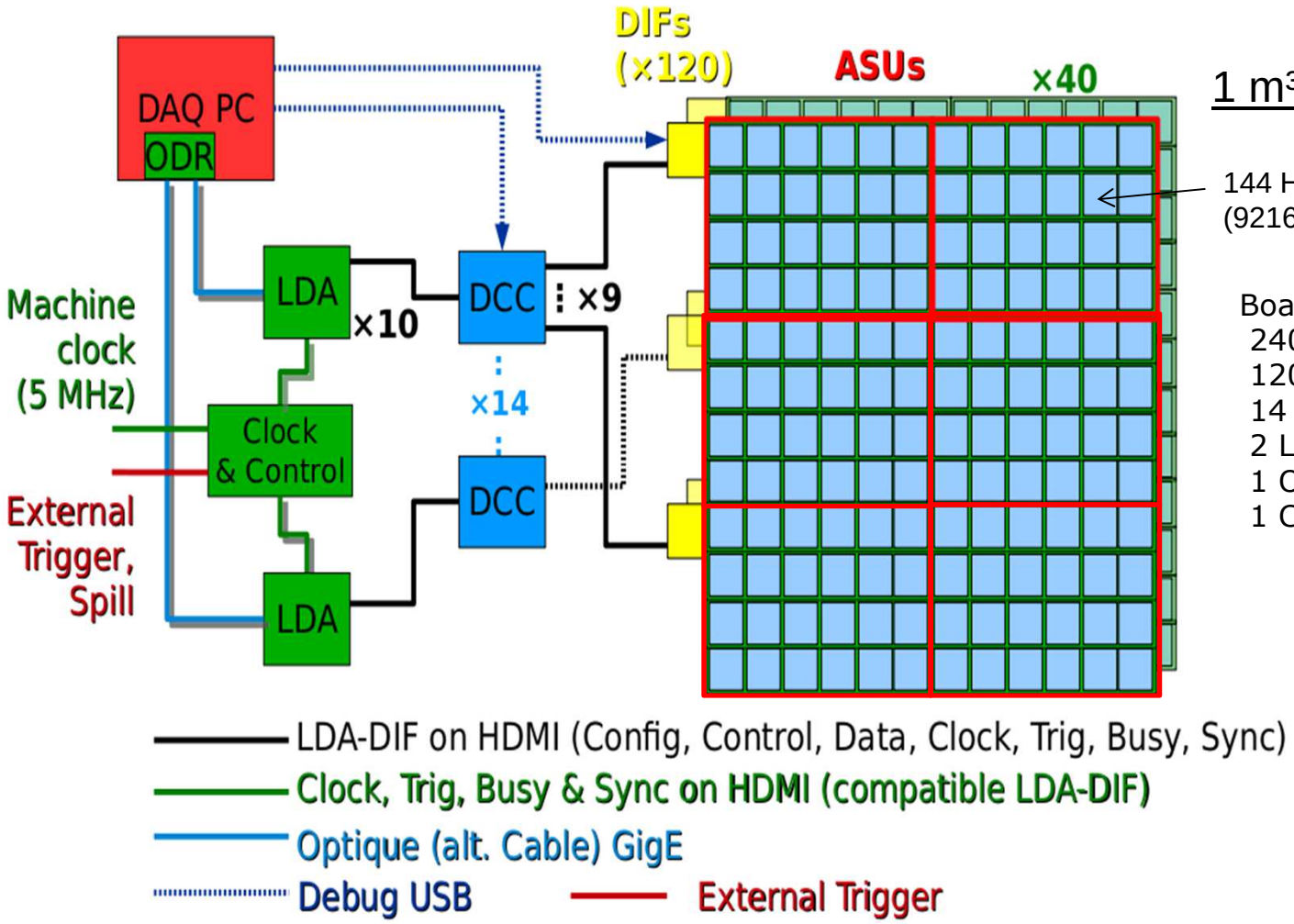
AIM:
Use a common DAQ for all the CALICE detectors and adapt to the different front-end technologies on the DIF board



Functionality:

- Receive, regenerate and distribute **clocks**
- Receive the **slow control data** (ASICs configuration) from DAQ and configuration of the ASICs with those data.
- Receive and decode incoming **commands from DAQ** and assert corresponding signals to the ASICs (start the acquisition, start readout)
- Performs **ASICs readout** and sends all the data received to the DAQ PCs.
- **Power supply** regulation & monitoring
- Control **power pulsing**
- Provide an **USB interface** for stand-alone running and debugging

DAQ – First Design



1 m³ prototype:

144 HR chips
(9216 channels/m²)

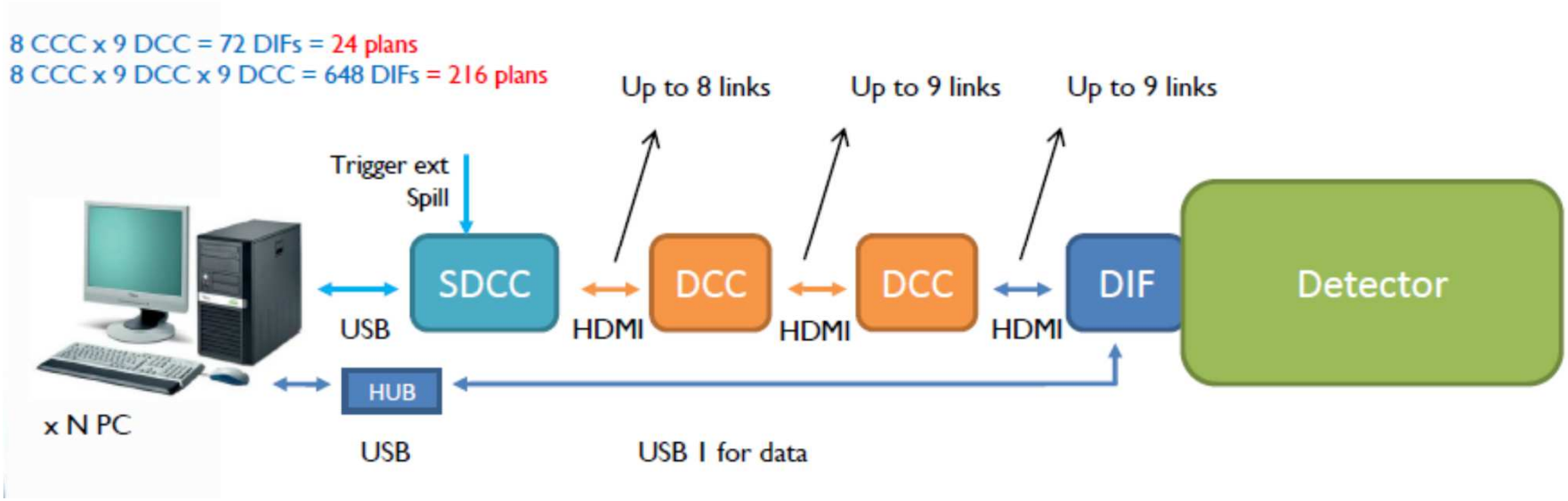
Boards:
240 ASUs
120 DIFs
14 DCCs
2 LDAs
1 ODR
1 CCC

LDA - Link Data Agregator
DCC - Data Concentrator Card
DIF – Detector InterFace
ODR - Off Detector Receiver
CCC – Clock & Control Card

Problems found

- Weakness of HDMI connectors
- Weakness of serial protocol over HDMI cables. No feedback mechanism (no retransmission in case of error)
- Problems in the DIF to ASU connectors
- LDA & CCC boards instabilities, not standard size

DAQ used during last SDHCAL tests



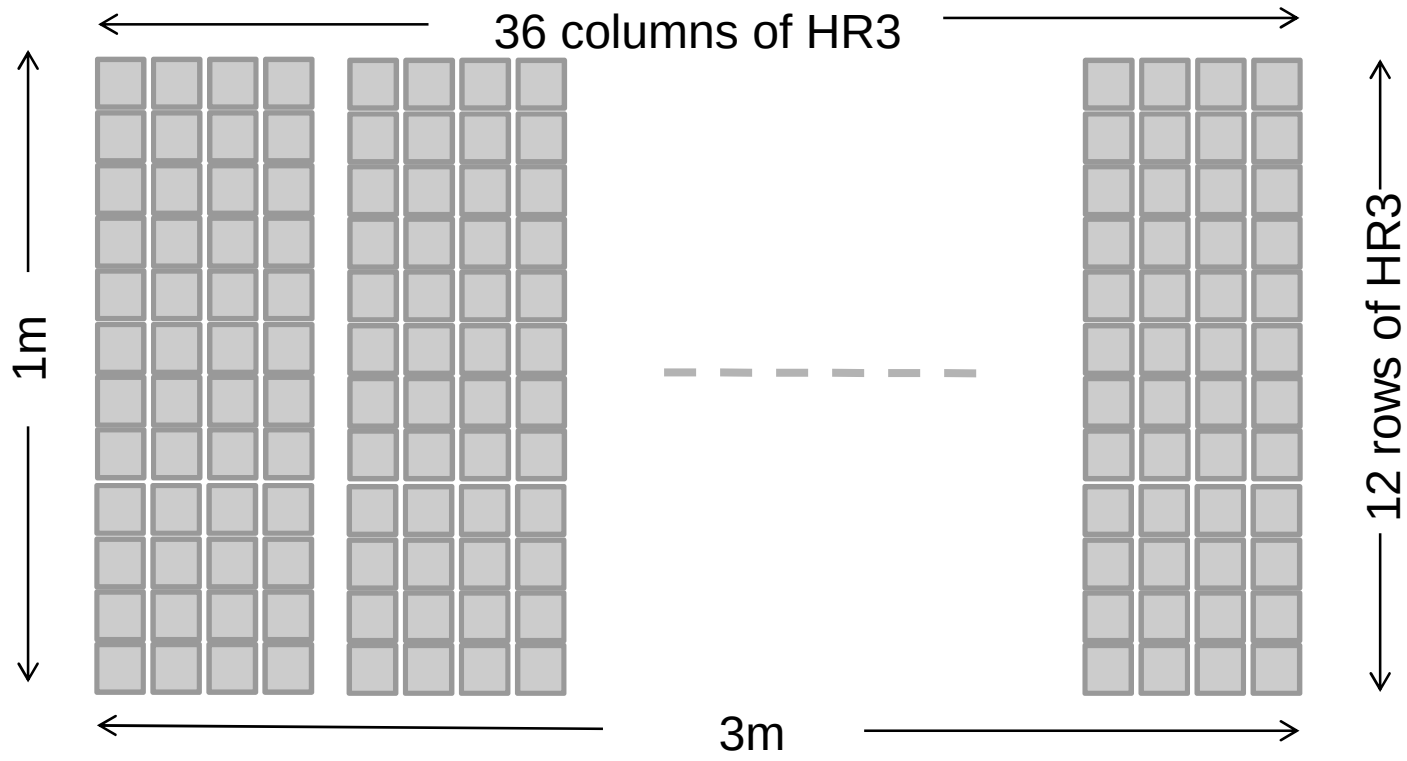
Simplified version of the original design:

- No LDA and CCC boards. All the concentration done with DCC
- Clock and synchronization using a modified version of the DCC
- USB used for data. Slow but more reliable than HDMI links.
- HDMI used only for clock and synchronization.

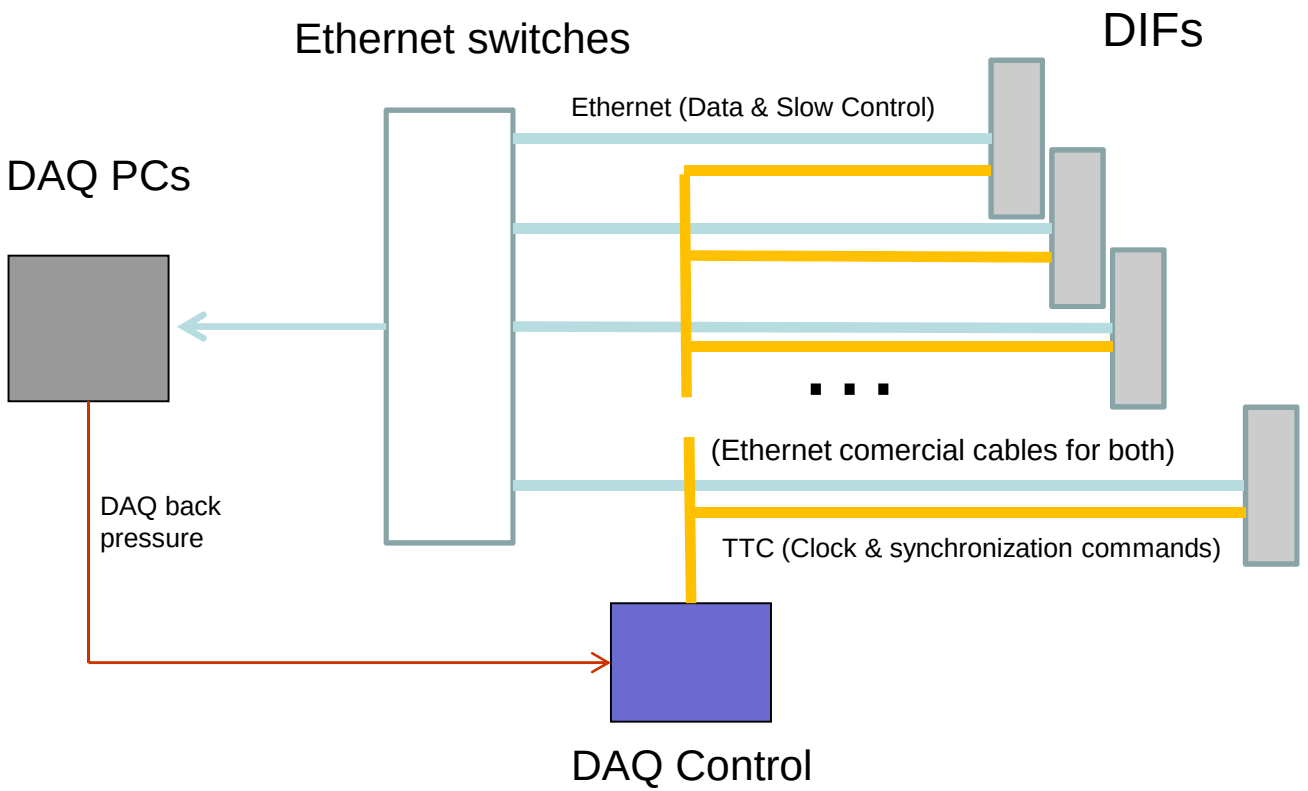
Next prototype

The aim of the next prototype is to test the feasibility of the longest detector cassettes (3m) from the mechanical and the electronics point of view.

From the electronics point of view the challenges are the high number of HR3 chips per plane: 432 (12 rows and 36 columns), the long PCB tracks and the connections between boards.



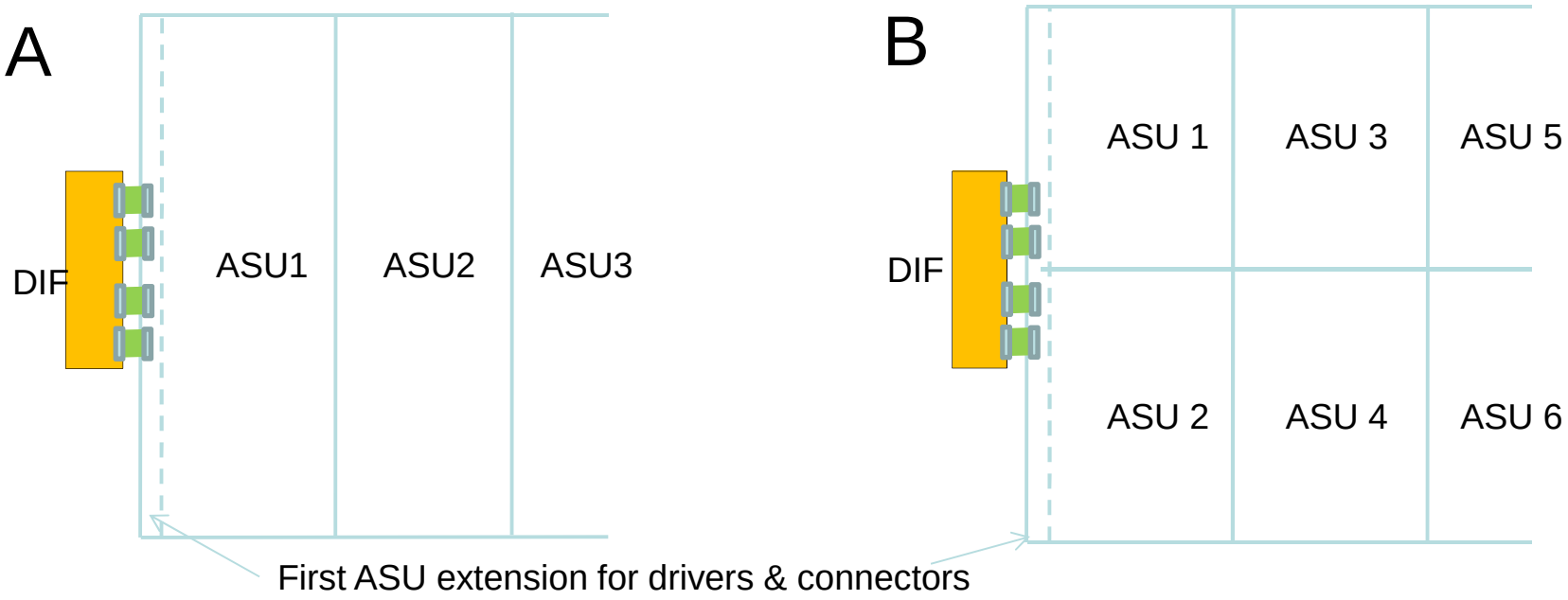
Next SDHCAL DAQ achitecture



- Only one DIF per plane (instead of three)
- Slow control & readout by Ethernet using commercial switches for concentration
- Clock and synchronization by the TTC system used in LHC experiments

New ASU layout options

As there will be only one DIF per plane, the distribution of the ASU boards in the plane could be rearranged to reduce the number of connections between the DIF and the plane

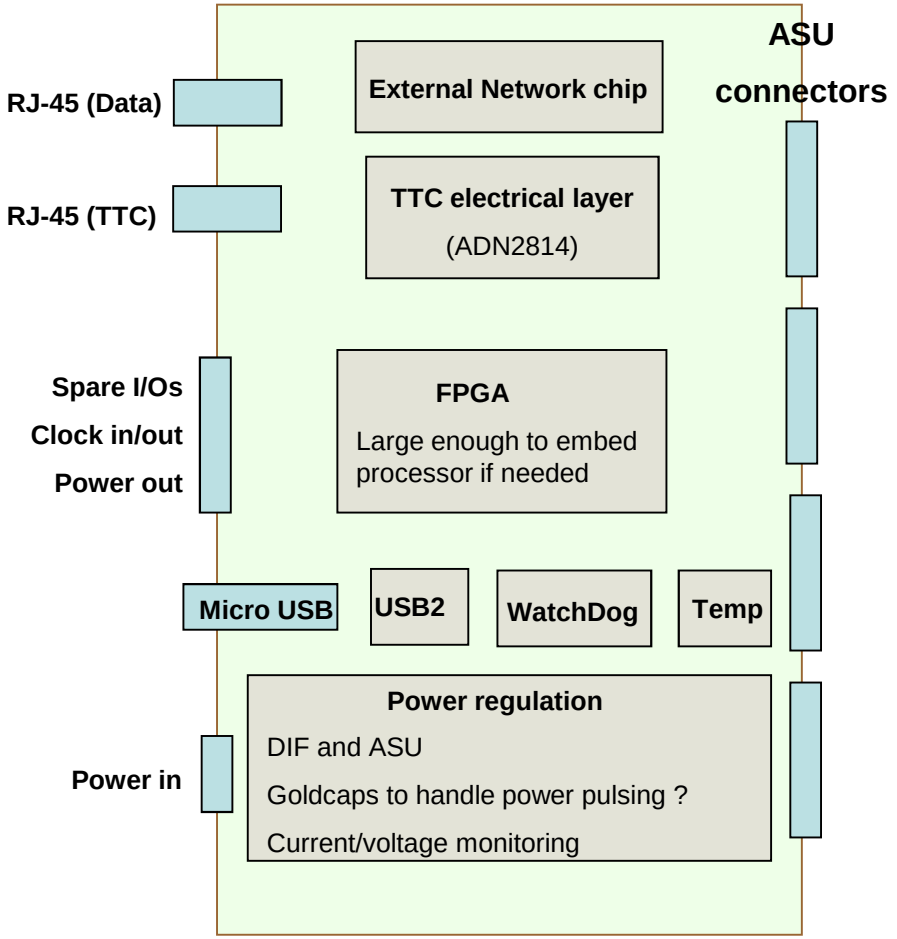


- Option A is more risky from the point of view of the feasibility of the 1m long ASU boards. But requires less pins on the connector as common signals can be sent only once

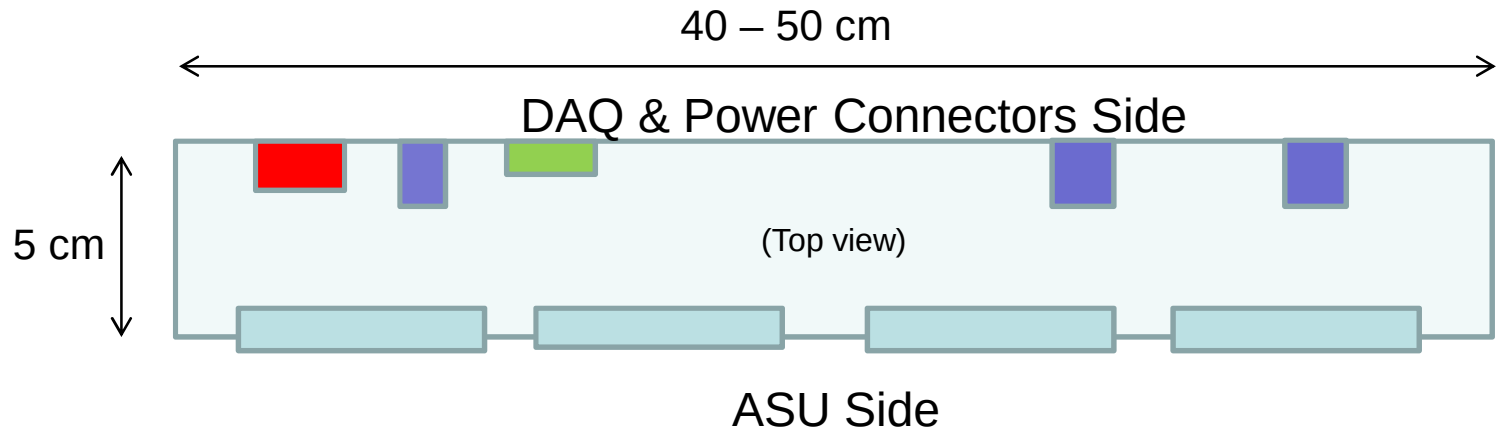
- In both options the ASUs connected to the DIF will be a bit longer to host the connectors and the buffers for driving the long lines.

New DIF main features

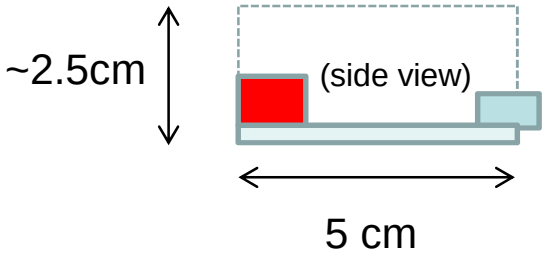
- Only one DIF per plane (instead of three)
  For the longest plane (1x3m) the DIF will handle 432 HR3 chips
- HR3 slow control through the new I2C bus
- Data transmission to/from DAQ by Ethernet using commercial switches for concentration
- Clock and synchronization by TTC
- USB 2.0 for debugging



DIF physical constrains



Max height for components



Our contribution

- We are responsible for the design, production and test of the new DIF board:
  - We have the commitment to have operational prototypes for the end of this year
  - We are finishing the design specification
  - Next month we will start the electronic design and VHDL coding in order to have a first prototype for this summer

- We are also participating in the design of the new DAQ and ASU as they are the interfaces of the DIF