IMB-CNM R&D Activities on Silicon Detectors for ILD

S. Hidalgo, P. Fernández-Martínez, M. Baselga, V. Greco, D. Quirion and G. Pellegrini

Centro Nacional de Microelectrónica (IMB-CNM-CSIC)
Barcelona, Spain

Outline

1) **Tracking Silicon Detectors with Internal Gain and Proportional Response**
   - ✓ PiN Detectors
   - ✓ Low Gain Avalanche Detectors (LGAD)

2) **Low Gain Avalanche Detectors**
   - ✓ Why Internal Gain?
   - ✓ Why Low Gain?
   - ✓ Linear Mode Operation. Gain Definition

3) **Pad Diodes with Internal Gain**
   - ✓ Multiplication Layer. Design considerations
   - ✓ Design of the Edge Termination. JTE Concept
   - ✓ Numerical Simulation of Irradiated Devices
   - ✓ Fabrication Process
   - ✓ Electrical and Technological Characterization
   - ✓ Experimental Results (Vbr, Ileak, Charge Collection Capabilities)
   - ✓ Irradiation Studies

4) **Low Gain Microstrips and Pixels Detectors**
   - ✓ Fabrication Process
   - ✓ Preliminary Electrical Performances

5) **Extension of the Low Gain concept to Thin Detectors**

6) **Target: Low Gain Thin Resistive MicroStrips and Pixels Detectors Fabrication**

Tracking Silicon Detectors with Internal Gain and Proportional Response

❑ **PiN** based Diodes

→ **Proportional Response**

→ **Good efficiency**

→ **Good spectral range**

→ **Segmentation is technologically available (strip and pixel detectors)**

Internal Gain →

❑ **Low Gain Avalanche Detectors (LGAD)**

→ **Proportional Response (Linear Mode Operation)**

→ **Good efficiency**

→ **Good spectral range**

✓ **Better Sensibility**

✓ **Thin detector integration with the same signal and higher collection efficiency**

✓ **Better signal/noise ratio**

→ **After Irradiation**

✗ **Worse signal to noise ratio (lower quality signal + noise increment)**

✗ **Increment of the power consumption**

✗ **Radiation Damage damage (specially relevant on n-on-p structures)**

→ **After Irradiation**

✓ **Similar pre & post irradiation signal (higher quality signal + lower noise increment)**

✓ **Lower increment of the power consumption**

✗ **Radiation Damage (specially relevant on n-on-p structures)**

Why Internal Gain?

❑ **Increases the radiation hardness of the detector, leading to similar signals before and after irradiation:**
  - ✓ **Charge multiplication off-sets the charge lost due to trapping during the drift of the carriers [1].**
  - ✓ **Higher electric fields reduce the collection times, reducing the trapping probability.**

❑ **Charge Collection Efficiency is improved, keeping a proportional response.**

❑ **Thinner detectors are available with the same signal. Fast detectors are also foreseen [1].**

❑ **The noise components are not increased at the same pace than the multiplied signal. As a consequence the signal to noise ratio is improved.**

Why Low Gain?

❑ **High Gain implies higher levels of multiplication noise (inherent to the stochastic process of multiplication [2]), spoiling the improvement of the Signal to Noise ratio.**

❑ **Collection times are increased with gain (more charge to be collected), increasing the trapping efficiency and avoiding the off-setting of the charge loss.**

❑ **Avoid cross-talk among adjacent pixels/strips.**

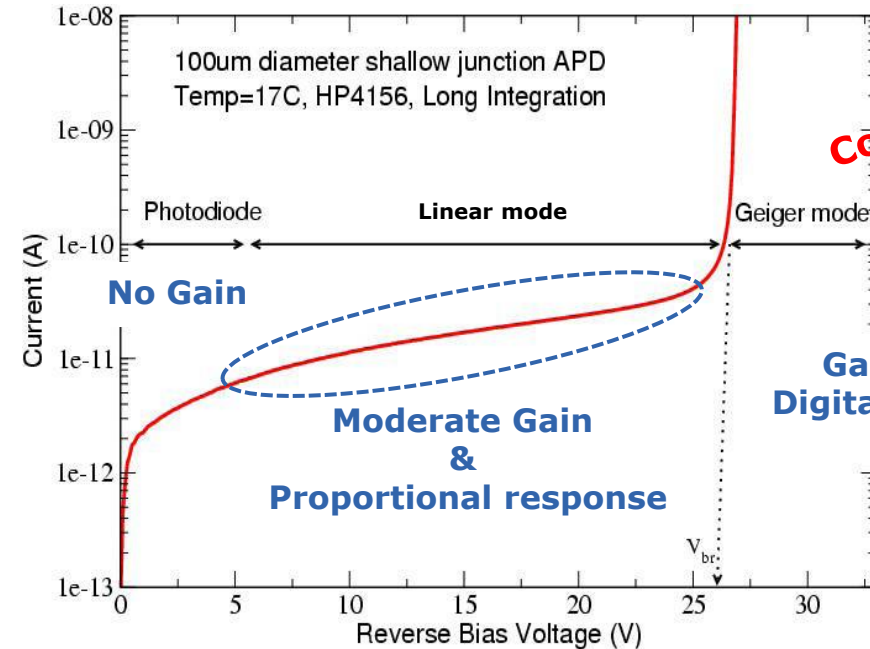[1] H. Sadrozinski, et al. 20th RD50 Workshop, Bari (Italy), 2012

[2] R.J. McIntyre. IEEE TED-13, No.1 p.164-168, 1966
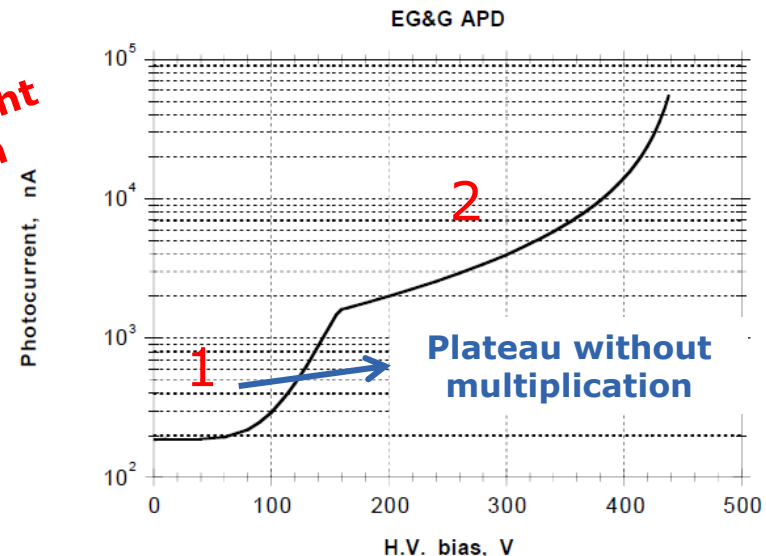
Linear Mode Operation. Gain Definition

❑ **Diodes with multiplication** can operate in Linear or Geiger mode

  ✓ **Linear** mode: Moderate gain & Proportional response

 ✓ **Geiger** mode: Very high gain & Digital response

Gain Definition

100um diameter shallow junction APD
Temp=17C, HP4156, Long Integration

Photodiode — Linear mode — Geiger mode

No Gain

Moderate Gain & Proportional response

Gain > 10⁴ Digital response

V_{br}

Reverse Bias Voltage (V)

Current (A)

Continuous light illumination

EG&G APD

2

1

Plateau without multiplication

Photocurrent, nA

H.V. bias, V

[1] A.G. Stewart et al. in Proc. of SPIE, Vol. 6119, 2006

I. Tapan ,et al. NIMA 388 (1997) 79-90: "The plateau for low bias voltage may be taken to correspond to unit gain […] and the gain for higher bias measured simply as the ratio of the pulse size to that plateau"

Pad Diodes with internal Gain

❑ **M. Bruzzi, IEEE TNS-48(4) 2001: "The general approach followed by the HEP community in radiation–damage studies has been to investigate the radiation effects in silicon detectors using the simplified geometry of a single pad detector."**

N^+ cathode

5 mm

300 µm

P-type (π)substrate

P^+ anode

Pad Diodes with internal Gain

❑ **M. Bruzzi, IEEE TNS-48(4) 2001: "The general approach followed by the HEP community in radiation–damage studies has been to investigate the radiation effects in silicon detectors using the simplified geometry of a** single pad detector**."**

N+ cathode

5 mm

300 µm

P-type multiplication layer

P-type (π)substrate

P+ anode
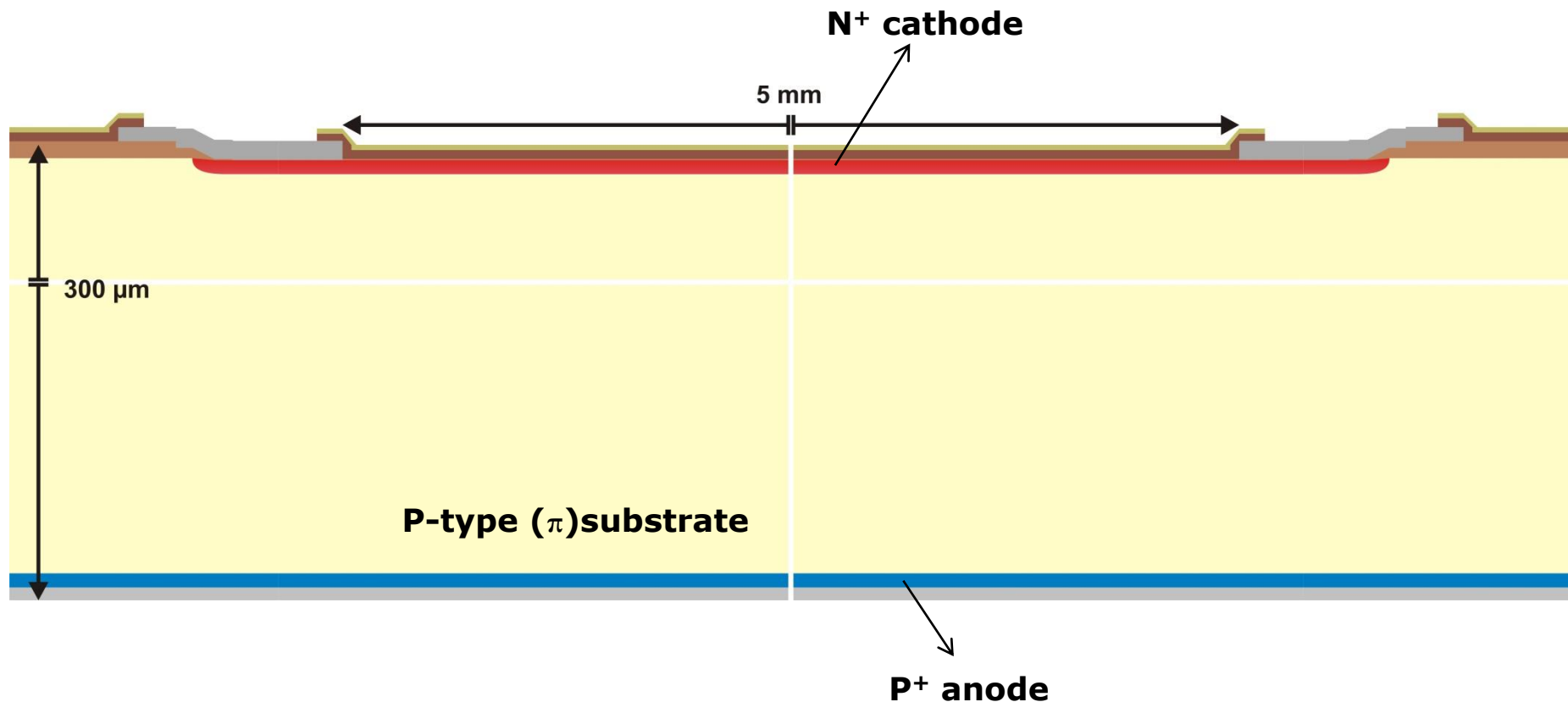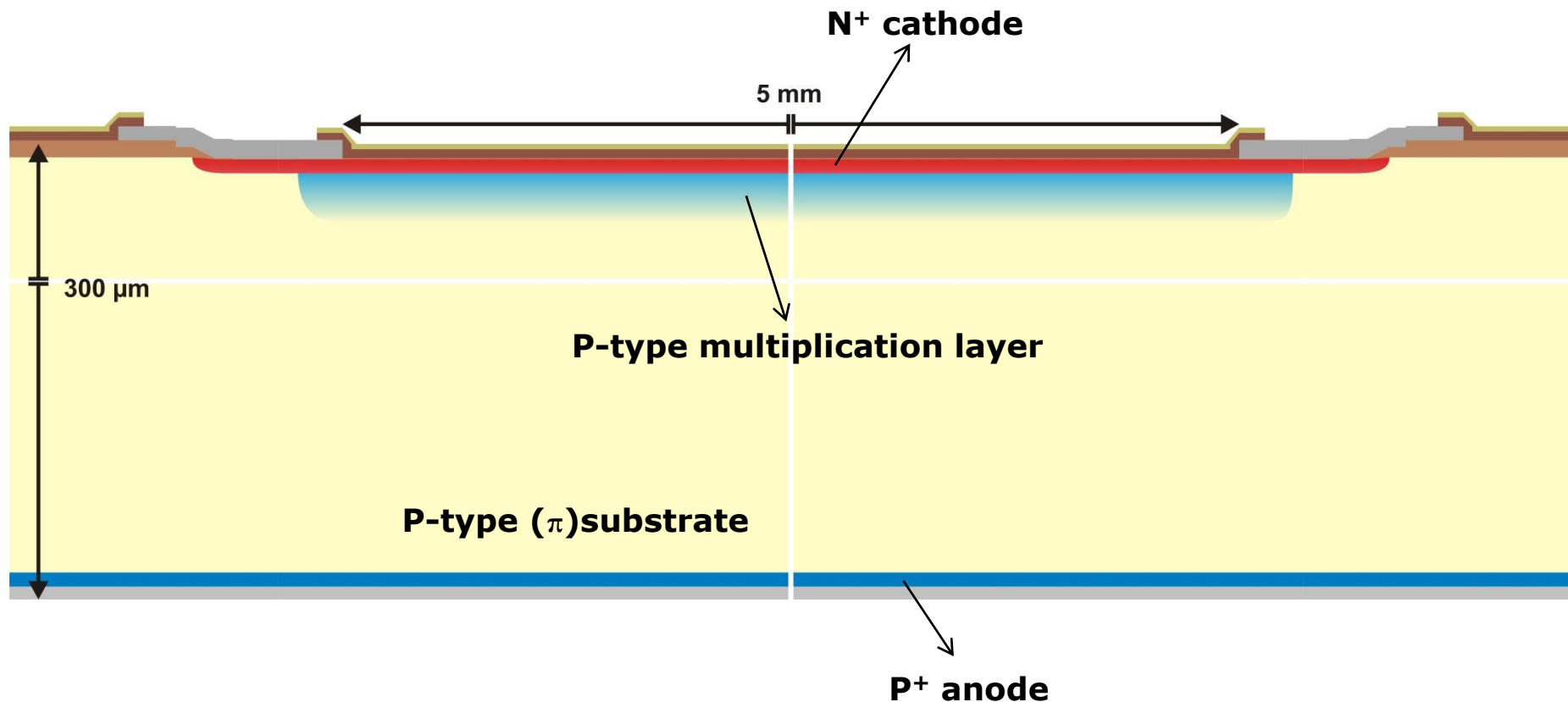
Design of the Multiplication Region

Gain/V_{BD} trade-off

✓ If implant dose increases:
  - Gain increases
  - V_{BD} decreases

❑ **Technological adjust of the multiplication region p-layer becomes critical**

1D Simulation @ Pad Centre

- Gain @ 200 V
- Gain @ 400 V
- Gain @ 500 V
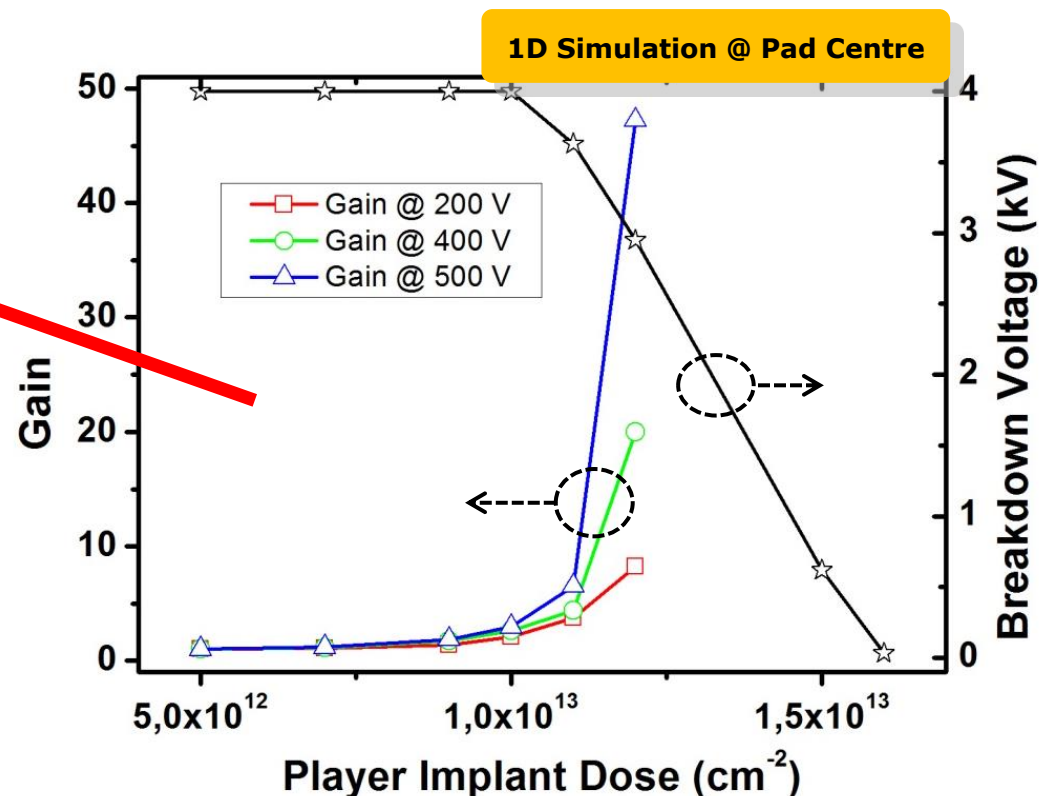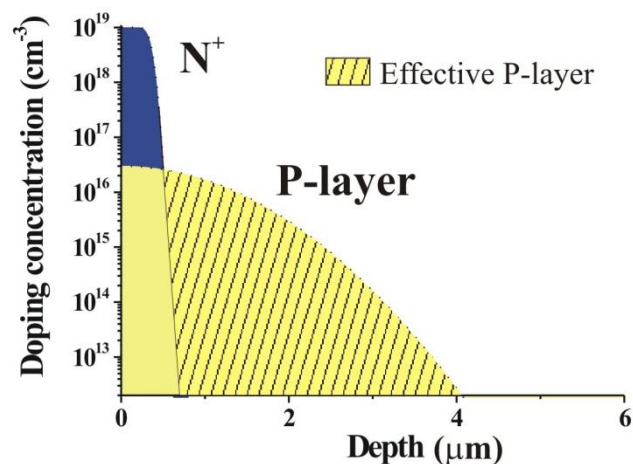
Small modifications in the Boron implant dose (~ 2 × 10¹² cm⁻²) induce great changes in Gain and V_{BD}

Design of the Edge Termination

Planar and uniform electric field distribution, high enough to activate charge multiplication
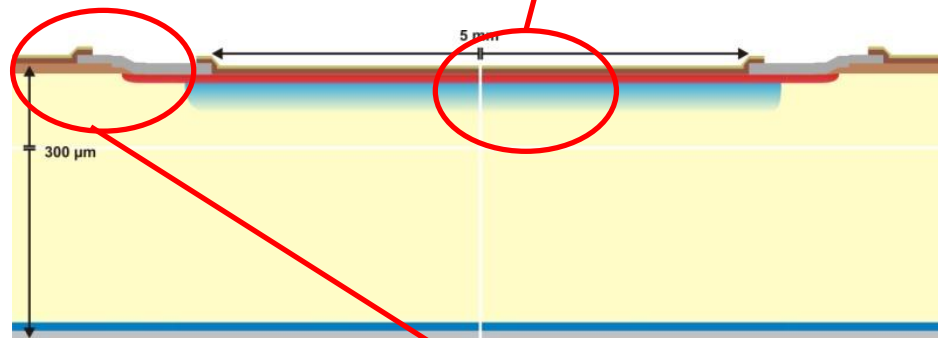
Electric Field @ 400 V
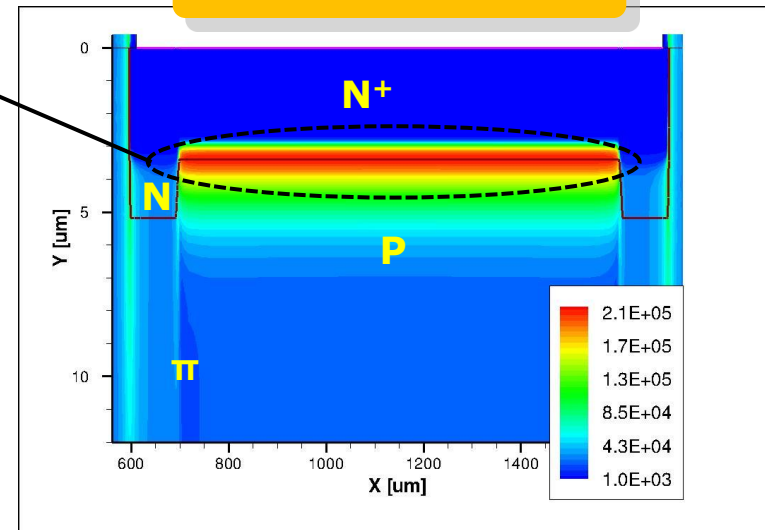
$$V_{BD}|_{Central} \ll V_{BD}|_{Termination}$$
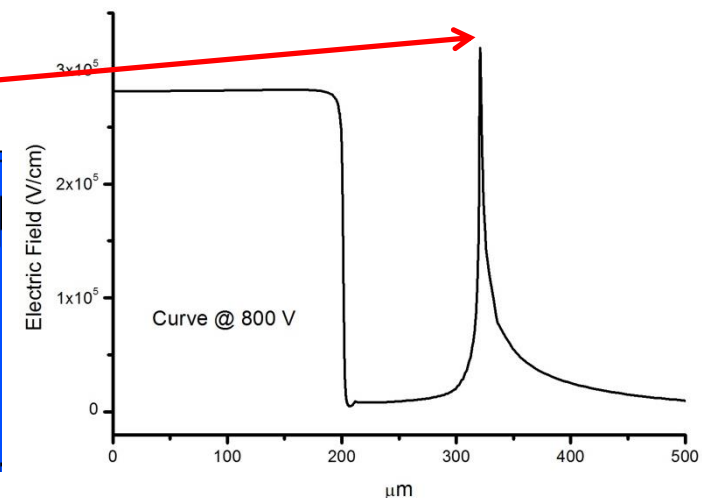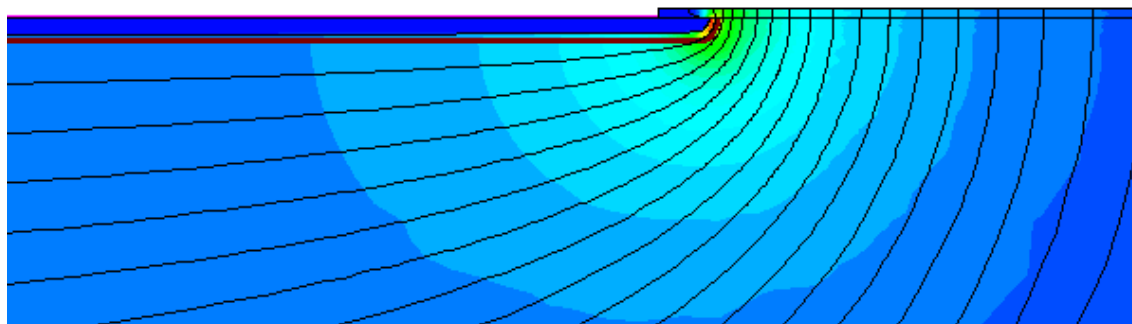
Design of the Edge Termination

- ❑ **Junction Termination Extension** (JTE). Peripheral low doping N-well to increase the voltage capability of this area, reducing the Electric Field in the periphery, allowing the maximum Electric Field is reached in the multiplication area (N^+/P junction)

N^+ cathode

5 mm

300 µm

P-type multiplication layer

JTE

P-type (π)substrate

P^+ anode
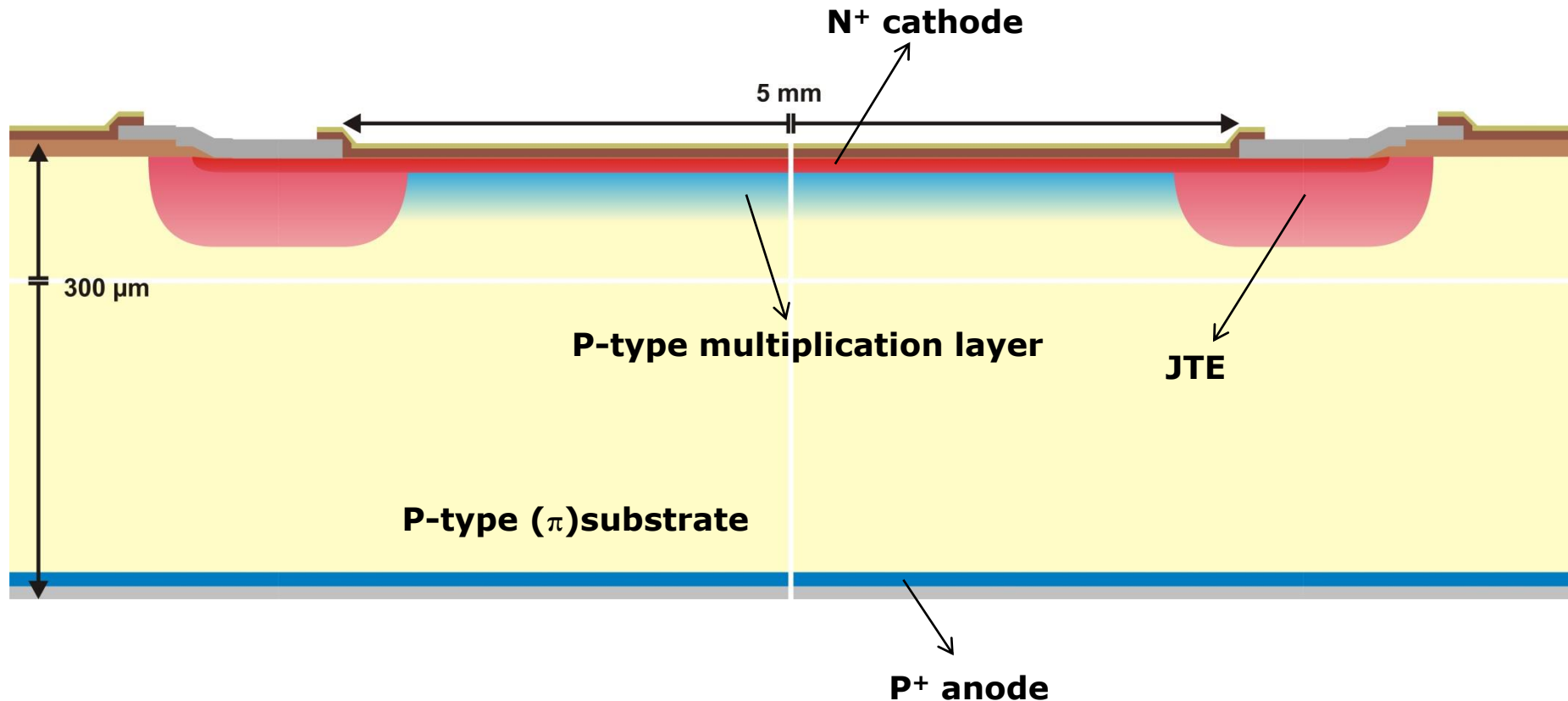
TABLE 3.1. High-Voltage Device Termination Techniques

Technique	Typical Breakdown Voltage (%)[a]	Peak Surface Electric Field (%)[b]	Typical Device Size	Device Types	Remarks
Planar junction	50	80	Small (<100 mils)	BJT, MOSFET	Seldom used for high-voltage devices
Planar junction with field ring	80	80	Medium (≤1 in.)	BJT, MOSFET, SCR	Well suited for a large number of devices per wafer
Planar junction with field plate	60	80	Medium (≤1 in.)	BJT, MOSFET	Usually used in conjunction with field ring
Positive bevel	100	50	Large (>1 in.)	Rectifier, SCR	Well suited for single device per wafer
Negative bevel	90	60	Large (>1 in.)	SCR	Well suited for single device per wafer
Double positive bevel	100	80	Large (>1 in.)	SCR	Well suited for single device per wafer only
Positive etch contour	90	60	All	BJT, MOSFET, SCR	Well suited for a large number of devices per wafer
Negative etch contour	80	60	All	BJT, MOSFET, SCR	Well suited for a large number of devices per wafer
Junction termination extension	95	80	All	BJT, MOSFET, SCR	Well suited for both single devices and a large number of devices per wafer; high leakage current; passivation sensitive

[a] As percentage of parallel-plane case.
[b] As percentage of bulk.
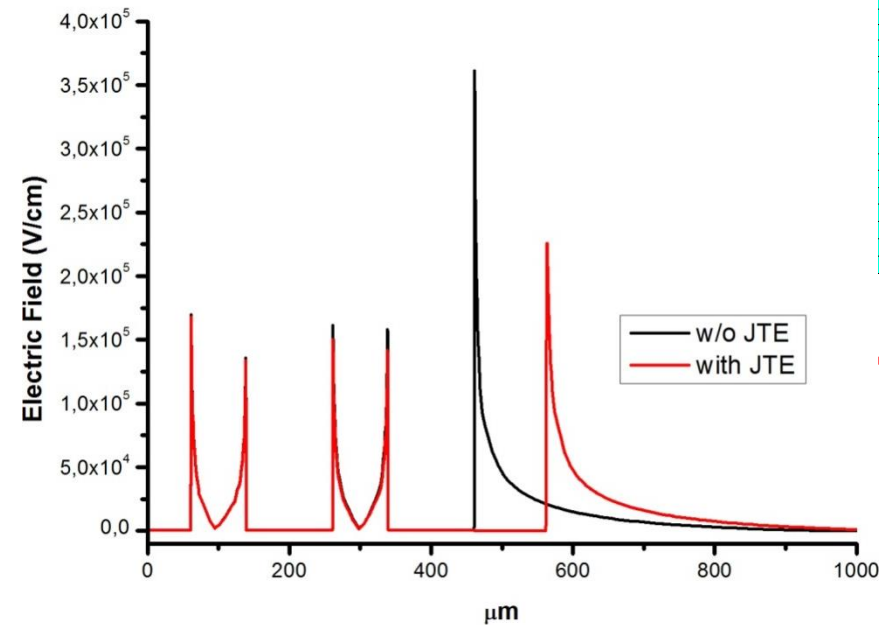
Design of the Edge Termination

PiN Diode

PiN Diode with JTE

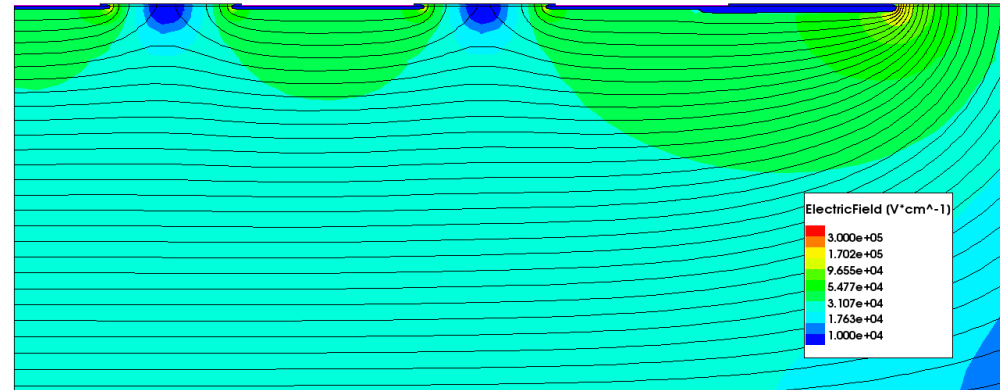V_{BD} increases from 800 V to 1200 V
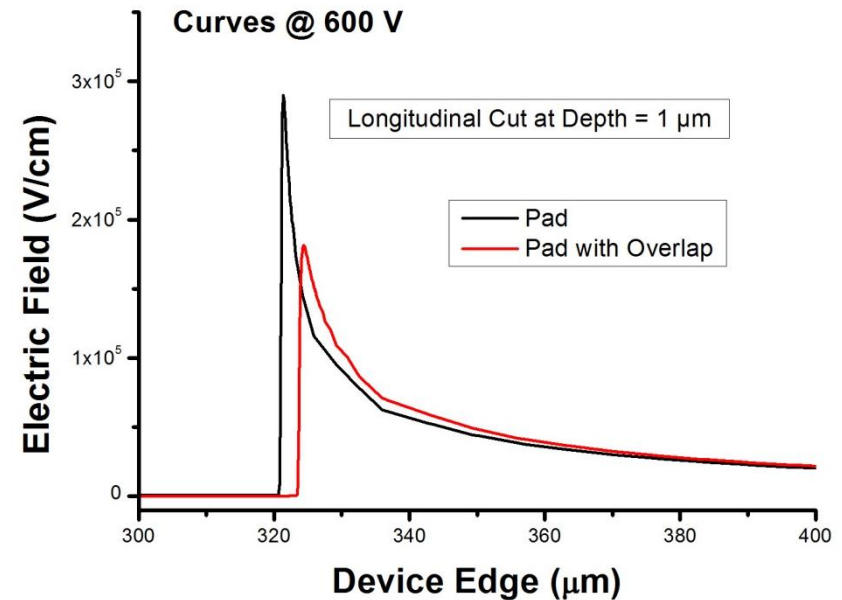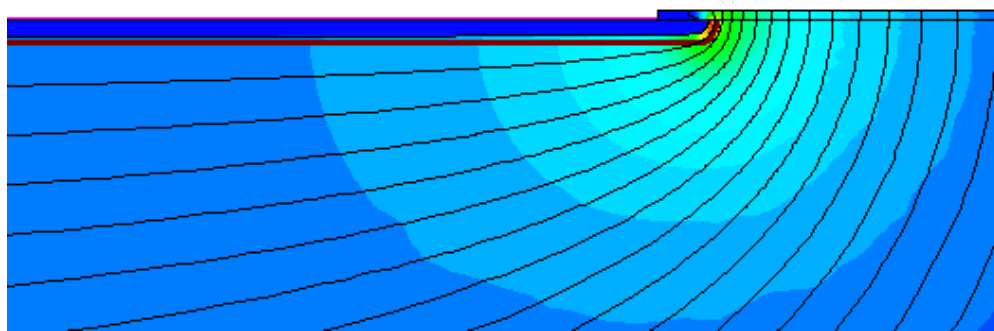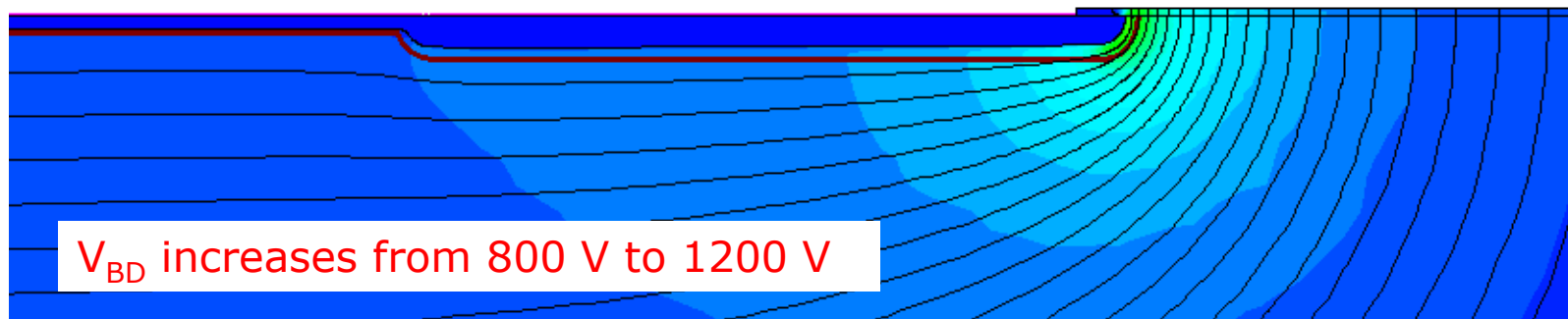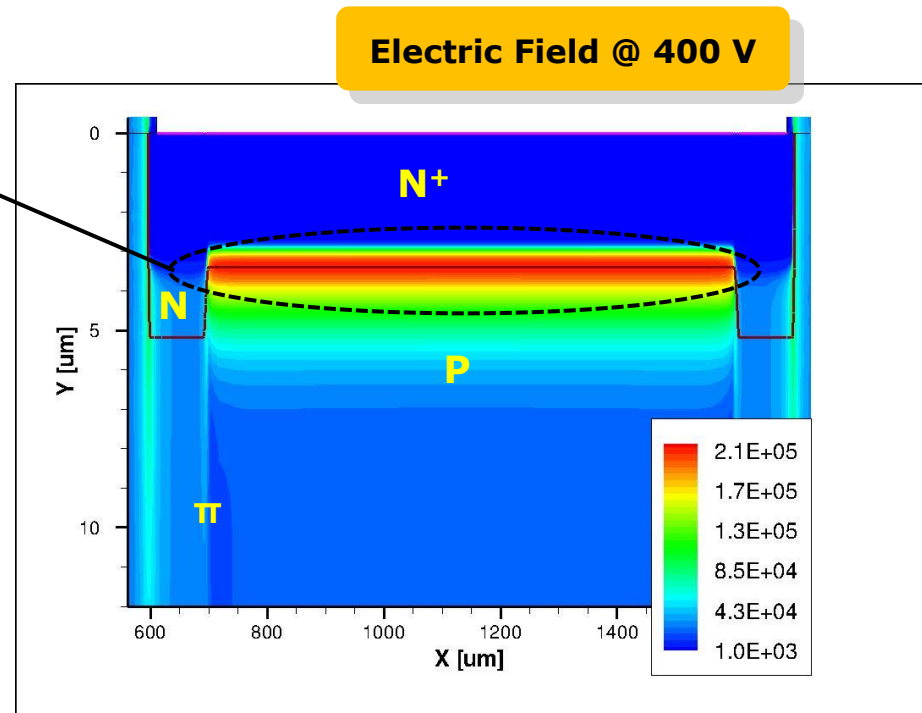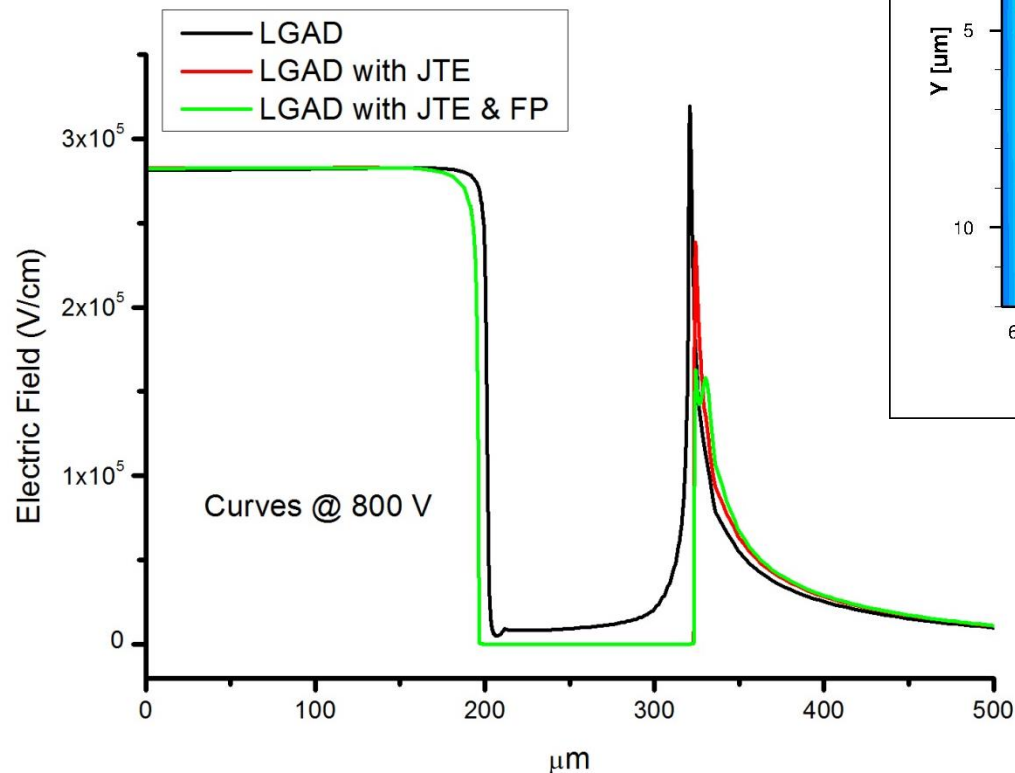
Strip Detectors Edge Termination
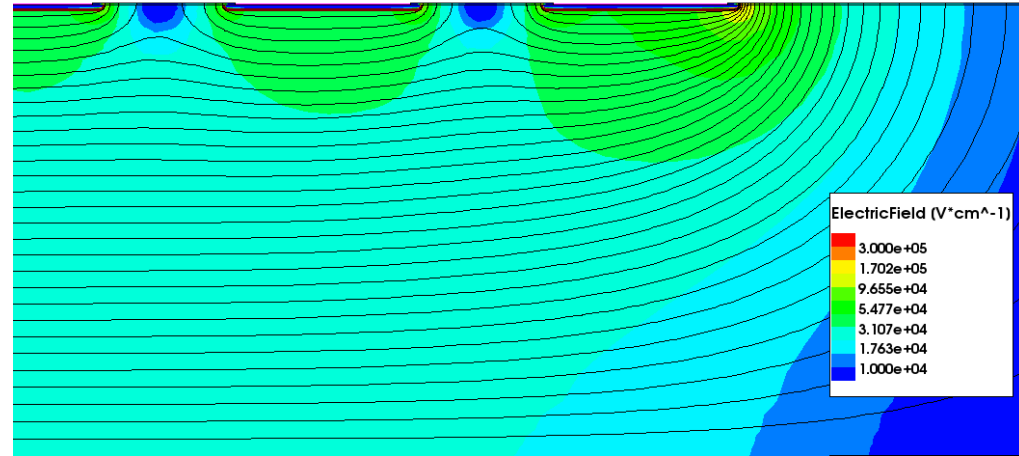
Micro Strip Diode

Micro Strip Diode with JTE

Design of the Edge Termination

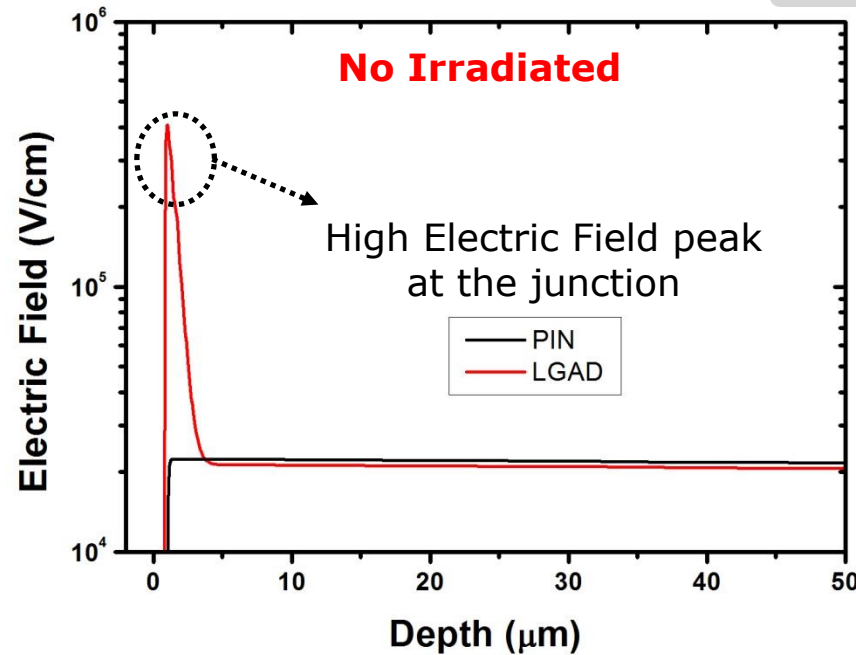Planar and uniform electric field distribution, high enough to activate charge multiplication

Electric Field @ 400 V

$$V_{BD}|_{Central} \ll V_{BD}|_{Termination}$$

Simulation of the Irradiated Devices

Curves @ 600 V

No Irradiated

High Electric Field peak at the junction

Irradiated. $\Phi_{eq} = 1 \times 10^{15}$
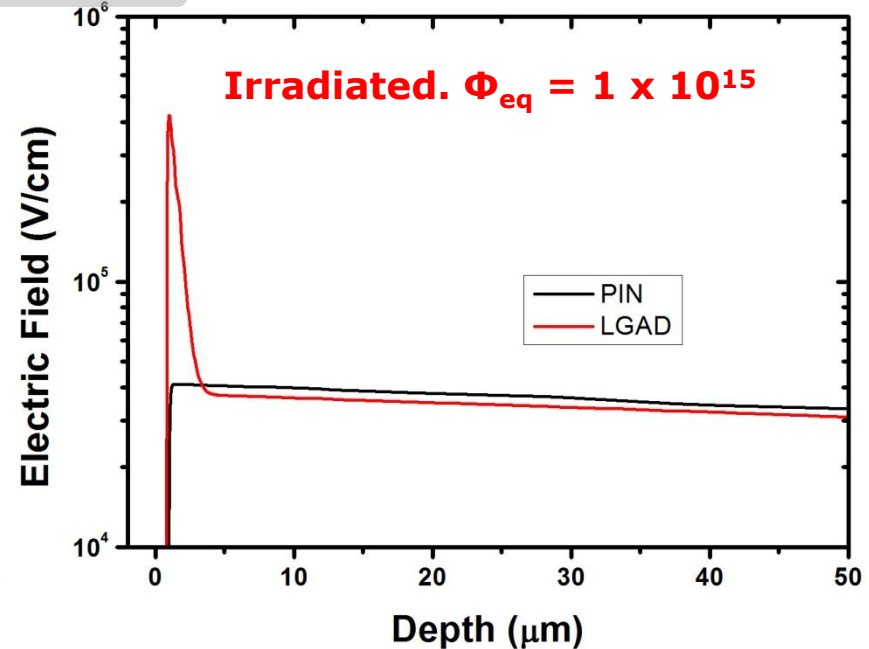
- **PiN**: electric field strength at the junction increases after irradiation

- **LGAD**: electric field strength at the junction is held after irradiation

- **Irradiation Trap Model (Perugia Model):**

Acceptor; E= E_c + 0.46 eV; η=0.9; σ_e = 5 x 10^{-15}; σ_h = 5 x 10^{-14}

Acceptor; E= E_c + 0.42 eV; η=1.613; σ_e = 2 x 10^{-15}; σ_h = 2 x 10^{-14}

Acceptor; E= E_c + 0.10 eV; η=100; σ_e = 2 x 10^{-15}; σ_h = 2.5 x 10^{-15}

Donor;   E= E_v - 0.36 eV; η=0.9; σ_e = 2.5 x 10^{-14}; σ_h = 2.5 x 10^{-15}

▪**Impact Ionization Model:**

Universty of Bolonia

$$Conc = \eta \cdot \phi$$

Simulation of the Irradiated Devices

Numerical Simulations   LGAD Wafer 8   **Experimental Measurements**

W8-H11 (Sr90 signal)
80 min at 60C annealing
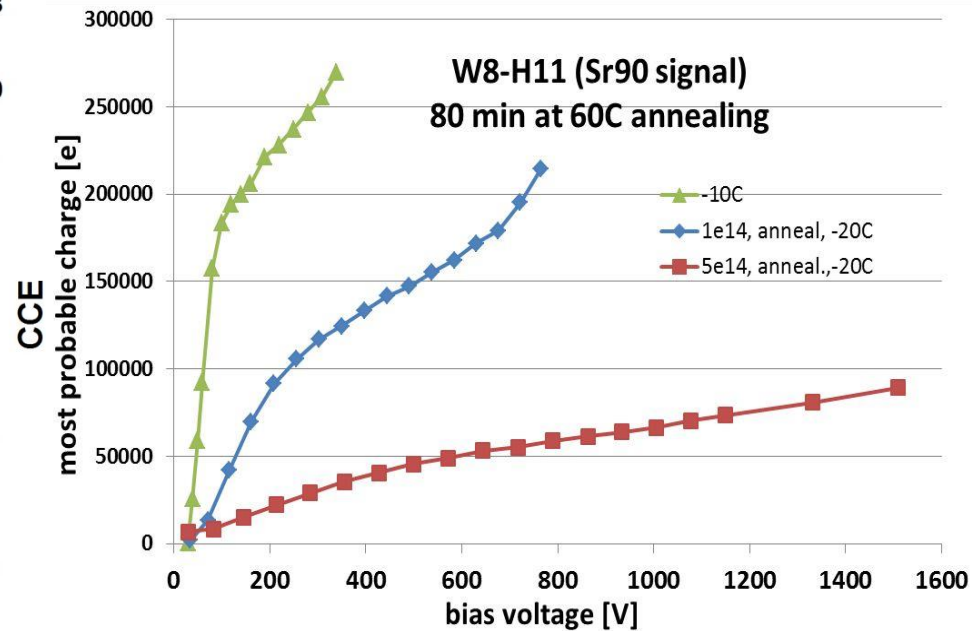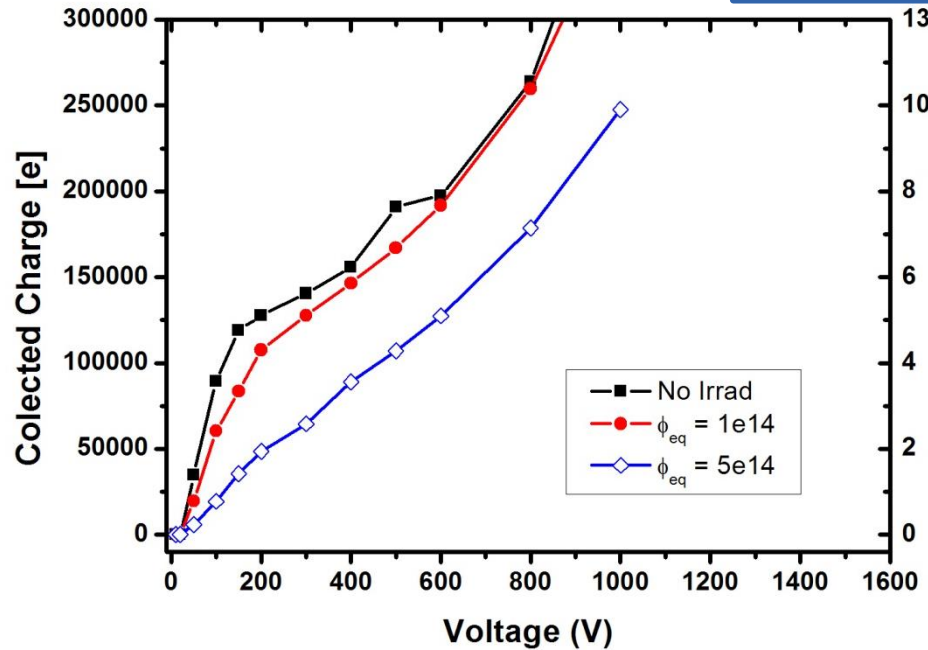
CCE @ 400 V

Φ_{eq} [cm^{-2}]	Simulated	Measured
No Irrad	7	10
1e14	6	6
5e14	3	2

See G. Kramberger at RD50 Albuquerque

First estimation by simulation. We must work to enhance this study
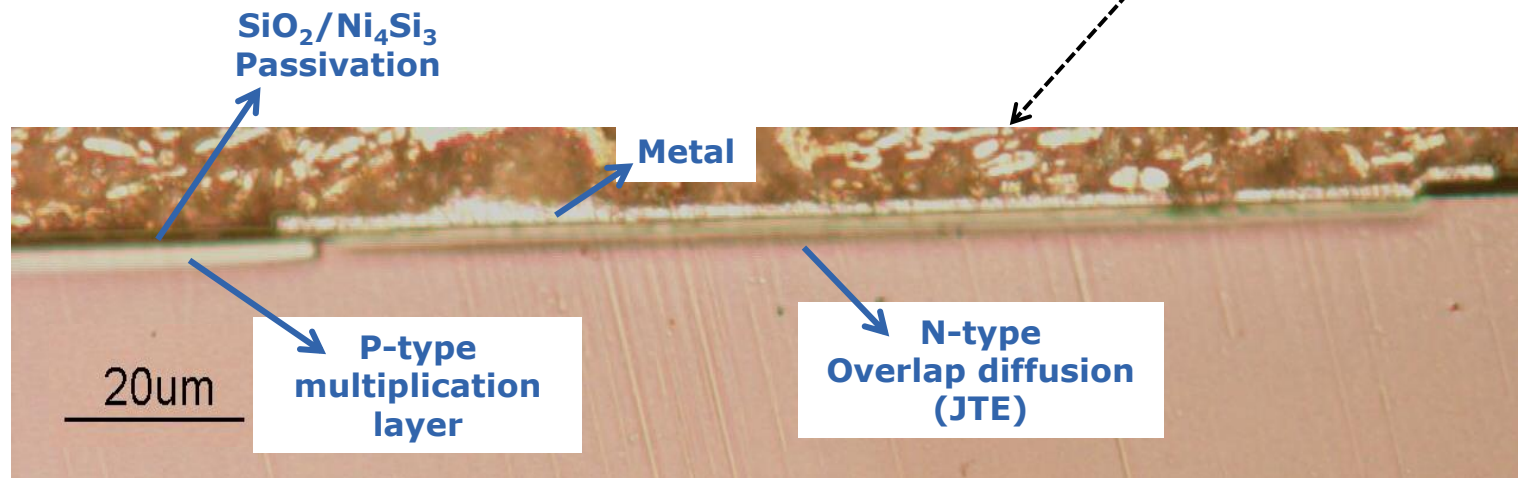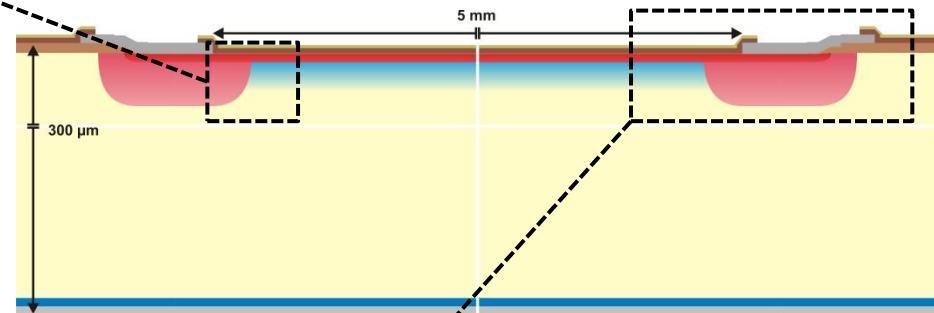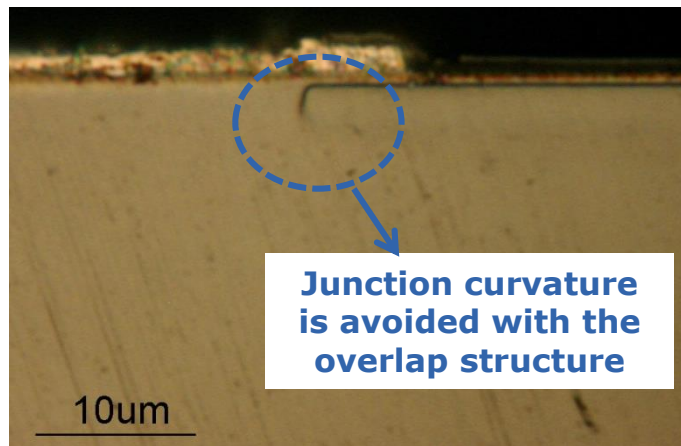
Fabrication (I)

4 Devices per dice

Channel Stopper

Collector Ring
(metallized)
(width=120 μm)

Optical window
(passivated)

5000 μm

1000 μm

Electrical test
structures

Overlap (metallized)
(width=120 μm)
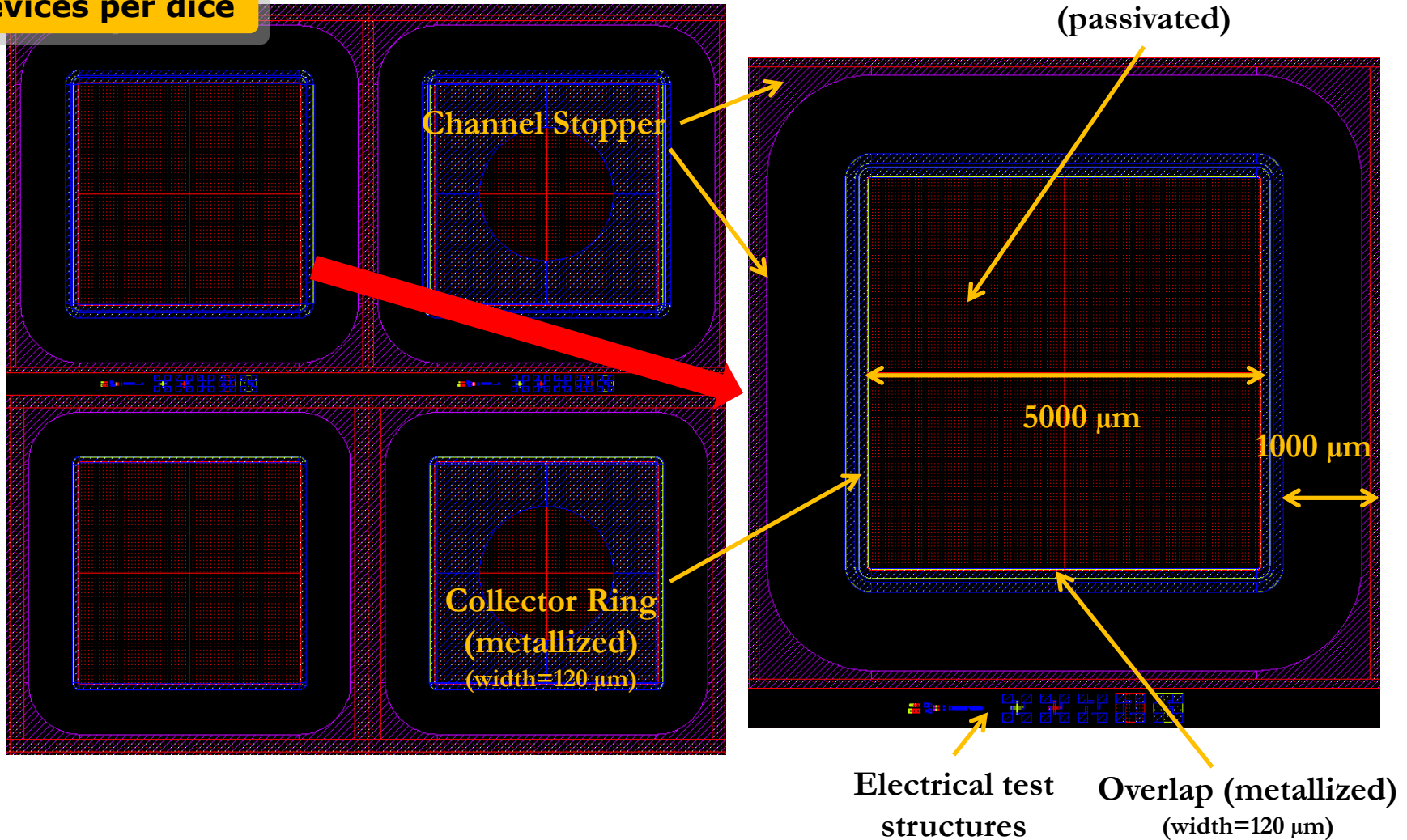
Fabrication (II)

Wafer Number	P-layer Implant (E = 100 keV)	Substrate features
1	1.0×10^{13} cm^{-2}	HRP 300 (FZ; ρ>10 KΩ·cm; <100>; T = 300±10 µm)
2	1.1×10^{13} cm^{-2}	HRP 300 (FZ; ρ>10 KΩ·cm; <100>; T = 300±10 µm)
3	1.2×10^{13} cm^{-2}	HRP 300 (FZ; ρ>10 KΩ·cm; <100>; T = 300±10 µm)
4	1.3×10^{13} cm^{-2}	HRP 300 (FZ; ρ>10 KΩ·cm; <100>; T = 300±10 µm)
5	1.4×10^{13} cm^{-2}	HRP 300 (FZ; ρ>10 KΩ·cm; <100>; T = 300±10 µm)
6	1.5×10^{13} cm^{-2}	HRP 300 (FZ; ρ>10 KΩ·cm; <100>; T = 300±10 µm)
7	1.6×10^{13} cm^{-2}	HRP 300 (FZ; ρ>10 KΩ·cm; <100>; T = 300±10 µm)
8	2.0×10^{13} cm^{-2}	HRP 300 (FZ; ρ>10 KΩ·cm; <100>; T = 300±10 µm)
9	----- (PIN wafer)	HRP 300 (FZ; ρ>10 KΩ·cm; <100>; T = 300±10 µm)
10	1.1×10^{13} cm^{-2}	HRP OXG (DOFZ; ρ = 5-15 KΩ·cm; <100>; T = 285±25 µm)
11	1.3×10^{13} cm^{-2}	HRP OXG (DOFZ; ρ = 5-15 KΩ·cm; <100>; T = 285±25 µm)

Technological Characterization

Junction curvature is avoided with the overlap structure

10um

5 mm

300 µm

SiO$_2$/Ni$_4$Si$_3$ Passivation
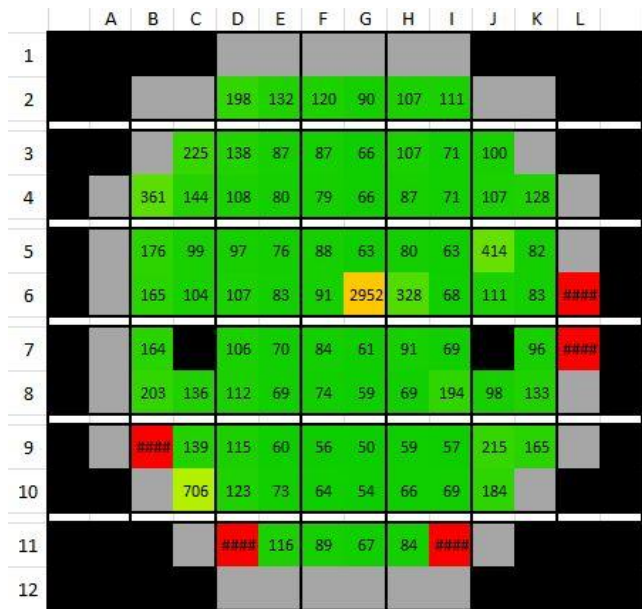
Metal

P-type multiplication layer

N-type Overlap diffusion (JTE)

20um
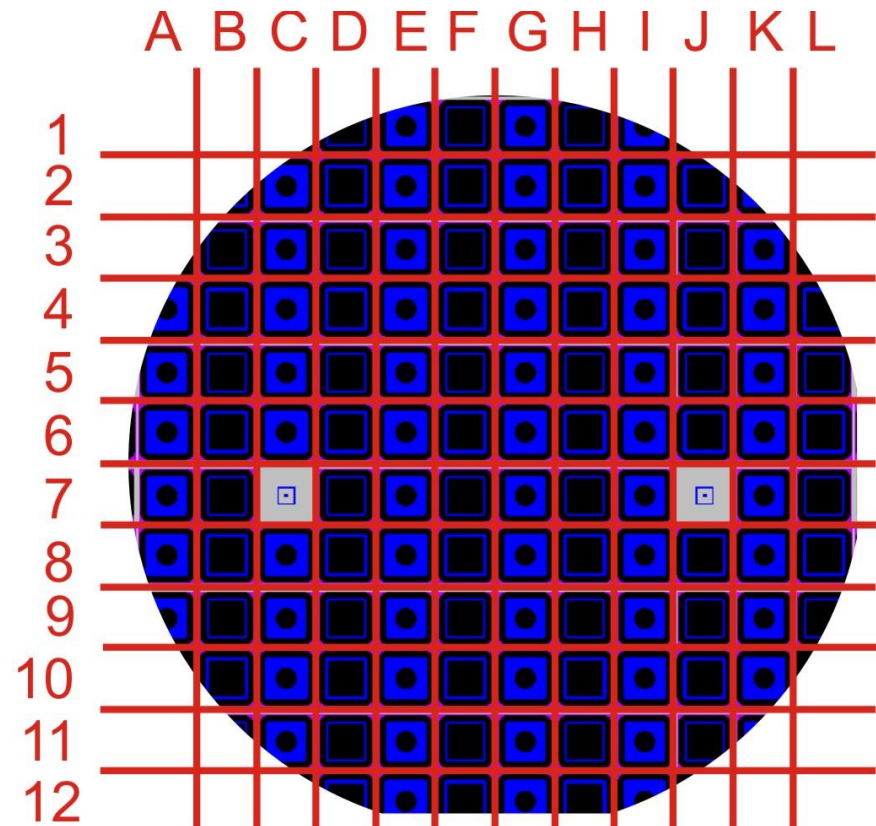
Electrical Characterization

❑ **Fabrication yield worsens with increasing implant dose for the p-type multiplication layer.**

Measured Current [nA] at 200 V

[100 nA]   [1µA]   [10 µA]

Wafers were fabricated in the same run, following exactly the same fabrcation steps. Only difference between W9 and W8 is that PiN wafer was not implanted with the multiplication implantation.

PiN Wafer (W9)
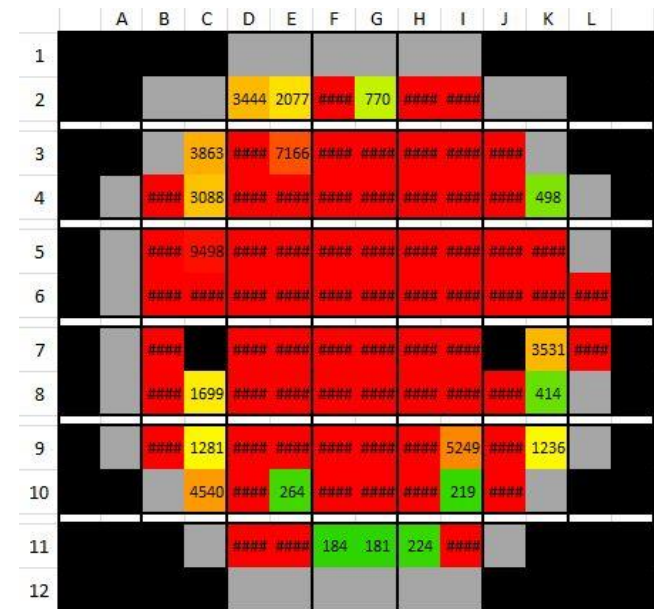
Wafer 8 (Implant dose = 2×10^{13} cm^{-2})

We are working in the yield improvement

Experimental Results (I)

✓ **"Good" Devices**

→ **Current levels below 1 µA thorough the whole voltage range**

→ **Junction breakdown above 1100 V (*Except Wafer 8: < 800 V, still good)**

Wafer 5 (1.4×10^{13} cm^{-2})

W5_F11

Junction breakdown above 1100 V

Current level (~ few hundreds of nA)
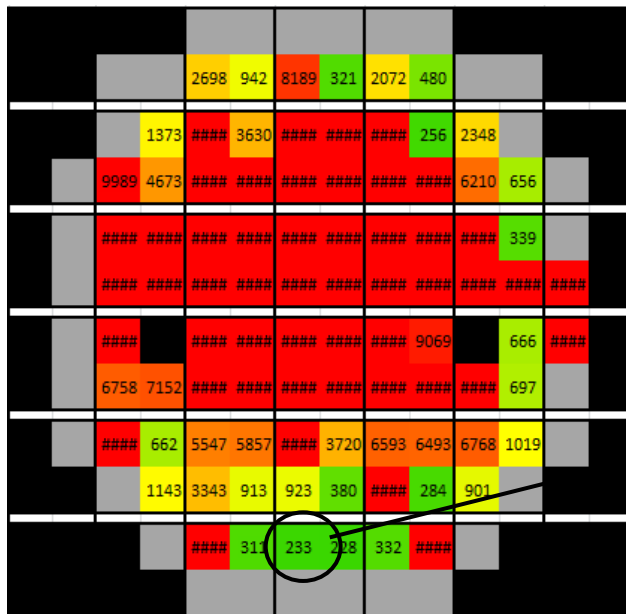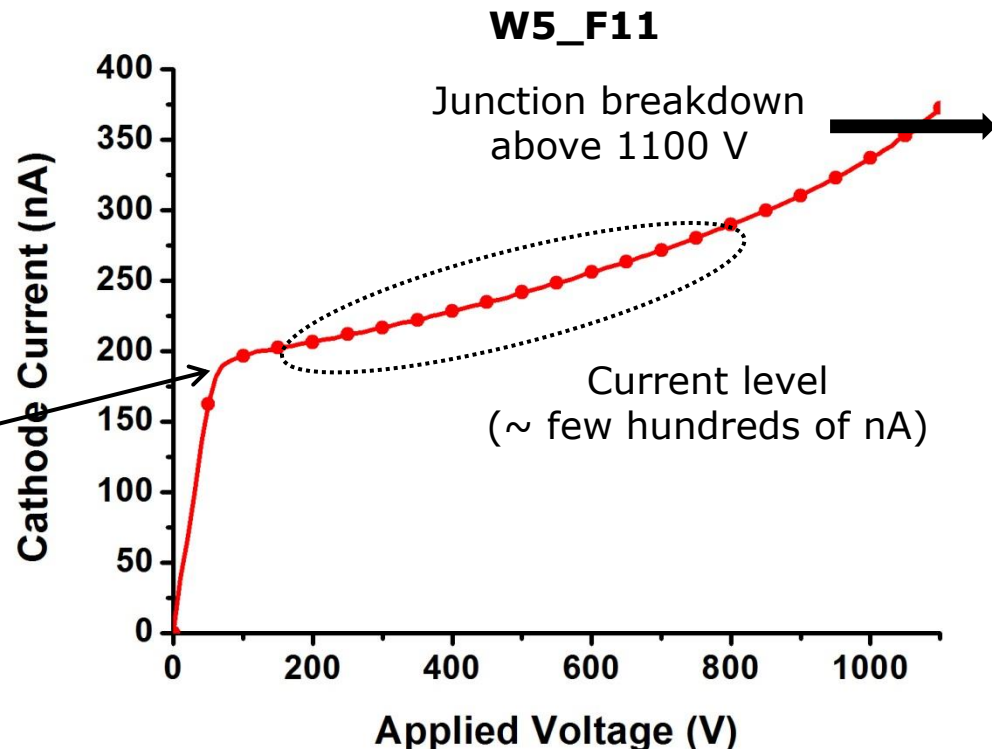
Experimental Results (II)

✖ "Bad" Devices

→ **Current levels above 1 µA thorough the whole voltage range**

→ **Junction breakdown above 1100 V (*Except Wafer 8)**
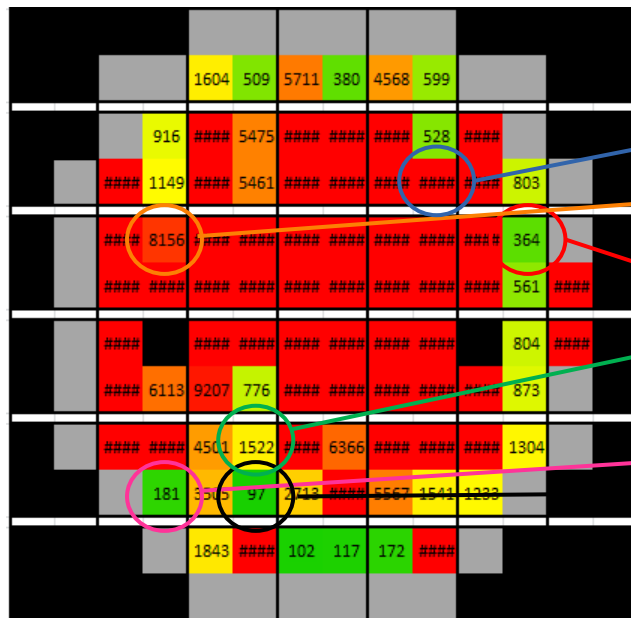
Wafer 6 (1.5×10^{13} cm^{-2})
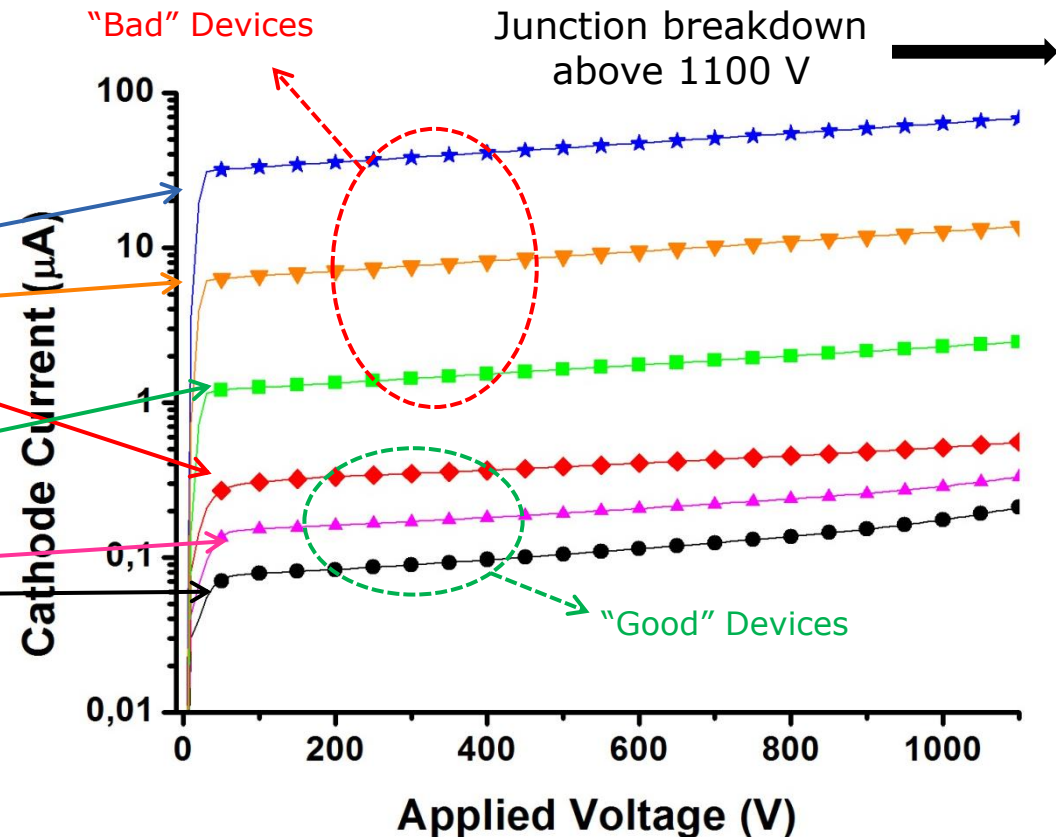
Charge Collection (Alpha)

☐ **Multiplication factor has been tested with tri-alpha (^{239}Pu/^{241}Am/^{244}Cm) source.**

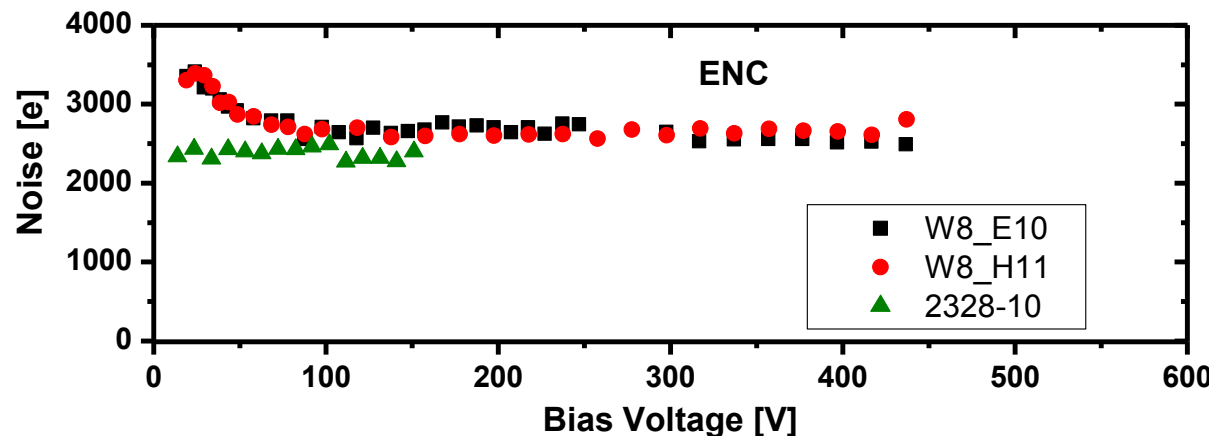→ **Irradiation through the anode (back side, 1 µm Aluminum):**

$$Gain_{@V} = \frac{Channel\ Central\ peak_{@V}}{Channel\ Central\ peak_{No\ multiplied}}$$
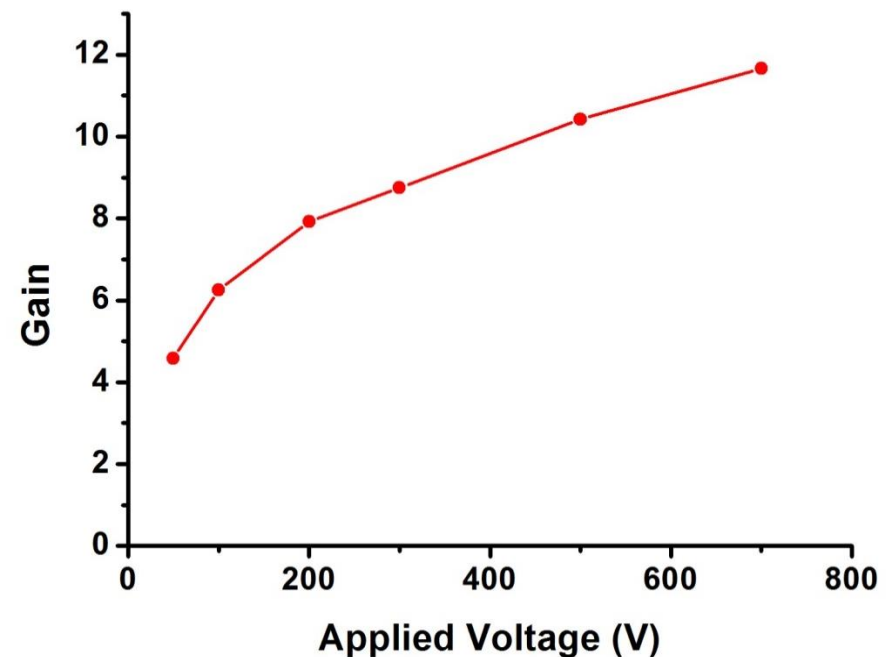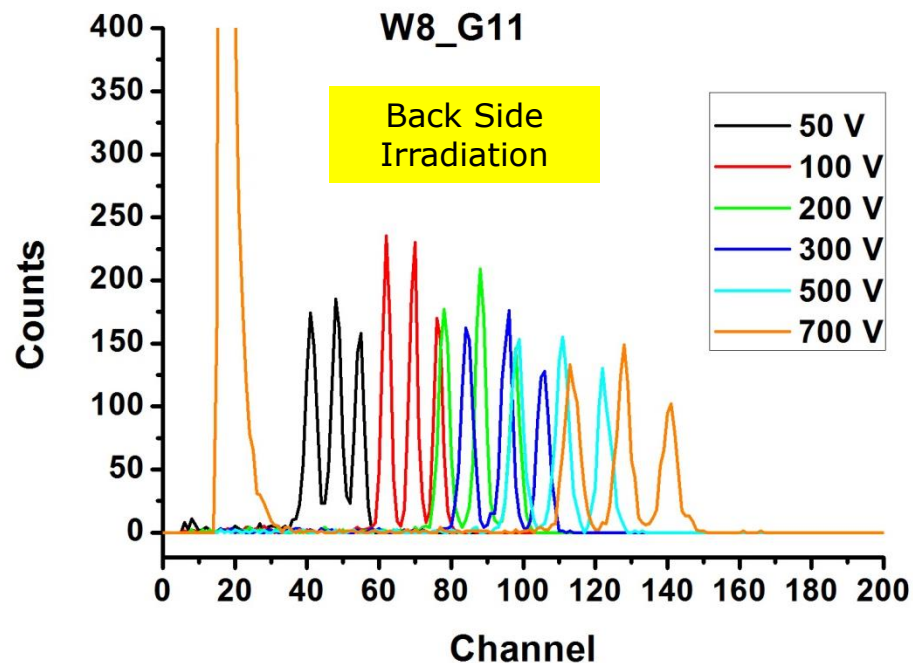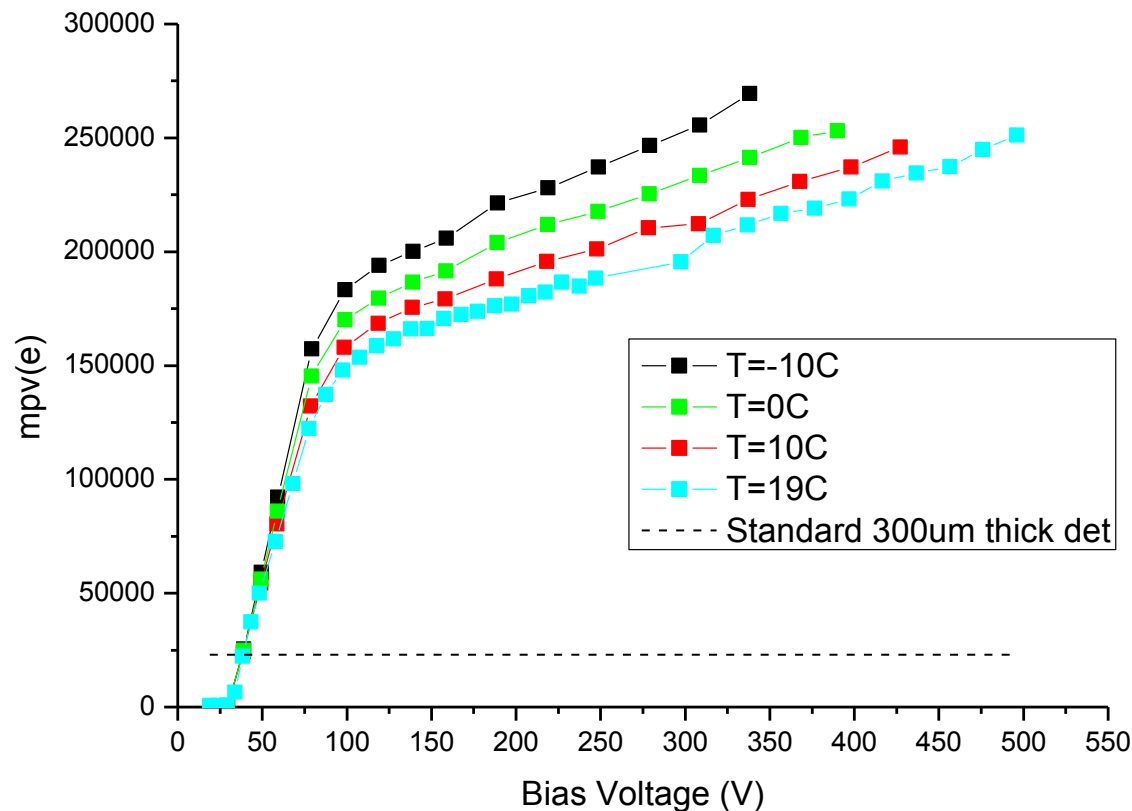
Charge Collection (Mips)
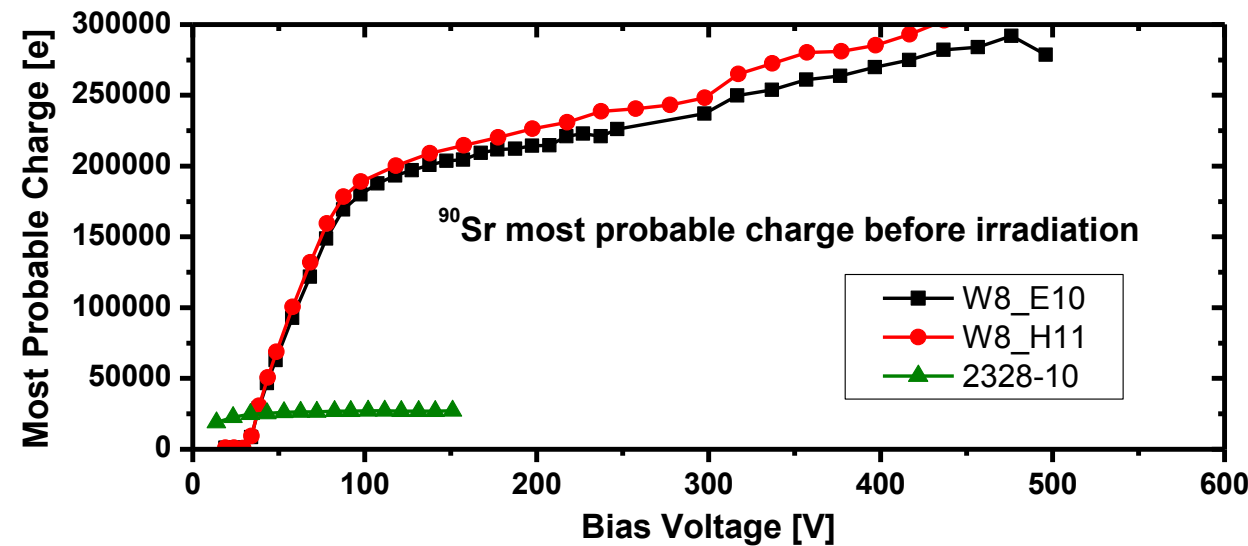
❑ **⁹⁰Sr Setup** (Done at "Jozef Stefan" Institut, Ljubljana, Slovenia):

  ✓ Measuring absolute charge collection for MIP with LHC-type electronics

  ✓ Measuring noise performance

❑ Improvement of signal for a **factor 8** at 300 V before irradiation

❑ **No significant** increase of noise (dominated by series noise)

Temperature Dependence of Multiplication

❑ Increase of multiplication at lower temperatures is expected do to larger impact ionization coefficients.

❑ It seems that there is a limit on multiplication of around a factor of 10.
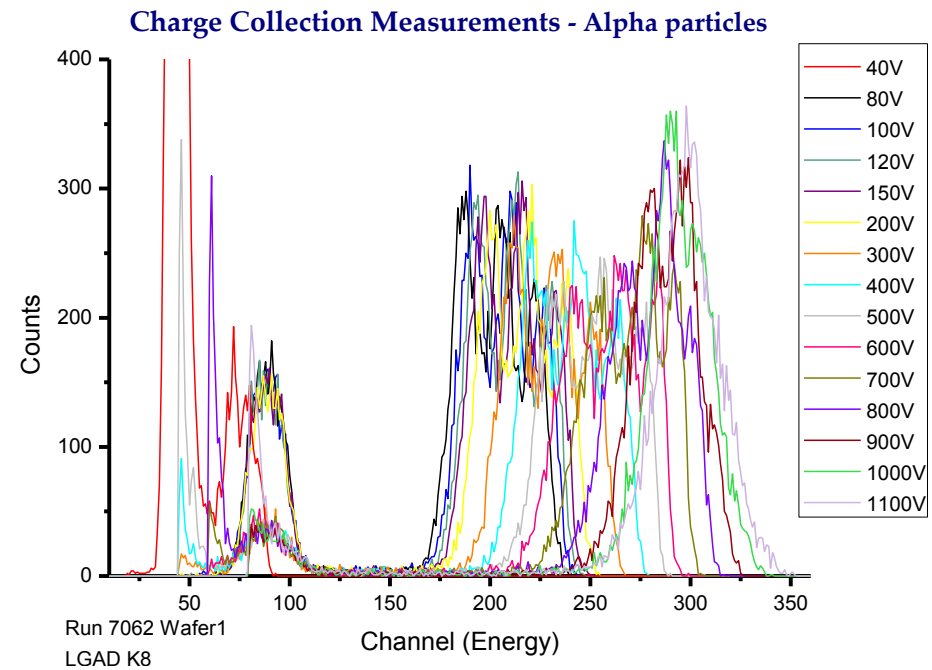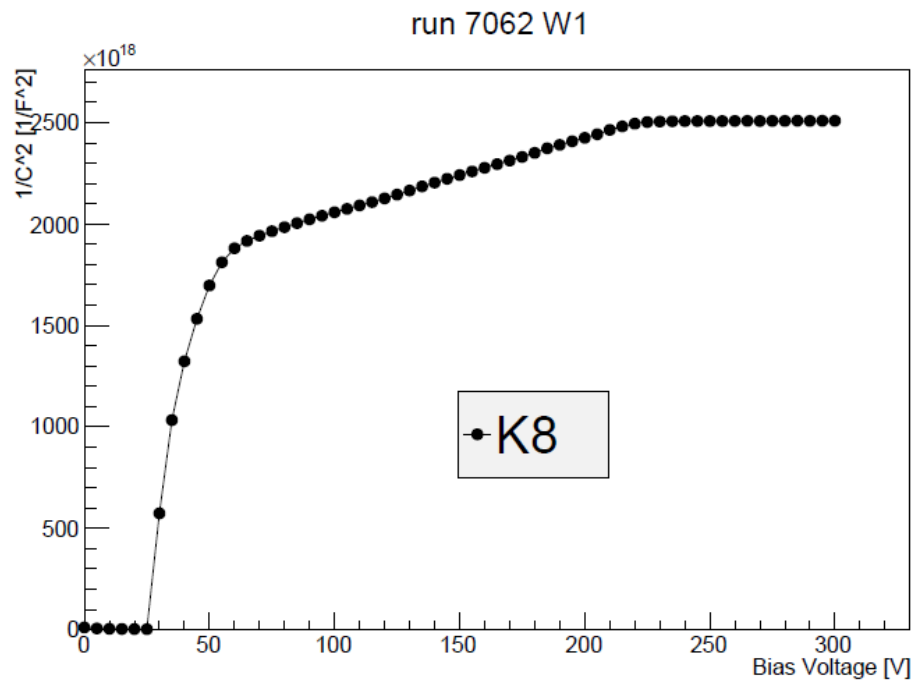
Irradiation Studies
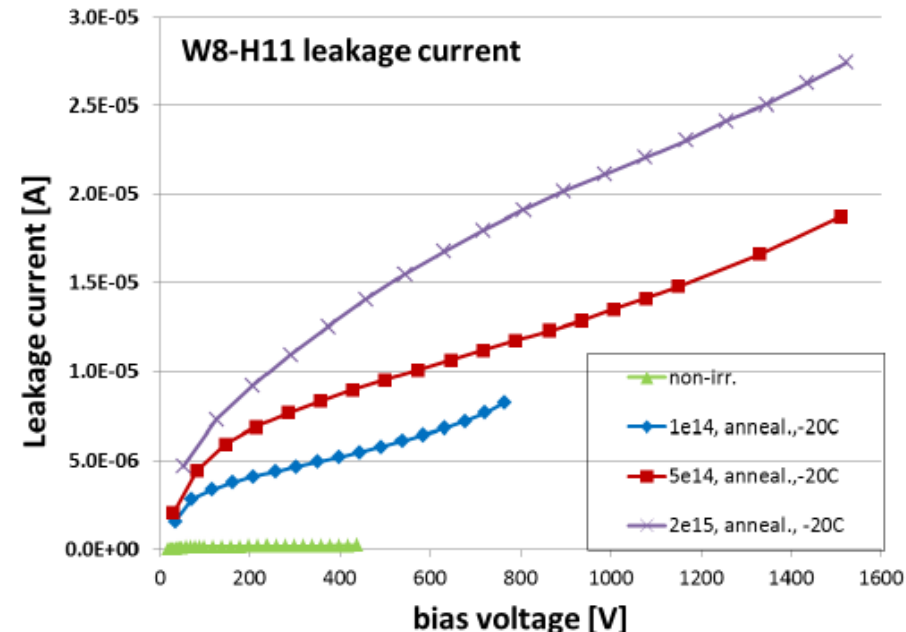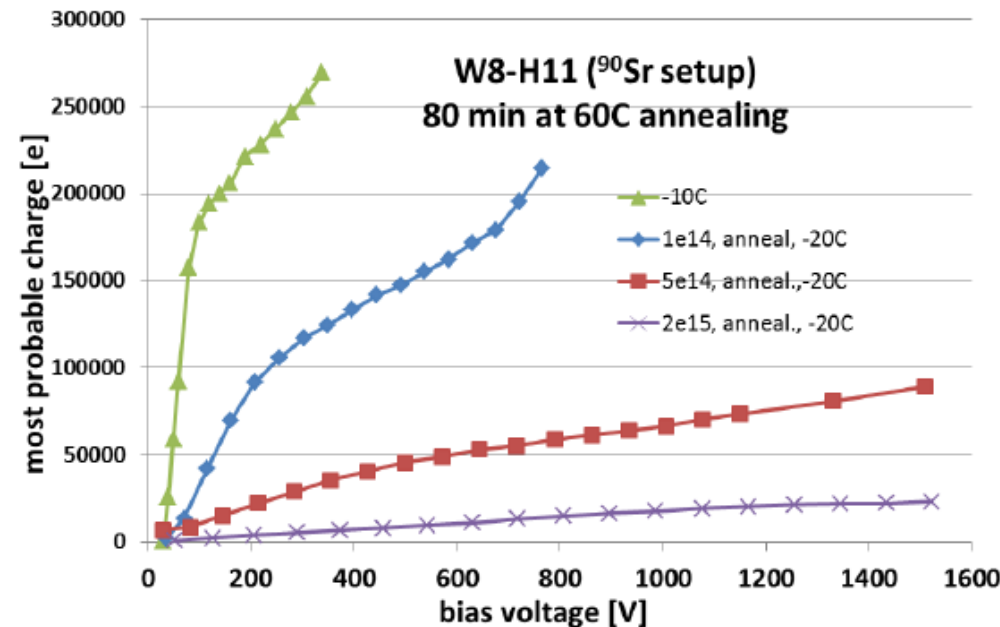
- ☐ Detectors irradiated with **neutrons** in IJS (Ljubljana)
- ☐ Multiplication **decreases** significantly with irradiation:
  - ✓ Breakdown performance is **good**,
  - ✓ Leakage current increase is **not linear** with fluence,
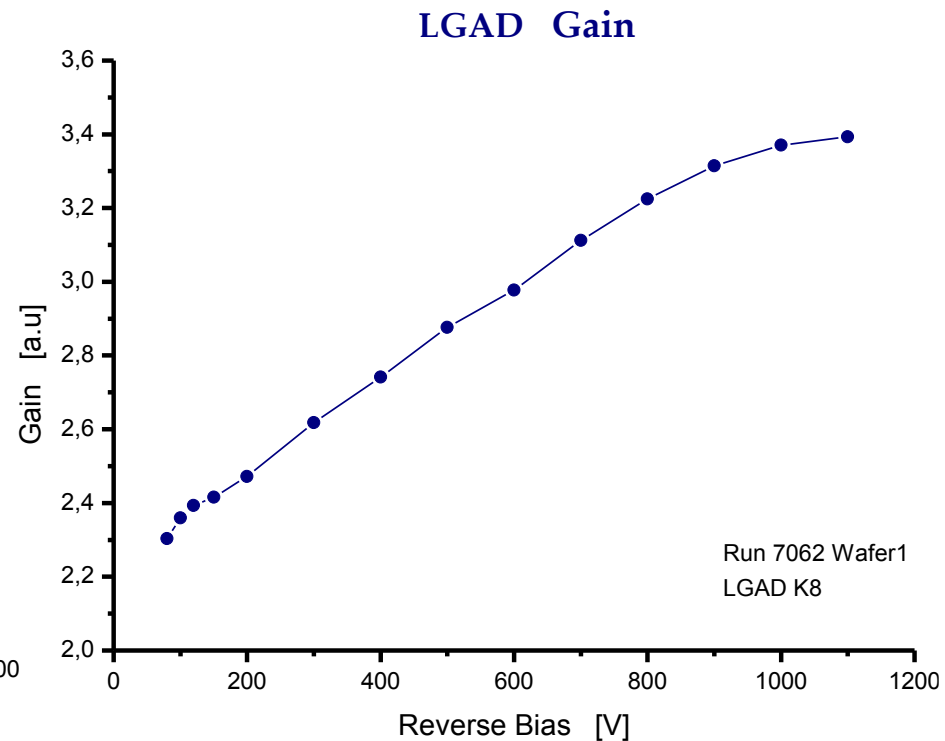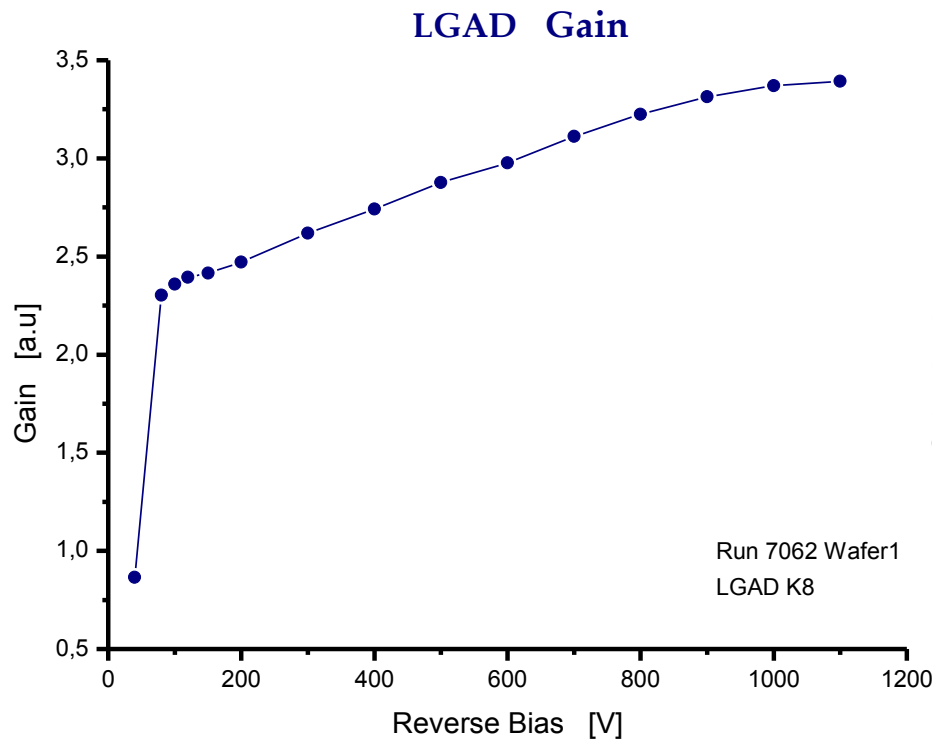 - ✓ I_{leak} increase with fluence is smaller due to **degradation** of multiplication.

$$I_{leak} = M_I \cdot I_{gen} = M_I \cdot \alpha \cdot \Phi$$

*For more details see G. Kramberger´s talk at 22nd RD50 Workshop, University of New Mexico, Albuquerque, USA*
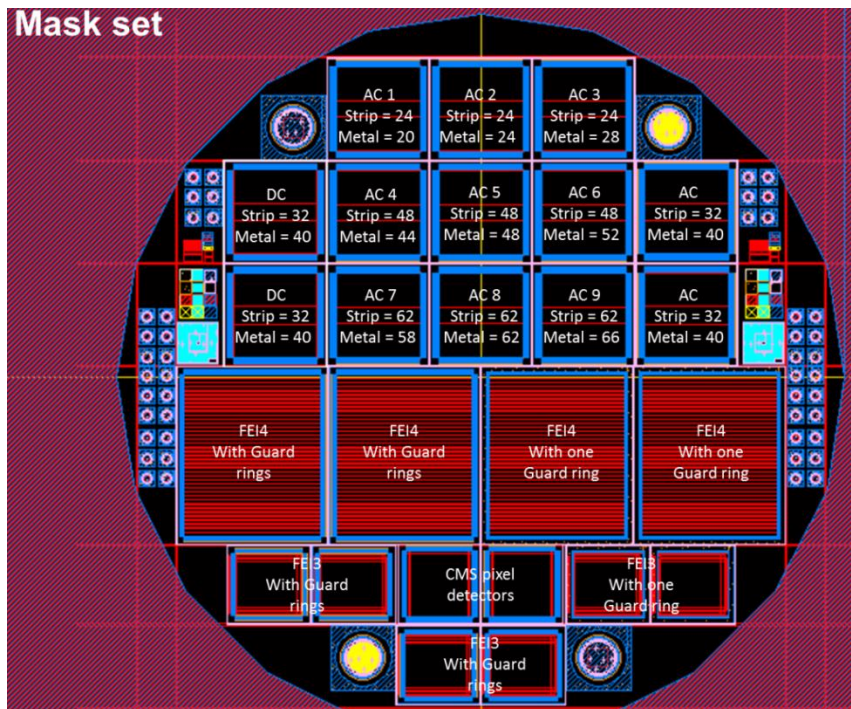
Electrical Characterization (New Run, W1)

run 7062 W1

K8

Charge Collection Measurements - Alpha particles

Run 7062 Wafer1
LGAD K8

Electrical Characterization (New Run, W1)

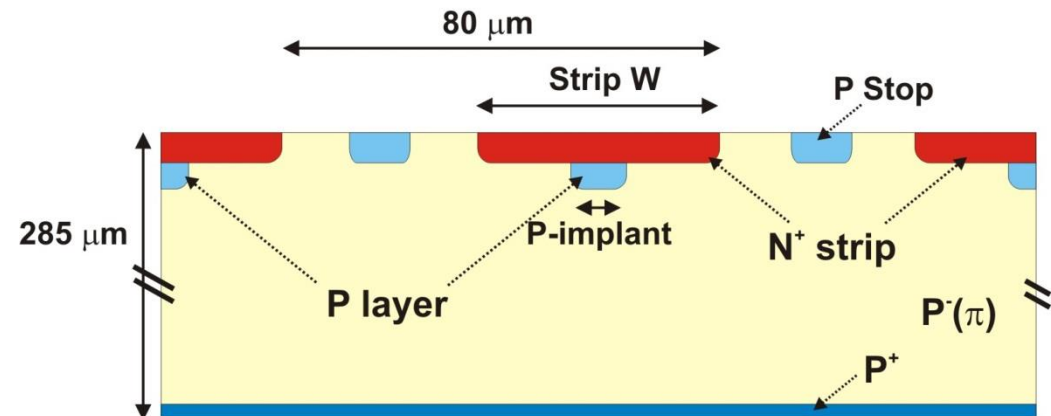**LGAD Gain**

Run 7062 Wafer1
LGAD K8

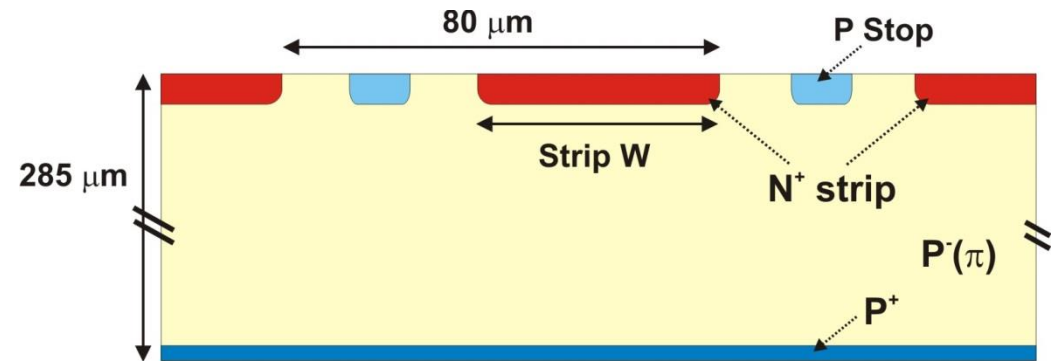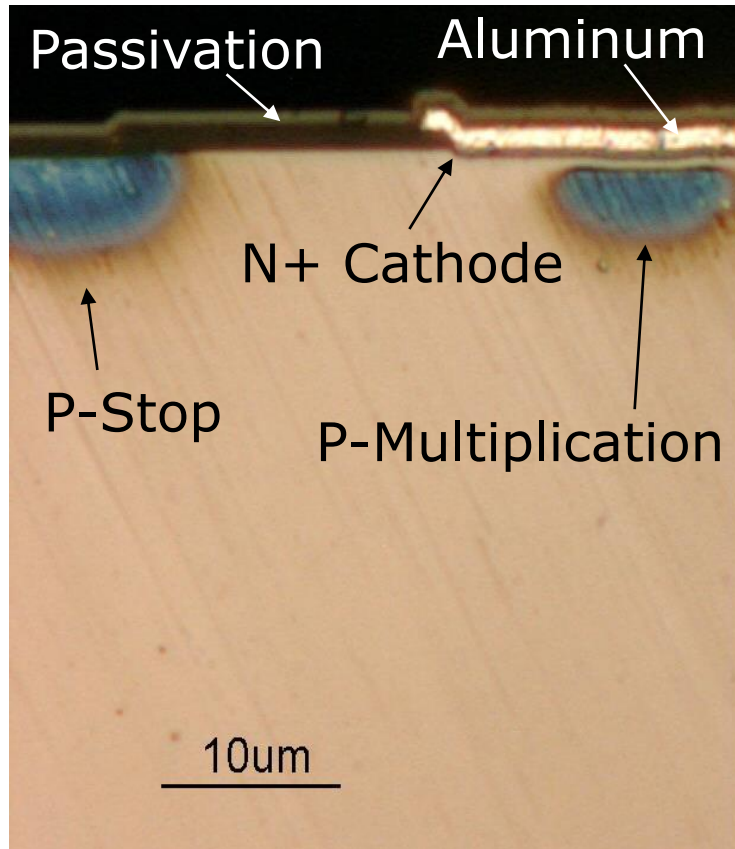**LGAD Gain**

Run 7062 Wafer1
LGAD K8

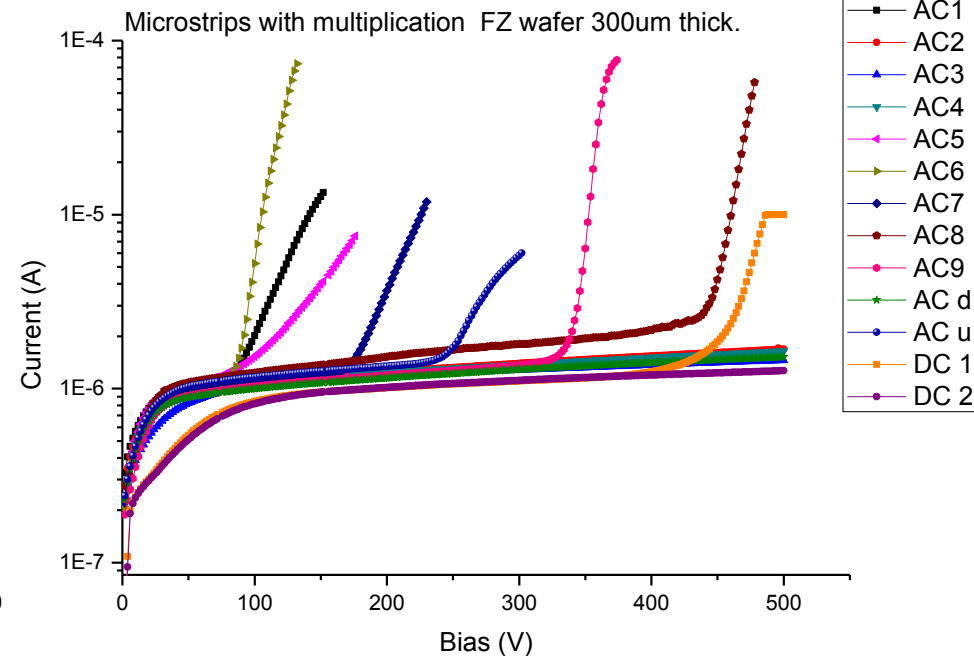# New Fabrication Run: Low Gain Microstrip and Pixel Detectors
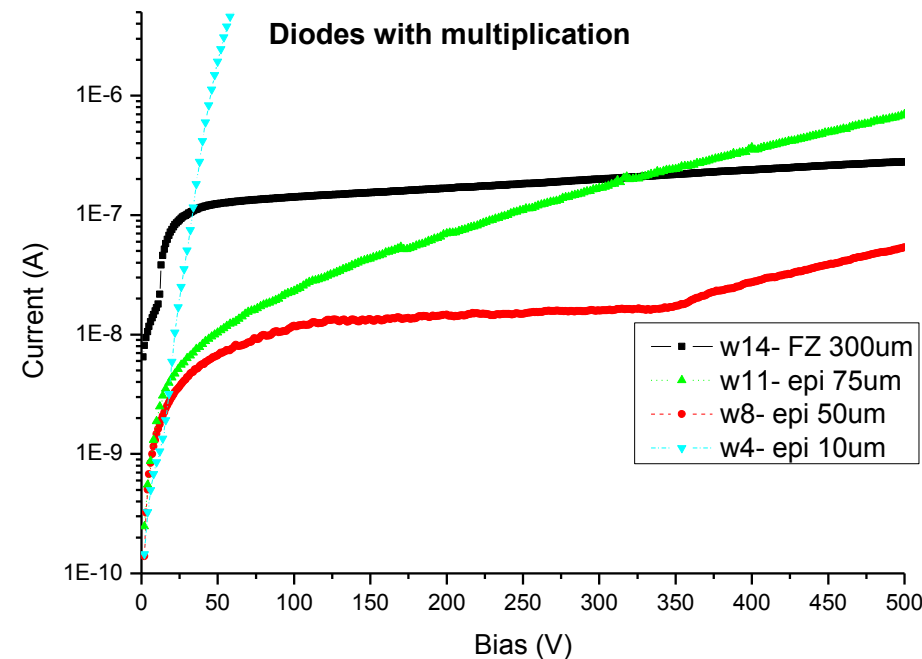
- ❑ Project financed by CERN **RD50** Collaboration.
- ❑ Fabrication **run** already **finished**, very preliminary measurements.
- ❑ **Different** geometries (pad, microstrip, pixel), implant doses and substrates.
- ❑ Junction termination extension (**JTE**) not implemented for this first run: **Lower** breakdown voltage may be expected.
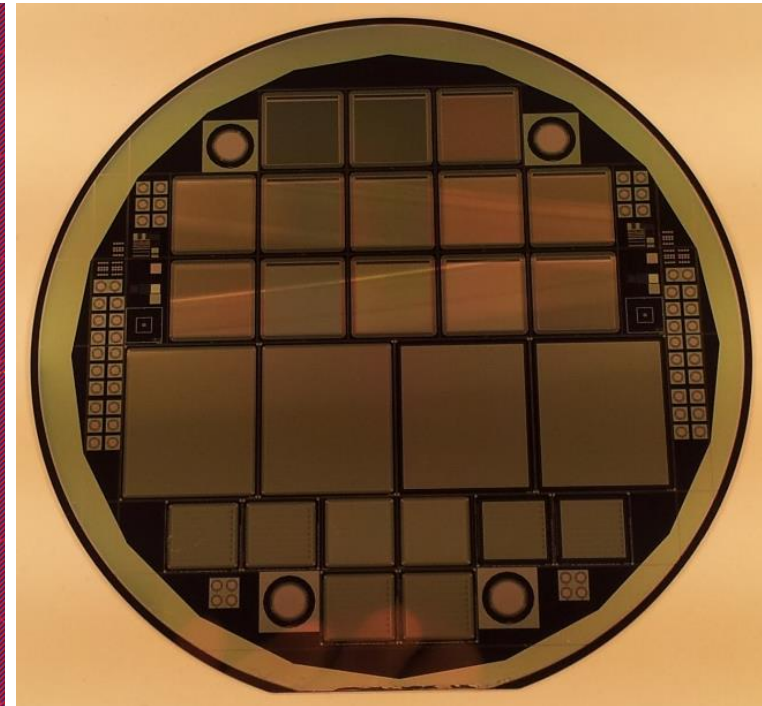
# Low Gain Microstrip and Pixel Detectors Technology

Electrical Characterization. Low Gain Pad and microStrips

Diodes with multiplication

- w14- FZ 300um
- w11- epi 75um
- w8- epi 50um
- w4- epi 10um

Microstrips with multiplication FZ wafer 300um thick.

- AC1
- AC2
- AC3
- AC4
- AC5
- AC6
- AC7
- AC8
- AC9
- AC d
- AC u
- DC 1
- DC 2
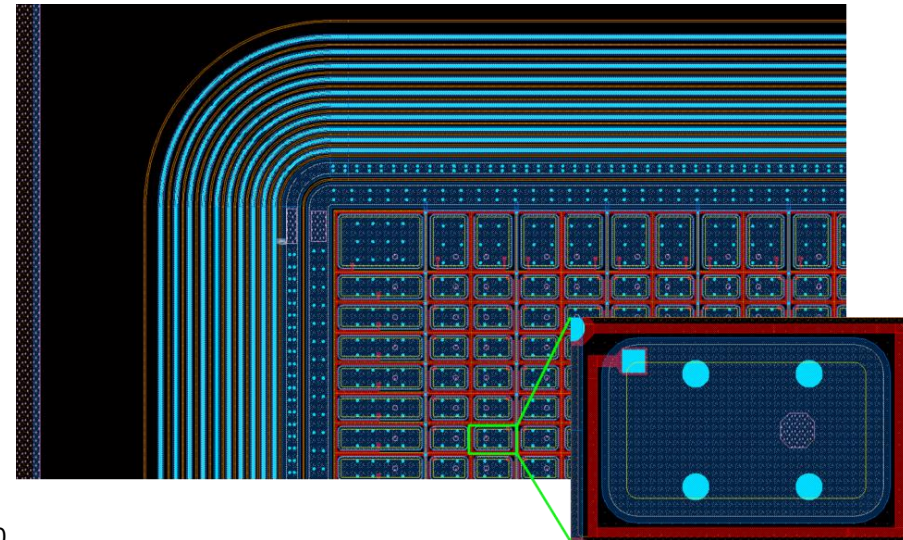
- ❑ Breakdown performance is good although the JTE was not used for these devices (V_{BR} > 500 V).
- ❑ Variations in breakdown voltage due to different metal layer over implant overlapping (**Field Plate** Overlapping).

Electrical Characterization. CMS pixel detectors
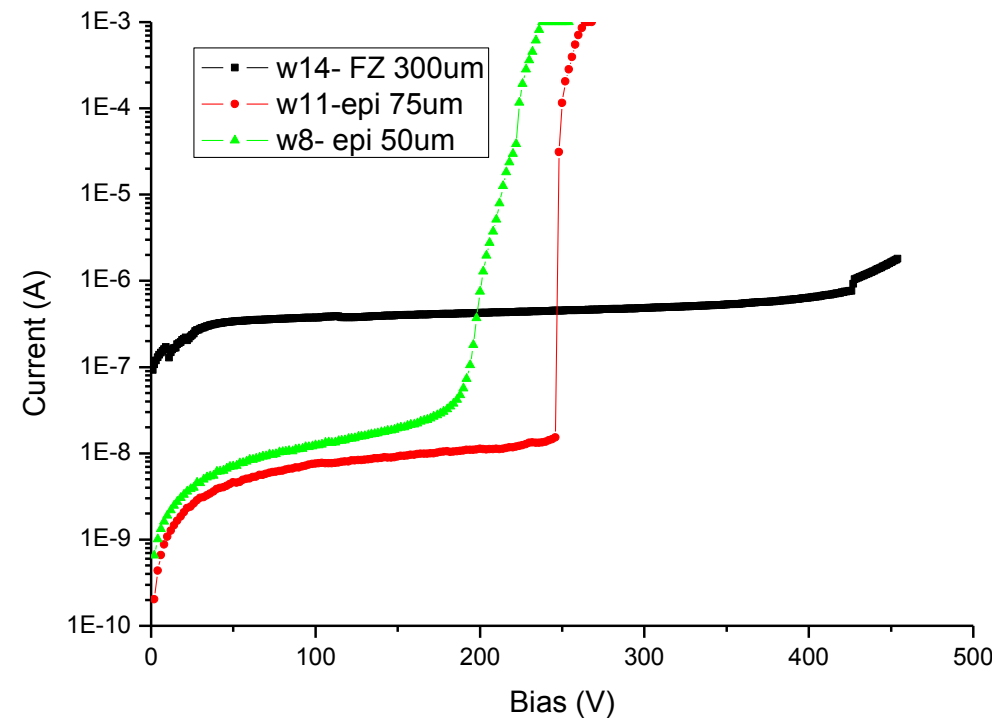
Pixels with Polysilicon bias resistor

- ❑ All pixels are connected through a 1 Mohm **polysilicon bias resistor**.
- ❑ **Breakdown** is again very good before irradiation.
- ❑ **Current** scales with volume, but for **thinner** devices breakdown occurs at lower voltages due to higher electric fields.

New Fabrication Run: Thin Detectors

- ❑ Fabrication run with **6 inch** wafers (285 microns thick)
- ❑ 5 more wafers ready to be thinned (**100 microns thick**)
- ❑ **Double metal** technology to implement integrated fanout
- ❑ **Polysilicon strip** detectors included in the mask

- ❑ Further **characterization** and **test-beam** missing
- ❑ Future **Low Gain** Implementation

deep anisotropic etching

1. Standard CMS pad diodes
2. CMS test structures
3. Standard AC strip det.
4. Strip det. with fan out v1
5. Strip det. with fan out v2
6. Detector with poly strips
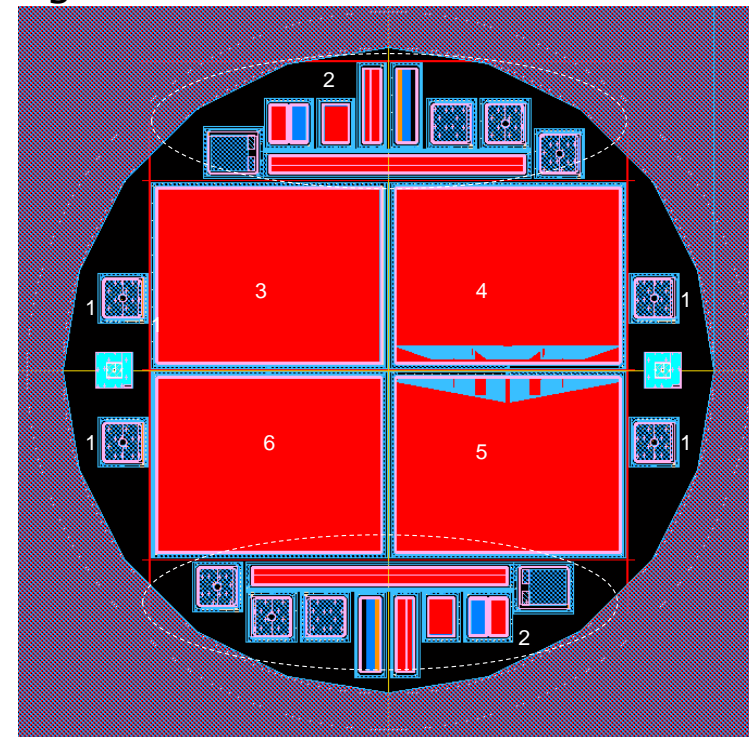
New Fabrication Run: Thin Detectors
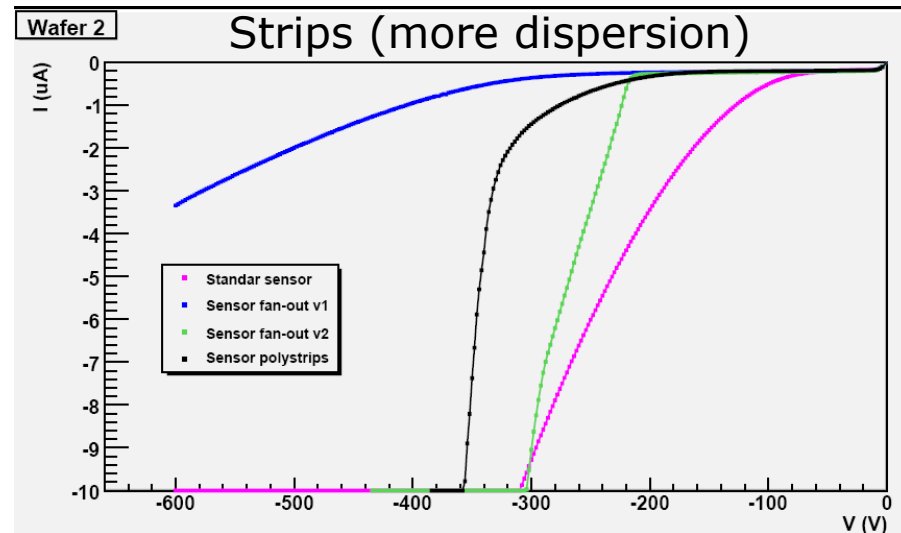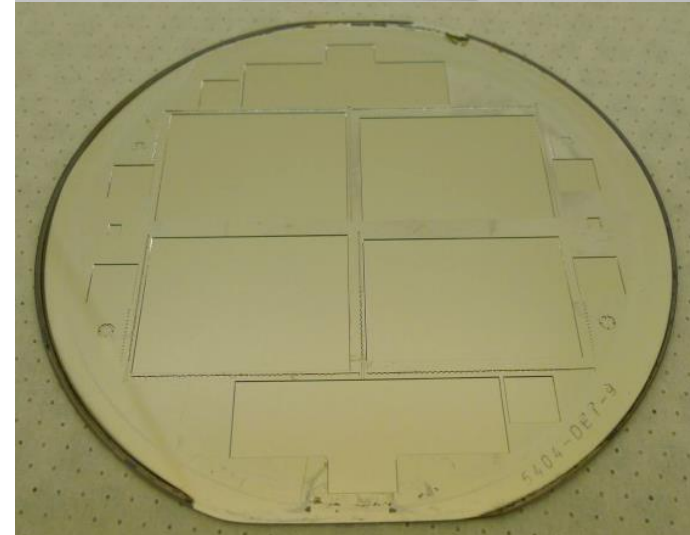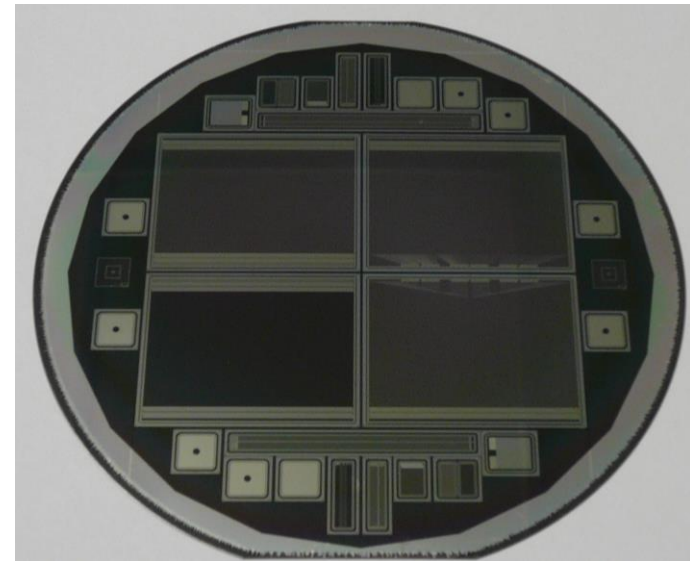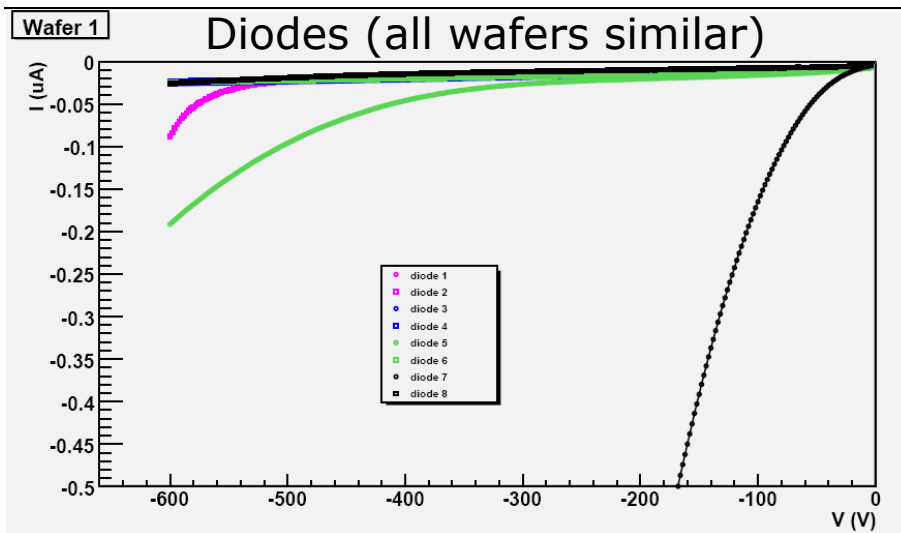
Conclusions

- ✓ We have presented the IMB-CNM activities on Silicon Detectors for ILD,
- ✓ Our work is focused to improve the performance and stability against radiation of silicon detectors for tracking applications,
- ✓ The concepts of avalanche and internal gain in pads, strips and pixel detectors are introduced
- ✓ LGAD is presented and compared with the PiN diode,
- ✓ First LGAD detectors have been fabricated,
- ✓ Excellent breakdown performance of the diodes before and after irradiation,
- ✓ Diodes with gain perform very well before the irradiation,
- ✓ Gain of ~10 for ^{90}Sr electrons,
- ✓ After irradiation the multiplication drops significantly :
  - ➢ At 2e15 cm^{-2} is around ~1.5 at 1000 V,
  - ➢ Current and noise scale as expected with multiplication,
- ✓ New fabrication run with low gain strips and pixel detectors under test. Preliminary results are very promising.
- ✓ Extension to thin detectors,
- ✓ Target: **Fabrication of low gain thin resistive microstrips and pixels detectors**.

Diffused Planar Junctions

▪ Using a planar diffusion technology we can fabricate a large number of devices on a single wafer by selective diffusion of impurities through a silicon dioxide masking layer.

▪ Due to the lateral doping extension through the window periphery, we can identify three important areas at the junction formed using this technology.,

   ▪ Plane into the diffusion window,

   ▪ Cylindrical at the mask edges (Line A at the figure), and

   ▪ Spherical at the sharp corners (Line B).

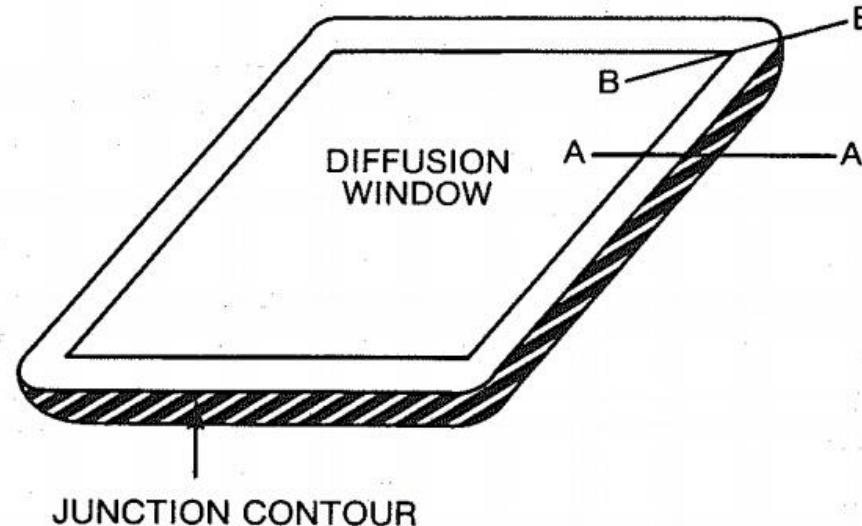▪ This curvature effects produce a reduction in the voltage capability (till 50 % of the ideal value).

Fig. 3.11. Planar junction formed by diffusion through a rectangular diffusion window.

Cylindrical Junction

▪ The breakdown voltage is given by,

$$\frac{BV_{CYL}}{BV_{PP}} = \left\{ \frac{1}{2}\left[\left(\frac{r_j}{W_c}\right)^2 + 2\left(\frac{r_j}{W_c}\right)^{6/7}\right] \ln\left[1 + 2\left(\frac{W_c}{r_j}\right)^{8/7}\right] - \left(\frac{r_j}{W_c}\right)^{6/7} \right\}$$

▪ Expression that can be approximated by,

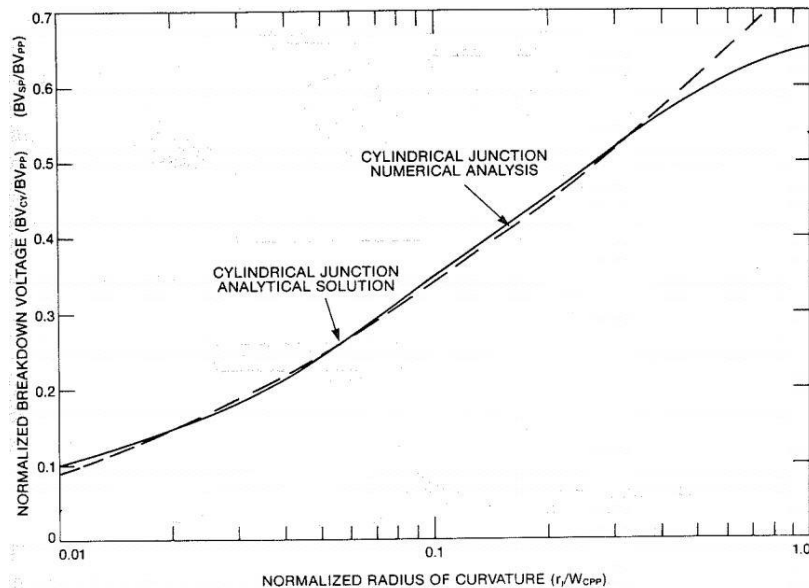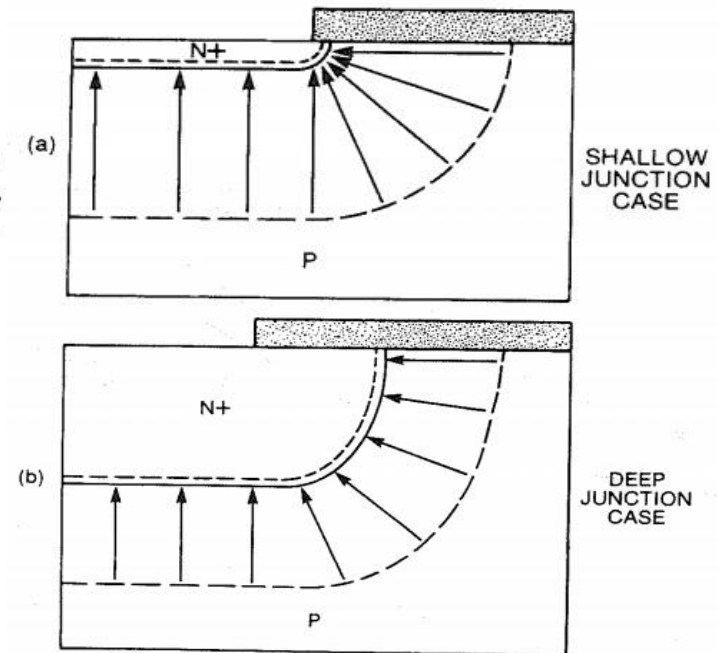$$\frac{BV_{CYL}}{BV_{PP}} = \left[0.871 + 0.125 \ln\left(\frac{r_j}{W_{c,PP}}\right)\right]^2$$

3.17. Electric field crowding at the edges of (a) shallow and (b) deep junction.

▪ BVcyl is always less than BVpp.

▪ If rj increases (which implies an increase in junction depth) BVcyl increases and reduces the difference with BVpp.

Fig. 3.16. Normalized breakdown voltage of cylindrical and spherical junctions as a function of the normalized radius of curvature.

Spherical Junction

- The breakdown voltage is given by,

- BVsp is always less than BVcyl.

$$\frac{BV_{SP}}{BV_{PP}} = \left(\frac{r_j}{W_c}\right)^2 + 2.14\left(\frac{r_j}{W_c}\right)^{6/7} - \left[\left(\frac{r_j}{W_c}\right)^3 + 3\left(\frac{r_j}{W_c}\right)^{13/7}\right]^{2/3}$$
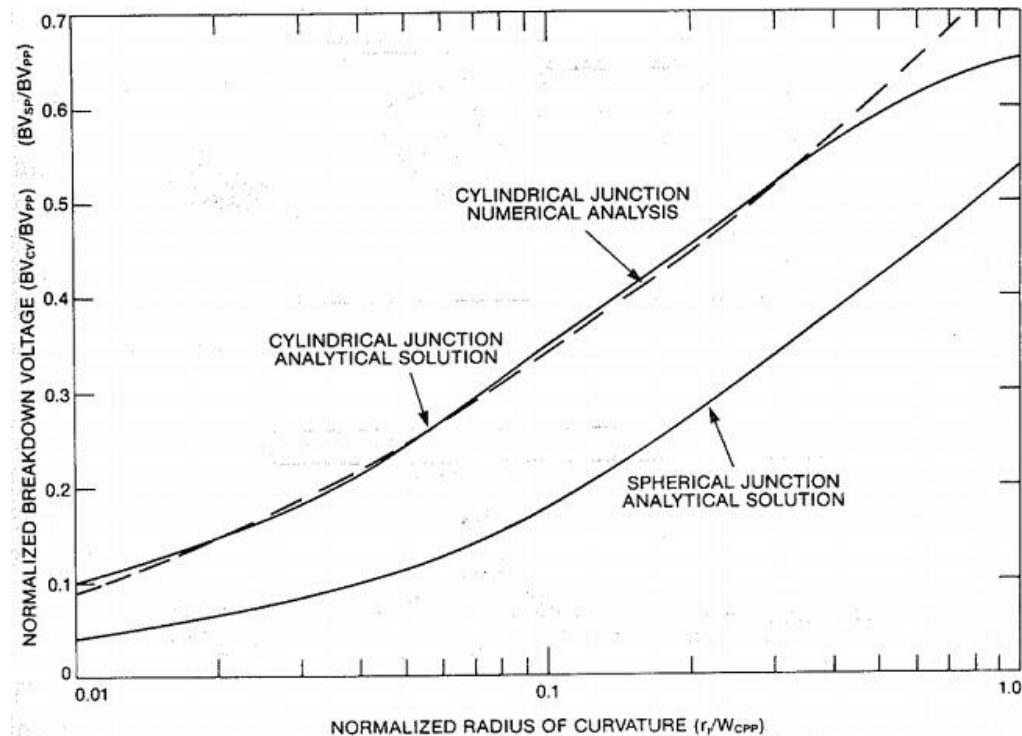
Fig. 3.16. Normalized breakdown voltage of cylindrical and spherical junctions as a function of the normalized radius of curvature.