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A CMOS Pixel Sensor Prototype for the Outer Layers of Linear Collider Vertex Detector

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The first CMOS pixel sensor prototype integrated with 4-bit column-level ADC for the outer layers of the ILC vertex detector has been fabricated and tested. The design is adapted to an original concept of minimizing the power consumption. It is composed of a matrix of 64 rows and 48 columns. Inside each pixel an amplification stage with a correlated double sampling is used. At the bottom of the pixel array, each column is terminated with a self-triggered ADC, which employs a threshold voltage to trigger the conversion. The test results of the prototype will be presented.

Summary

The International Linear Collider (ILC) is expected to provide high precision measurements for flavor tagging. This requires a high-resolution and low-mass vertex detector (VXD). CMOS pixel sensors (CPS) have been considered as an option for the VXD of the International Large Detector (ILD), one of the detector concepts proposed for the ILC. MIMOSA-31 is the first CPS integrated with 4-bit column-level ADC for the outer layers of the VXD, adapted to an original concept minimizing the power consumption. It is composed of a matrix of 64 rows and 48 columns. The proposed architecture with pixel pith of 35 μm is estimated to provide a single point resolution of ˜ 3.5 μm.

The pixel array is readout in a rolling shutter mode which is steered through a row sequencer. The voltage signal induced by the charges collected through an Nwell/Pepi diode is amplified in each pixel. The signal information is obtained through a correlated double sampling operation. All of the in-pixel circuits are implemented with NMOS transistors. In the rolling shutter mode only one row is powered on, and therefore the power consumption of the pixel array is dedicated to one row. The pixel output signal is transmitted to the bottom of the pixel array where column-level ADC performs the digitization. The ADC resembles the successive approximation register architecture. The prototype also remains other micro-circuits such as analog read-out circuit, biasing circuit and digital control (memory and JTAG controller).

The ADC converts the pixel output signal in parallel by using a multi-bit/step approximation. It was optimized for power saving at a sampling frequency of 6.25 MS/s. As in the outer layers of the ILD VXD hit density is of the order of a few per thousand, in order to reduce power consumption, this ADC is designed to work in two modes: active mode and idle mode. It is self-triggered by employing a threshold voltage. If the pixel output is higher than the threshold voltage, the ADC is triggered to do the conversion. Otherwise, it works in idle mode and goes asleep until the next conversion.

The sensor prototype was fabricated in a 0.35 μm CMOS technology, covering an area of 4 x 4.8 mm2. The prototype chip is measured with 100 MHz basic clock to generate required timing and transmit the digital outputs. The read-out time of each frame is ˜ 10 μs, allowing a time resolution of 100 μs for the full size sensor (about 2 x 2 cm2). The measured equivalent noise charge corresponds to ˜ 18.6 e-. With the calibration peak, the measured charge collection efficiency on seed pixel is ˜ 18%. The power consumption of each column equals 662 μW, assuming a typical occupancy of ˜ 0.5% in the whole sensor. This value slightly rises to 664 μW with a safety factor of 3. This paper will describe the details of the prototype chip and the laboratory experimental results.

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