Task List (Feb/25/2014)

Calibration implementation:

- Calibration console integration (Matthias)
  - RCEpixelLab Twiki update for Calib Console table
  - TopLevel panel for SR1 and P1 ?
  - Bookkeeping aspects clear on what to do ? Converters ?
- calibGUI FE-I4 calibration implementation (Dmitri/Brian, Martin)
  - Implementation of a delay-adjustable double trigger seeded by cosmic trigger input in HSIO FPGA. Already working for sometime. (Martin)
- calibGUI FE-I3 calibration suite for test beam (Ben/Martin)
  [Scans for test beam all in place.]

RCE performance:

- Resume profiling work to check major CPU costs (Matthias/Martin)
  [Recollection on SR1 setup: ~ linear vs nChannel for nChannel>2]
- Formatter going to firmware ? (Nick)
  [Development on hold. Formatter speed OK for most purposes. Accumulative packaging of calibration data (e.g. from multiple slices together) could lead to significant speed up ?]

DAQ

- Test beam rate capability, including logging (Martin)
  - Buffering optimization can improve for close triggers
  - Test for occasional missing triggers is important to bring into IBL stave test program for more robust high rate operation. Some tests done but occurrence rather erratic. (Michael)
  - Resynch frontend overflow due to close triggers exceeding 16 FE-I4 is slow. Is there a way to do complex dead time protection ? The event processing being a mini event-building to collect fragments from same events seems to be doing fine.
  - Readout blank time of 14 BCID is adequate complex deadtime protection for test beam.
- Formal DAQ rate tests vs number of channels. Stave noise scans with all FE enabled can run up to 25KHz.

Generic Applications

- RCE data I/O loop basic utility example with emulated data (Nick)
  [Basic tests worked, but need to recover setup after outage and release update. Documentation next.] - Is this running again (Matthias) ?

Infrastructure / Hardware / Firmware:

- Crate hardware recommendation updated. (Su Dong)
- New Hardware status (Mike)
  Pre-Production V6 COB debugging in progress. Still a few P3 user signals not clean. Revised testing loopback RTM helped some channels.

DPM and DTM are production ready.
SFP RTM in testing, 96 channel MPO RTM in design.
Prototype TTC firmware has initial version in testing.

Software infrastructure:

- Remote installation capability – overhaul for multi-system support (Matthias/Ric)
- New TDAQ release integration [on hold to implement for Gen-III RCE only]
- SLC6 migration (Matthias)
- PGP2 migration: RCE firmware, HSIO firmware – on hold. No clear benefit.
- Migrate to new RCE interface code [on hold until this is stable]
- Which RTEMS version ? [core is moving to an adapted SLAC version V10-11]
- Getting ZedBoard to try software migration on ZYNQ [Su Dong]

Pixel/IBL RTM, HSIO

- New optical interface card for new HSIO: P3 connector has 2x40=80 LVDS pairs. Can host 4+4 (TX+RX) MPO fibers of 8 channels each = 32 channels. For the IBL optical interface card, HFBR-772BWZ / HFBR-782BZ are used (same as IBL BOC) which worked for 100+m of long fiber, while lower grade transceivers became marginal for long fibers.
- RTM compatible with V6 COB and Gen-III is 12 MPO through connectors spread to miniPods for 96 channel COB. Is MiniPOD TX light yield strong enough to drive long fiber ? Why commercial transceiver not adequate for RX ? By channel power/phase adjustment ?
- HSIO update: Another new signal diagram and updated layout. Issues identified and further clarified after meeting:
  - DTM USB/UART group has been in the schematics but not listed in the signal diagram. This is the RCE USB serial console.
  - I2C header may remain as a simple header. This is the IPMI link on the COB for configuring shelf/slot info in an ATCA shelf which is mostly not needed with HSIO stand alone.
  - The DTM RCE booting is from an SD card on the DTM. A reset button should be added to force booting.
  - The two native 1GE Ethernet ports on the ZYNQ are led out through Marvell chips on the DTM and then RJ45, without using the MGTs. Considered the COB approach of SFP cage with switchable RJ45/SFP plug-in but decided not worth the complication.
  - 2x2SMA should space out into a 1x4 for easy access.
  - Pack of LEMOs should be spaced out for easier access also. Not on board edge OK (check with UK) ?
  - Power moving to 12V supply to reduce unnecessary switching noise.
  - TTC interface needs to be a small mezzanine. Jumper resistor to redirect one MGT channel towards the TTC card to user SFP I/O.