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**IO\_CONNECTORS**

SHEET=66

**PGP**

SHEET=2

**ZONE3\_CONNECTORS**

SHEET=13

**FRONT\_PNL\_CNTRL**

SHEET=SHEET

**EV**

SHEET=3

**ZONE3\_GPIO**

SHEET=13

**BANK\_32**

SHEET=13

**PCIE**

SHEET=4

**PWR\_REG**

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SHEET=6

**FPGA\_CONFIG**

SHEET=7

FPGA\_POR — FPGA\_POR

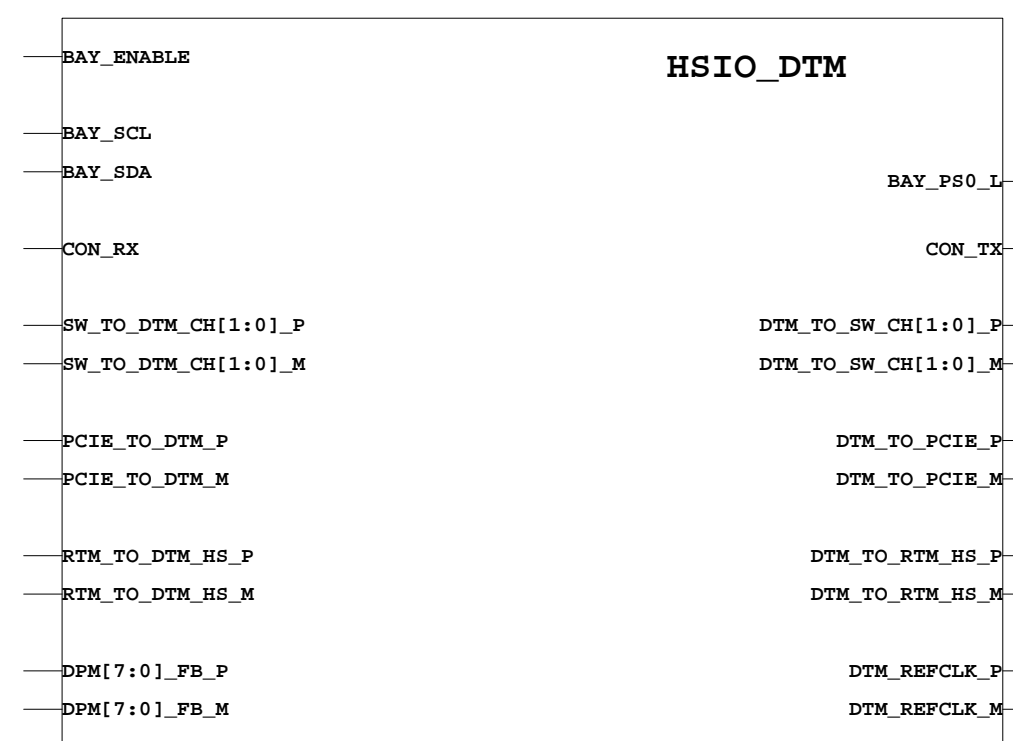
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AD7M  
AD15P  
AD15M

AD7P  
AD7M  
AD15P  
AD15M

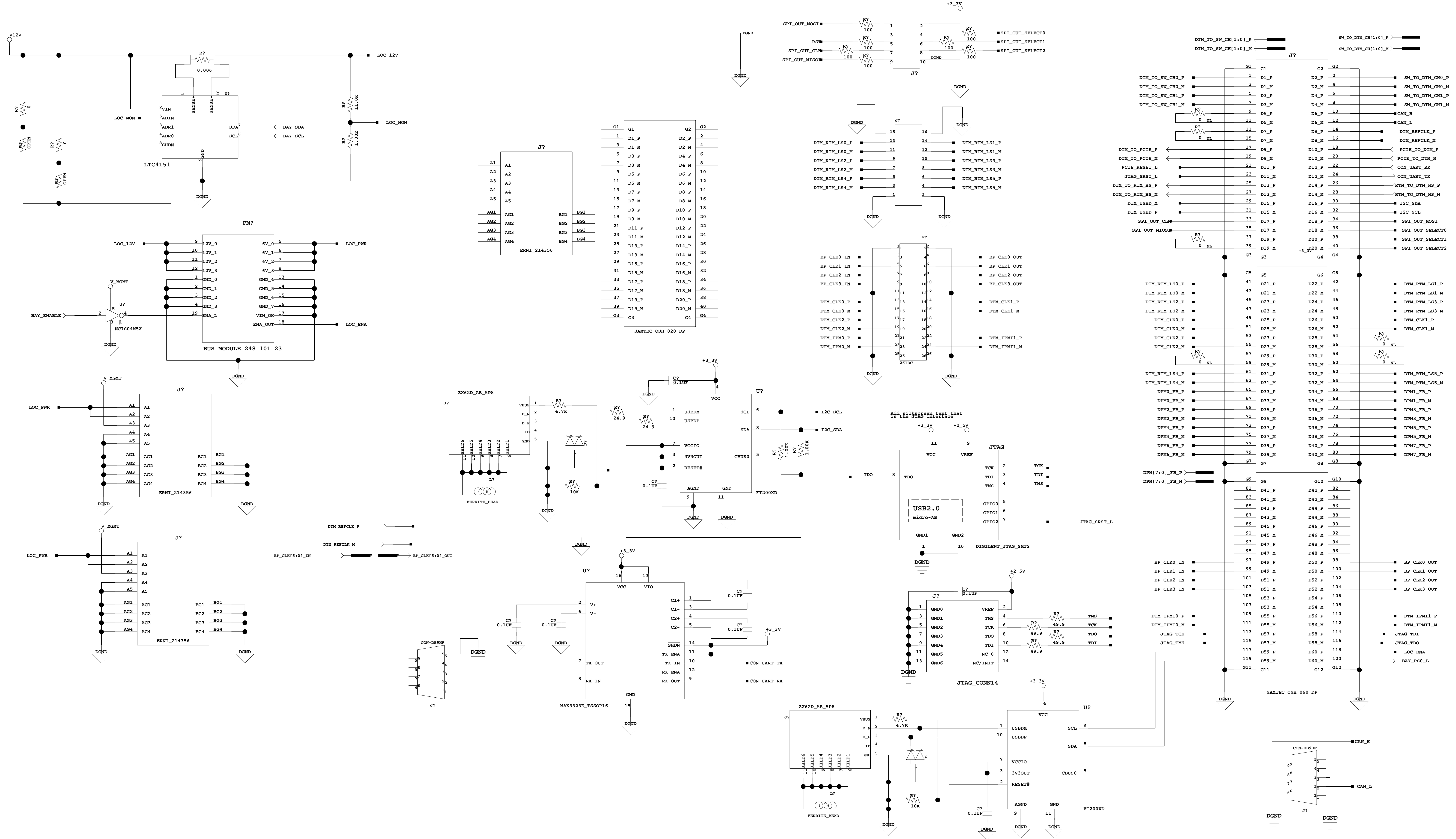
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AD7M  
AD15P  
AD15M



SLAC NATIONAL ACCELERATOR LABORATORY U.S. DEPARTMENT OF ENERGY <small>STANFORD UNIVERSITY STANFORD, CALIFORNIA</small>		
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ENR	DATE	APPROVALS
Larry Ruckman	2013	
DFR		
CHK		

SHEET 1 OF 8
<b>PGP CARD Generation 3</b> <b>TOP LEVEL BLOCK</b>
<b>LOCATED AT SHEET TOP</b>
SD-260-101-03-C00

31/01/2014:13:46

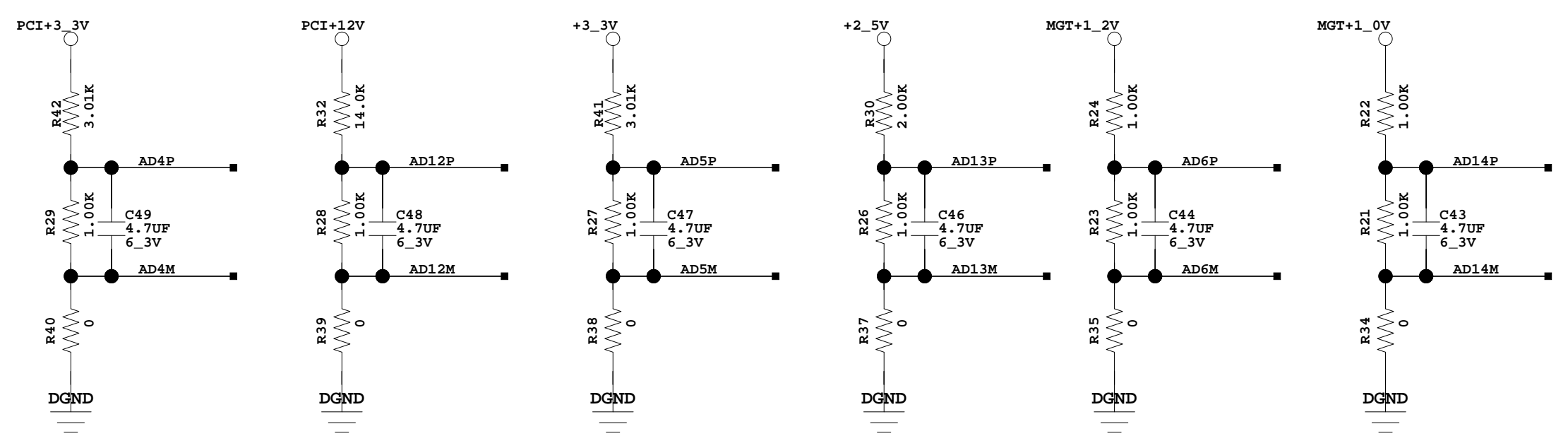
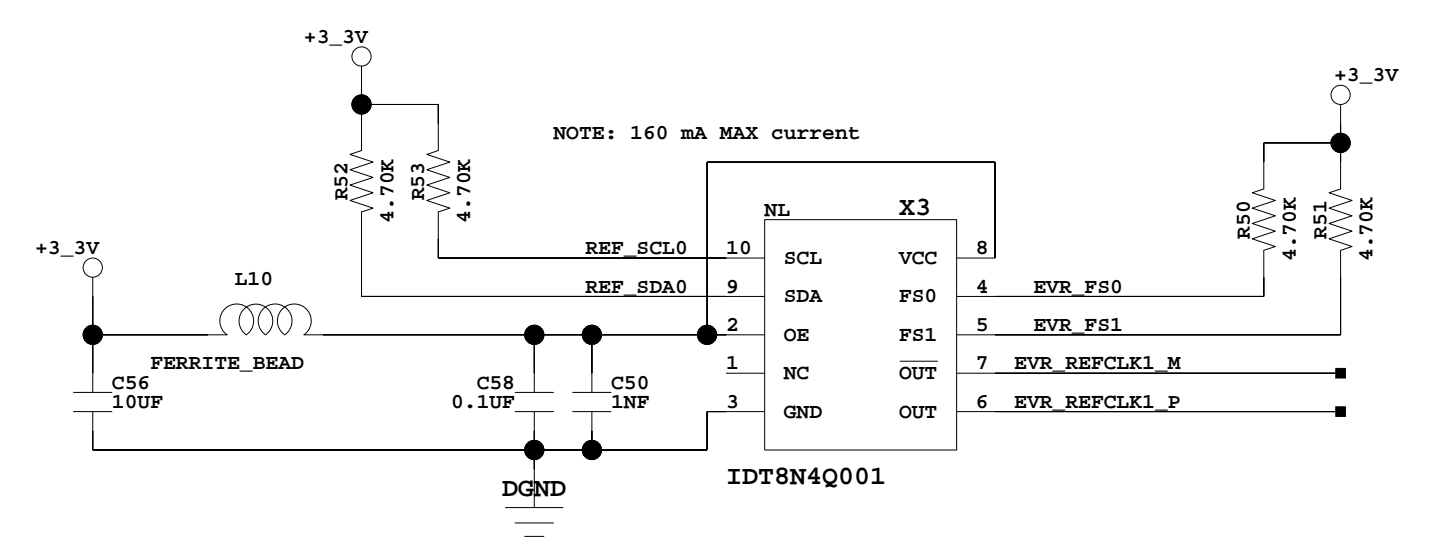
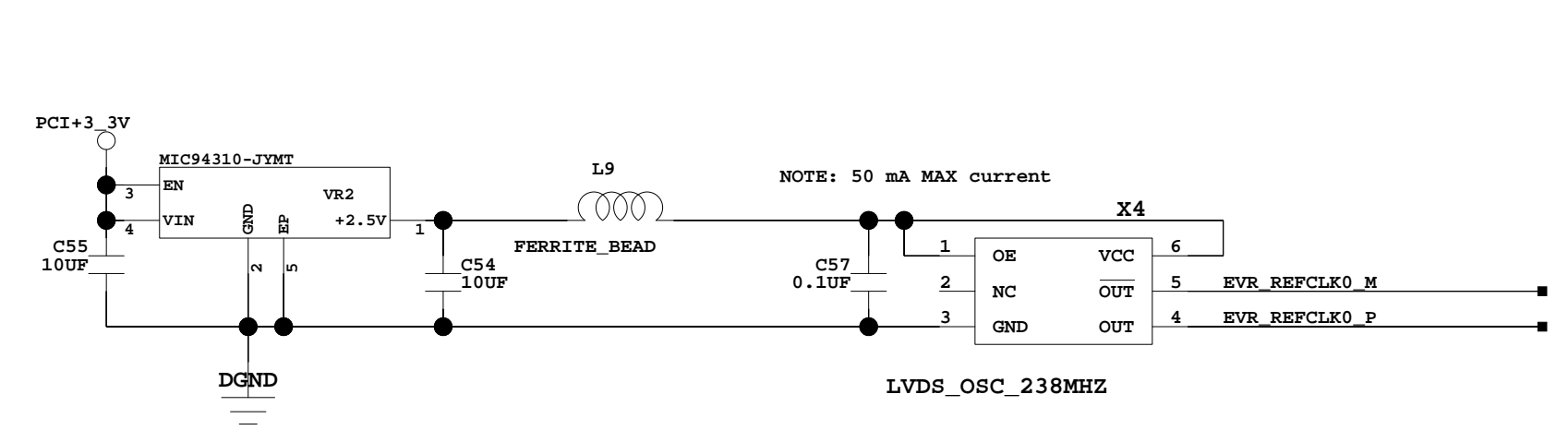
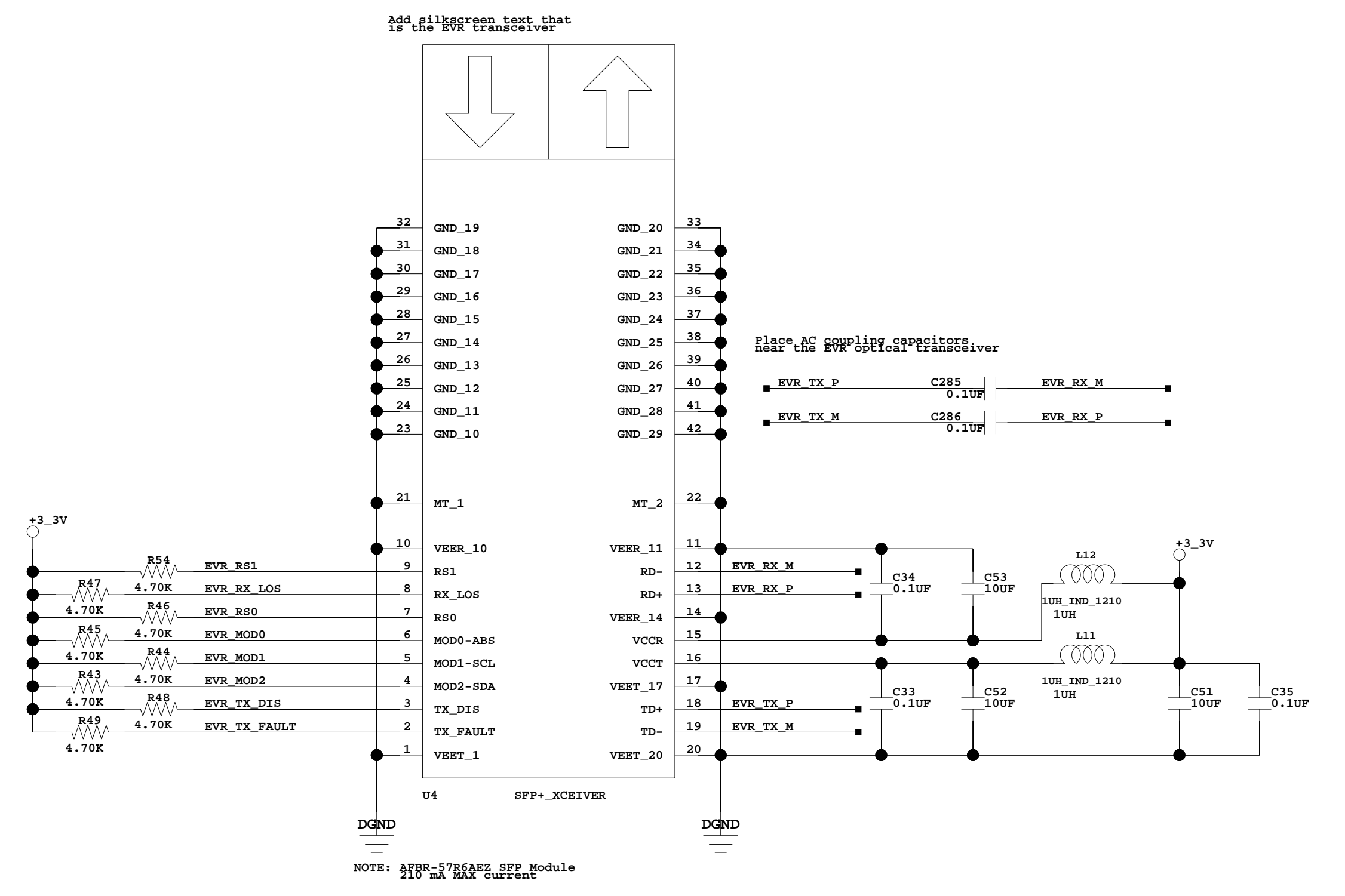
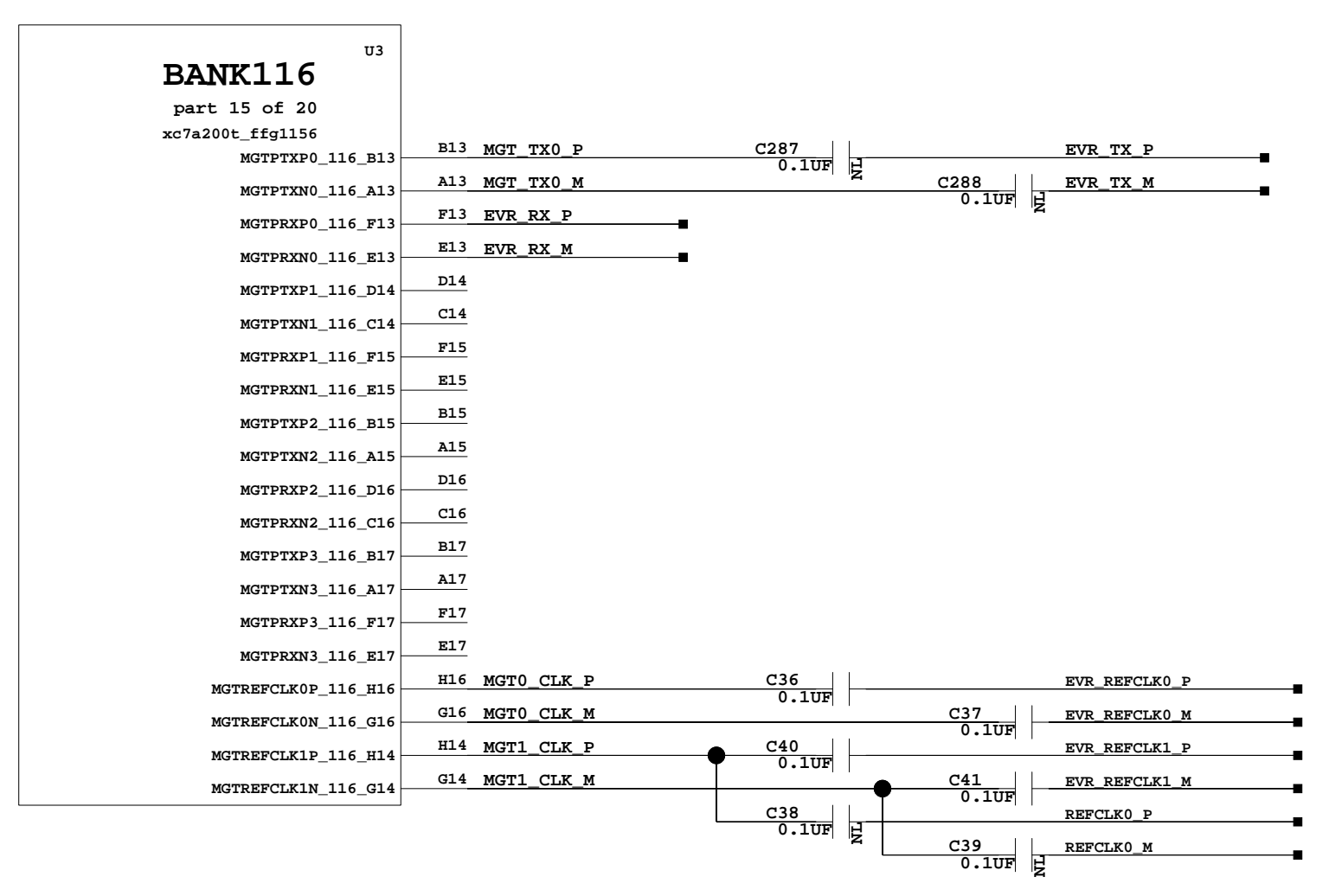
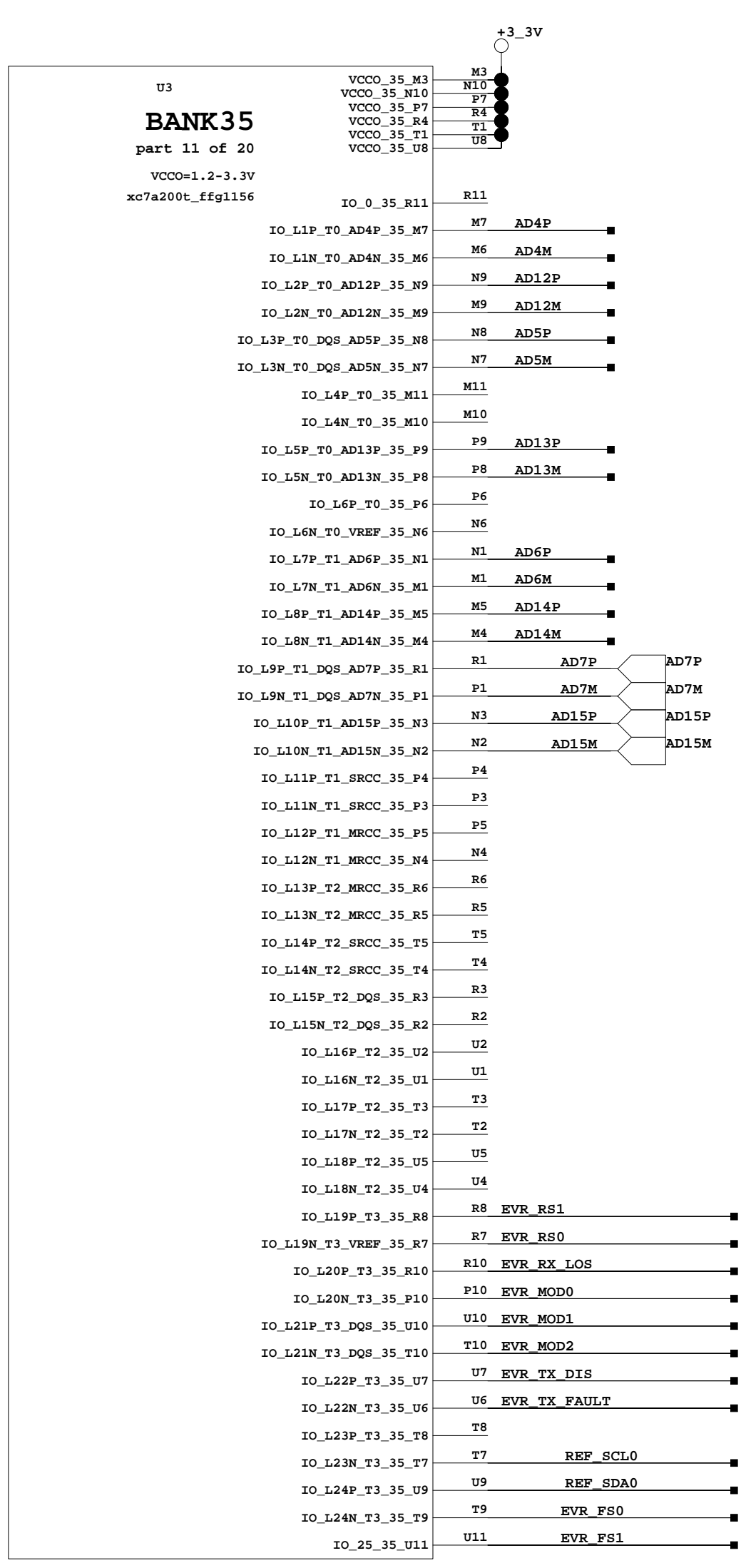
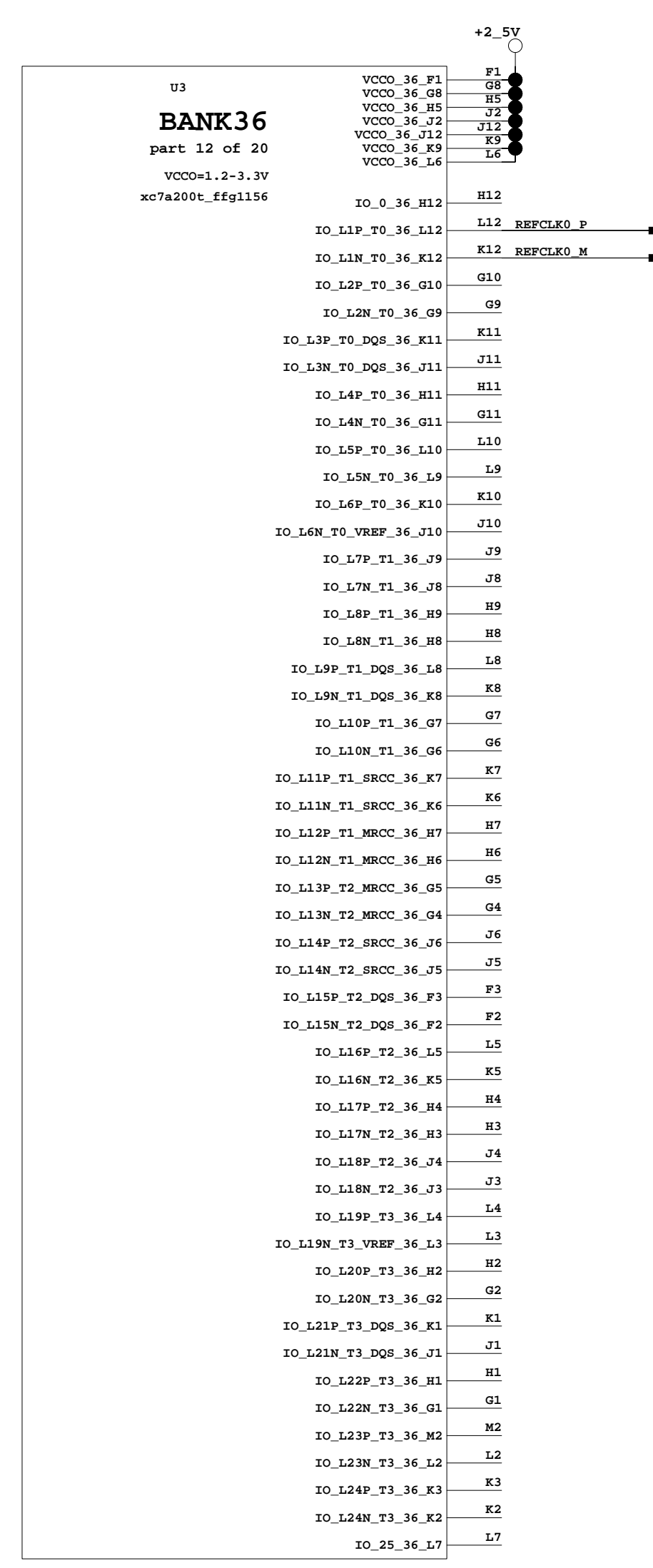


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04/11/2013:10:36

SLAC NATIONAL ACCELERATOR LABORATORY U.S. DEPARTMENT OF ENERGY STANFORD UNIVERSITY STANFORD, CALIFORNIA		SHEET 3 OF 8
PROPRIETARY DATA OF STANFORD UNIVERSITY AND/OR U.S. DEPARTMENT OF ENERGY. RECIPIENT SHALL NOT PUBLISH THE INFORMATION WITHIN UNLESS GRANTED SPECIFIC PERMISSION OF STANFORD UNIVERSITY.		GPG CARD Generation 3 EVR Block
ENR Larry Ruckman DFR CDR	DATE 2013 APPROVALS	LOCATED AT SHEET 1 SD-260-101-03-C00



U3  
part 19 of 20  
xc7a200t\_ffgl156

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A2	GND_A2	
A3	GND_A3	
A4	GND_A4	
A5	GND_A5	
A6	GND_A6	
A7	GND_A7	
A8	GND_A8	
A9	GND_A9	
A10	GND_A10	
A11	GND_A11	
A12	GND_A12	
A13	GND_A13	
A14	GND_A14	
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U3  
part 20 of 20  
xc7a200t\_ffgl156

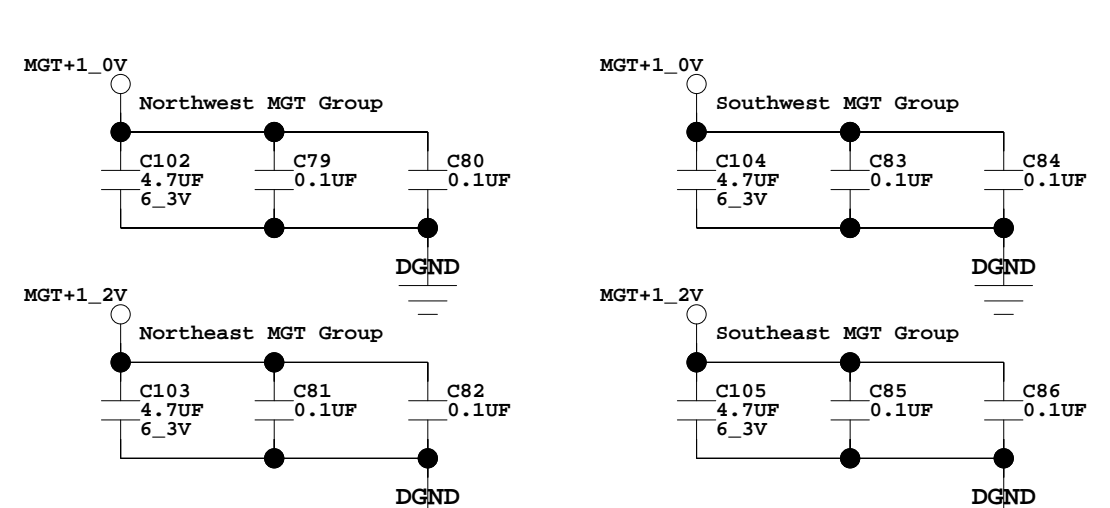
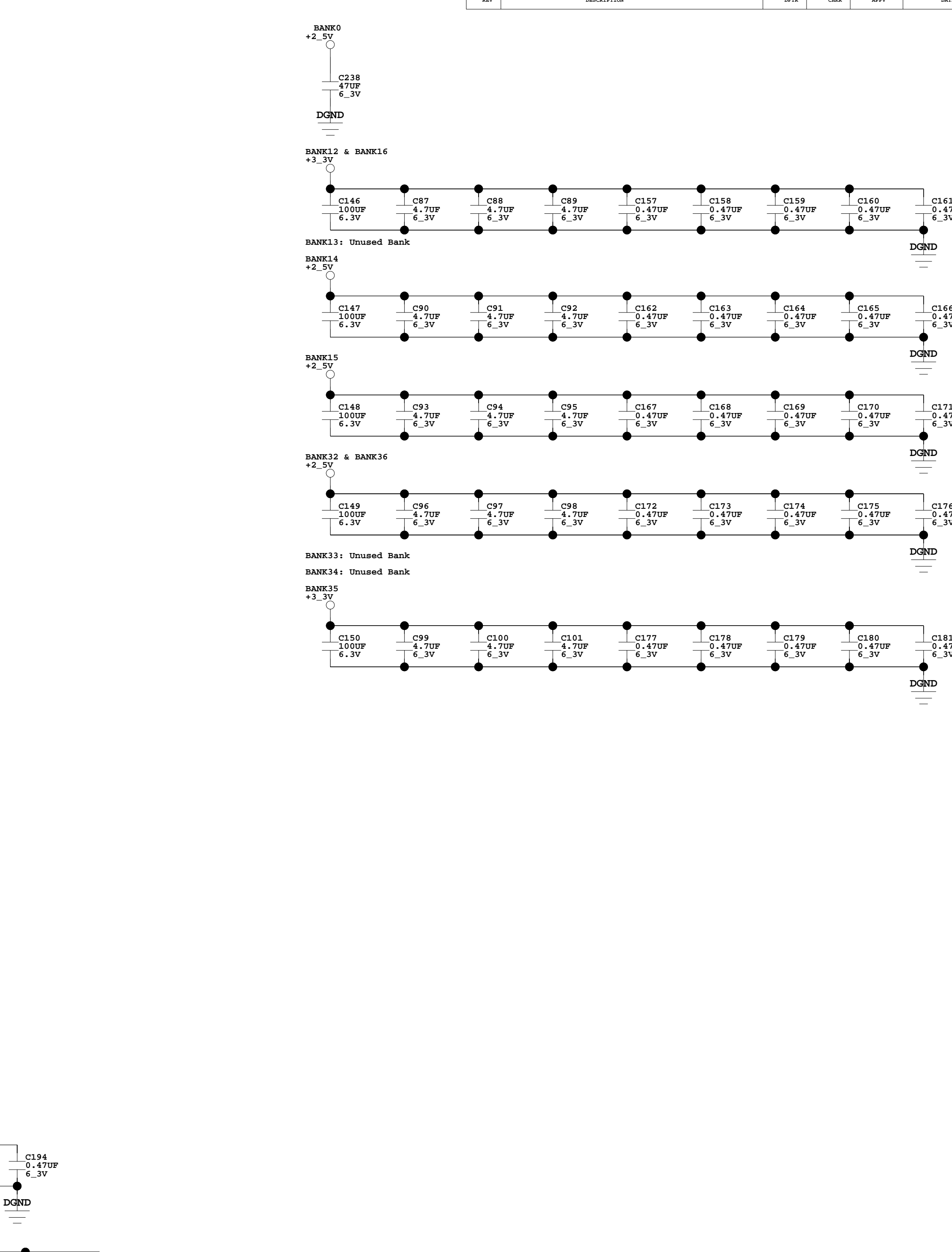
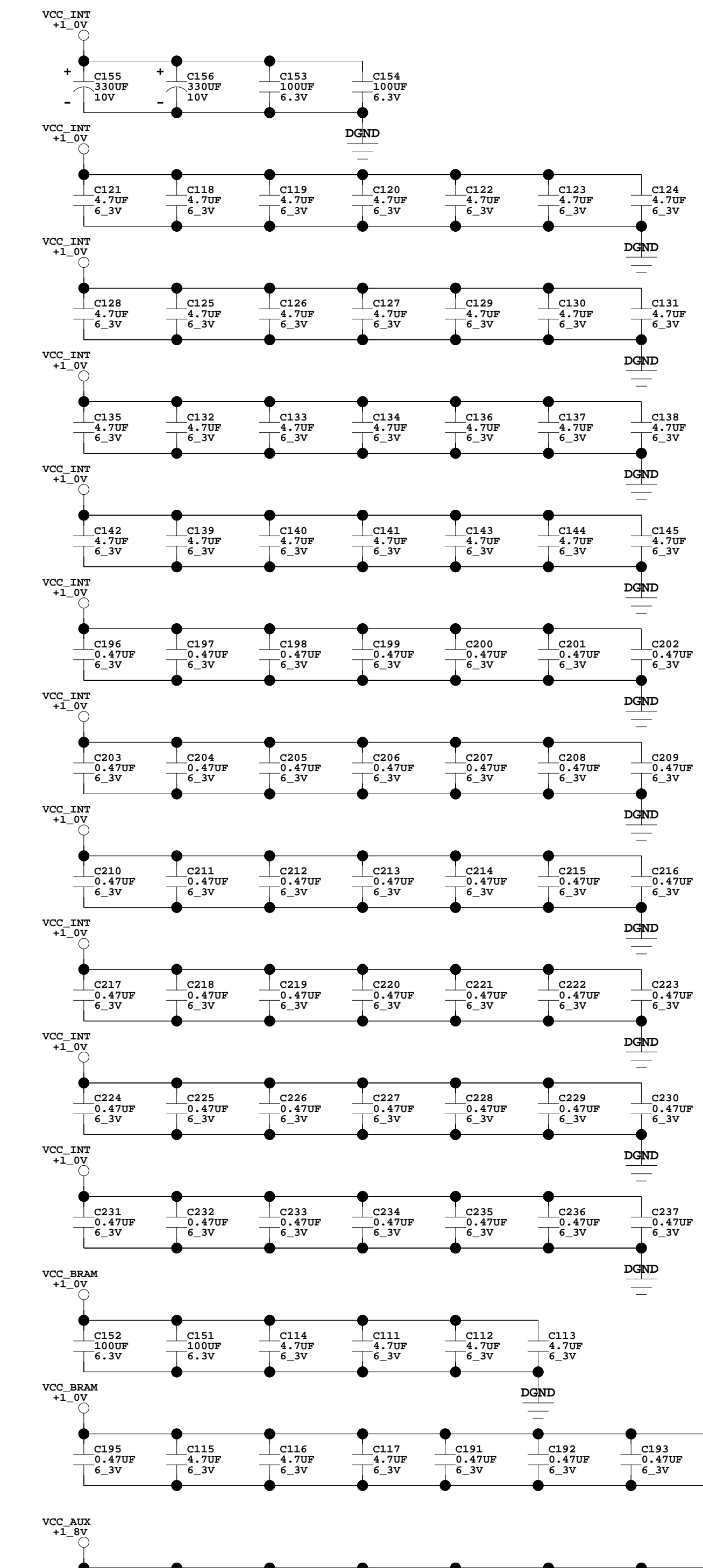
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K99	VCCINT_E99	
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U3  
part 18 of 20  
xc7a200t\_ffgl156

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M99	VCCBRAM_M99	
M100	VCCBRAM_M100	

U3  
part 18 of 20  
xc7a200t\_ffgl156

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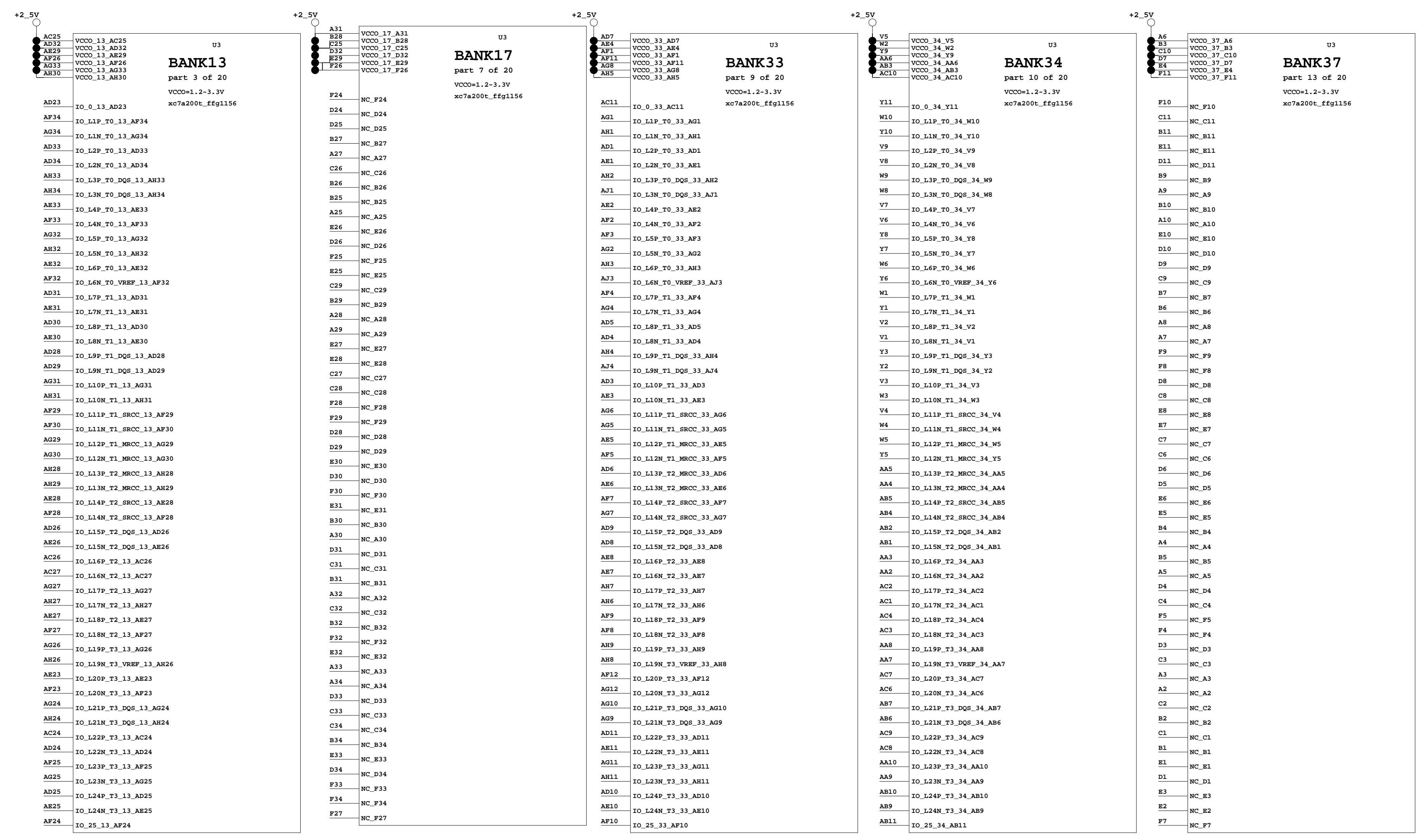


Place resistor close to FPGA input

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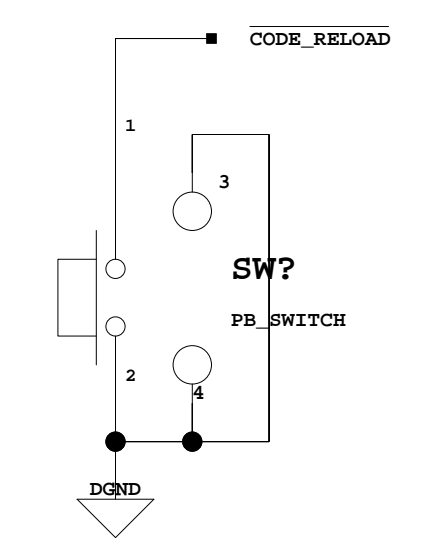
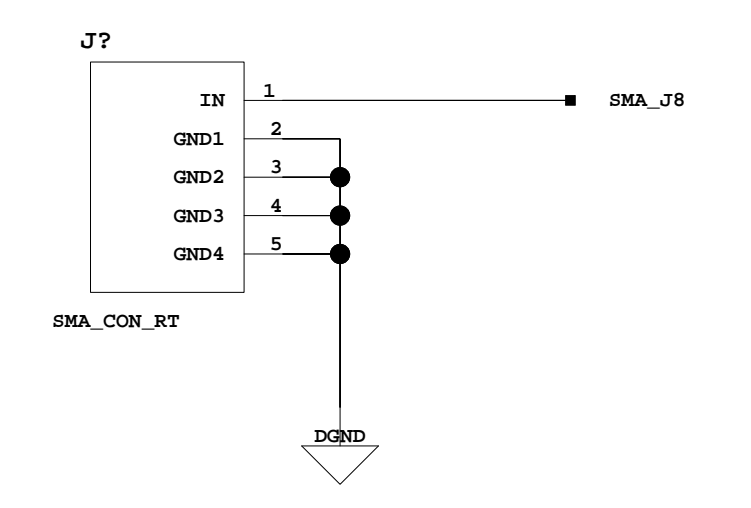
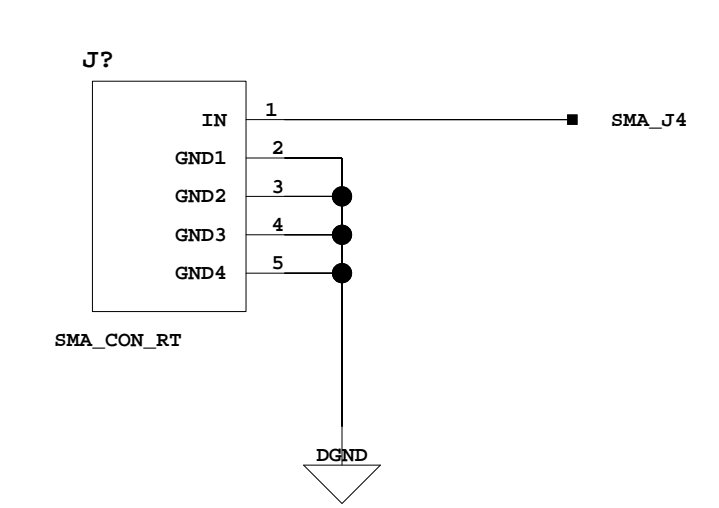
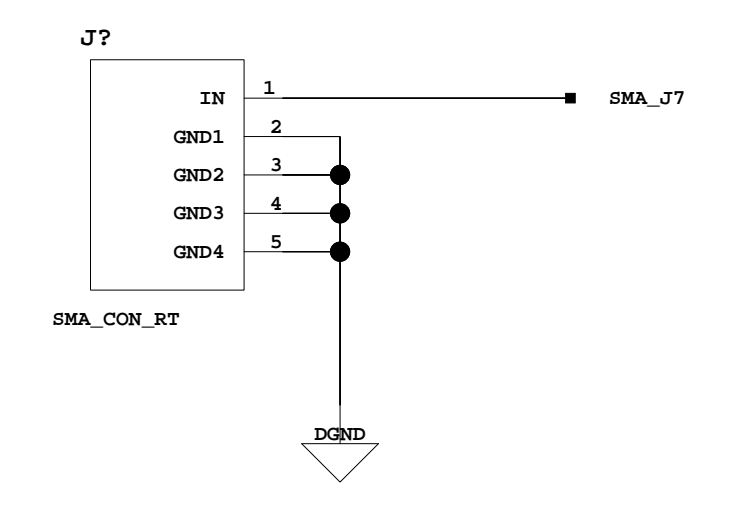
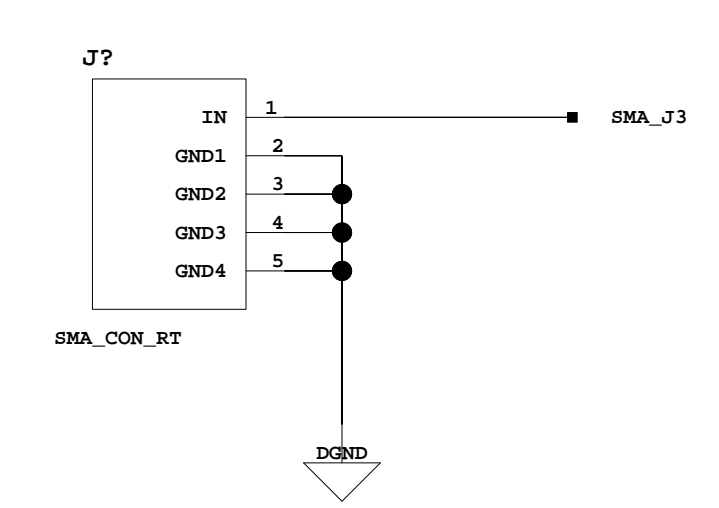
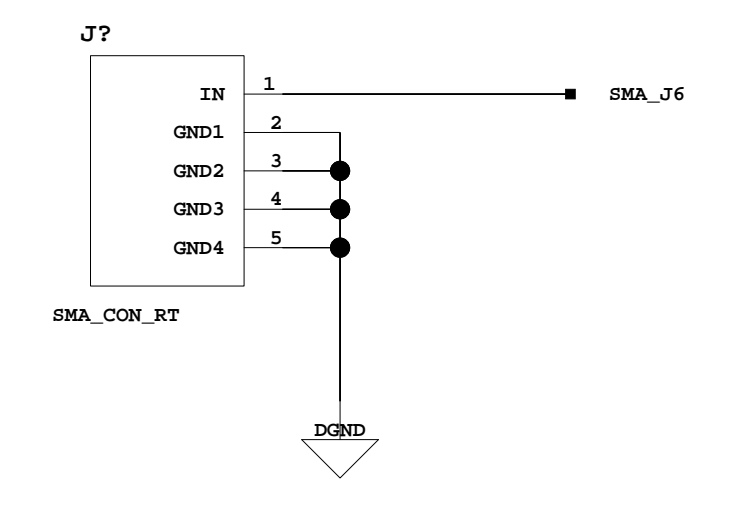
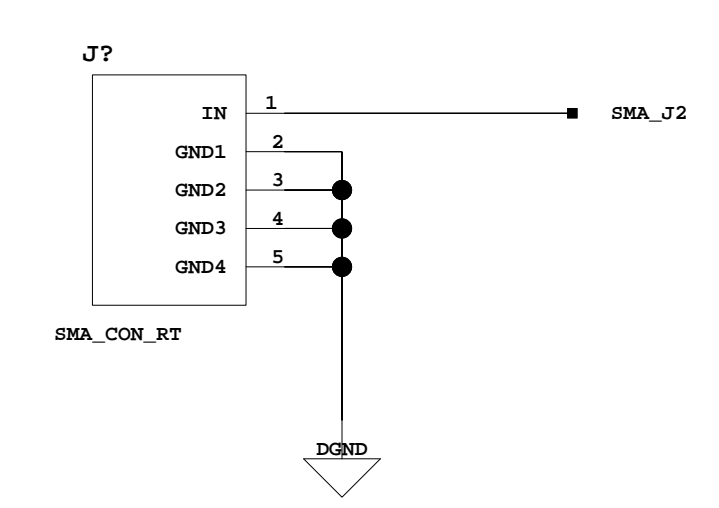
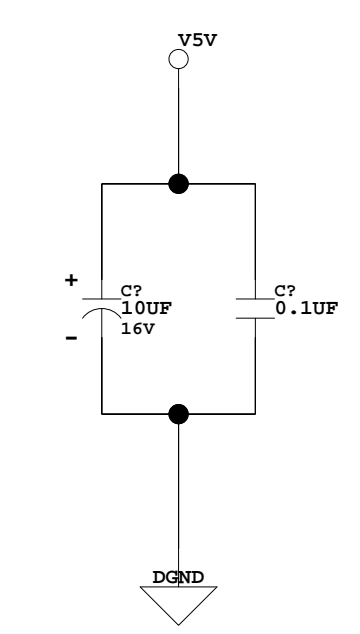
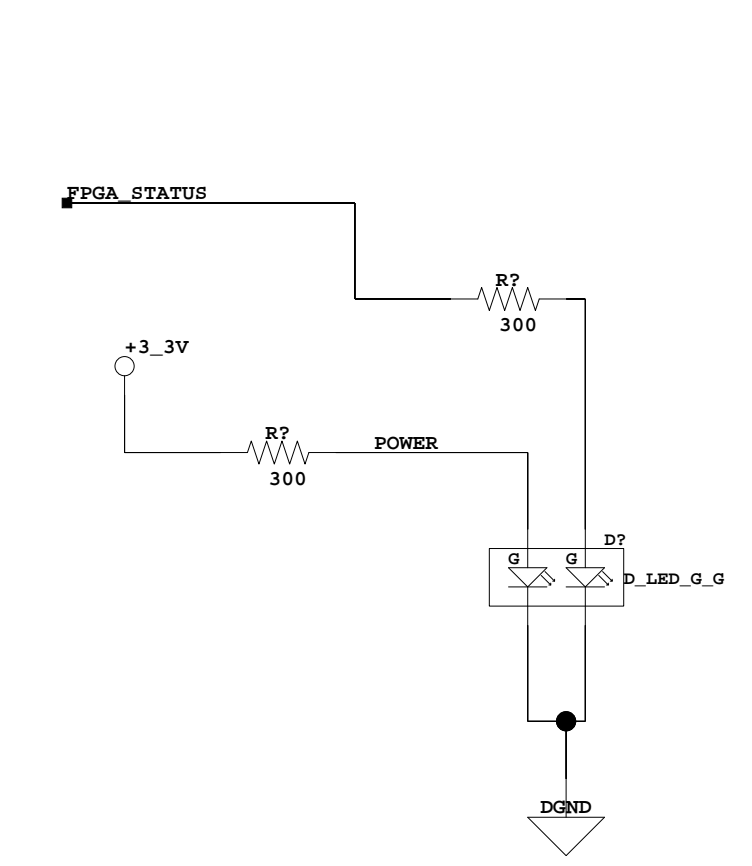
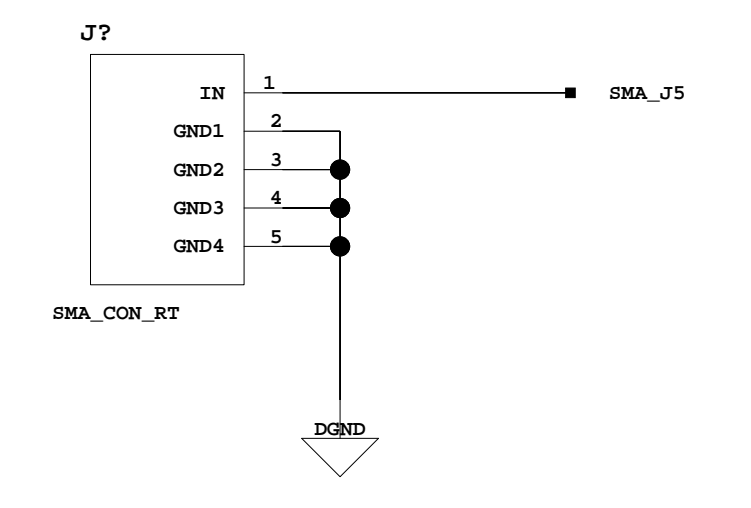
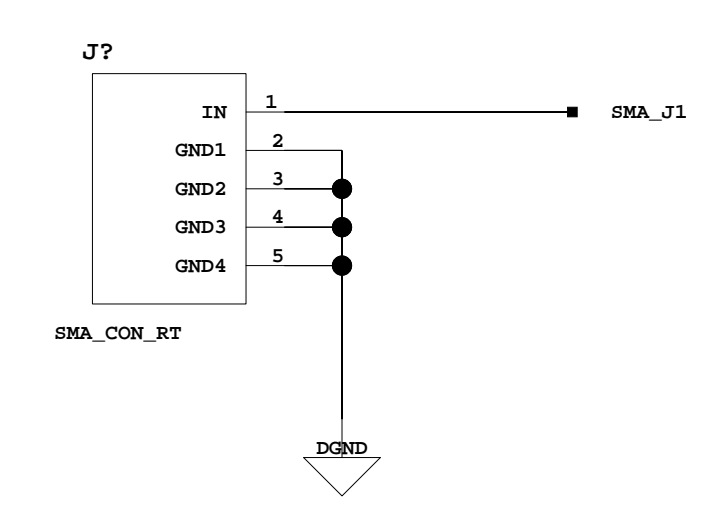
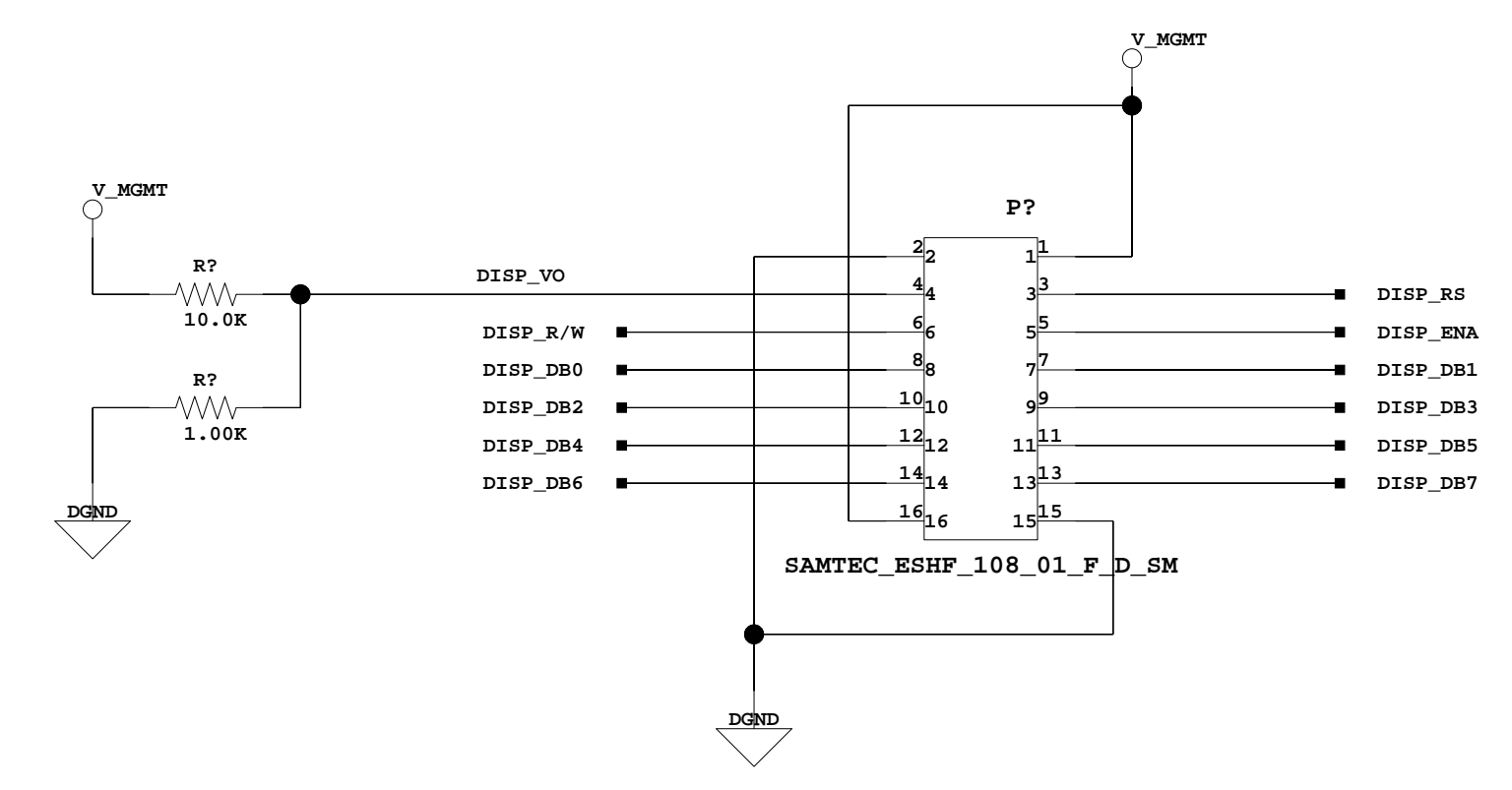
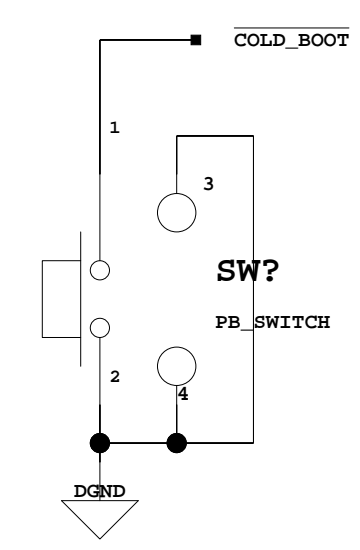
SLAC NATIONAL ACCELERATOR LABORATORY U.S. DEPARTMENT OF ENERGY		SHEET 6 OF 8
STANFORD UNIVERSITY STANFORD, CALIFORNIA		<b>FGP CARD Generation 3</b> <b>FPGA POWER Block</b>  LOCATED AT SHEET 1 SD-260-101-03-C00
PROPRIETARY DATA OF STANFORD UNIVERSITY AND/OR U.S. DEPARTMENT OF ENERGY. RECIPIENT SHALL NOT PUBLISH THE INFORMATION WITHIN UNLESS GRANTED SPECIFIC PERMISSION OF STANFORD UNIVERSITY.		
DATE 2013	APPROVALS Larry Ruckman	
OTHER INFORMATION		





04/11/2013:10:36

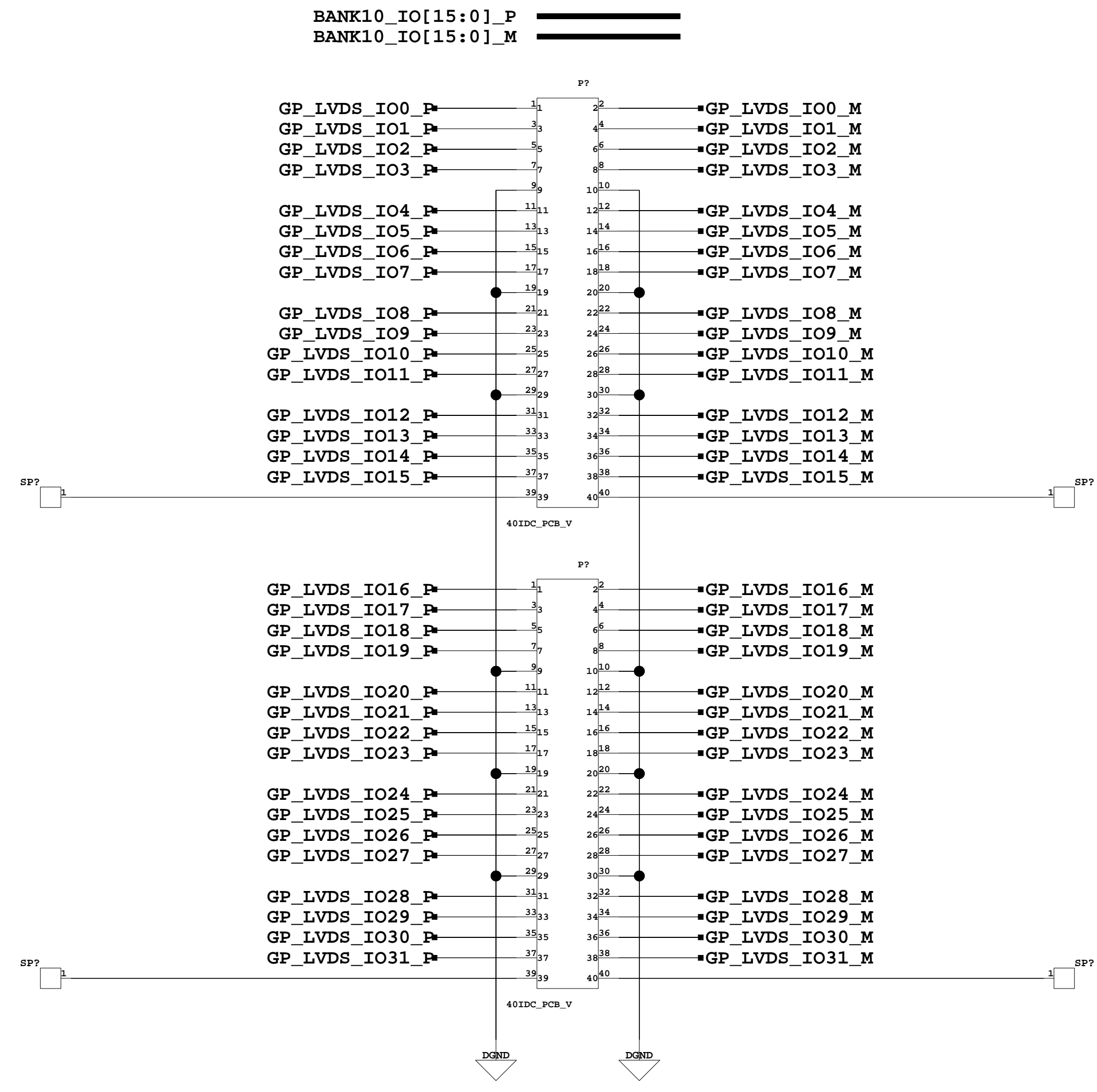
SLAC NATIONAL ACCELERATOR LABORATORY U.S. DEPARTMENT OF ENERGY <small>STANFORD UNIVERSITY STANFORD, CALIFORNIA</small>		SHEET 5 OF 8								
PROPRIETARY DATA OF STANFORD UNIVERSITY AND/OR U.S. DEPARTMENT OF ENERGY. RECIPIENT SHALL NOT PUBLISH THE INFORMATION WITHIN UNLESS GRANTED SPECIFIC PERMISSION OF STANFORD UNIVERSITY.		FGP CARD Generation 3 FPGA UNUSED BANK Block								
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DATE	APPROVALS									
2013	Larry Ruckman									



SMA\_J[8:1]

<b>SLAC NATIONAL ACCELERATOR LABORATORY</b> <b>U.S. DEPARTMENT OF ENERGY</b> <small>STANFORD UNIVERSITY STANFORD, CALIFORNIA</small>		
<small>PROPRIETARY DATA OF STANFORD UNIVERSITY AND/OR U.S. DEPARTMENT OF ENERGY. RECIPIENT SHALL NOT PUBLISH THE INFORMATION WITHIN UNLESS GRANTED SPECIFIC PERMISSION OF STANFORD UNIVERSITY.</small>		
ENGR	DATE	APPROVALS
DFTK		
CHKD		

<b>SHEET</b> <b>OF</b>  <b>SLAC</b>  <b>SD-</b>	<b>D</b>
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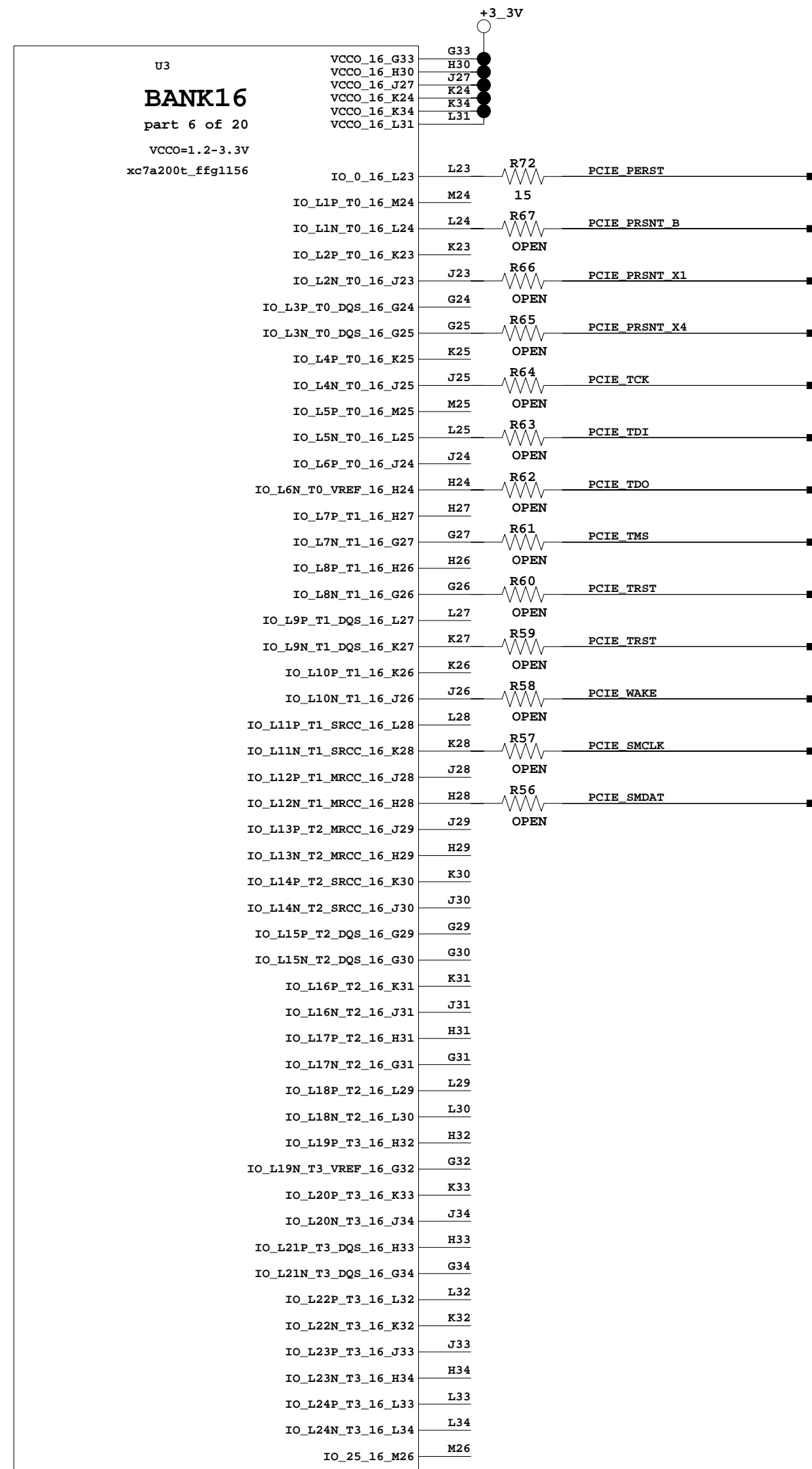
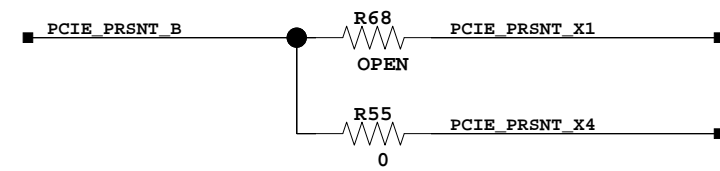
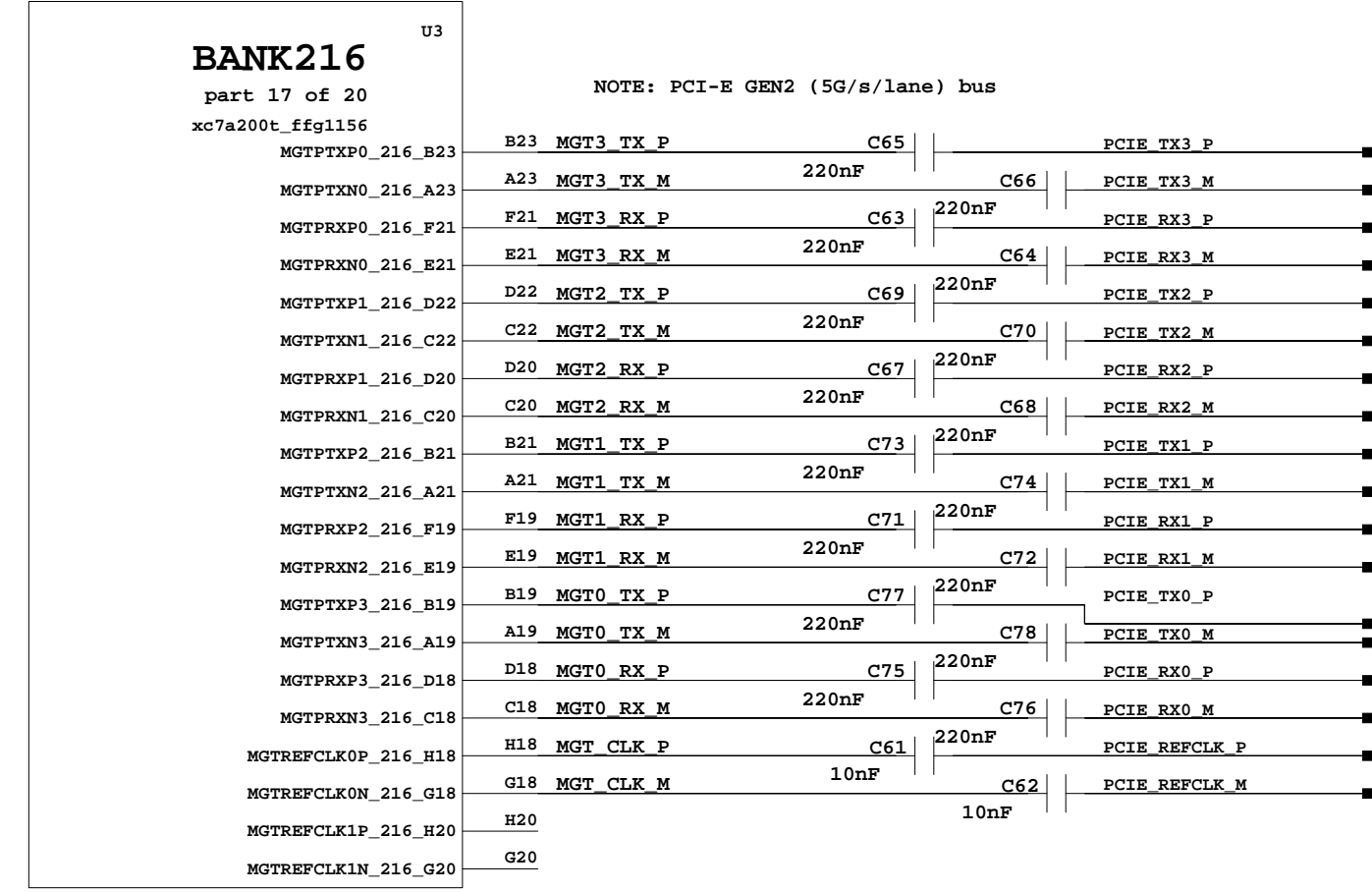


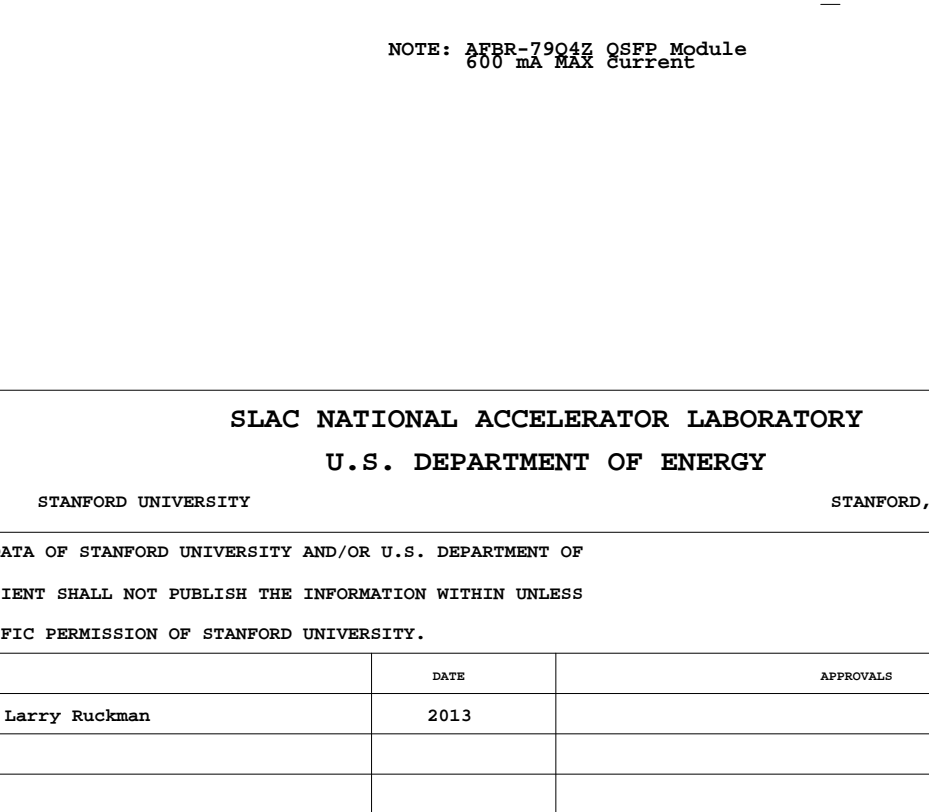
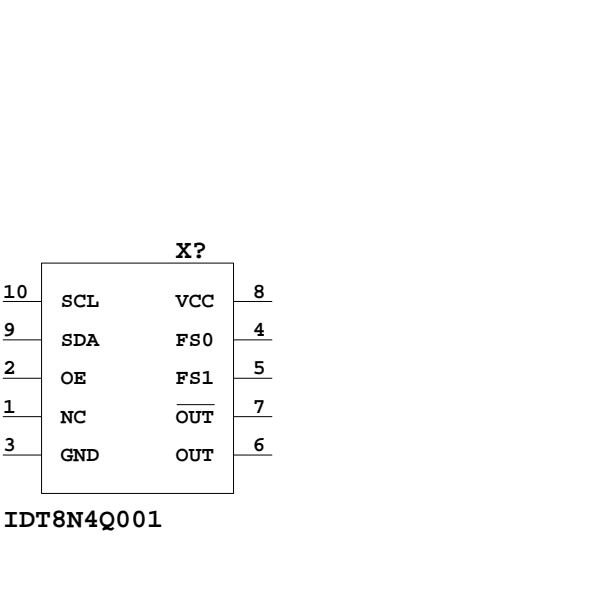
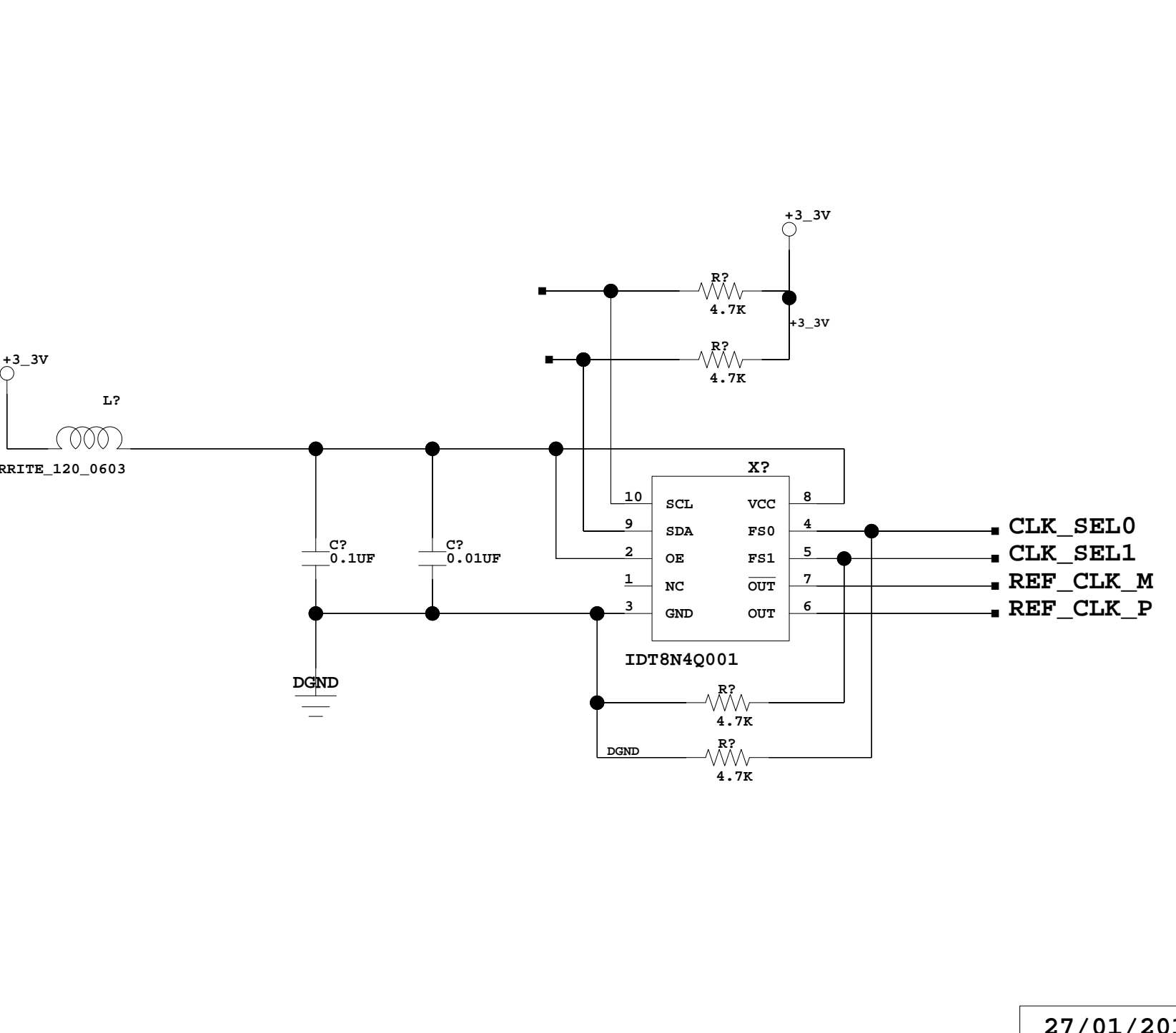
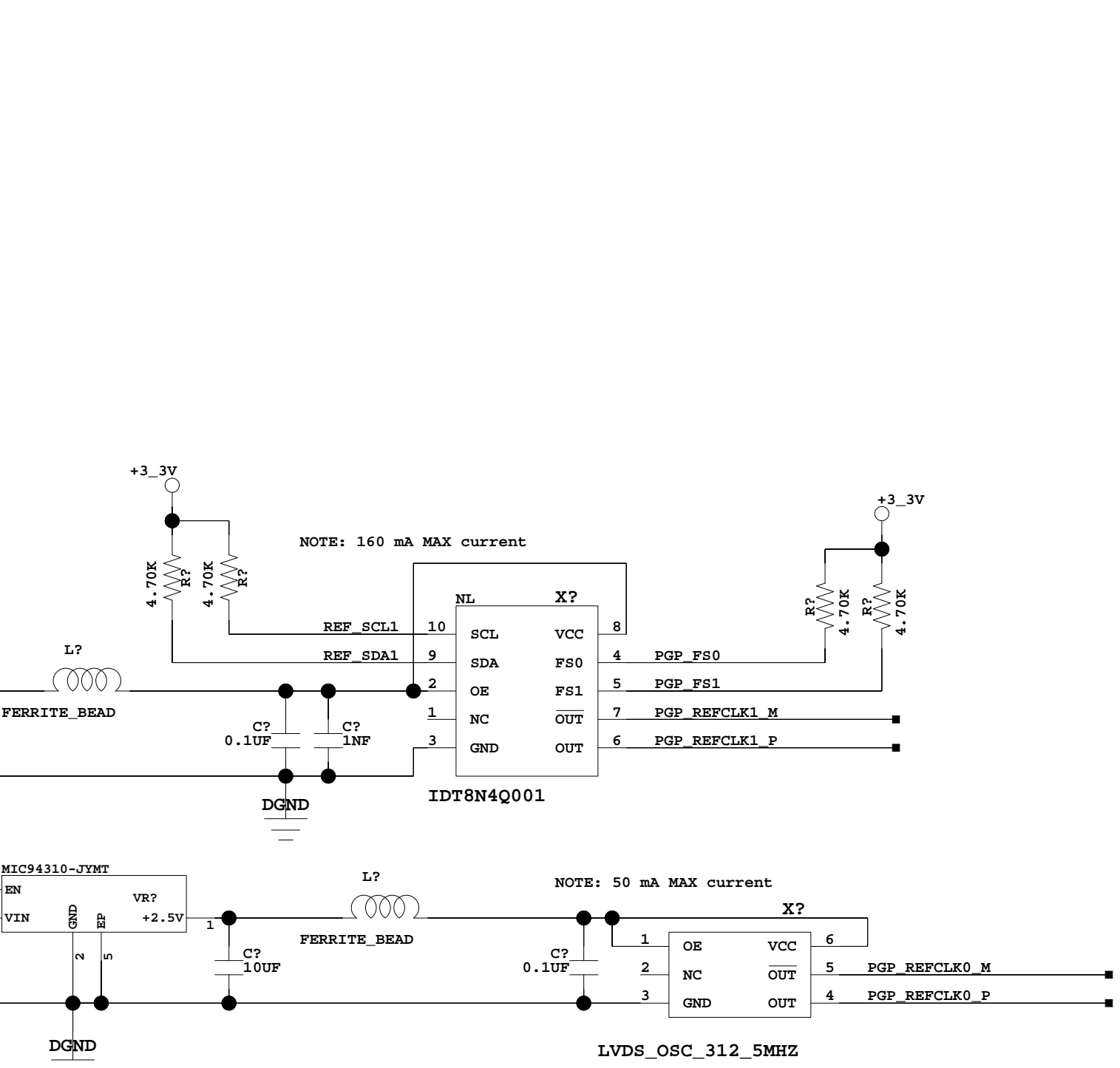
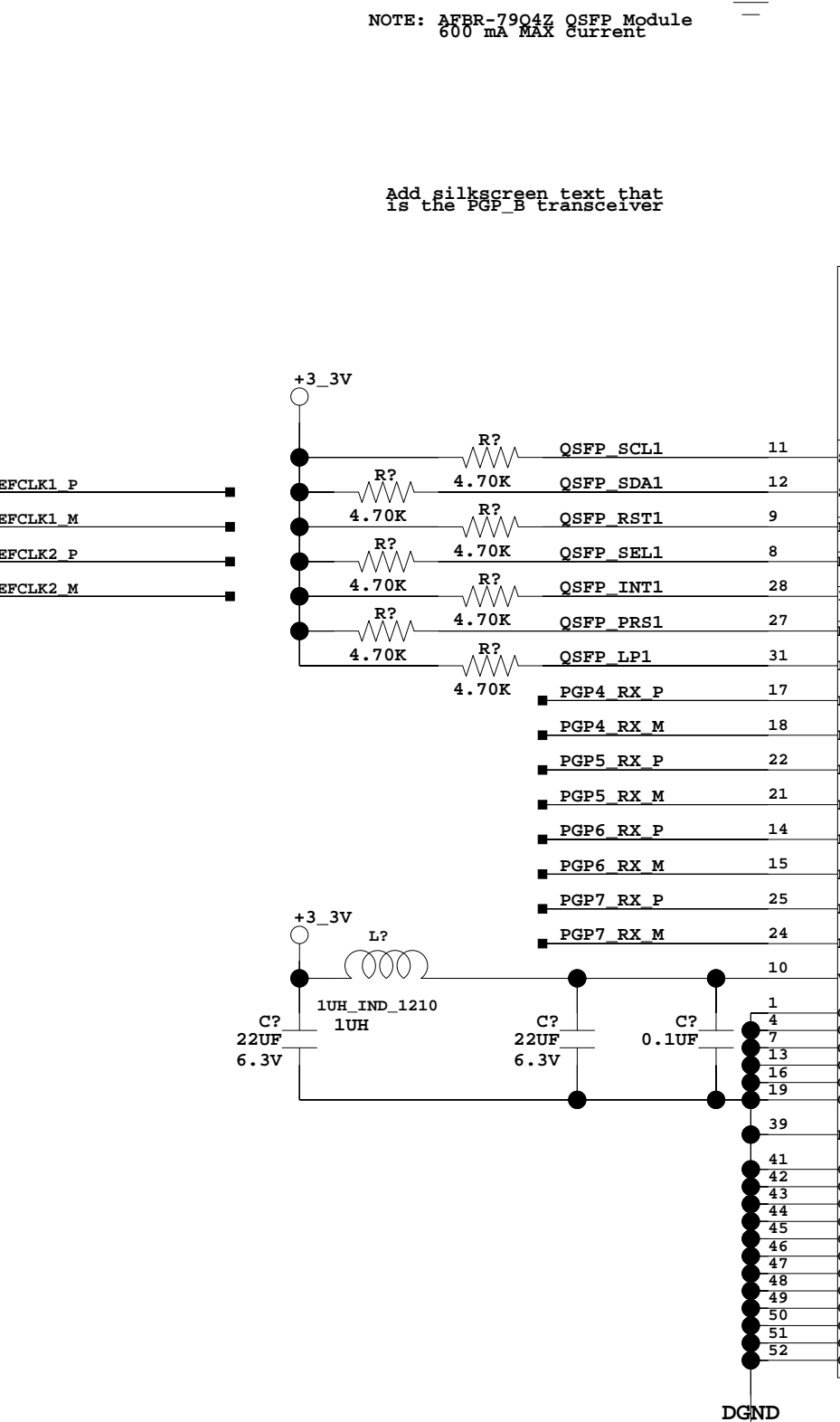
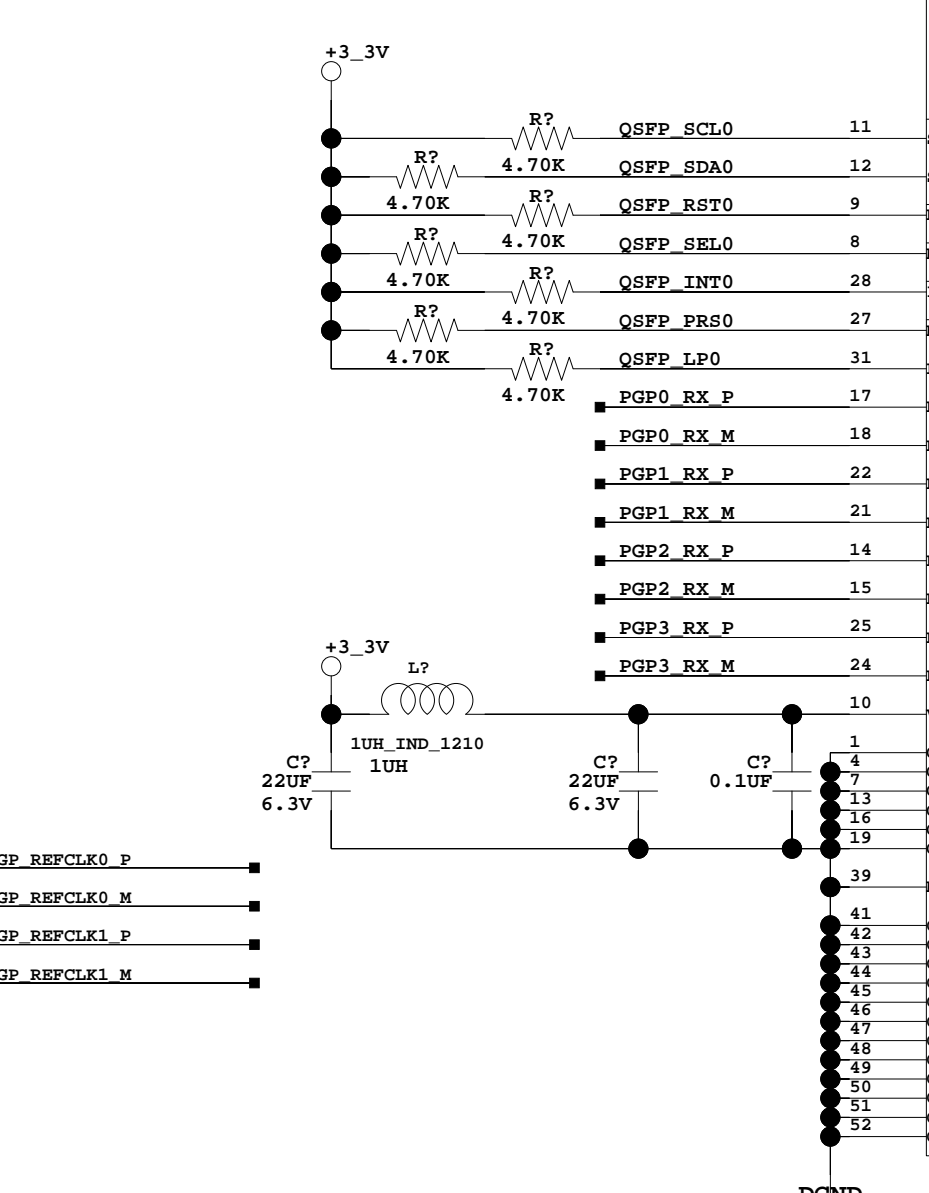
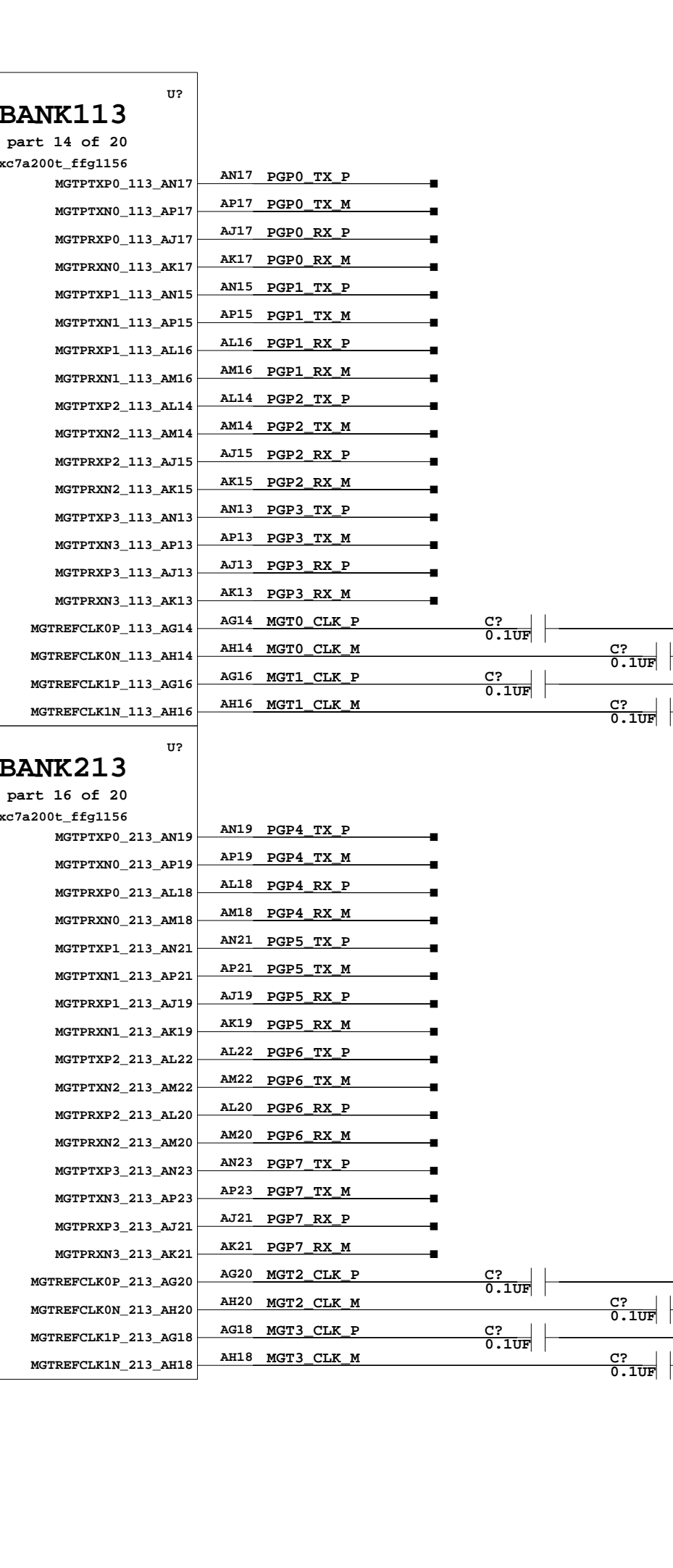
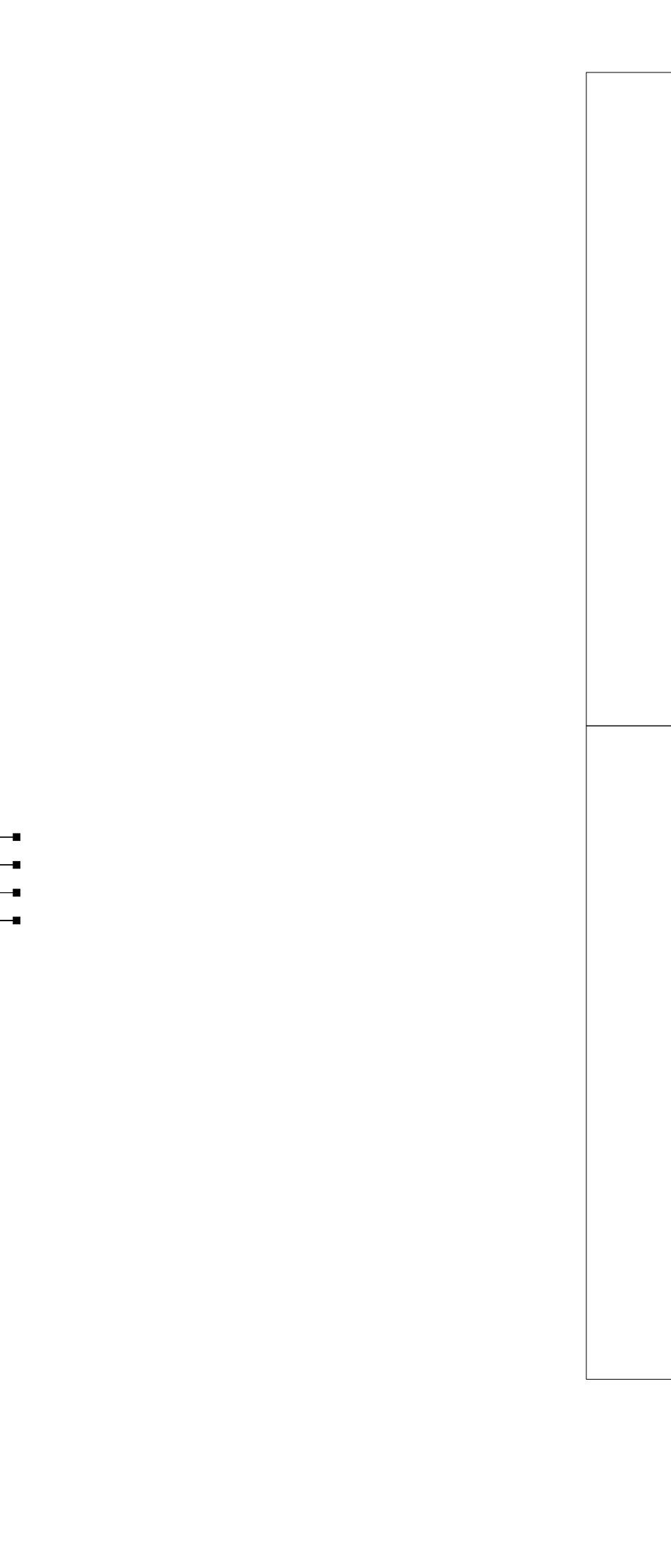
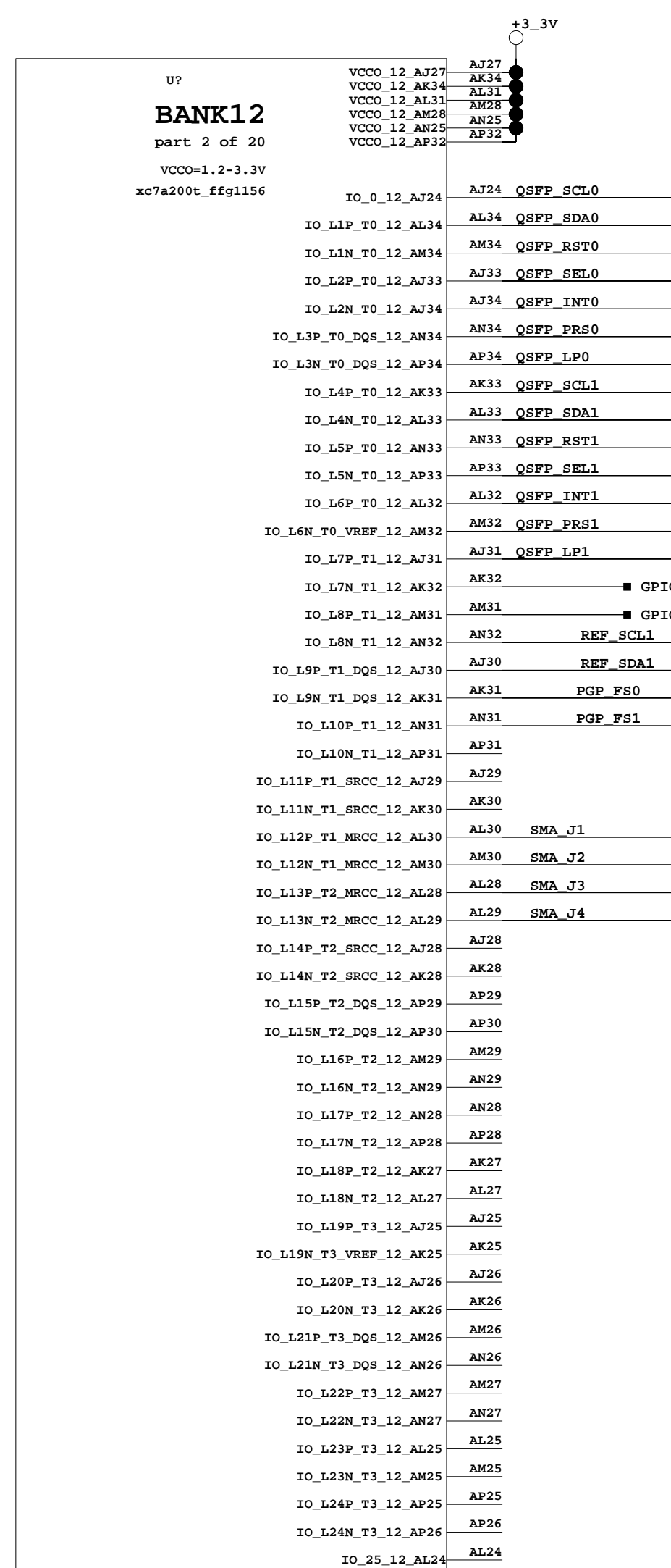
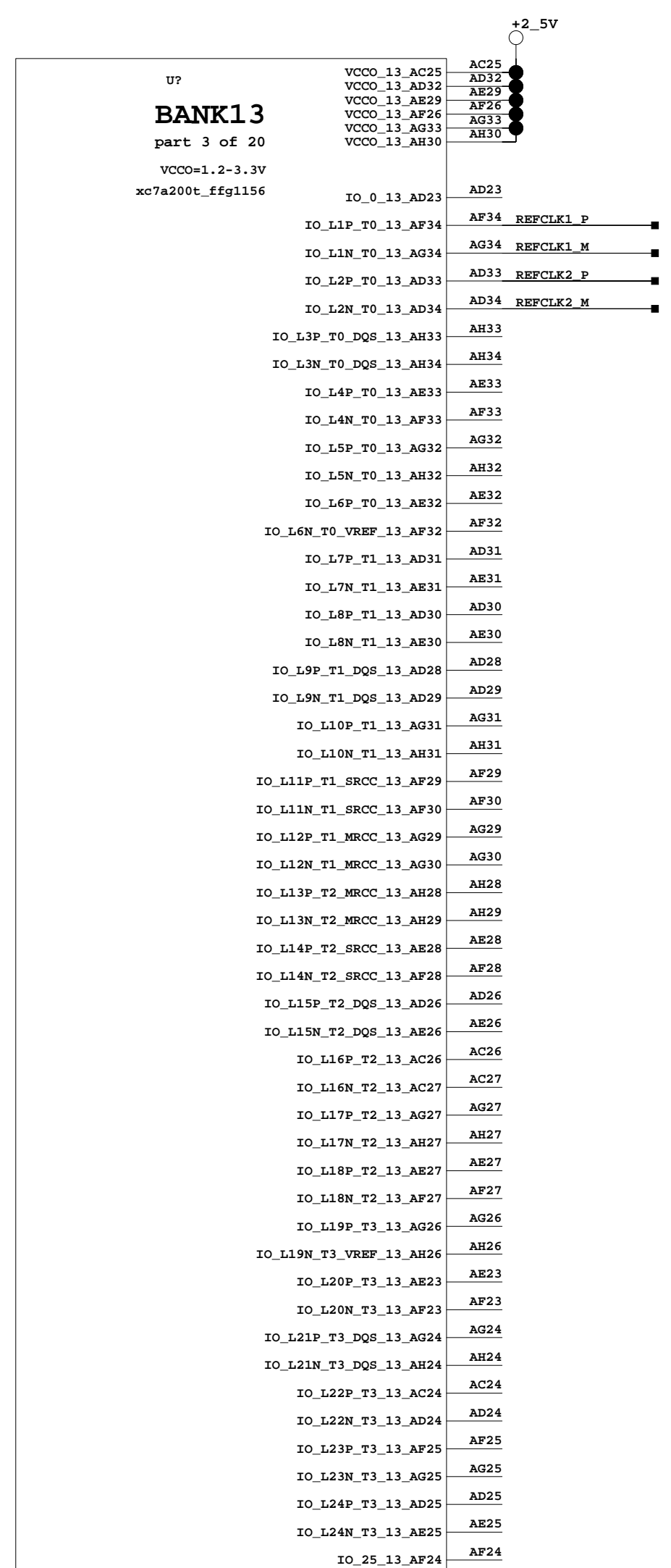
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ENR	DATE	APPROVALS

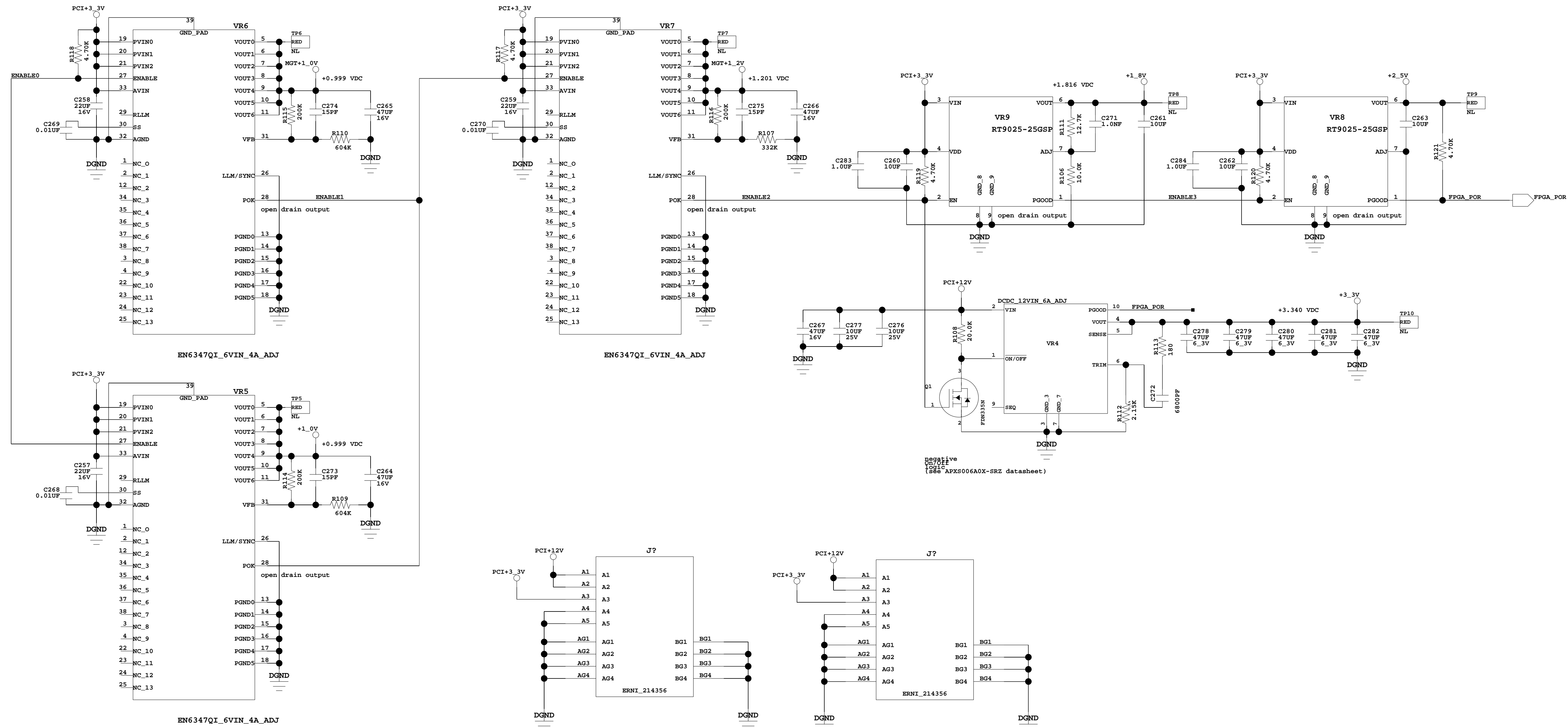
SHEET	OF
SLAC	
SD-	D

# NOTE: Not 10W slot Compatible

NOTE: PCI-E Hard IP core located in U3, and U3 group 216 (GIP\_X0V4, GIP\_X0V5, GIP\_X0V6, and GIP\_X0V7)

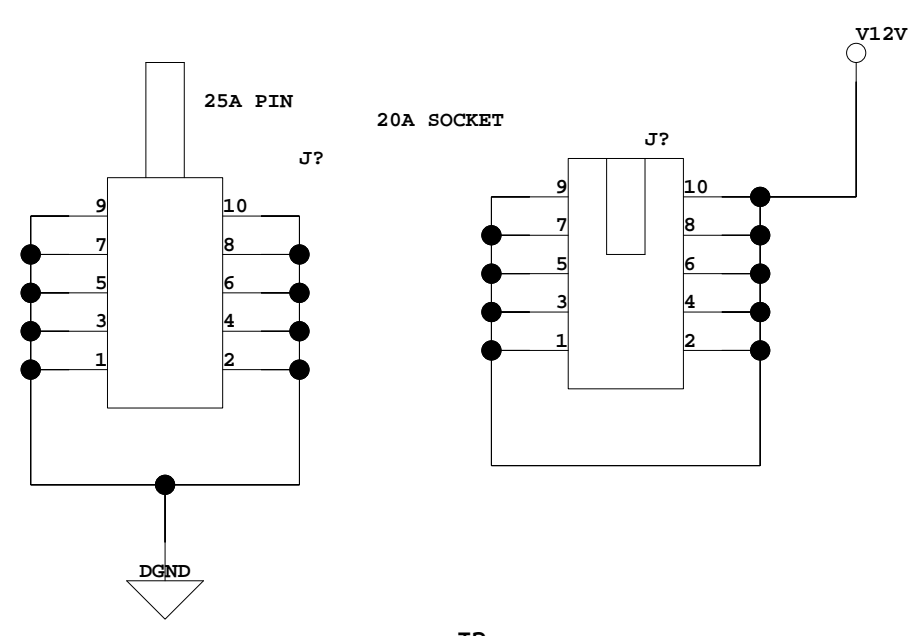






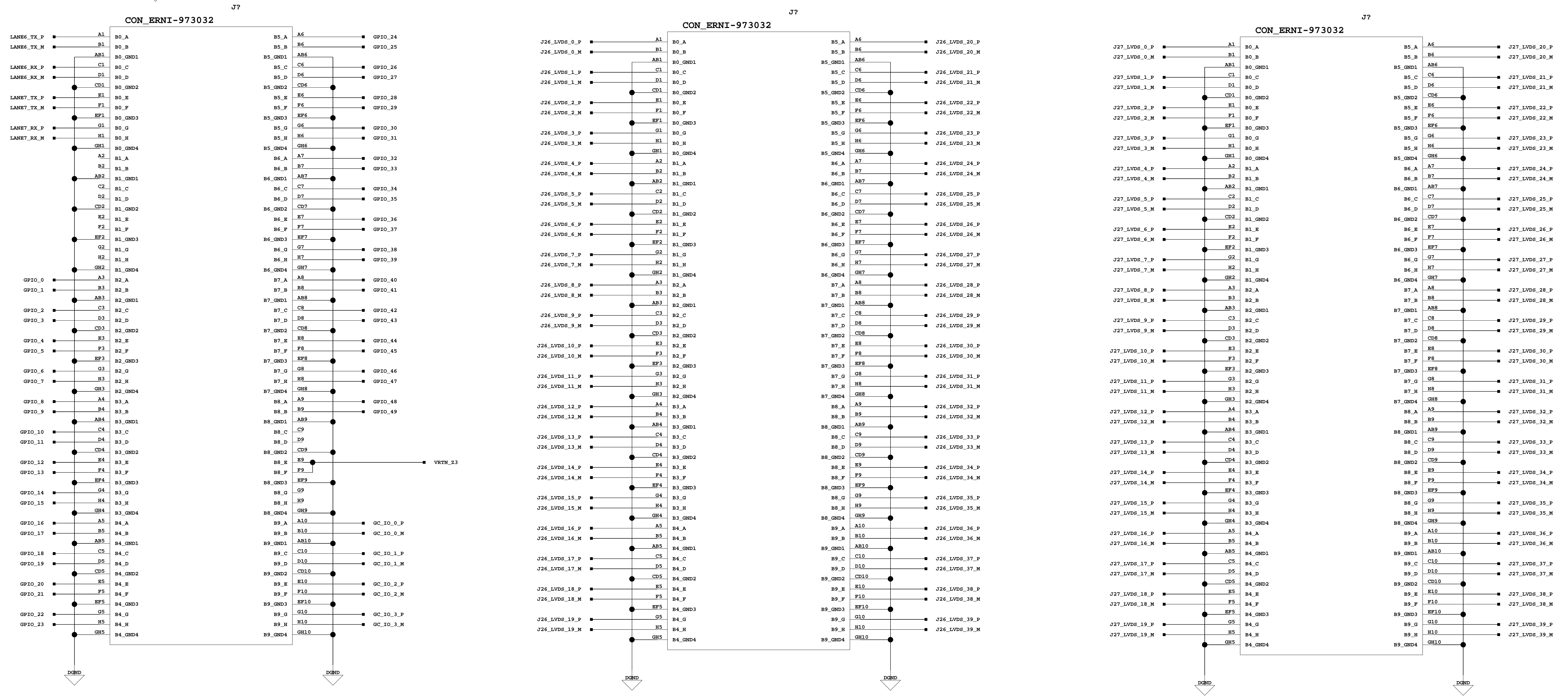
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STANFORD UNIVERSITY STANFORD, CALIFORNIA		PGP CARD Generation 3 Power Regulation Block
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DATE	APPROVALS	LOCATED AT SHEET 1 SD-260-101-03-C00
DRN Larry Ruckman	2013	
DFR		
CDR		



J26\_LVDS\_[31:0]\_P  
 J26\_LVDS\_[31:0]\_M  
 J26\_LVDS\_[39:32]\_P  
 J26\_LVDS\_[39:32]\_M

J27\_LVDS\_[7:0]\_P  
 J27\_LVDS\_[7:0]\_M  
 J27\_LVDS\_[39:8]\_P  
 J27\_LVDS\_[39:8]\_M



GPIO\_[49:0]

LANE[7:6]\_TX\_P  
 LANE[7:6]\_TX\_M  
 LANE[7:6]\_RX\_P  
 LANE[7:6]\_RX\_M  
 LANE[17:16]\_TX\_P  
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 LANE[17:16]\_RX\_P  
 LANE[17:16]\_RX\_M

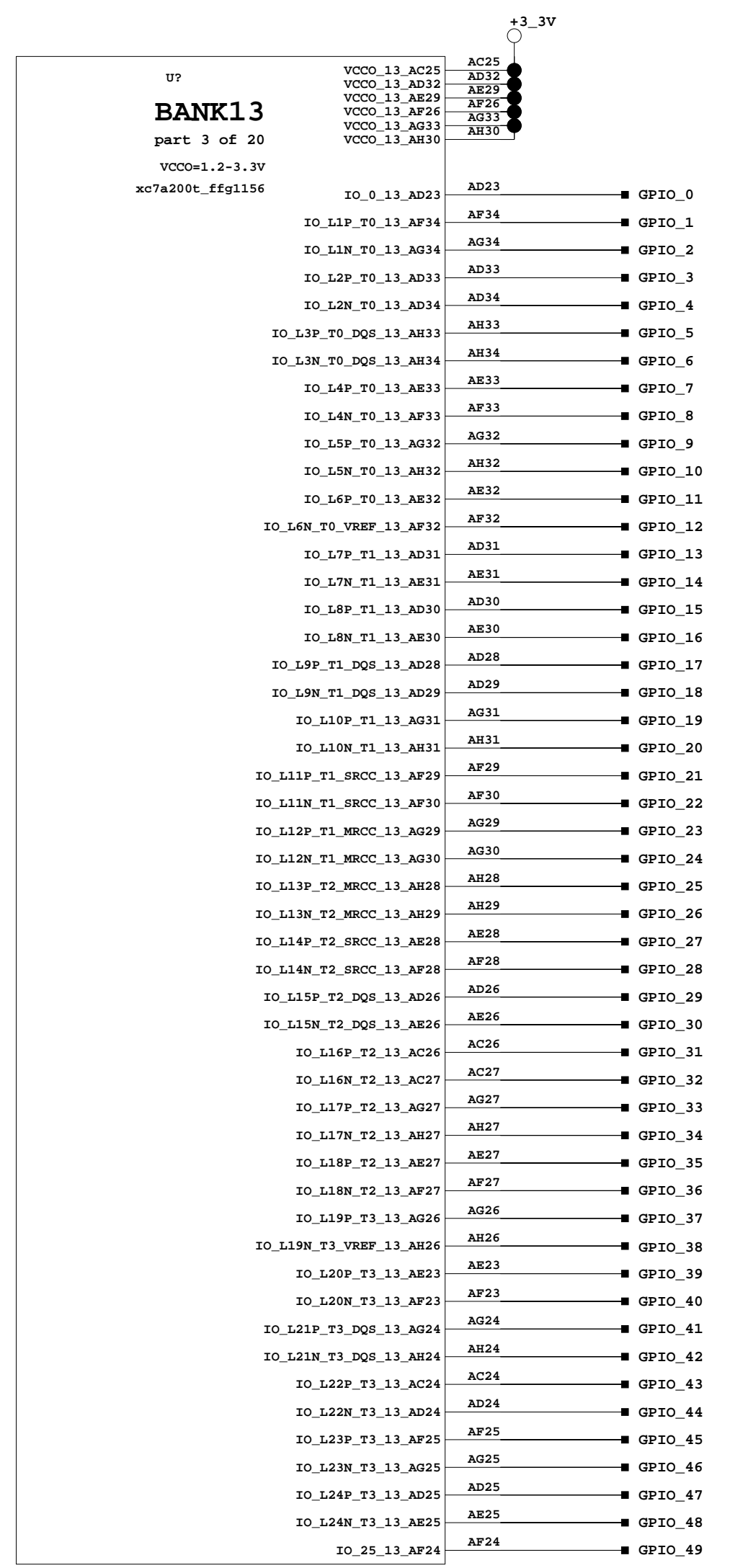
GC\_IO\_[3:0]\_P  
 GC\_IO\_[3:0]\_M

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DATE	APPROVALS



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ENR	DATE	APPROVALS

SHEET OF

**SLAC**

**SD-**

**D**



