

Characterization of CCPDv3 HV-CMOS sensors capacitively coupled to CLICpix 65 nm CMOS readout ASIC

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On behalf of the CLICdp Collaboration

Outline

- **The CLIC Accelerator and detector**
 - Machine characteristics
 - Detector requirements and Vertex R&D
- **Capacitively-coupled HV-CMOS assembly building blocks**
 - The CLICpix 65nm pixel ASIC prototype
 - The AMS 180nm CCPDv3 HV-CMOS sensor
- **Experimental setup and results**
 - Interconnect and readout development for the CLICpix + CCPDv3 assemblies
 - First test beam results
- **Conclusion**

CLIC and ILC machine, detectors and requirements

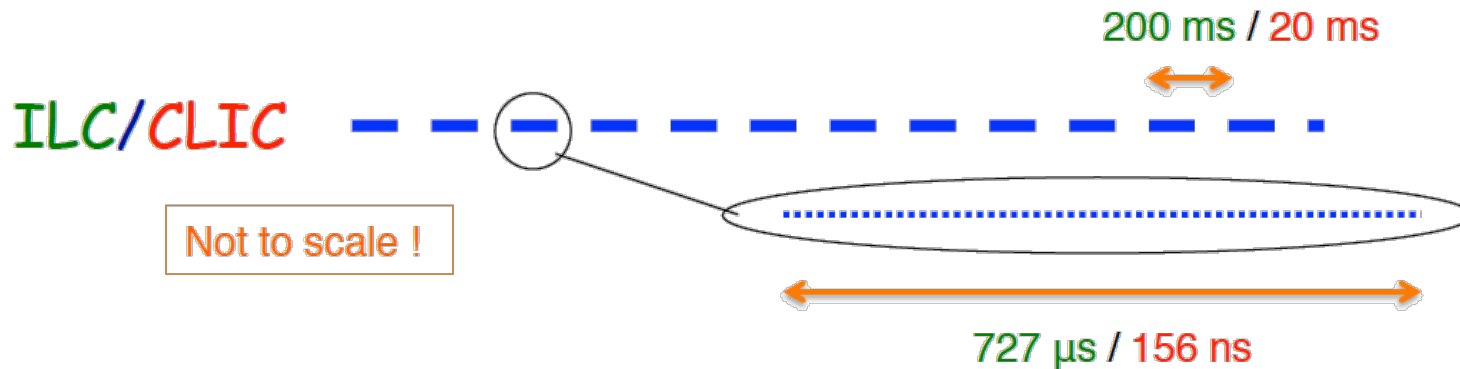
ILC versus CLIC machine environment

	ILC at 500 GeV	CLIC at 3 TeV
L (cm ⁻² s ⁻¹)	2x10 ³⁴	6x10 ³⁴
BX separation	554 ns	0.5 ns
#BX / train	1312	312
Train duration	727 μs	156 ns
Train repetition rate	5 Hz	50 Hz
Duty cycle	0.36%	0.00078%
σ _x / σ _y (nm)	474 / 6	≈ 45 / 1
σ _z (μm)	300	44

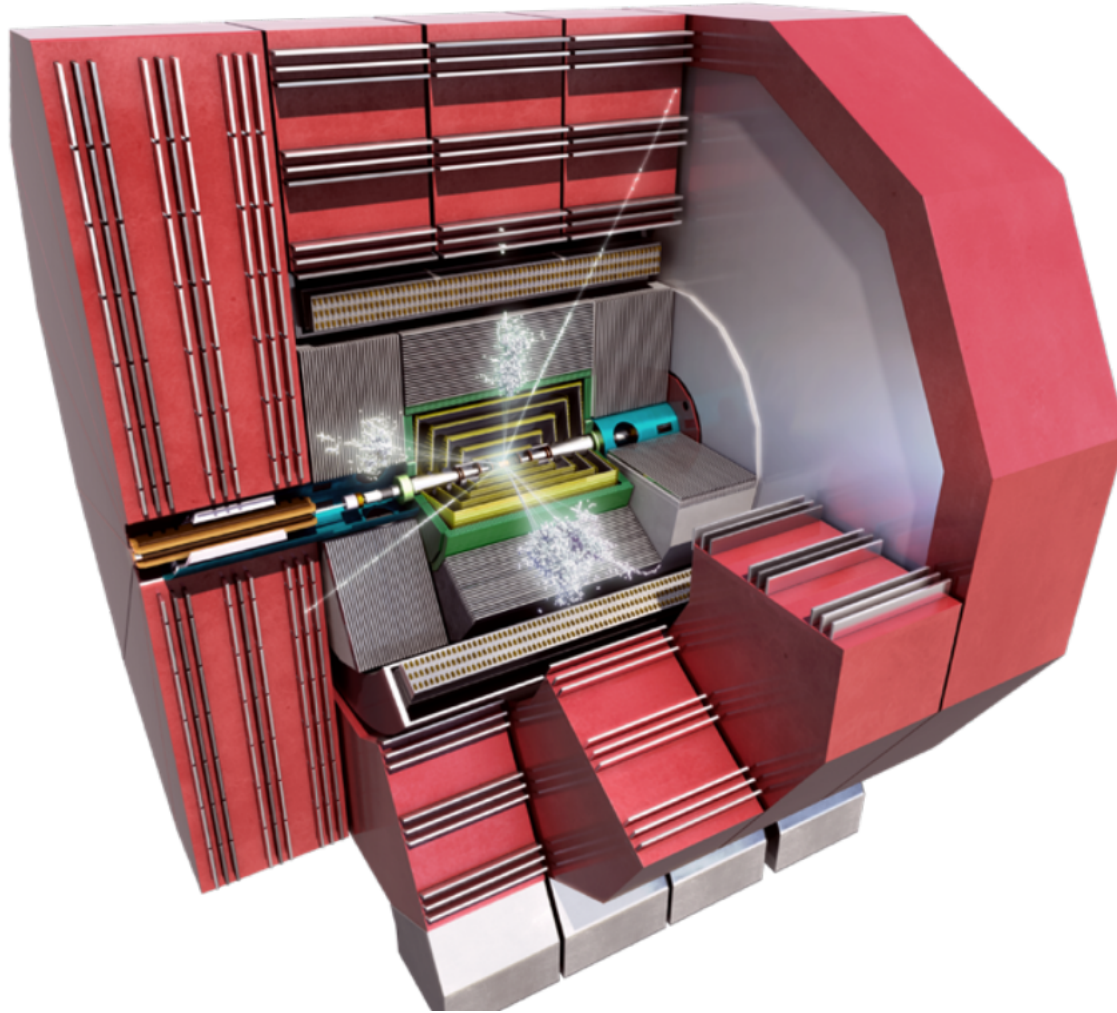
drives timing requirements for detectors

very small beam sizes → high rates of e⁺e⁻ and hadronic backgrounds

ILC ESD-2012/2 / CLIC CDR



The CLIC Detector



Precision physics in a challenging environment: broad programme of R&D

Highly granular particle flow calorimetry, using tungsten absorber

5.5 m diameter cryostat for superconducting solenoid, B field 4-5 T

All silicon tracker

Instrumented steel return yoke

Complex forward region

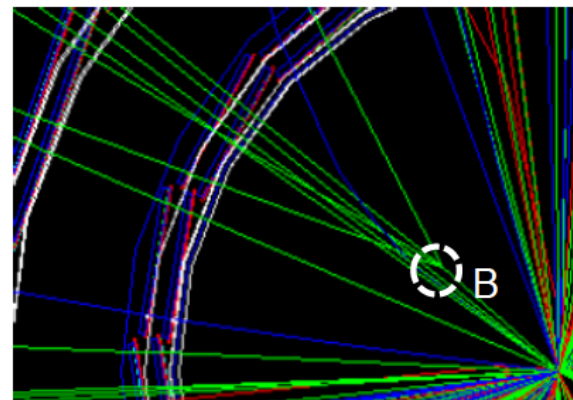
LC vertex-detector requirements

- efficient tagging of heavy quarks through precise determination of displaced vertices:

$$\sigma(d_0) = \sqrt{a^2 + b^2 \cdot \text{GeV}^2 / (p^2 \sin^3 \theta)}$$

$a \sim 5 \mu\text{m}, b \sim 10\text{-}15 \mu\text{m}$

- good single point resolution: $\sigma_{\text{SP}} \sim 3 \mu\text{m}$
 - small pixels $< \sim 25 \times 25 \mu\text{m}^2$, analog readout
- low material budget: $X \lesssim 0.1\text{-}0.2\% X_0$ / layer
 - corresponds to $\sim 100\text{-}200 \mu\text{m}$ Si, including supports, cables, cooling
 - low-power ASICs ($\sim 50 \text{ mW/cm}^2$) + gas-flow cooling



- 20-200 ms gaps between bunch trains → trigger-less readout, pulsed powering
- $B = 4\text{-}5 \text{ T}$ → Lorentz angle becomes important
- few % maximum occupancy from beam-induced backgrounds → sets inner radius
- moderate radiation exposure ($\sim 10^4$ below LHC!):
 - NIEL: $< 10^{11} \text{ n}_{\text{eq}}/\text{cm}^2/\text{y}$
 - TID: $< 1 \text{ kGy} / \text{year}$

- for CLIC: Time stamping with $\sim 10 \text{ ns}$ accuracy, to reject background
 - high-resistivity / depleted sensors, readout with precise time stamping

CLICpix + CCPD building blocks

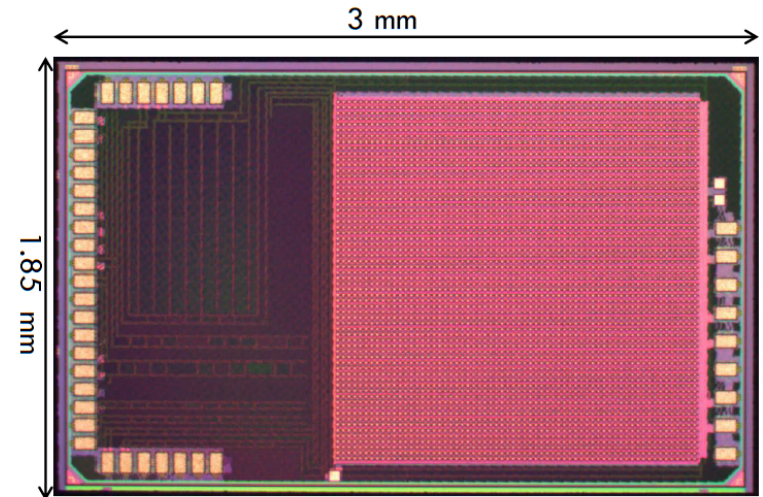
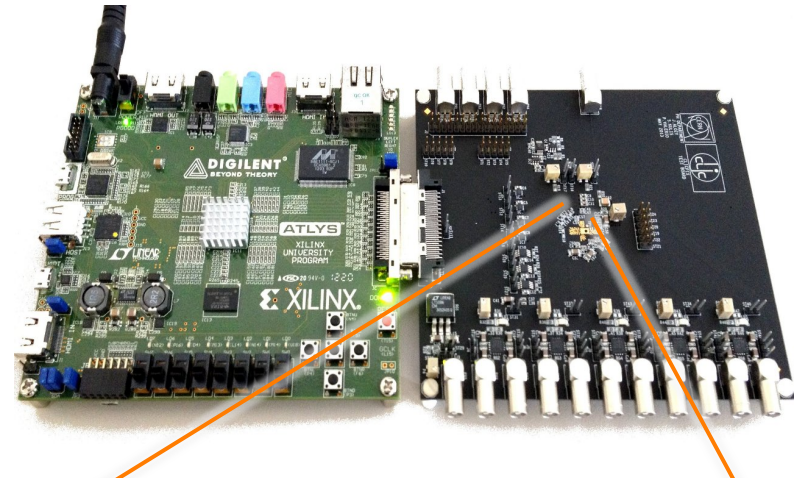
ASIC Development : CLICpix

Main features:

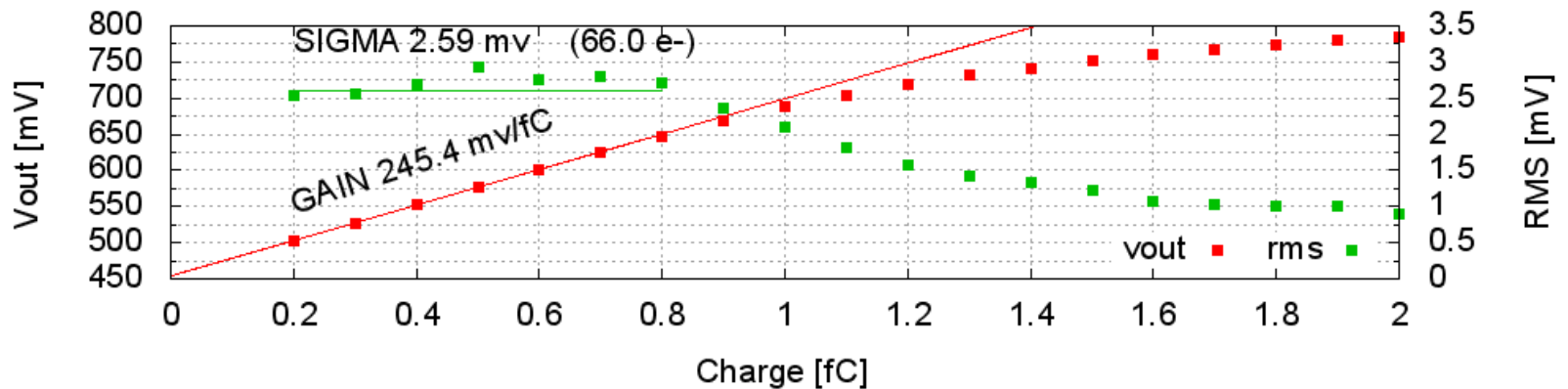
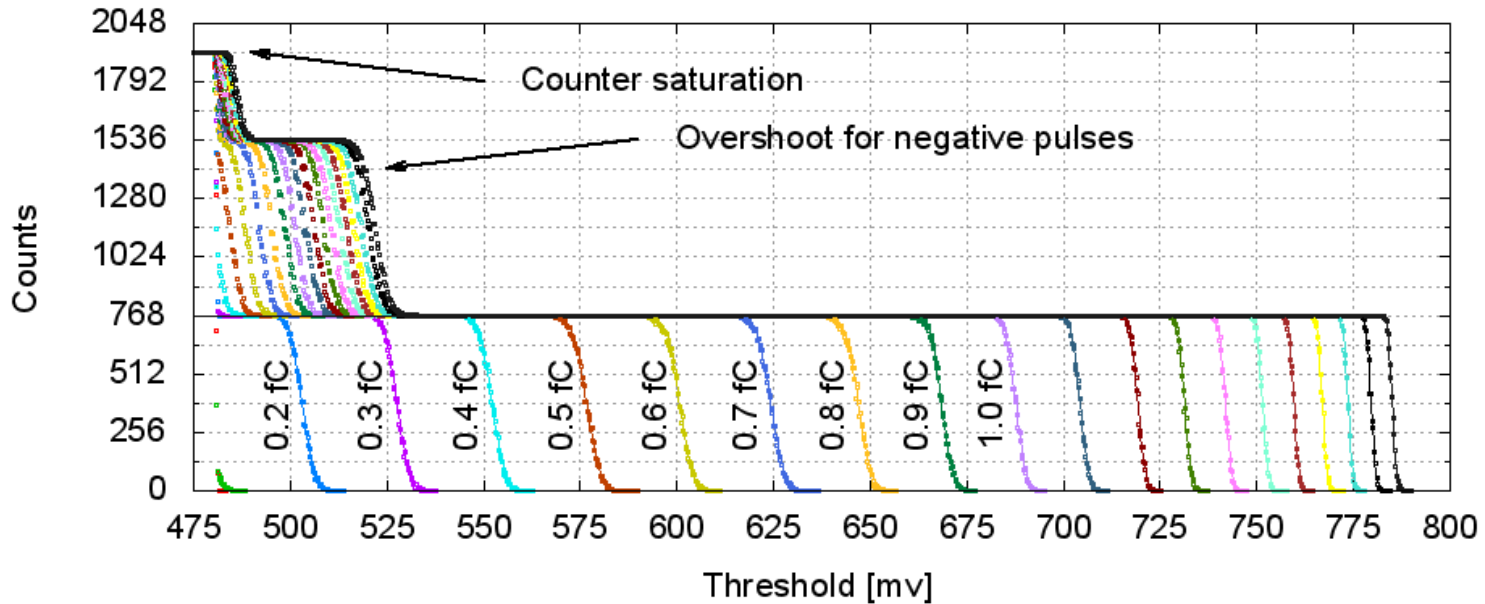
- Small pixel pitch (**25 μm**),
- **Simultaneous TOA (4 bits) & TOT (4 bits)** measurements
- **100MHz measurement clock** and **320 MHz** readout clock
- **Power pulsing**
- **Data compression**
- Both pulse polarities can be handled

Demonstrator CHIP:

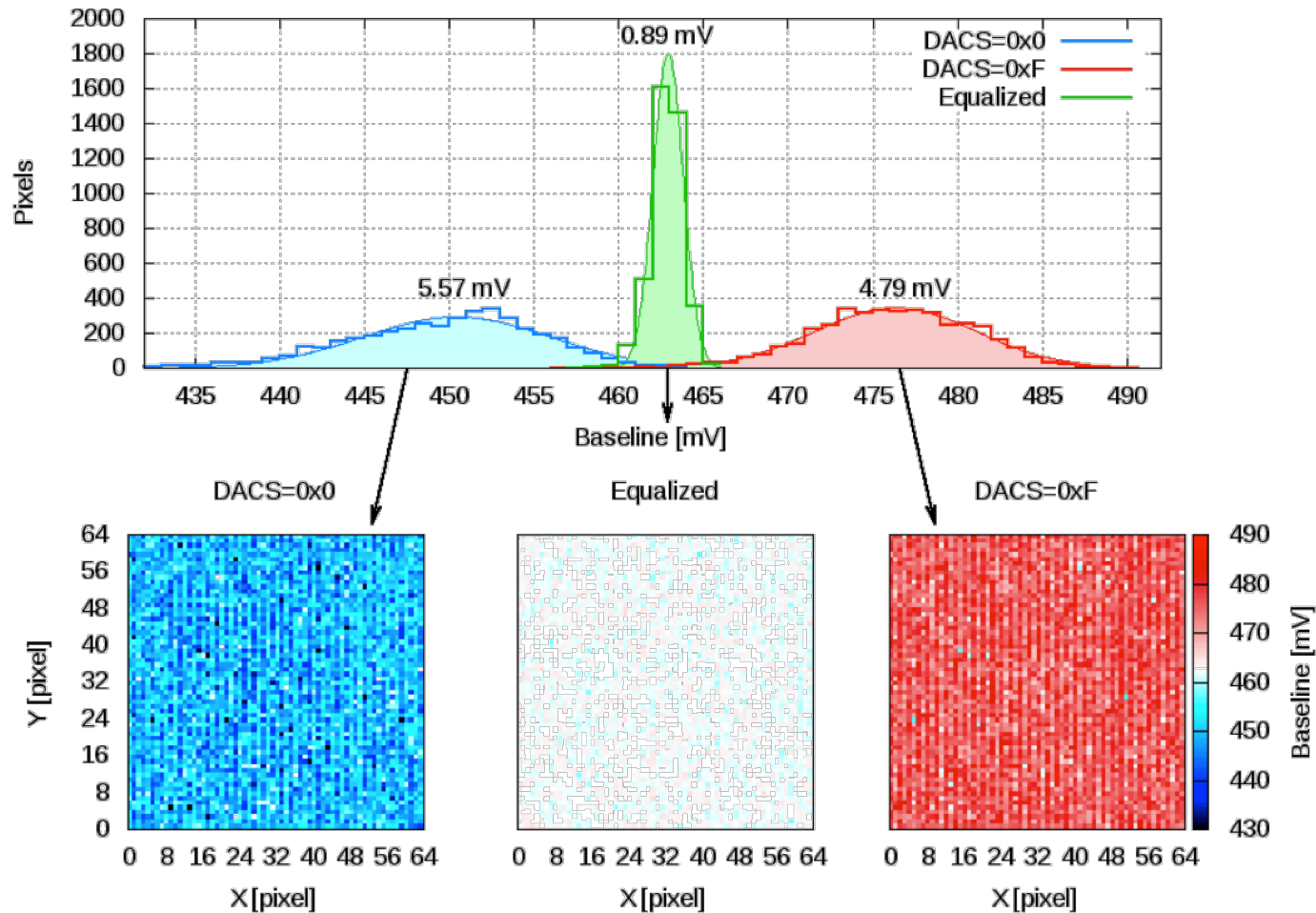
- commercial **65 nm CMOS technology** (proven to be radiation resistant)
- **array of 64x64** pixels
- The **Krummenacher architecture**, with a single ended preamp, a two stage discriminator and a 4-bit DAC



ASIC Development : CLICpix



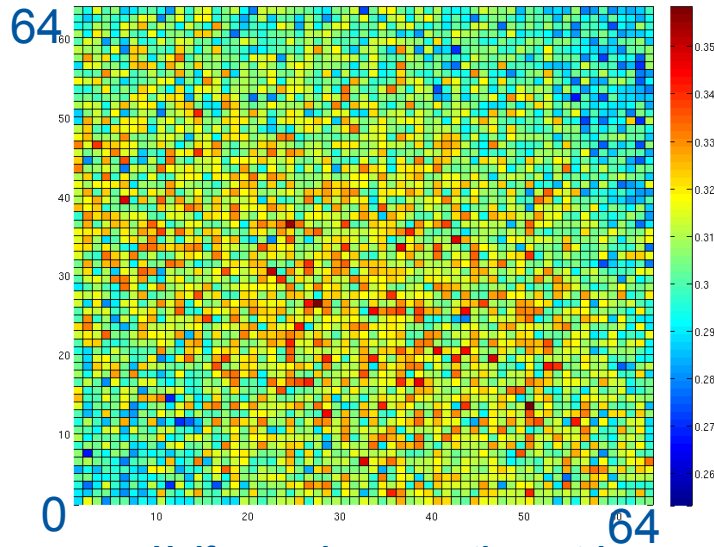
ASIC Development : CLICpix



Calibrated spread is 0.89 mV (about 22 e-) across the whole matrix

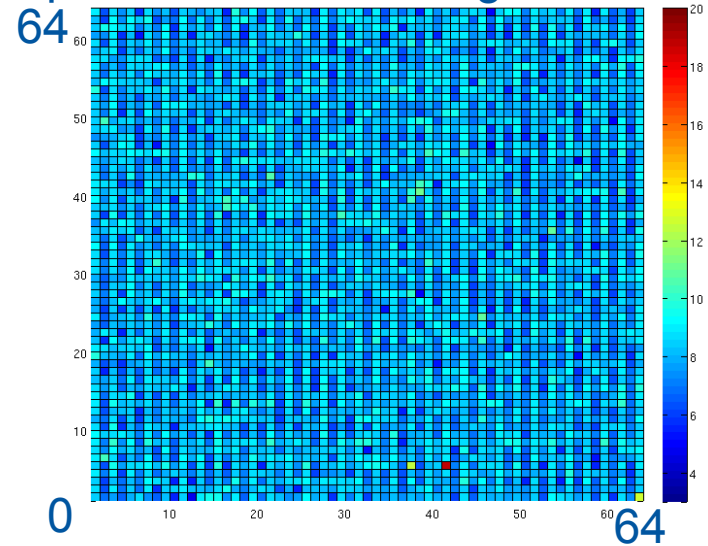
ASIC Development : CLICPix

TOT Gain Distribution



- Uniform gain across the matrix
- Gain variation is 4.2% r.m.s. (for nominal feedback current)

Equivalent Noise Charge distribution



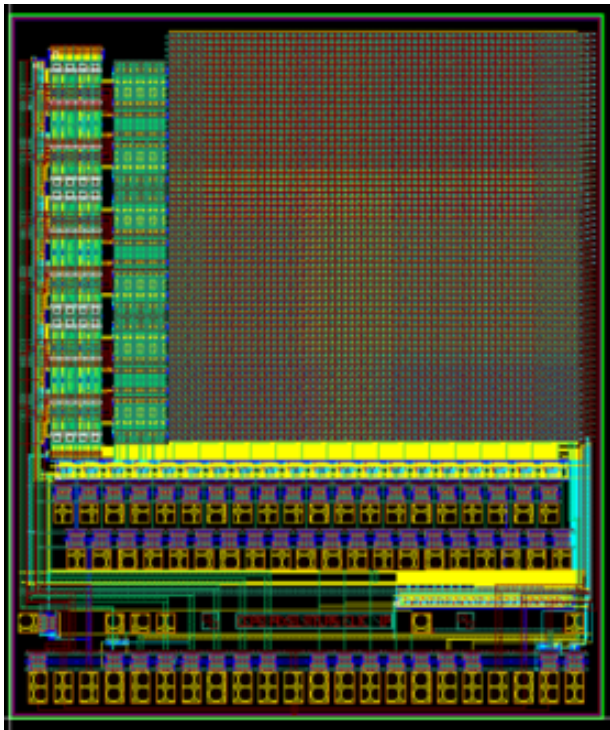
- Uniform ENC across the whole matrix
- Mean ENC is 55 e⁻ (without sensor)

- CLICPix prototype behave as expected from simulation and meet CLIC Vertex Detector specifications
- Hybridation to Sensor is an ongoing issue
 - Multi-Project Wafer -> Only single dies available
 - 25 μm pitch challenging for the industry
- Patterned noise found in the CLICpix design was found for one polarity -> fixed in next version of the design

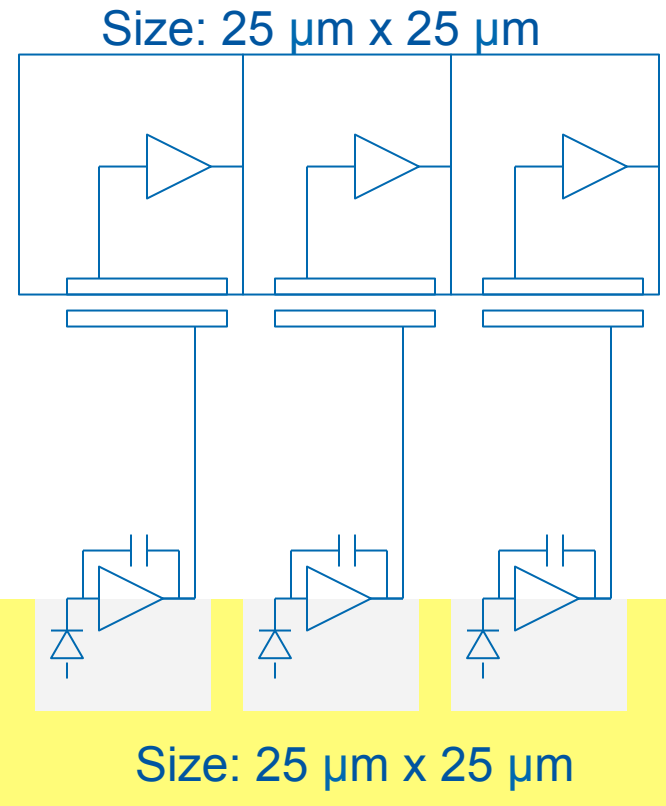
CCPDv3 HV-CMOS sensor

CCPDv3 HV-CMOS sensor

- CLIC requirements – little material, high spatial and time resolution
- Option: capacitively coupled pixel detector (HV-CMOS, AMS180nm)
- Test detector has been produced (CCPDv3) that can be readout with CLICPIX chip
- Pixel size: $25\ \mu\text{m} \times 25\ \mu\text{m}$
- Every HVCMOS pixel has its own readout cell



CLICpix

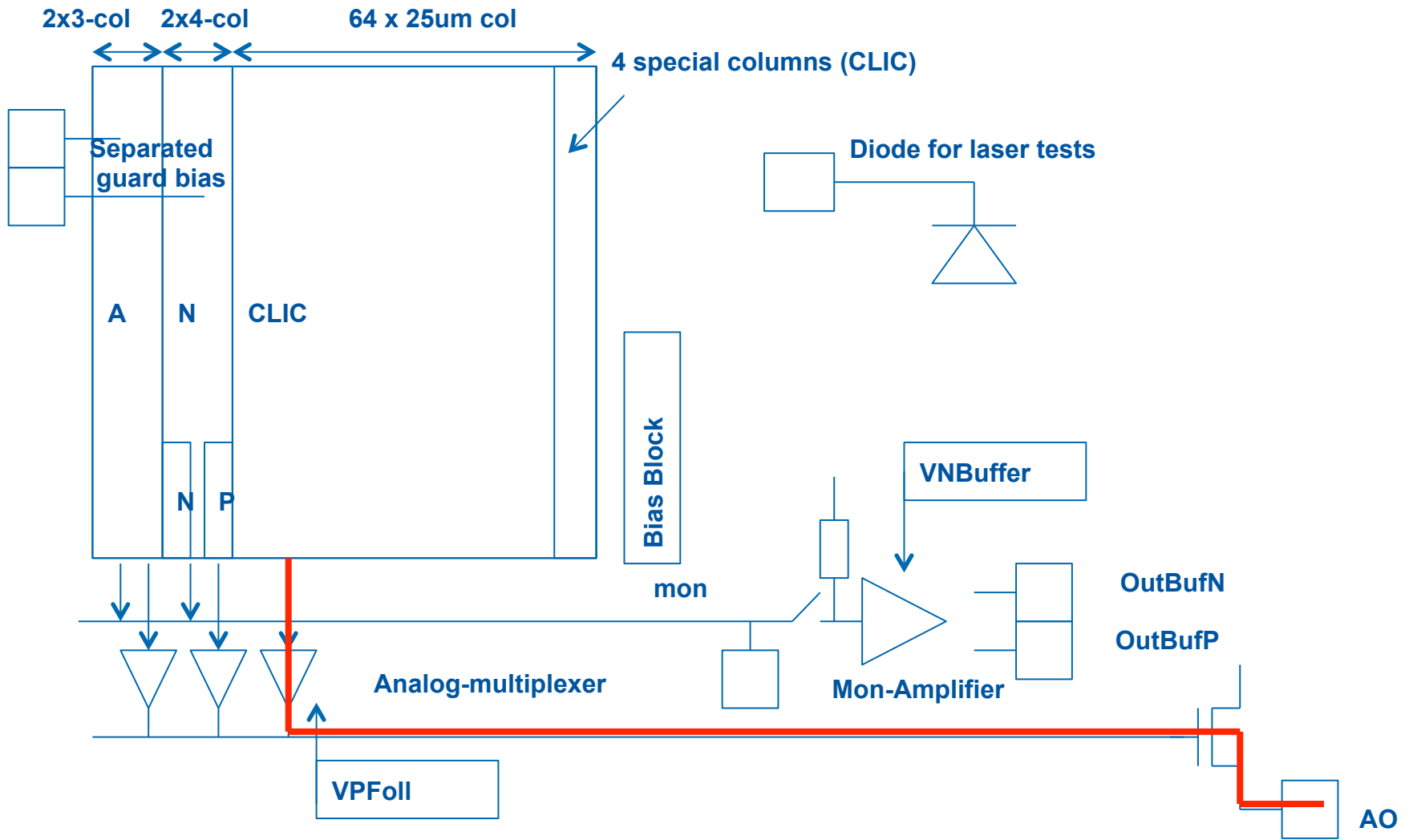


CCPDv3

Size: $25\ \mu\text{m} \times 25\ \mu\text{m}$

Design by Ivan Peric, collaboration with ATLAS-UNIGE group

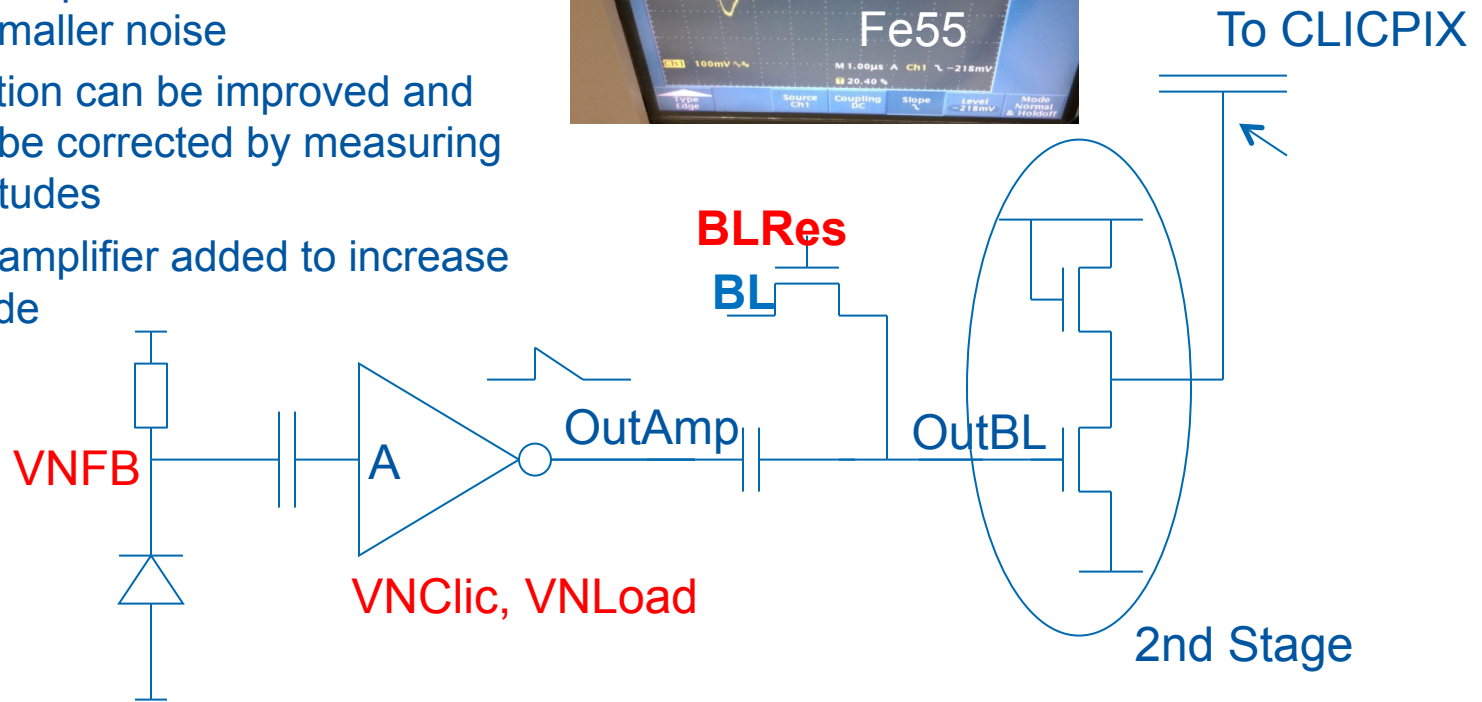
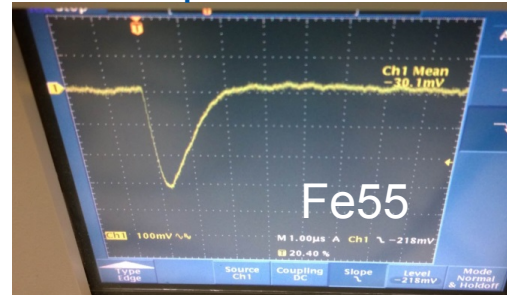
CCPDv3 HV-CMOS sensor



CCPDv3 HV-CMOS sensor

- to CLICPIX readout chip, no discriminator in pixel
- Simple and small pixels, small capacitance, smaller noise
- Spatial resolution can be improved and time-walk can be corrected by measuring of signal amplitudes
- Second stage amplifier added to increase output amplitude

Amplitude 300mV



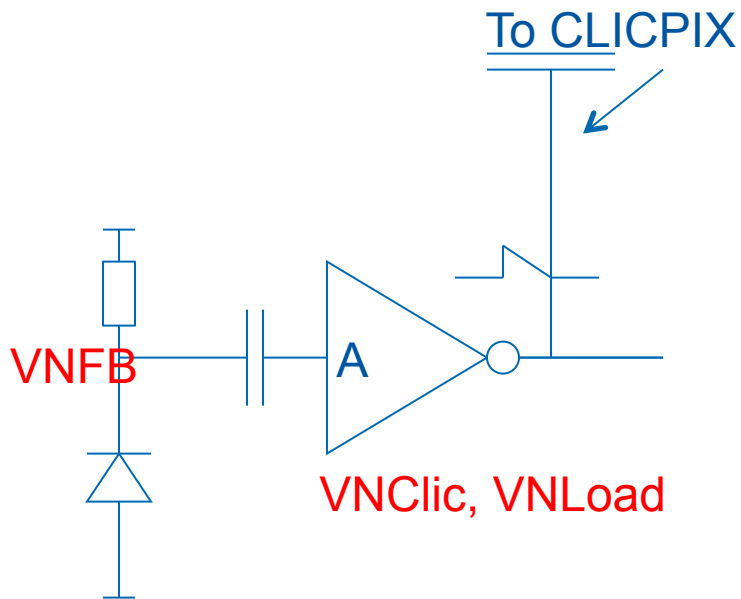
VNCLic, VNLoad

RED: Bias Voltages generated internally

BLUE: External Voltages

CCPDv3 HV-CMOS sensor

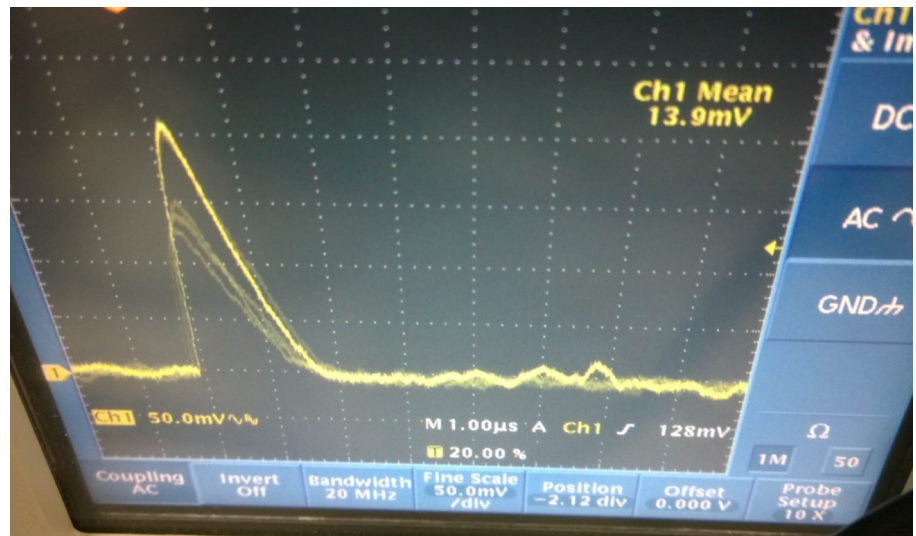
- Four columns have the output of first stage connected to CCPD electrode



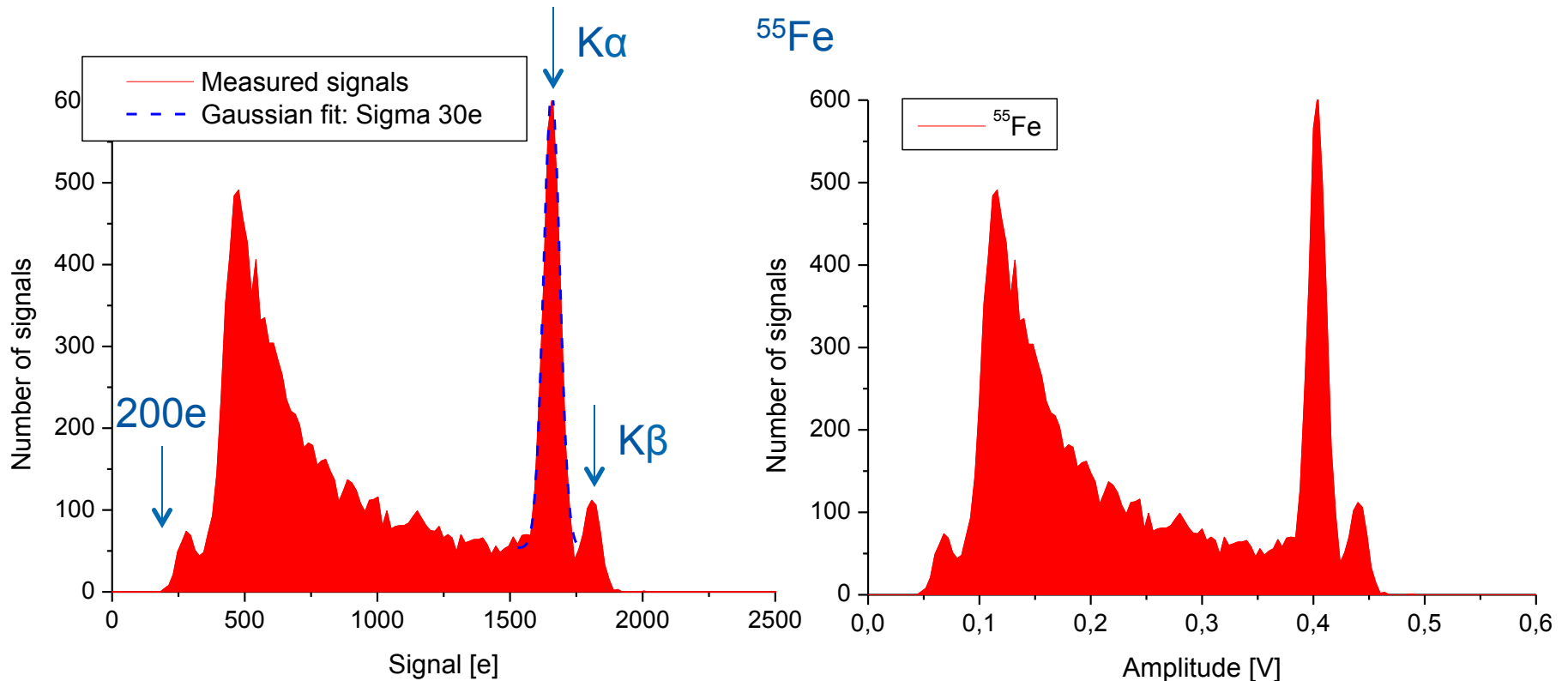
RED: Bias Voltages generated internally

BLUE: External Voltages

Amplitude 200mV



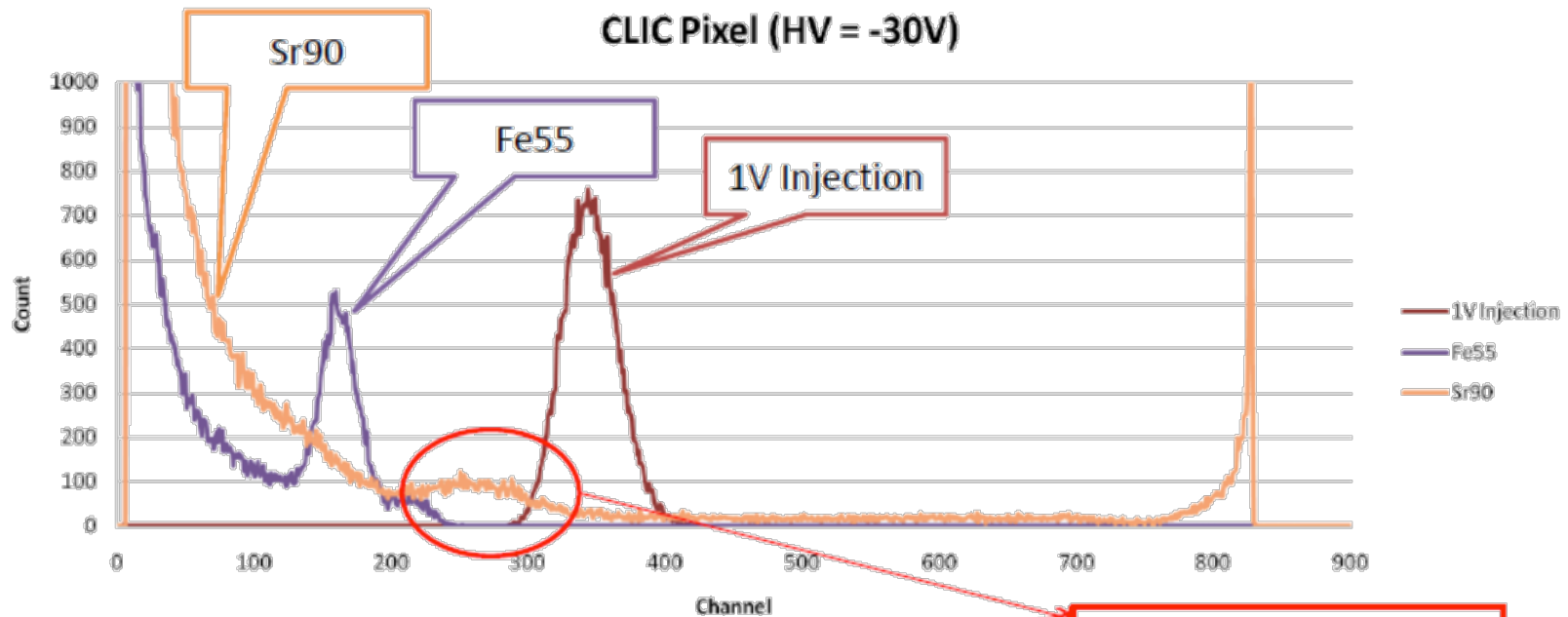
CCPDv3 HV-CMOS sensor



- CLIC pixels – excellent SNR
- Noise for small pixels (25 μm x 25 μm) with analog readout 30e

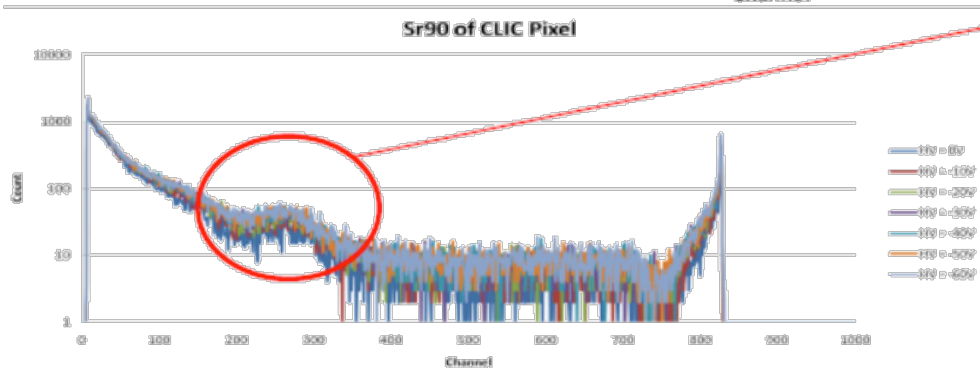
CCPDv3 HV-CMOS sensor

- Jian Liu: CPPM Measurements



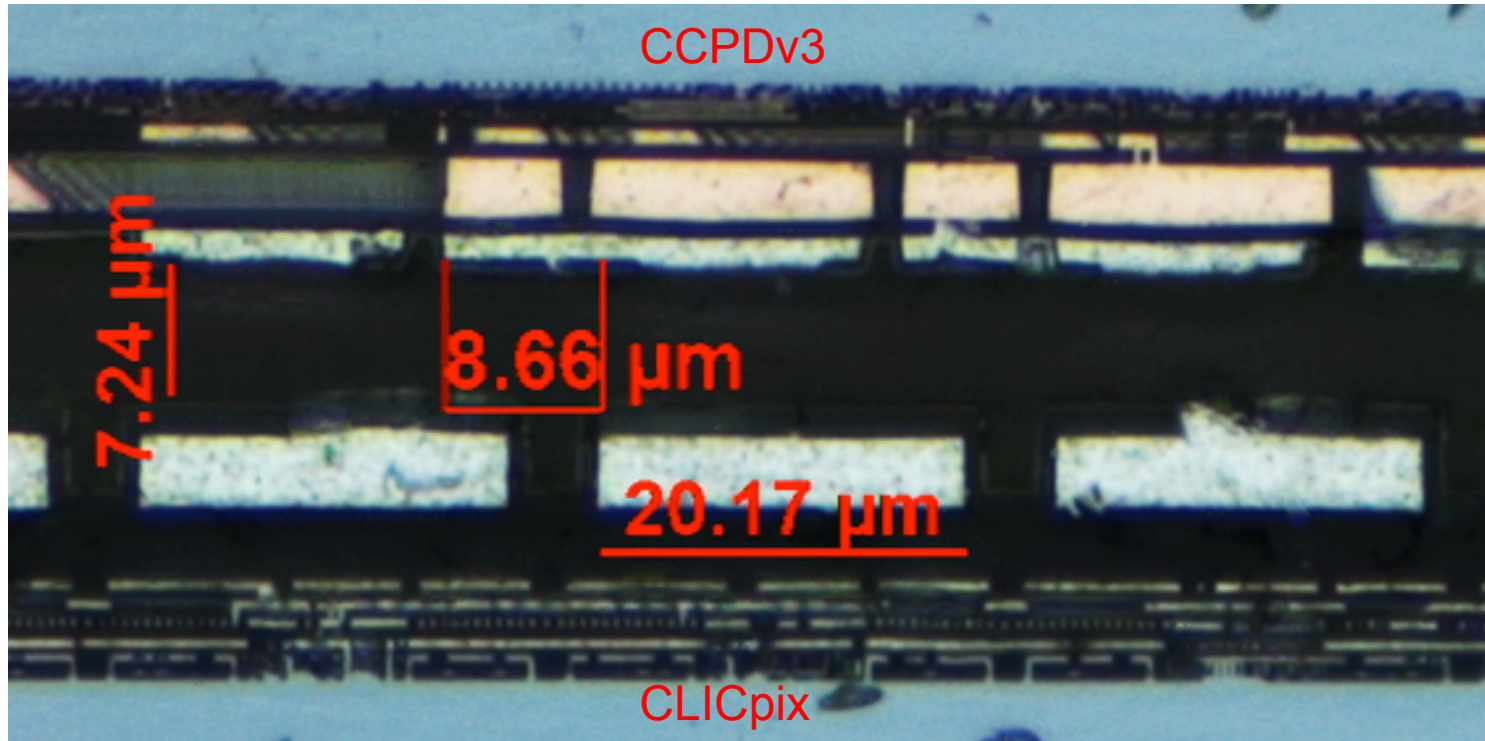
A bump \sim 260 channels.

Very low noise of CLIC.
No noise counting by MCA.



CCPDv3 + CLICpix interconnection and readout system

Gluing of assemblies



Credit to PH-ADE group and Karola Dette for the gluing and measurement work

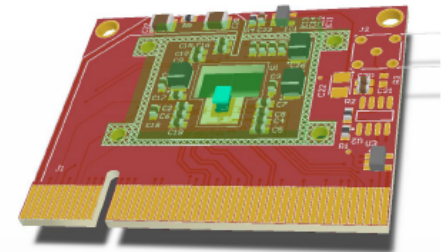
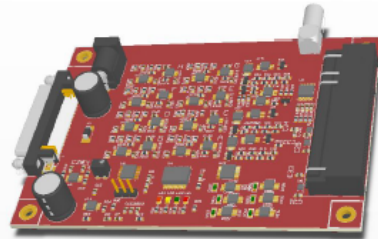
CCPDv3 + CLICpix Readout System

**FPGA
(Atlys board)**

Interface board

- voltage regulators (with monitoring)
- current generators
- level translators
- ADC / DAC

CHIP under test
(decoupling capacitors)



VHDCI connector

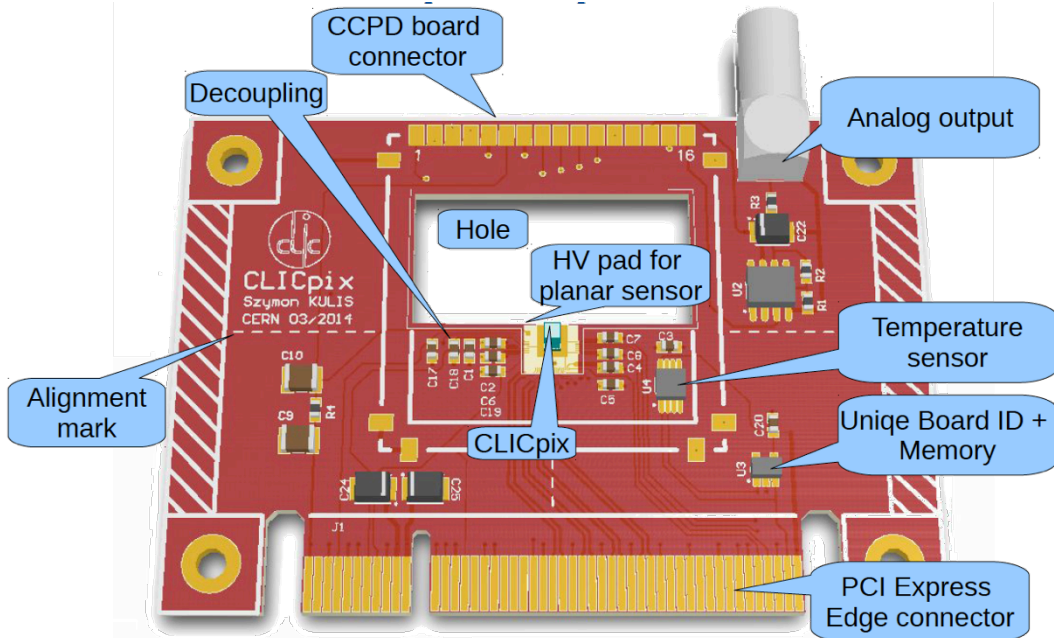
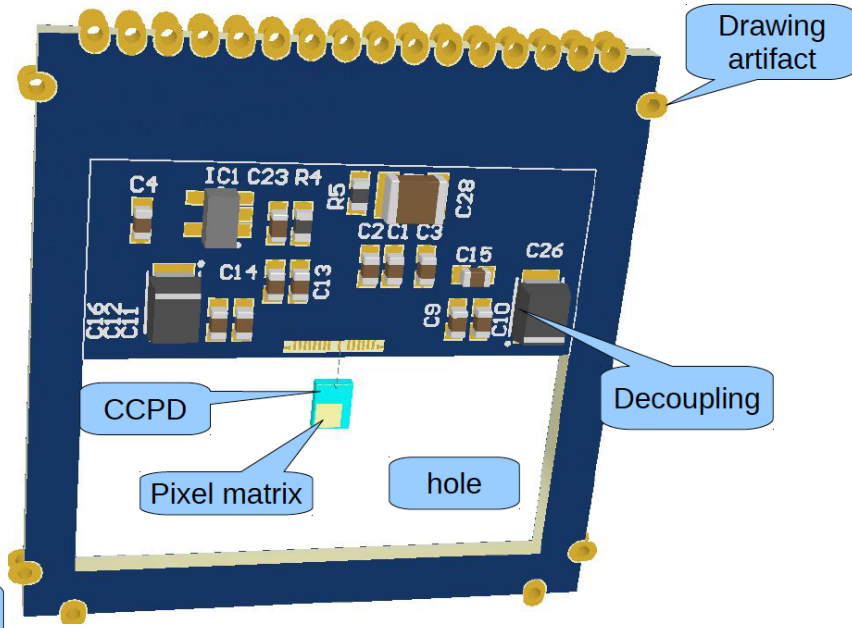


PCI Express

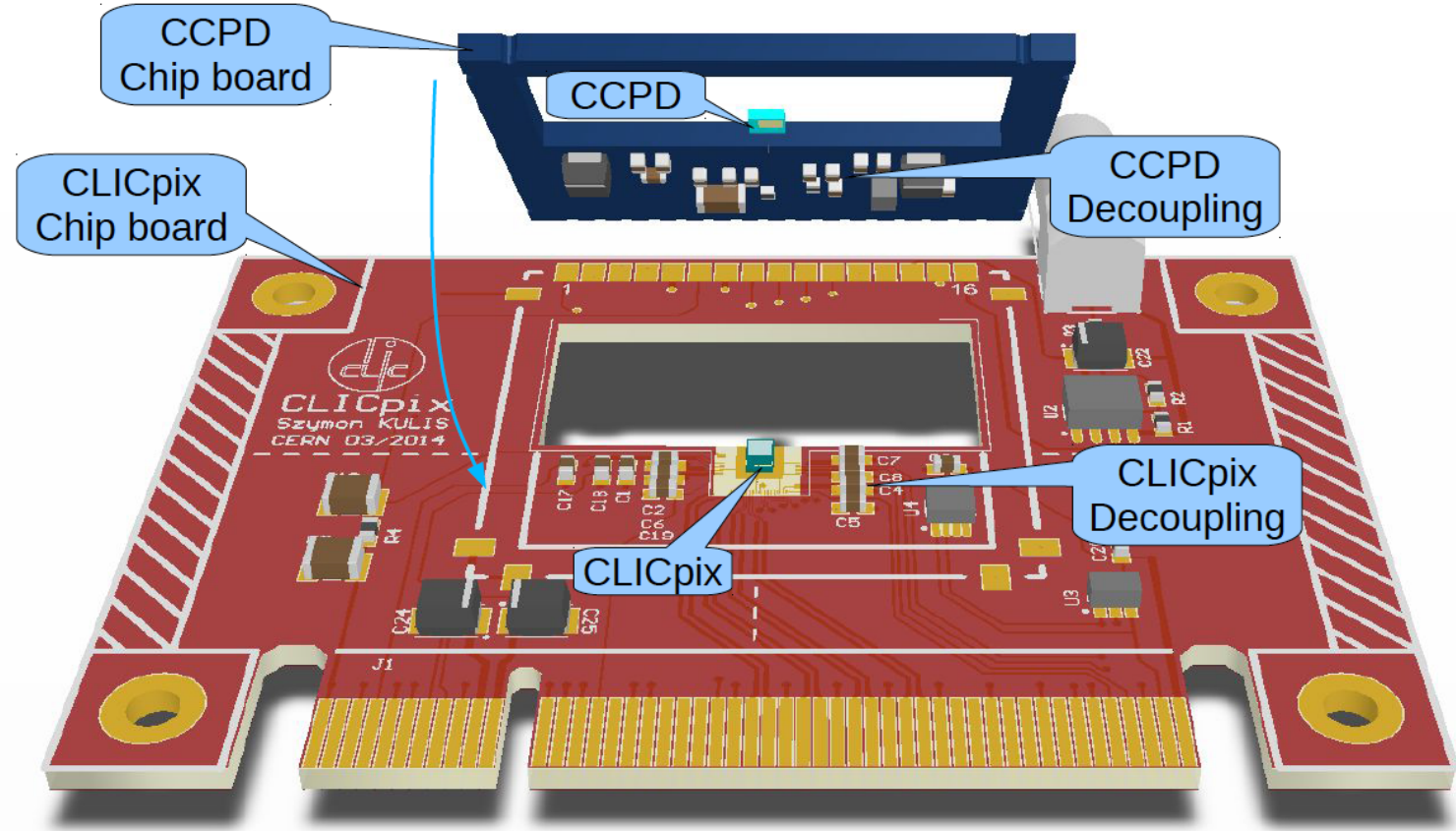
CCPDv3 + CLICpix Readout System

Interconnection of the CCPDv3 and CLICpix
Was done using two simple daughter boards
Containing only the minimum electronics

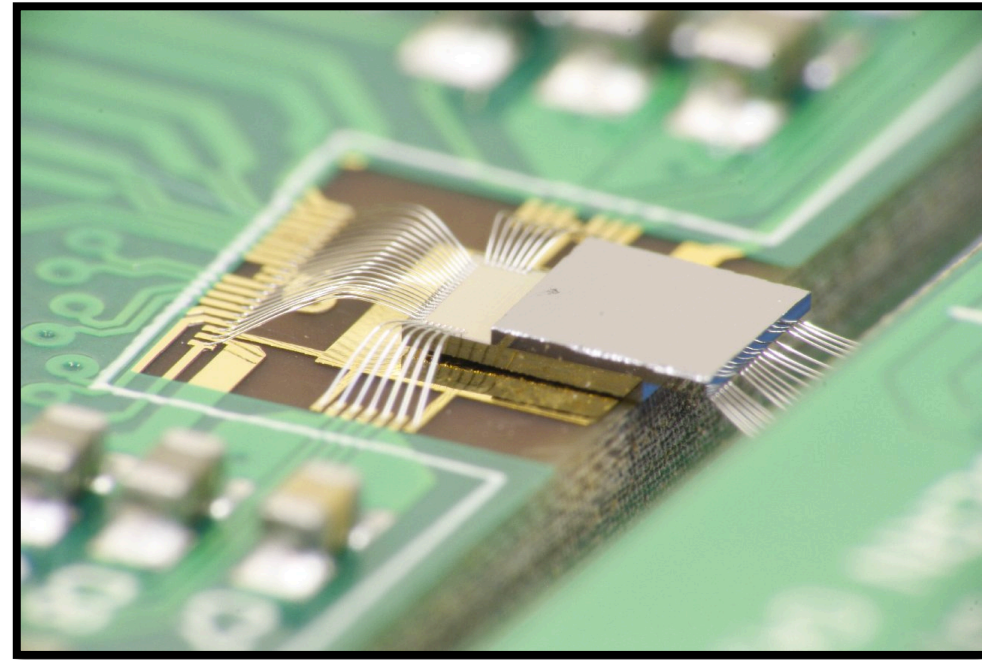
- Shorter wire bonds
- Wire bonding pads and ccpdv3 pads at the same level



CCPDv3 + CLICpix Readout System



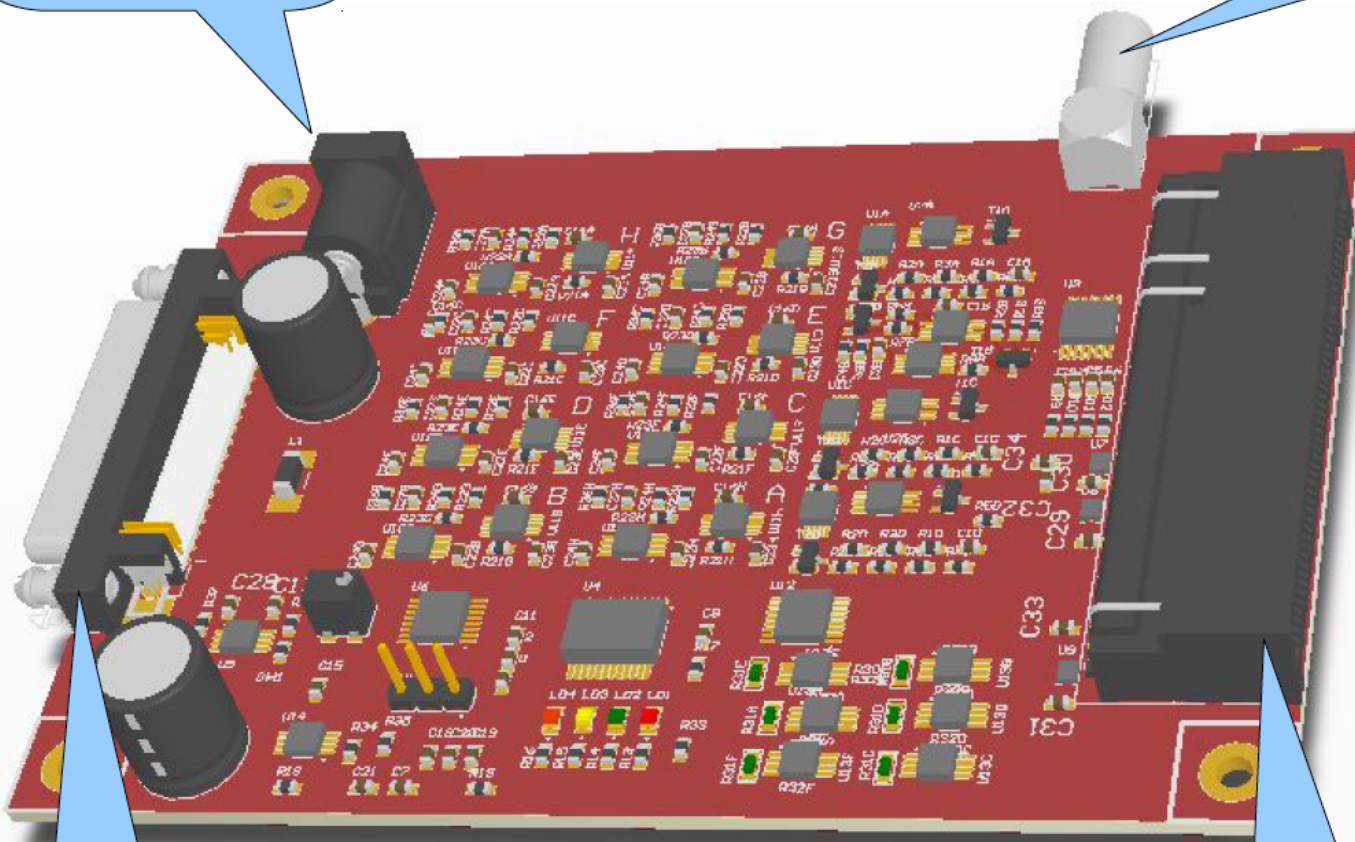
CCPDv3 + CLICpix Readout System



Interface board

External power

High voltage



VHDCI
(to FPGA board)

PCI express
(to chip board)

Interface board

External power

High voltage

- 8 x general purpose power supply

- Voltage range 0 – 4 V (set resolution ~1 mV)
- Maximum current 0.5 A
- Monitoring resolution : ~1mV / 25 μ A

- 4 x voltage output

- Voltage range 0 – 4 V (set resolution ~1 mV)

- 4 x current output

- Current range 0 – 1 mA (set resolution <1 μ A)

- 4 x voltage input

- Voltage range 0 – 4 V (set resolution ~1 mV)

- High voltage input

(to FPGA board)

- 12 x general CMOS signals (Input / Output)

- Two independent groups (8+4) with adjustable voltage level 0.9 – 3.6 V (determined by one general purpose power supply)

- 12 x differential pairs (Input / Output)

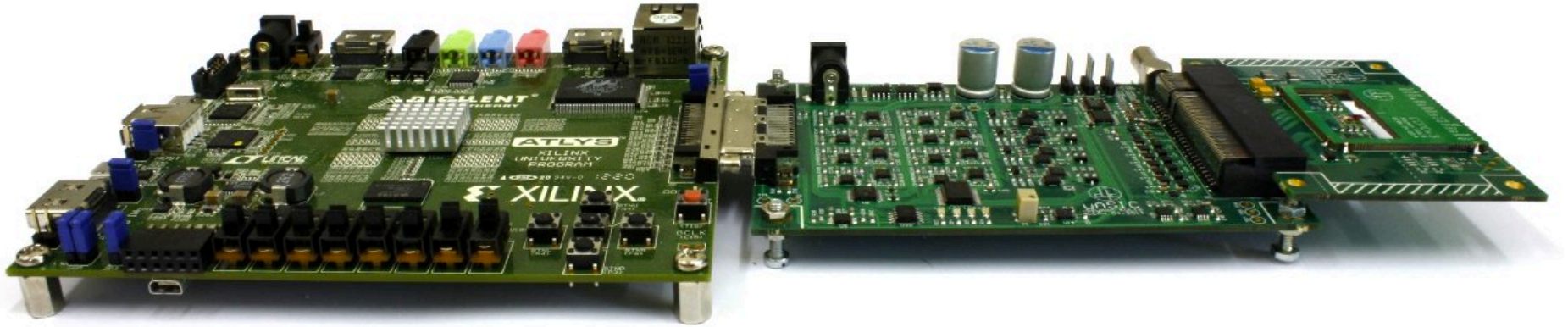
- 100 Ohm differential impedance

- I²C bus

- Status LEDs

PCI express
(to chip board)

Full readout + DUT system



Readout system fully developed at CERN

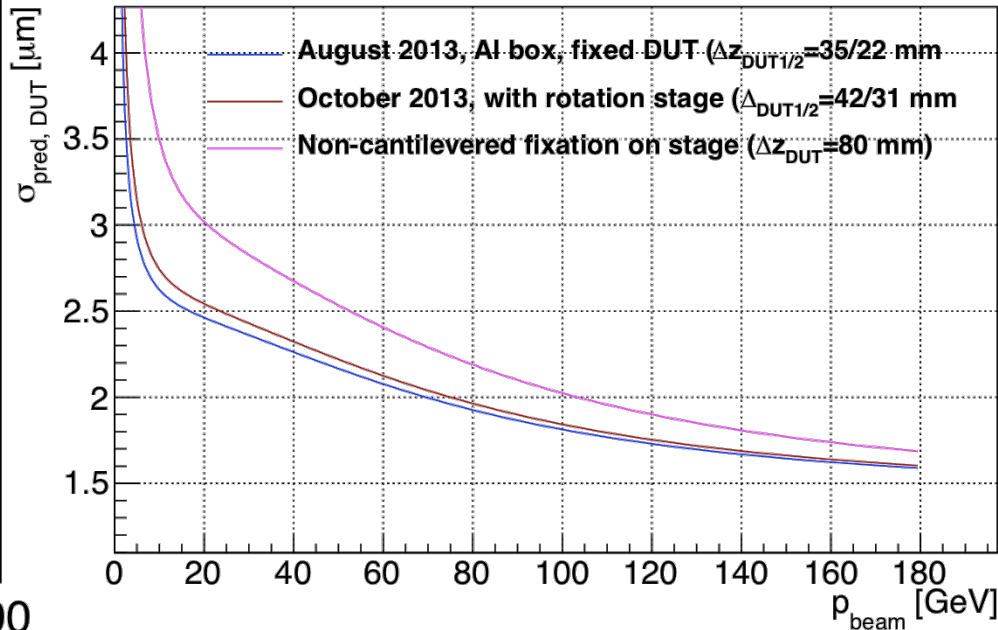
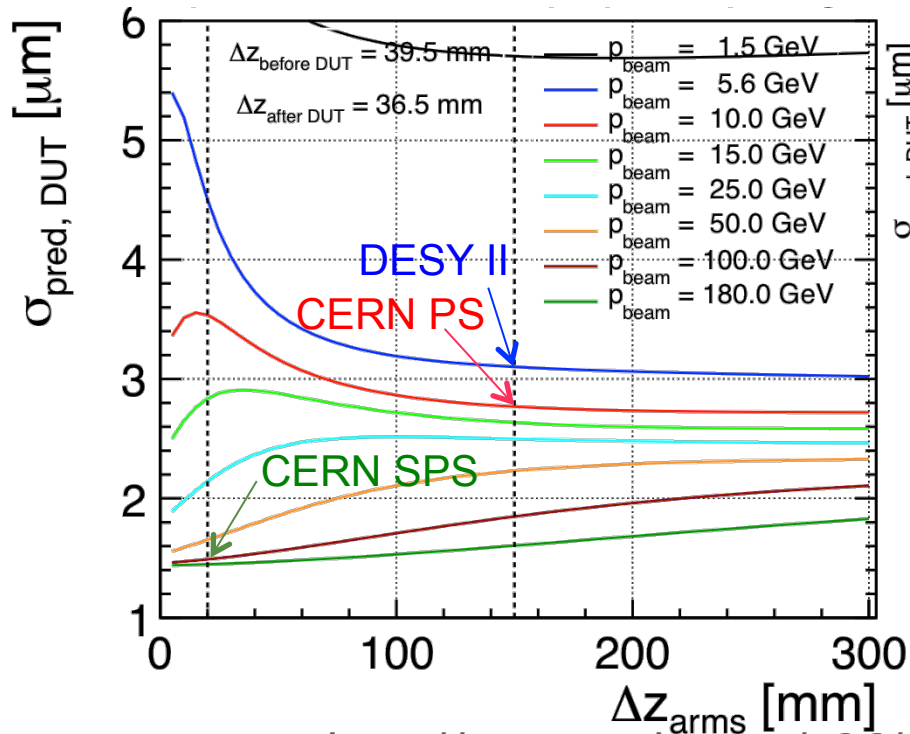
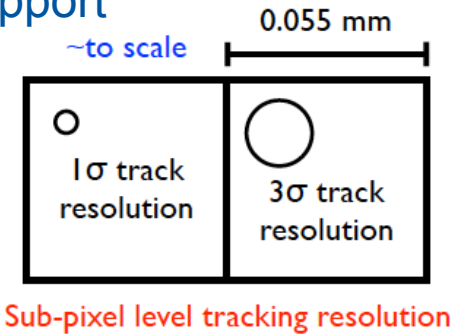
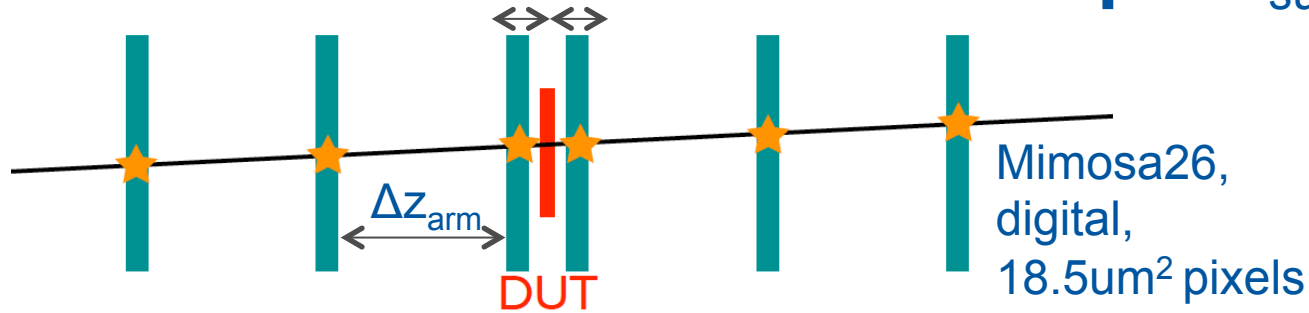
- Rough integration to EUDET DAQ (EUDAQ) completed, allowing for first test beam in August 2014
- Work ongoing to integrate the readout to the SPIDRman visualization and control software developed for Timepix3 SPIDR readout



First (**Very preliminary !**) test beam results @ CERN PS using EUDET/AIDA Telescope

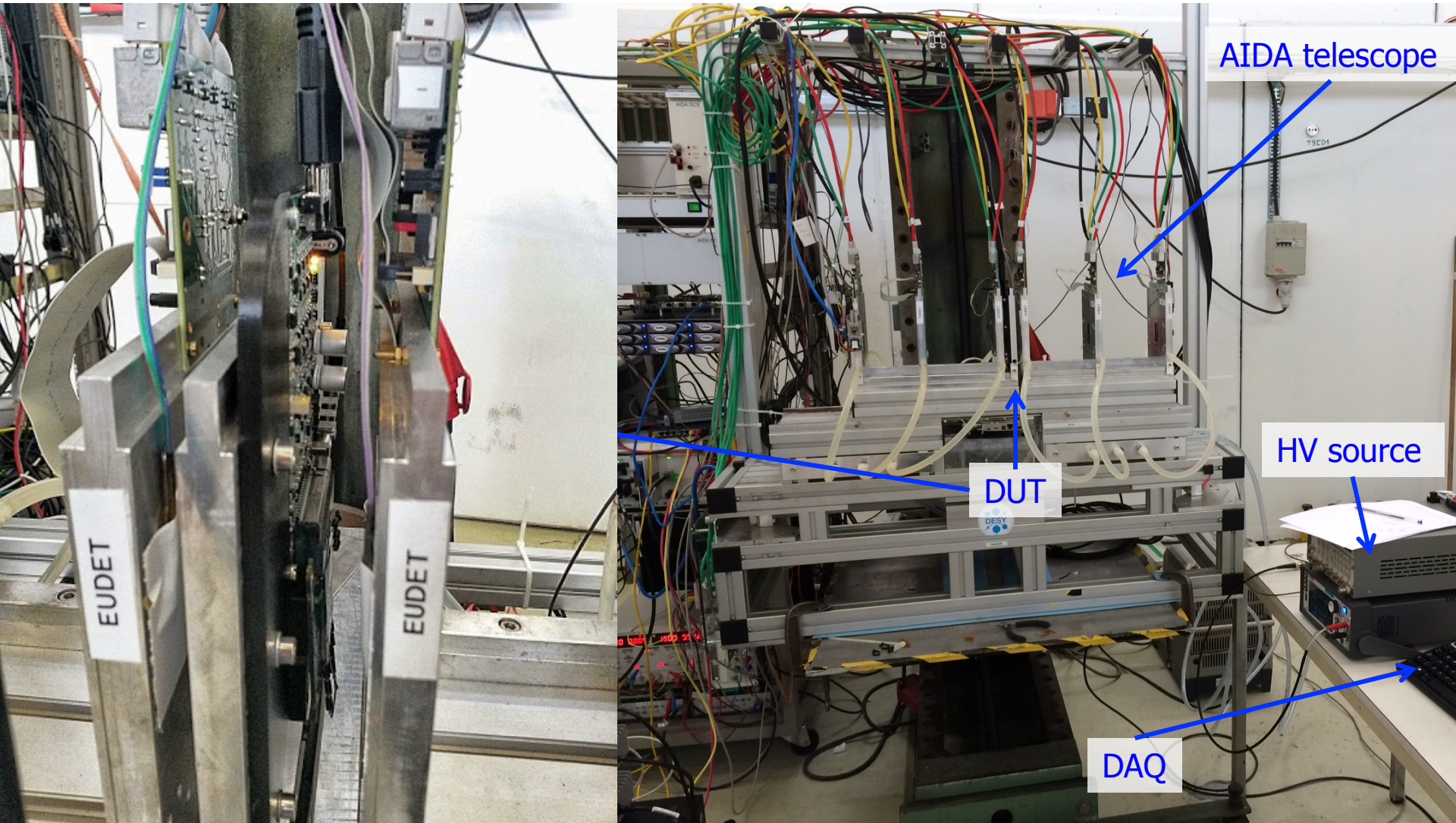
The EUDET Telescope

Thanks to the DESY telescope team for the support

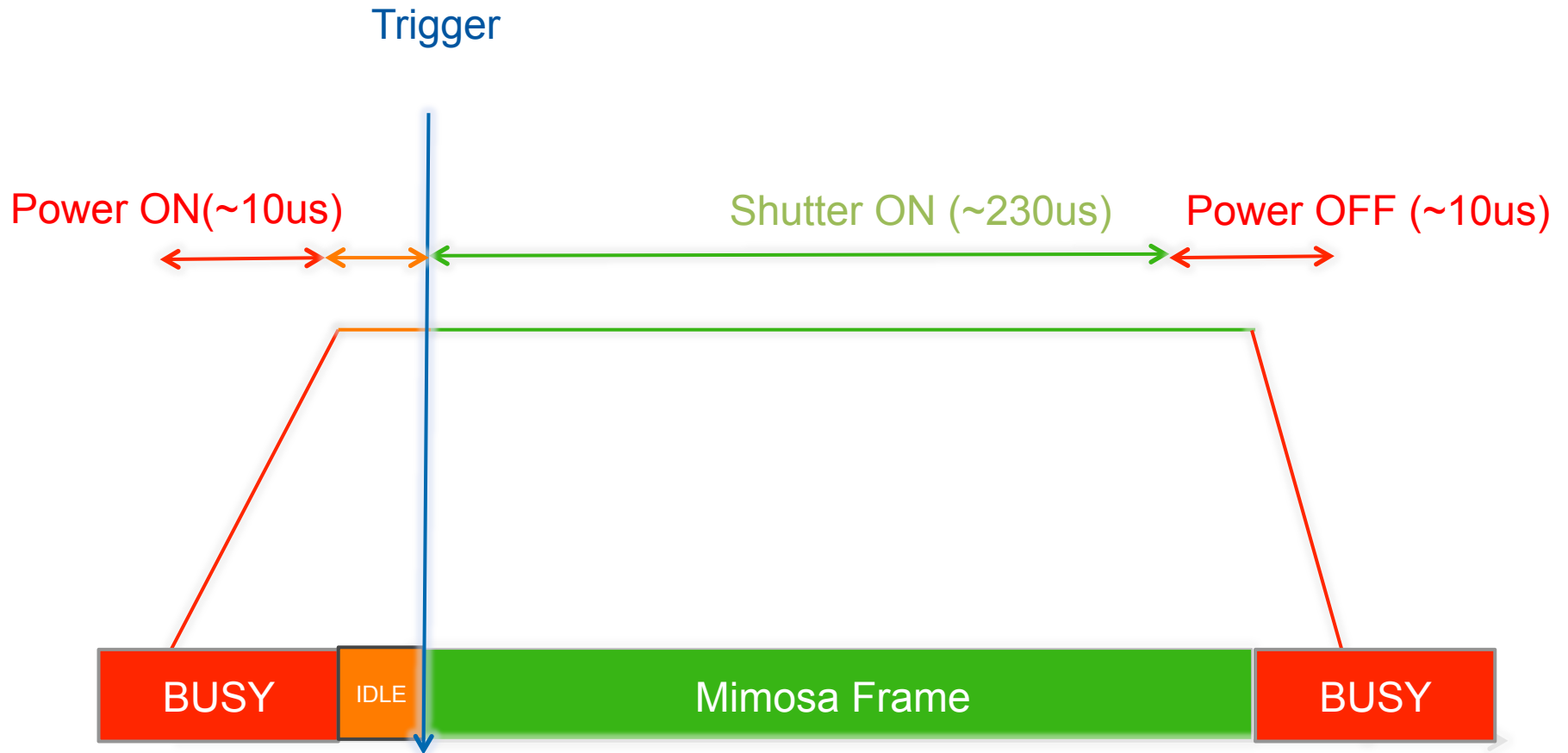


<http://www.eudet.org/e26/e27/e295/eudet-report-2007-01.pdf>

CERN PS test beam setup

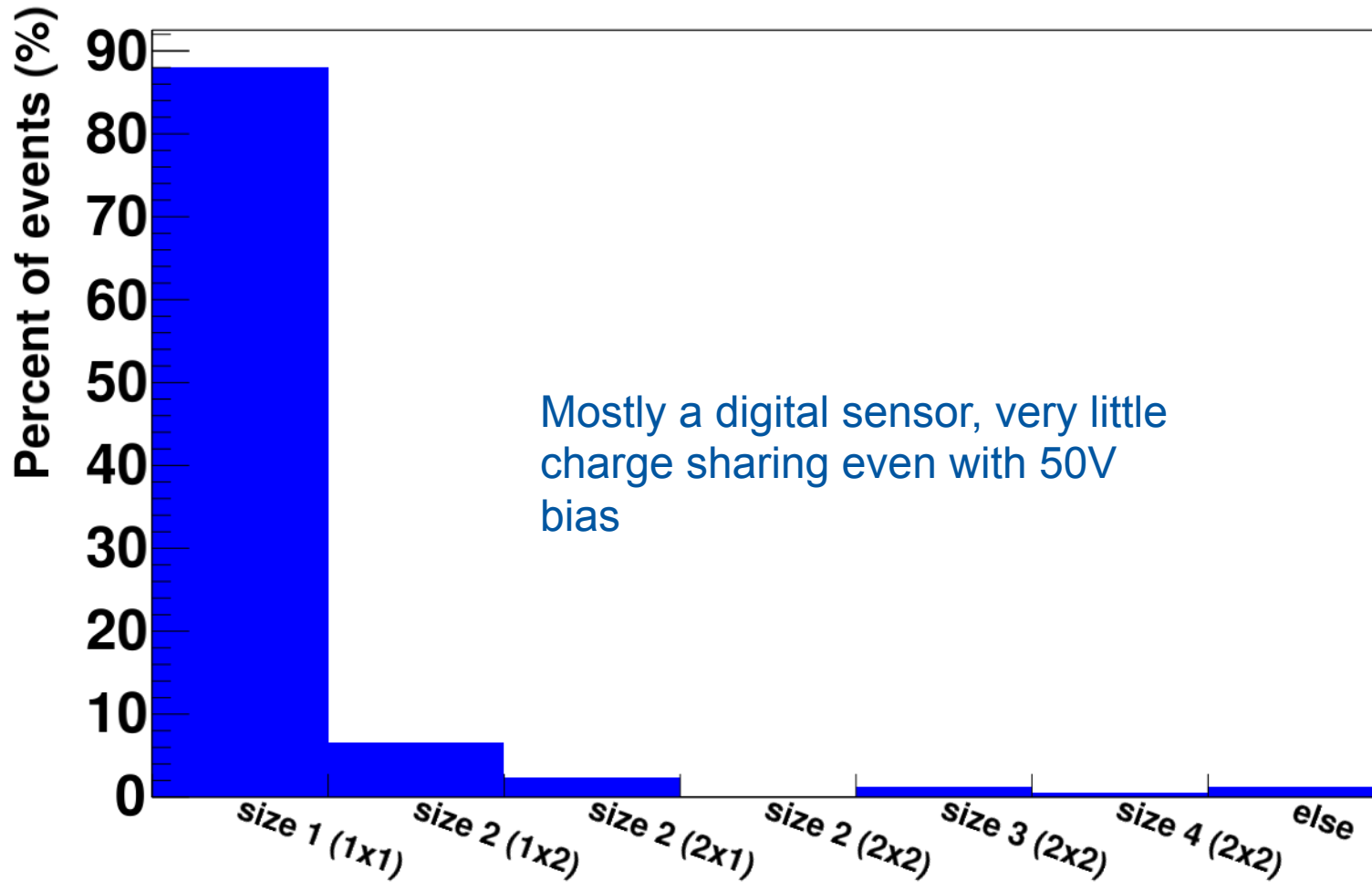


Triggering Scheme



Cluster size distribution

Percentage of clusters for different sizes

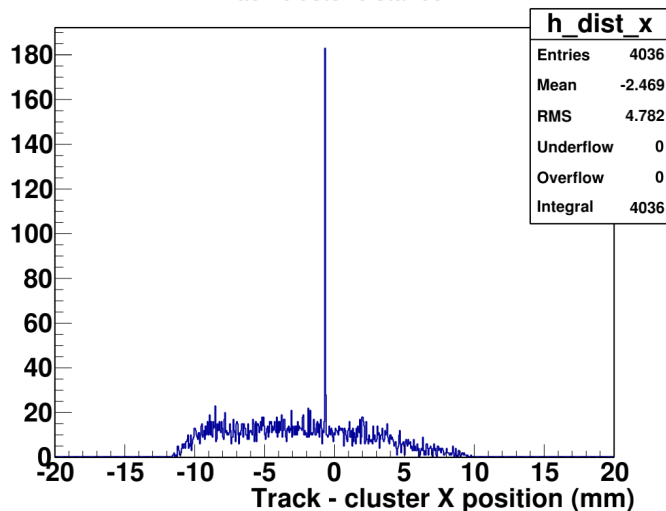




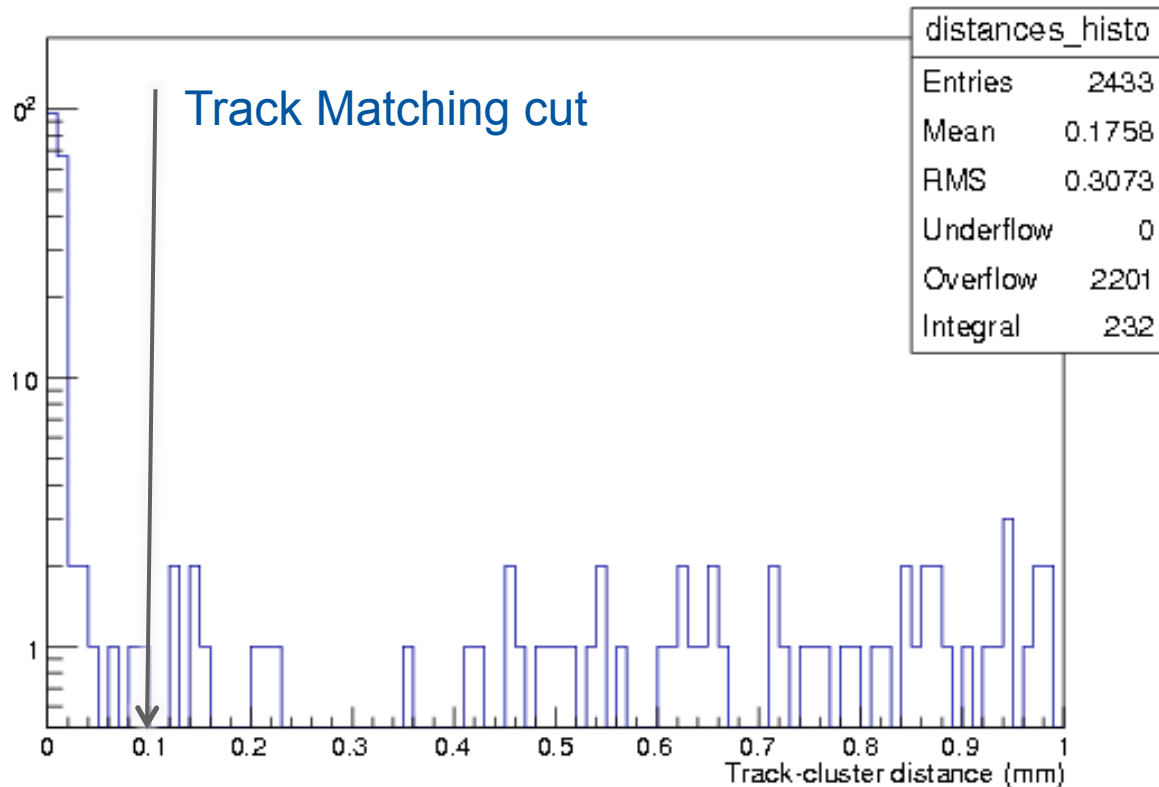
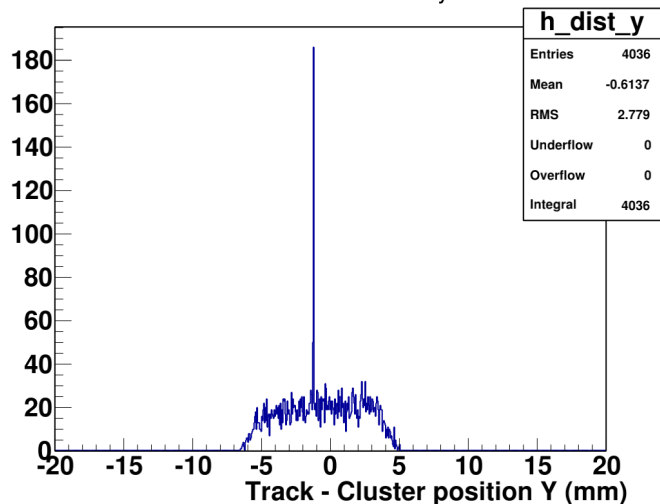
What is going on ??

Track reconstruction

Track-cluster distance x

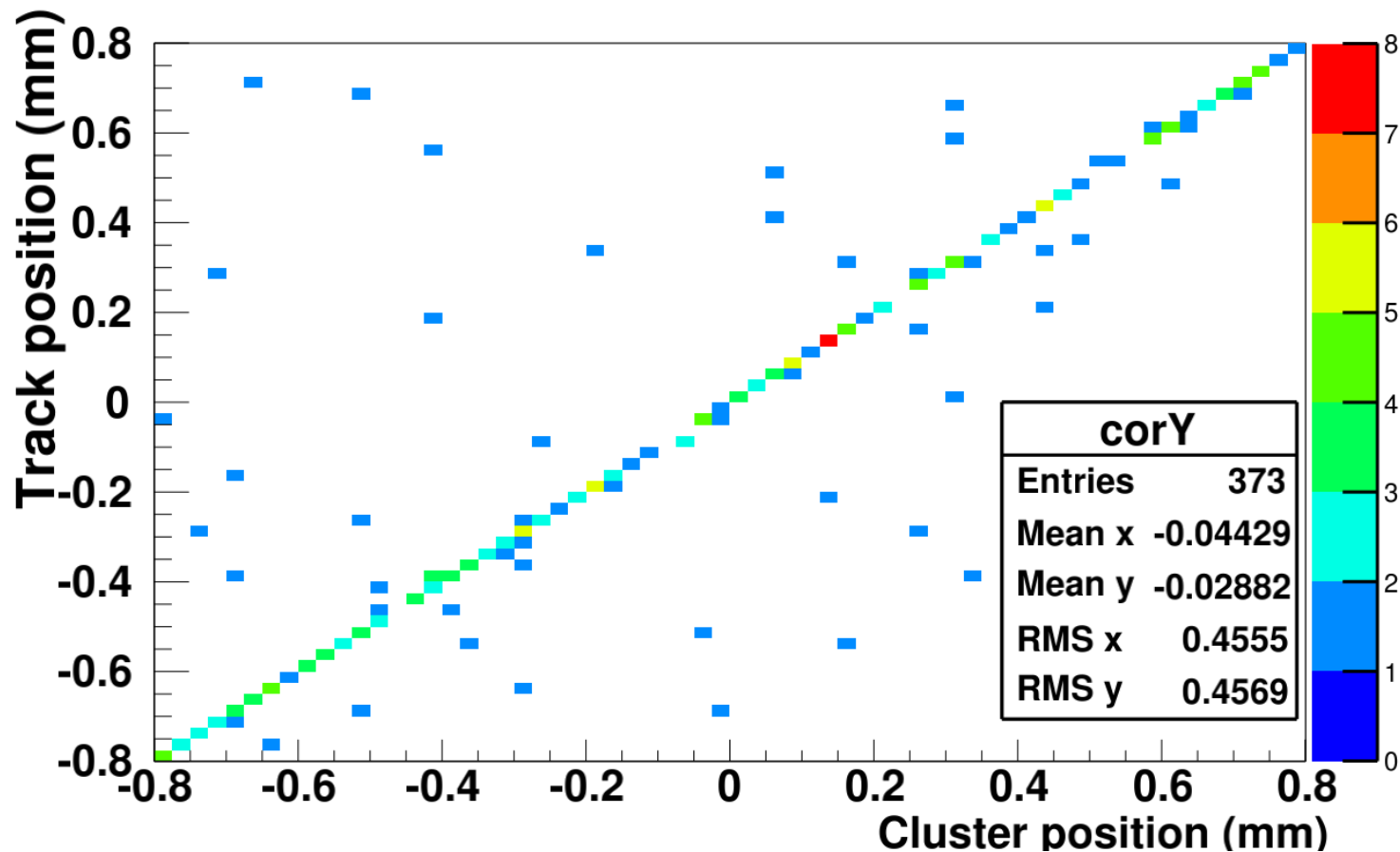


Track-cluster distance y



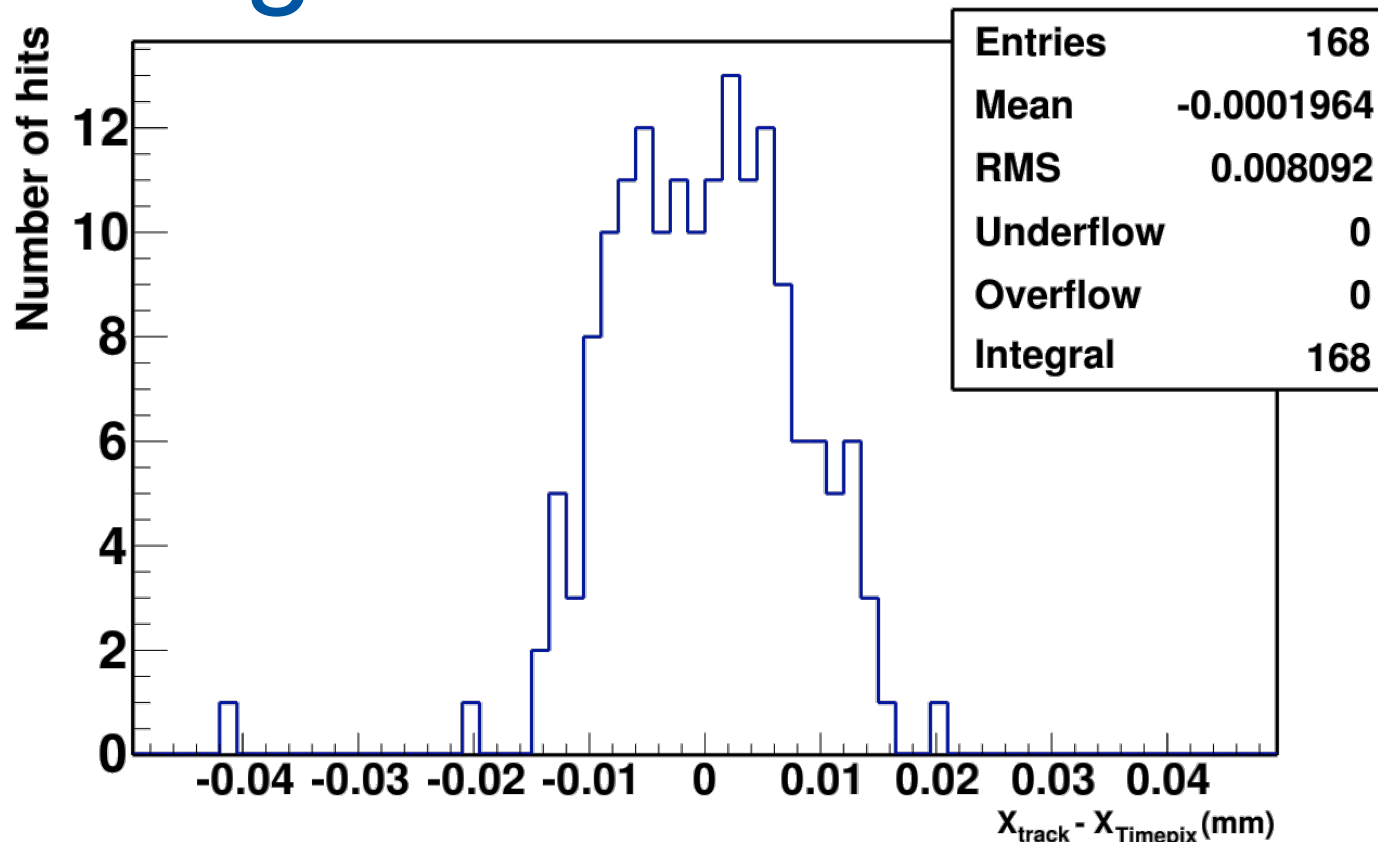
Analysis using in-house framework, compatible with most sensor :
<https://github.com/pyEudetAnalysis/pyEudetAnalysis>

Track cluster correlation



Detection efficiency ~11% -> Problem with threshold, timing, etc...

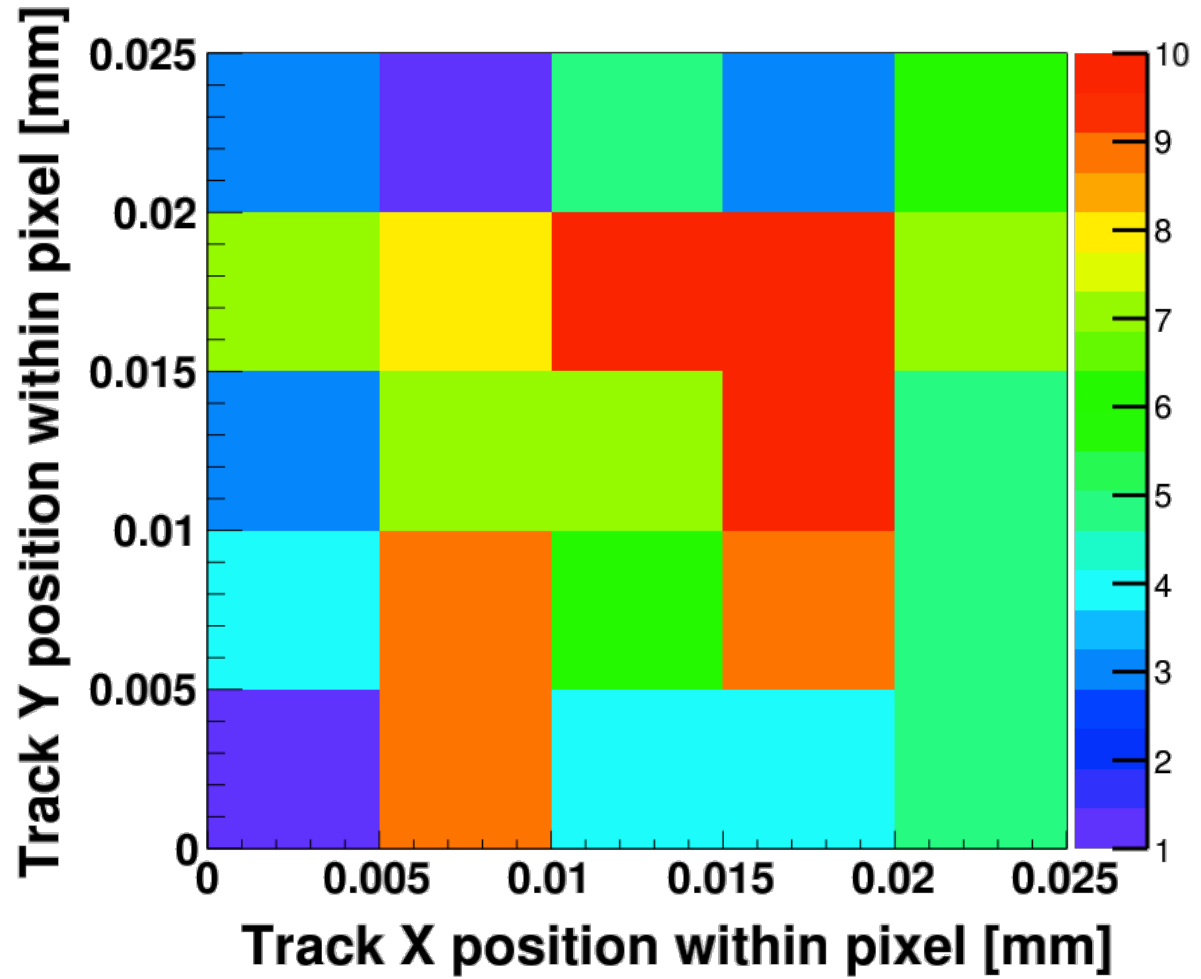
Tracking resolution



As the detector behave as a digital sensor (mostly cluster with single pixel), we expect a resolution of $25\mu\text{m}/\sqrt{12} \rightarrow 7.2\mu\text{m}$. Assuming $3\mu\text{m}$ pointing resolution, we obtain $7.4\mu\text{m}$. Obviously here statistical uncertainty dominate all the rest.

Track position vs Cluster size (single pixel cluster)

No obvious dependency between cluster size and track hit position within pixels



Future plans

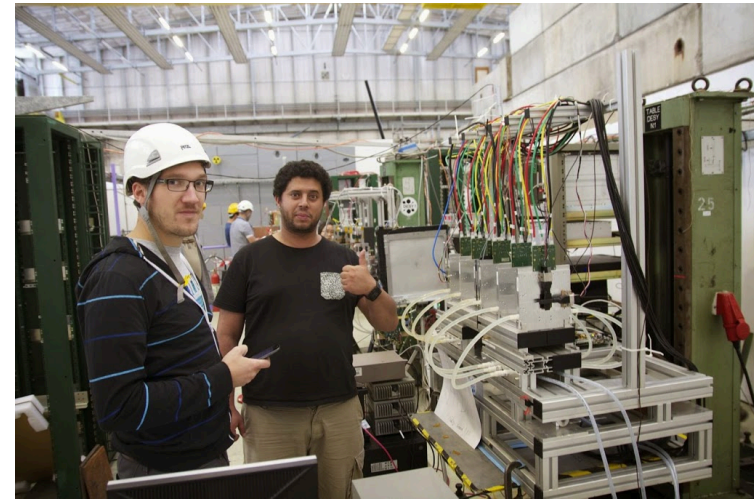
- Understand the very low efficiency observed in our preliminary test
 - Better comprehension of Threshold equalization on CLICpix for electron signal (optimized for opposite polarity)
 - Systematic measurements of electrical characteristics (gain, TOT gain , etc..) for various biasing conditions
 - Glue more prototype, maybe CLICpix or CCPDv3 were defective
 - Explore various gluing scenario
- Increase statistics in the beam
 - Use ROI trigger available in the EUDET telescope (using FEI4)
 - Re-Design of CLICpix ASIC (larger size, better handling of signal of both polarities, increase counter size)

Conclusion

- A 65nm prototype ASIC was produced meeting CLIC requirements in terms of power, timing and pitch.
- An AMS 180nm CCPD Sensor was produced matching the CLICpix footprint
- Performance of the both part alone are promising
 - Low noise , low power
- A full readout system integration control for CCPD and CLICpix was produced , integrated to the EUDET DAQ (EUDAQ)
- Preliminary test in beam show data taken in sync with the telescope, but efficiency is very low
 - Need to understand better the full system
 - More time will be dedicated to the CLICpix +ccpdv3 in our October and November test beam in PS/SPS



CLIC Detector and Physics Collaboration



But we keep smiling 😊

backup

CCPDv3 HV-CMOS sensor

- Jian Liu: CPPM Measurements

