Development of DMAPS sensors

in ESPROS technology

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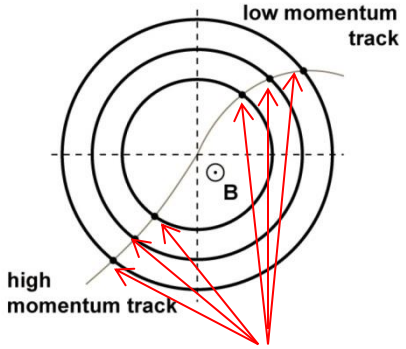
Workshop on CMOS Active Pixel Sensors for Particle Tracking (CPIX2014)

Physikalisches Institut, Universität Bonn, 15th September 2014

Sensor requirements for particle tracking

General requirements

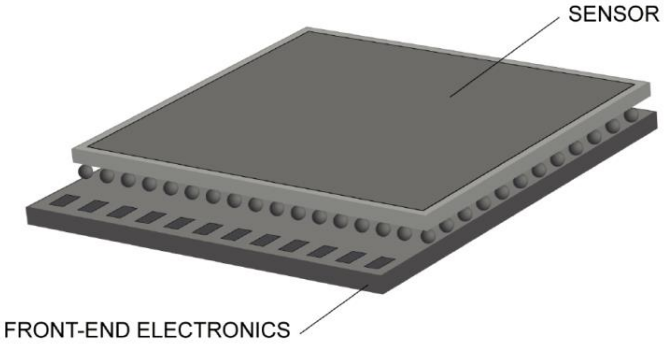
- Minimize multiple scattering to increase momentum resolution
  => low mass (thinned) sensors needed
- Granularity (currently 400×50 resp. 250×50 μm^2 (IBL))
- Sufficient signal to noise ratio (hybrid pixels ≈ 100)
- Radiation hardness (≈ 100 Mrad)
- Low power (3.5 mW/mm^2 for innermost layer (RD53))
- => in case of 50x50 μm^2 pixels we need 8.75 µW/pixel

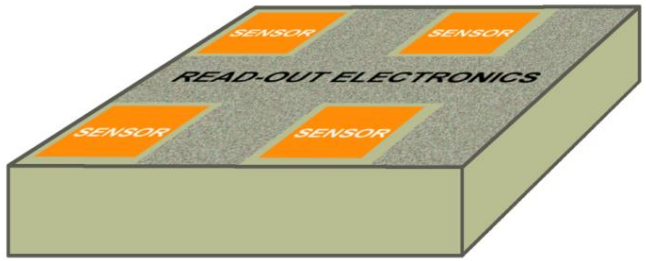


Multiple scattering

Monolithic pixels

- High granularity (small pixels)
- Low mass (thinned sensor) possible
- One chip – no bump-bonding – fast prototyping
- Large SNR – questionable
- Potentially low cost solution for large area tracker
- Complex electronics in pixel – questionable
- Radiation hardness - questionable

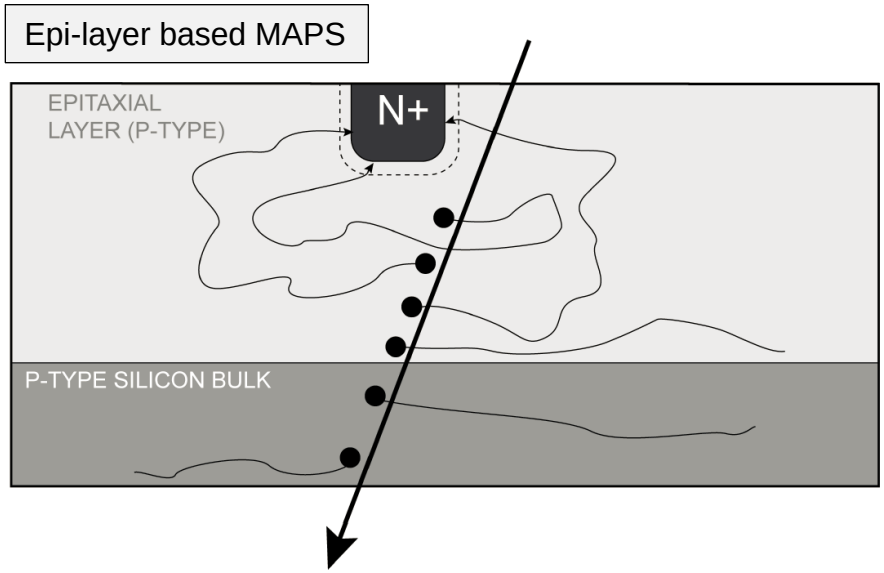


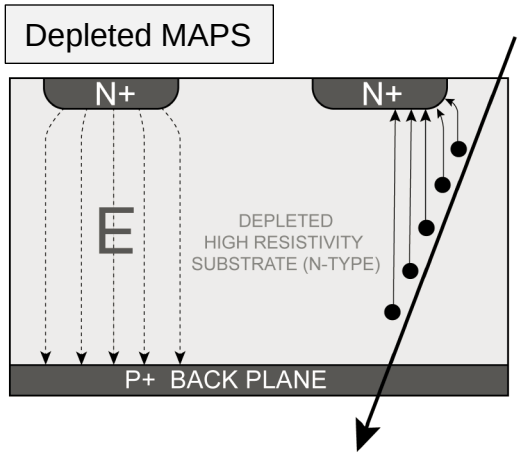


Depleted Monolithic Active Pixel Sensor

- **Existing MAPS technologies:**
  - standard CMOS MAPS, HV MAPS, epi-layer MAPS, INMAPS, T3 MAPS …..
  - not all of them suitable for HEP experiments

- **Problem of the "standard" MAPS**
  - slow and incomplete charge collection
  - not full CMOS in pixel
  - limited radiation hardness





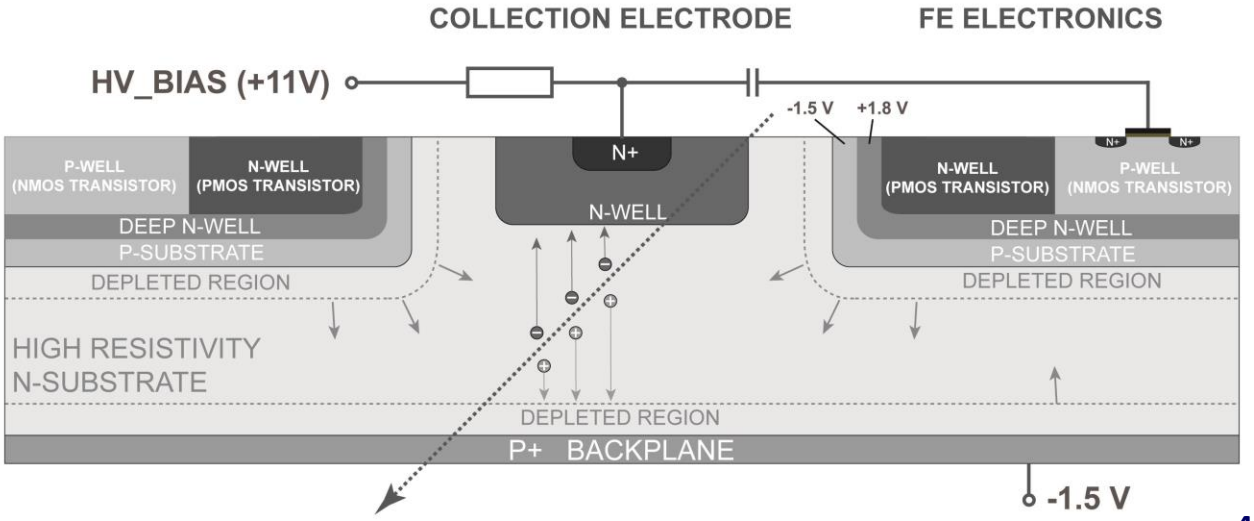
- **Depleted MAPS – non-standard CMOS process**
  - large signal from depleted bulk
  - possibility to integrate full CMOS
  - enhanced radiation tolerance
  - even thin sensor can provide good SNR

ESPROS - technology for DMAPS fabrication

- **Technology options needed**
  - High resistive substrate
  - High voltage (≈10 V)
  - Quadruple well

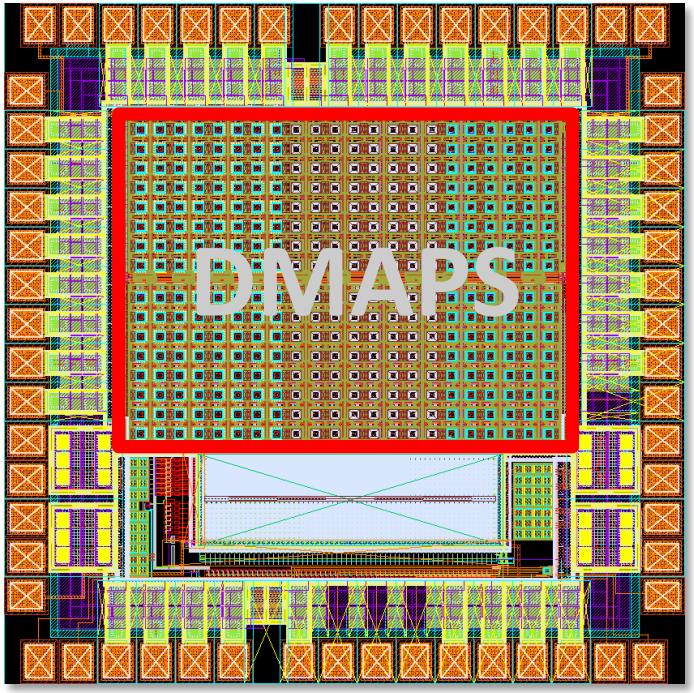
- **Advantages w.r. to standard CMOS MAPS**
  - Large signal (theoretically 4 ke^-/MIP at 50 µm thick silicon substrate)
  - Fast charge collection
  - Potentially high radiation hardness

- **ESPROS Photonic Process**
  - 150 nm CMOS process
  - Near IR sensors
  - 1.8 V domain
  - 6 metal layers



Test chip – EPCB01

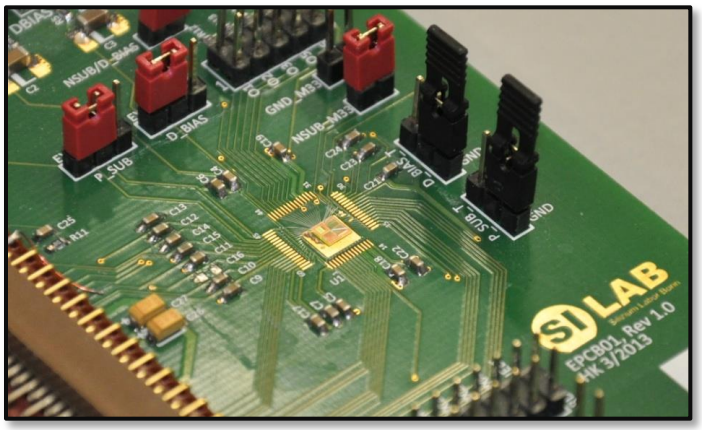
- **Test-chip submitted in late 2012**
  - chip size 1.4×1.4 mm^2
  - six different DMAPS pixel matrices
  - thinned down to 50 µm
  - 8×8 and 6×8 matrix dimension



- **Chip output**
  - configuration and read-out with a shift register
  - each matrix (except V4) has analog output from one pixel

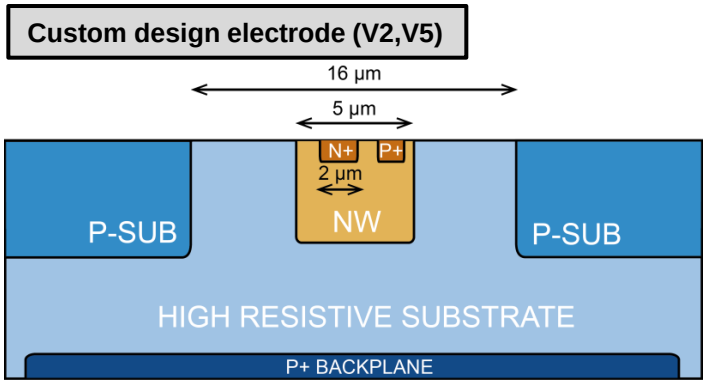
344	343	328	327	312	311	296	295	280	279	264	263	248	247	232	231	216	215	200	199	184	183
345	342	329	326	313	310	297	294	281	278	265	262	249	246	233	230	217	214	201	198	185	182
346	341	330	325	314	309	298	293	282	277	266	261	250	245	234	229	218	213	202	197	186	181
347	340	331	324	315	308	299	292	283	276	267	260	251	244	235	228	219	212	203	196	187	180
348	339	332	323	316	307	300	291	284	275	268	259	252	243	236	227	220	211	204	195	188	179
349	338	333	322	317	306	301	290	285	274	269	258	253	242	237	226	221	210	205	194	189	178
350	337	334	321	318	305	302	289	286	273	270	257	254	241	238	225	222	209	206	193	190	177
351	336	335	320	319	304	303	288	287	272	271	256	255	240	239	224	223	208	207	192	191	176
7	8	23	24	39	40	55	56	71	72	87	88	103	104	119	120	135	136	151	152	167	168
6	9	22	25	38	41	54	57	70	73	86	89	102	105	118	121	134	137	150	153	166	169
5	10	21	26	37	42	53	58	69	74	85	90	101	106	117	122	133	138	149	154	165	170
4	11	20	27	36	43	52	59	68	75	84	91	100	107	116	123	132	139	148	155	164	171
3	12	19	28	35	44	51	60	67	76	83	92	99	108	115	124	131	140	147	156	163	172
2	13	18	29	34	45	50	61	66	77	82	93	98	109	114	125	130	141	146	157	162	173
1	14	17	30	33	46	49	62	65	78	81	94	97	110	113	126	129	142	145	158	161	174
0	15	16	31	32	47	48	63	64	79	80	95	96	111	112	127	128	143	144	159	160	175

analog outputs

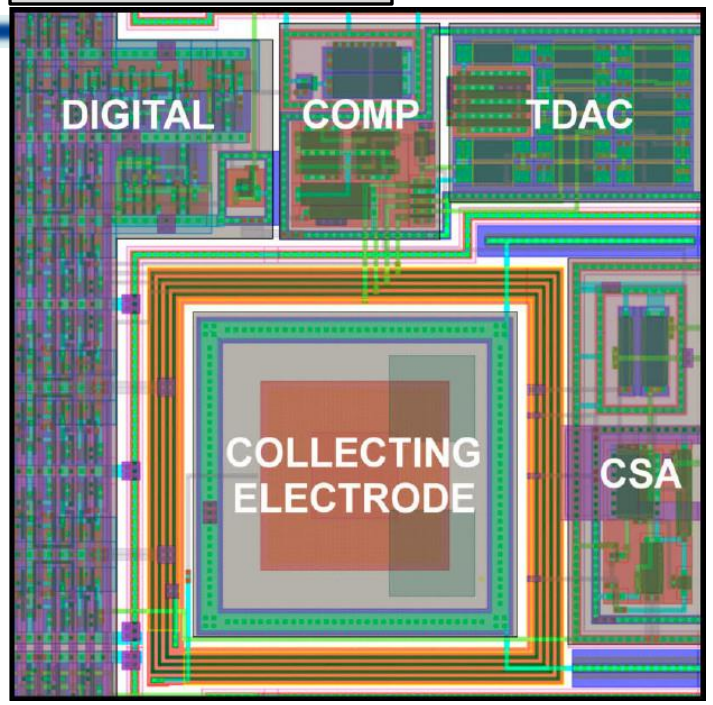


DMAPS pixel

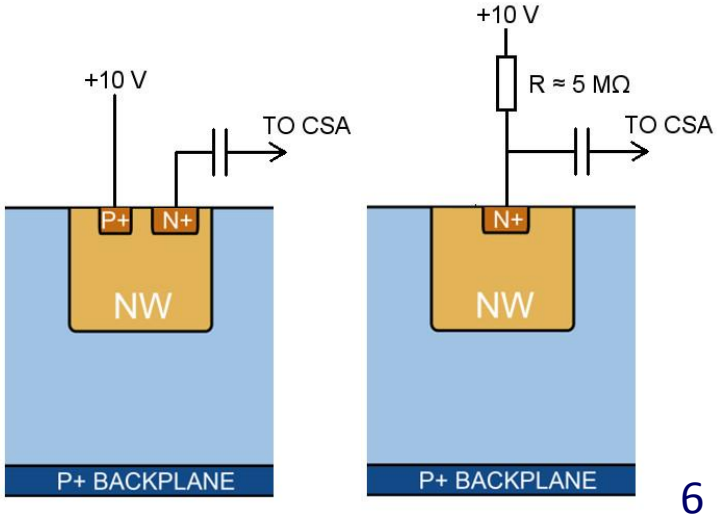
- **Complex CMOS electronics in pixel**
  - 160-180 transistor per pixel
  - Pixel size 40×40 μm^2
  - Sensitive electrode ≈20×20μm^2 (depends what we include)



DMAPS pixel layout



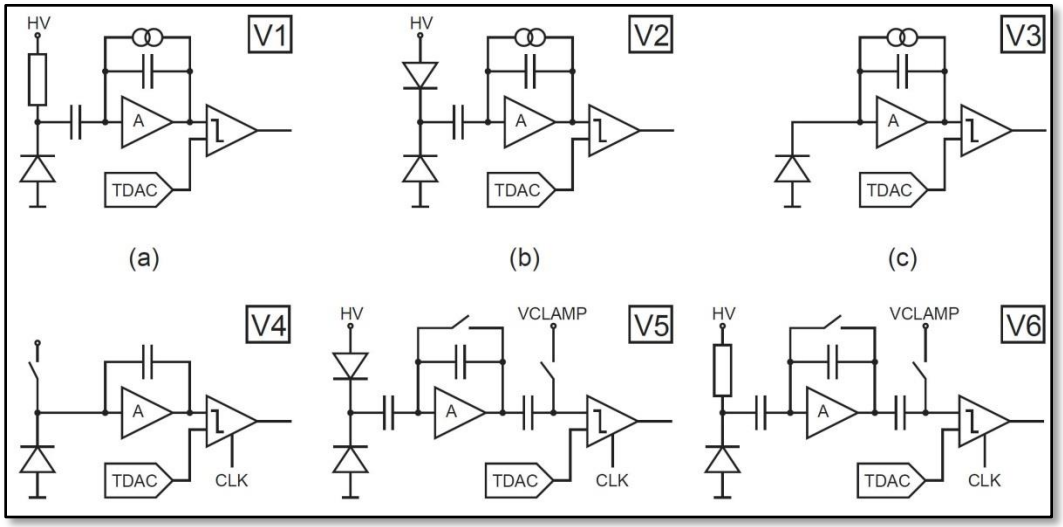
- High voltage domain (≈10V) Low voltage domain (1.8 V)
- **Two sensor biasing options:**
  - biasing with a diode
  - biasing with a resistor



DMAPS pixel variants

- **Explore potential of DMAPS pixels**
  - six matrix variants
  - different sensor geometry
  - different biasing options
  - different front-end architectures

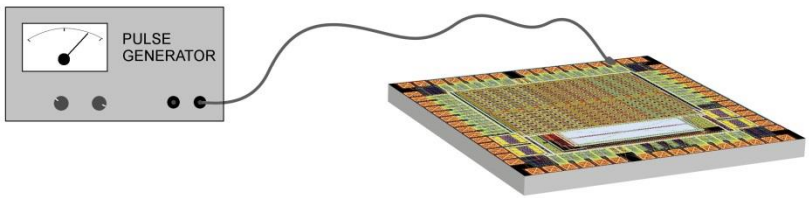
Variants of DMAPS matrices

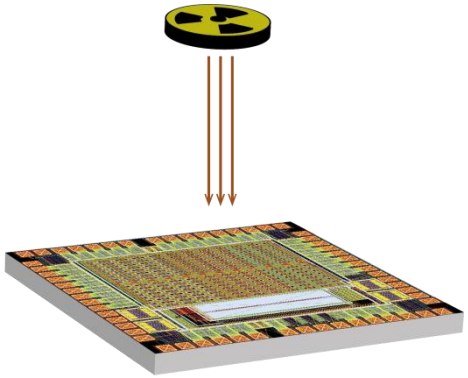


Variant	Sens. el.	Biasing	Coupling	FE arch.	Dimension
V1	Foundry	Resistor	AC	Continuous	8x8
V2	Custom	Diode	AC	Continuous	8x8
V3	Foundry	CSA FB	DC	Continuous	6x8
V4	Foundry	Switched	DC	Switched	6x8
V5	Custom	Diode	AC	Switched	8x8
V6	Foundry	Resistor	AC	Switched	8x8

Tests done with EPCB01

- Initial testing, configurability, response to radioactive sources
- Testing with charge injection, gain, noise
- Cluster size measurement with ^{90}Sr
- Gain determination with ^{55}Fe





- More detailed characterization (laser scan, beam test . . .) will be presented in:

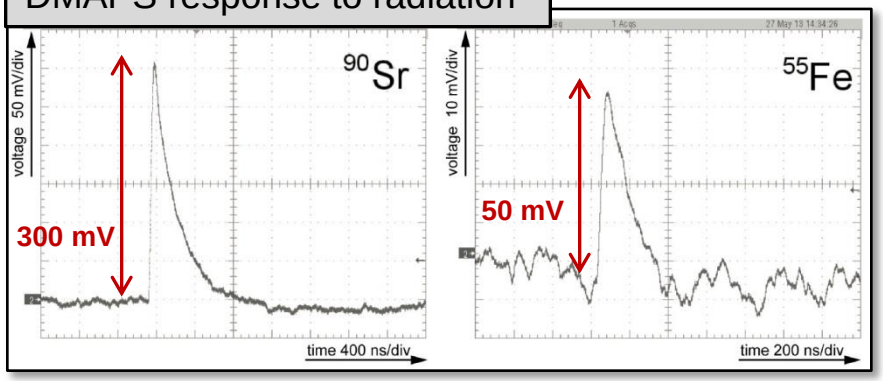
ESPROS DMAPS: Results and Radiation Hardness

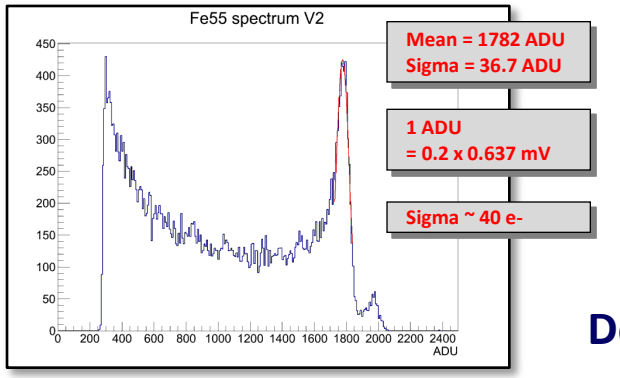
by *Theresa Obermann*

on Wednesday at 16:30

First tests

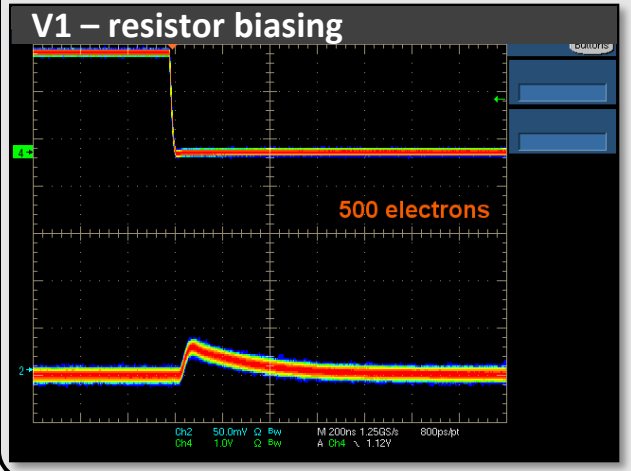
DMAPS response to radiation

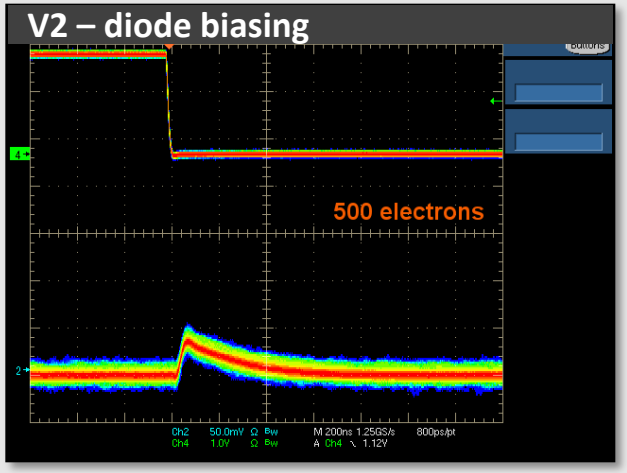


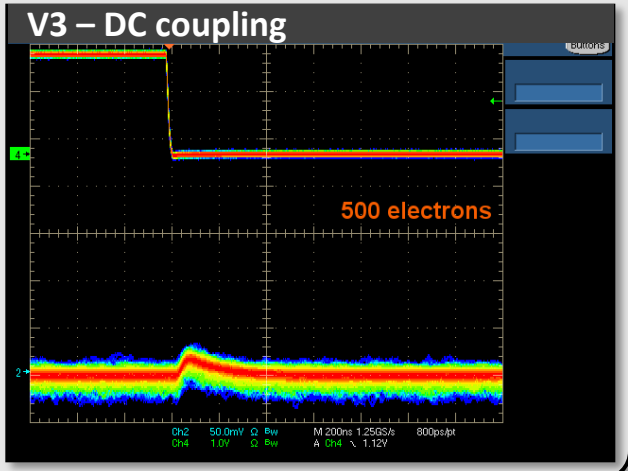


Detector is alive!!

Injection of various signal charge



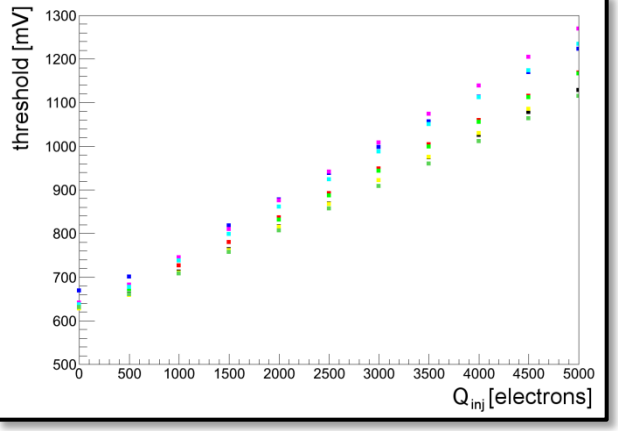




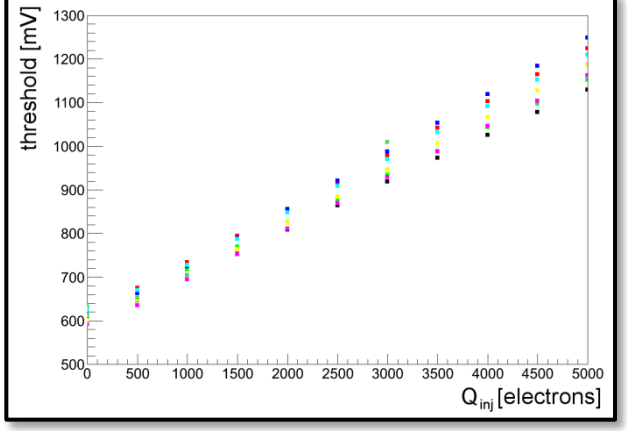
Observation nr. 1: DMAPS pixels respond to signal (injection and irrad.) but each pixel version gives different amplitude

Response to charge injection

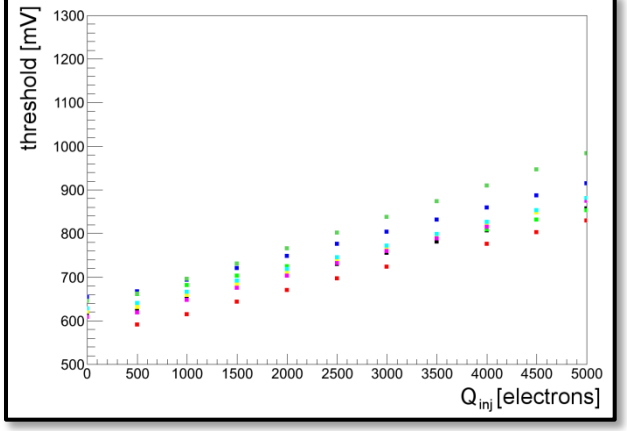
V1 - continuous FE, EPC sens. (AC*, RB*)



V2 - continuous FE, custom sens. (AC, DB**)

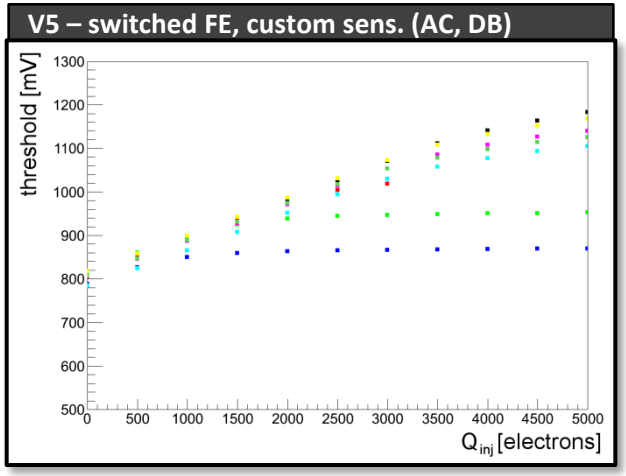


V3 - continuous FE, custom sens. (DC*)

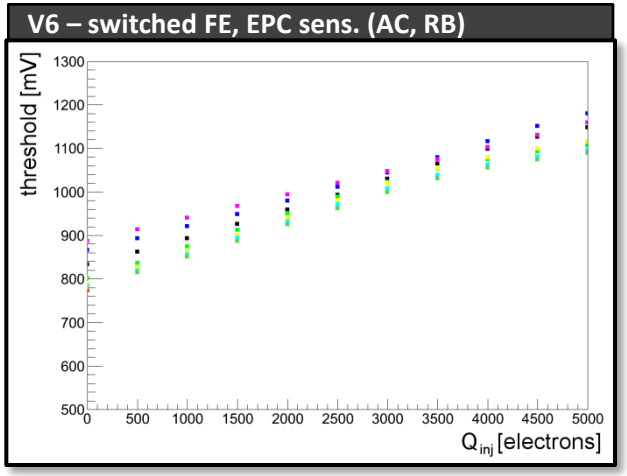


- **Linearity measured with threshold scan (threshold = 50% hits)**
- **Dispersion between channels:**
  - threshold
  - gain

V5 – switched FE, custom sens. (AC, DB)



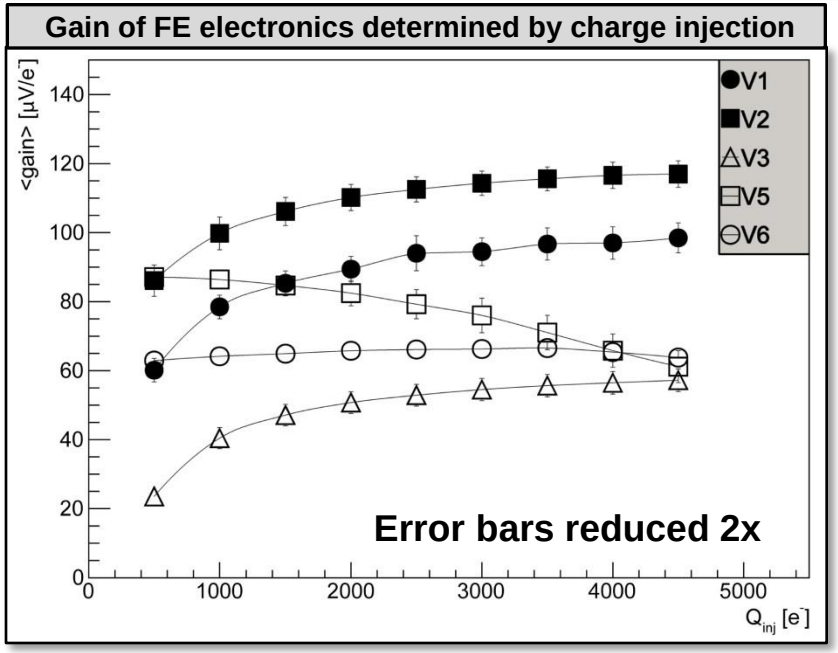
V6 – switched FE, EPC sens. (AC, RB)

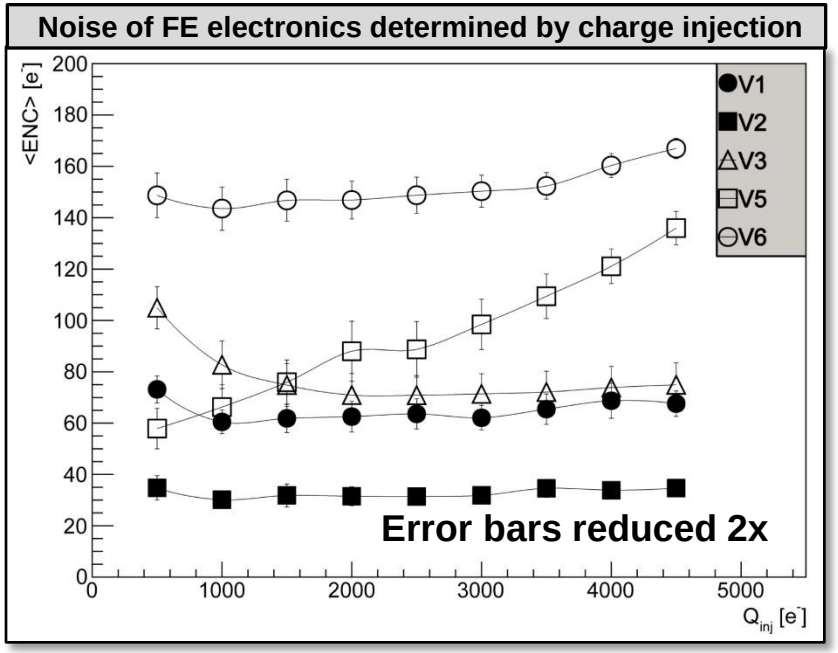


* AC/DC – coupling between sensor electrode and FE

** RB/DB – resistor or diode biased sensor electrode

Gain and noise



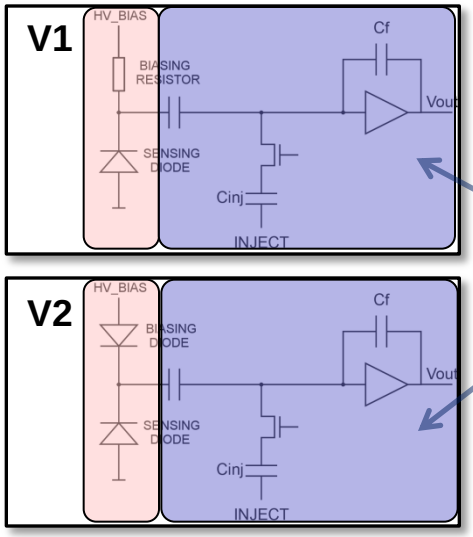


- V2 – best performance: gain ≈ 100 μV/e⁻; noise ≈ 30e⁻
- V1, V2 – identical FE but different gain – WHY?

=> Most likely due to different capacitance of the Sensitive electrode

$$gain = \frac{1}{C_f + \frac{C_d + C_f}{a}}$$

If open loop gain *a* is small, the closed loop *gain* of the CSA can be altered by sensor capacitance C_d



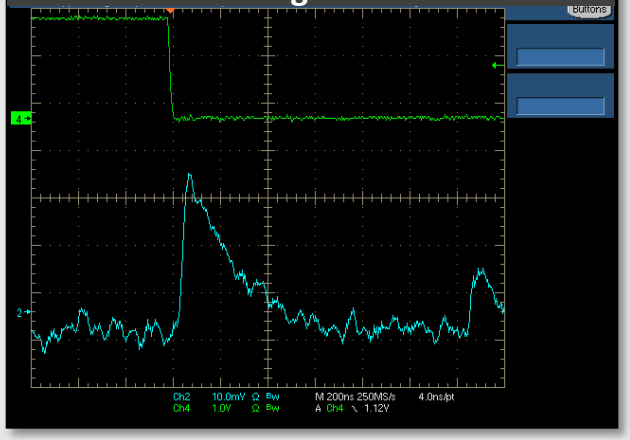
IDENTICAL LAYOUT

Signal and noise of DMAPS pixels

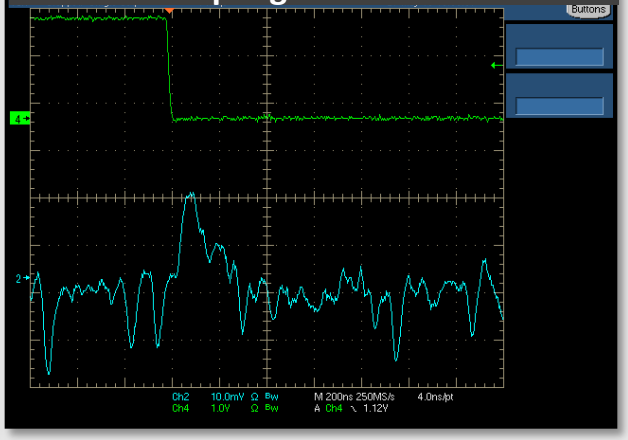
Large noise superimposed on signal (500 e^-)

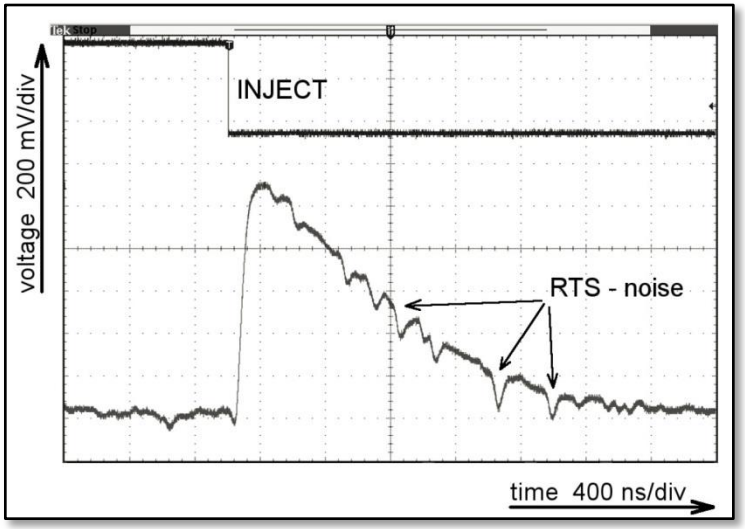
V1 – resistor biasing

V2 – diode biasing



V3 – DC coupling

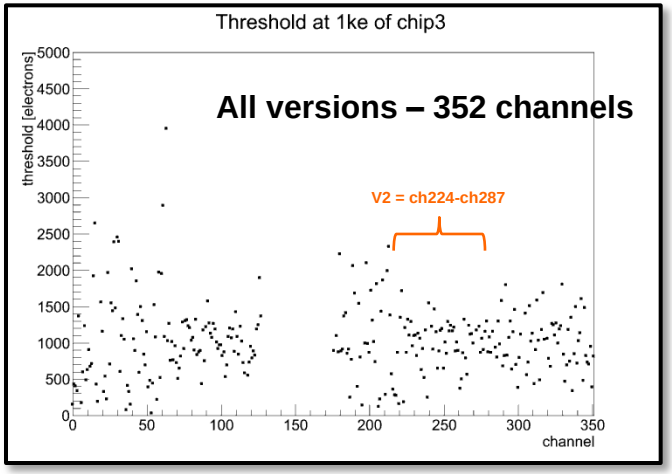


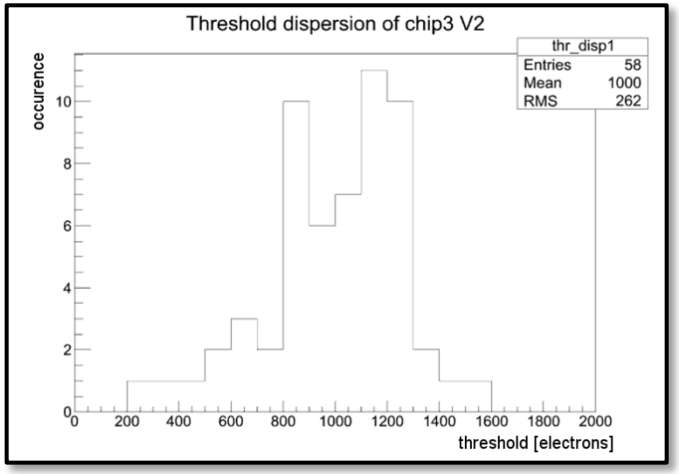


- Excessive noise observed by oscilloscope
- Present in all DMAPS variants
- Random telegraph noise
- Can be caused by too small transistors

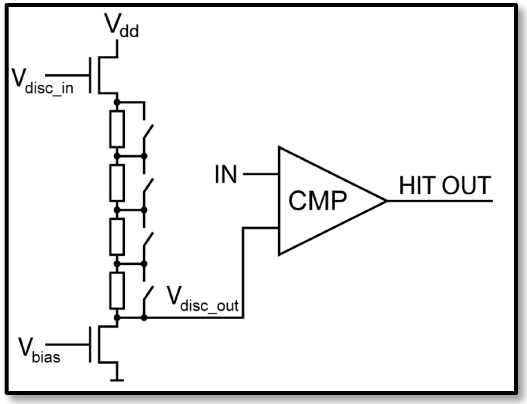
Threshold tuning

- Untuned chip has large threshold fluctuations

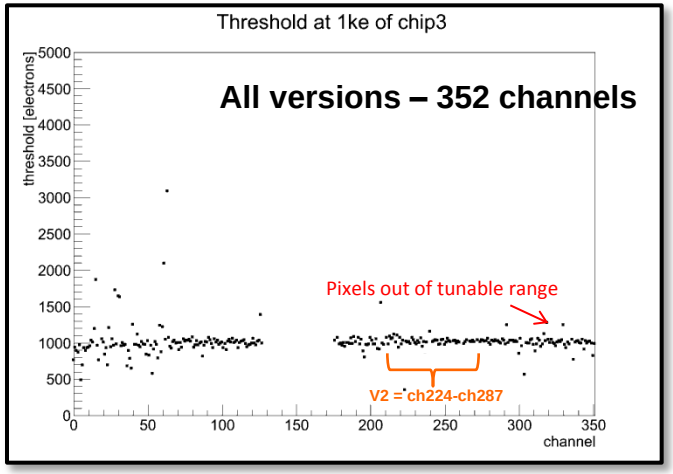


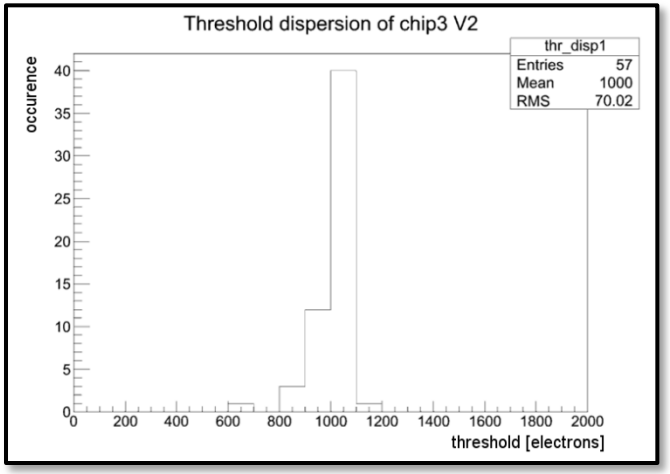


TDAC in V1-V3:

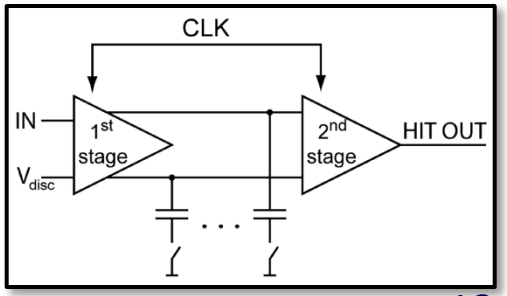


- Tuning helps to reduce fluctuations in all versions

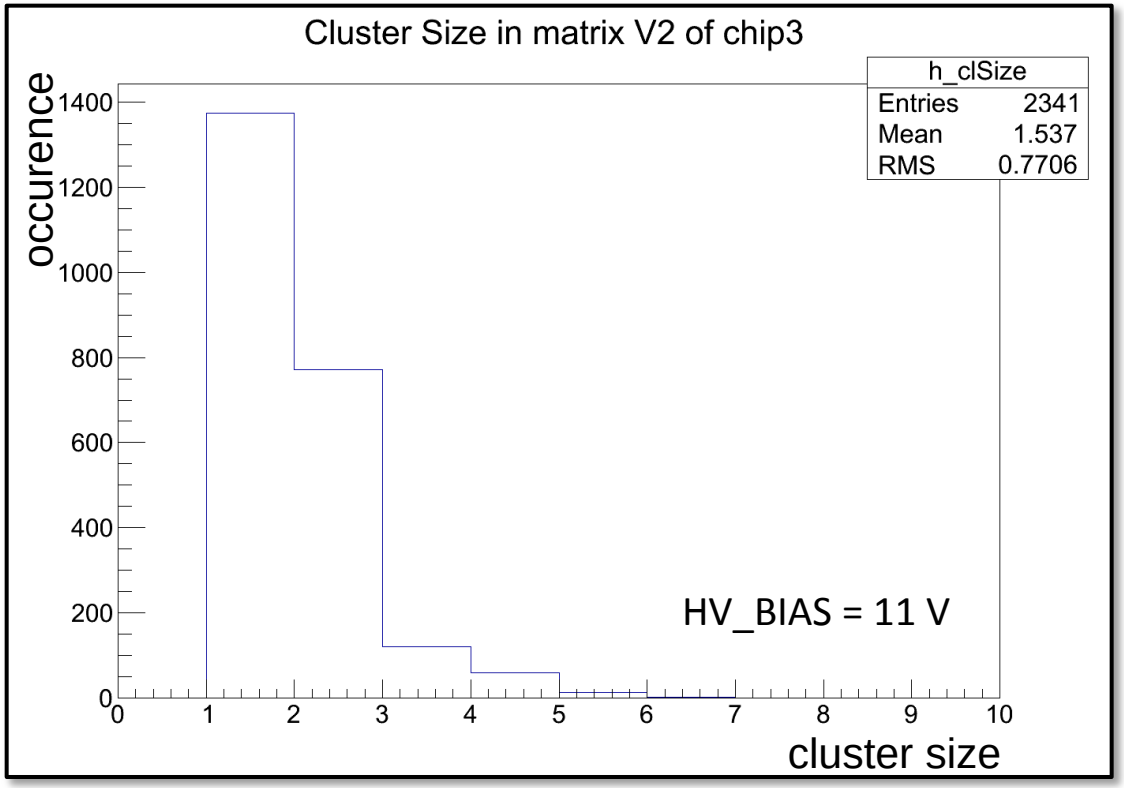


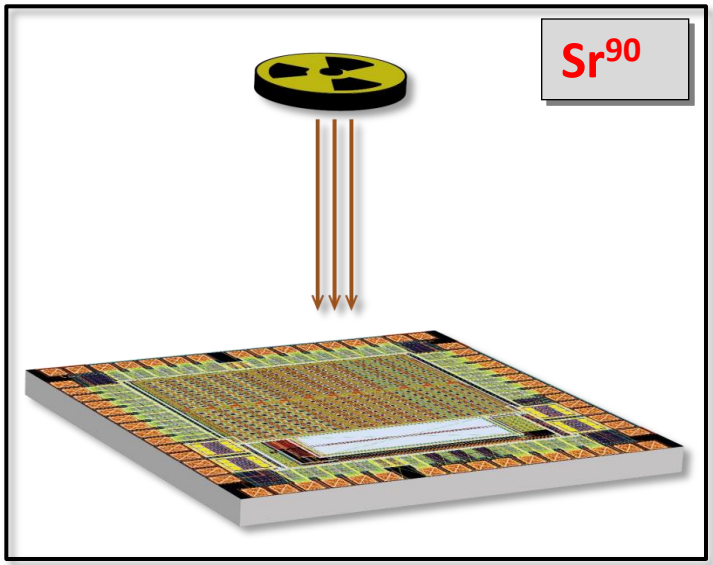


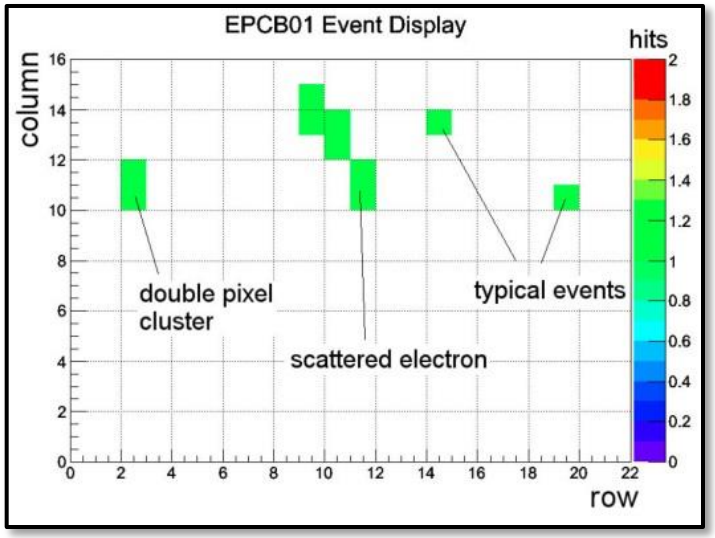
TDAC in V4-V6:



Cluster size

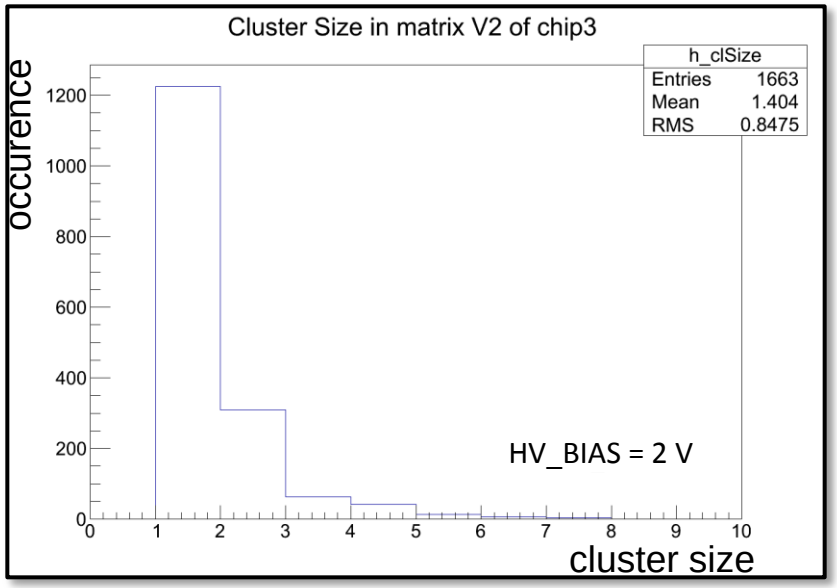


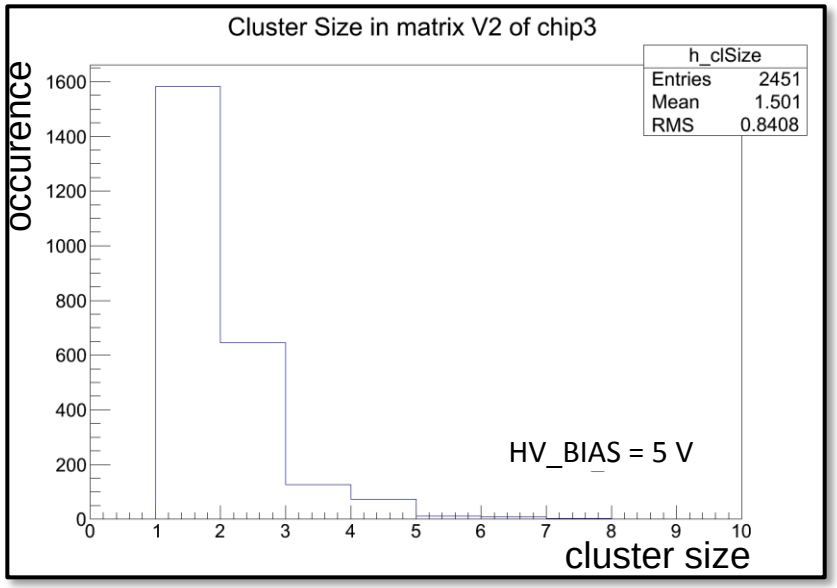


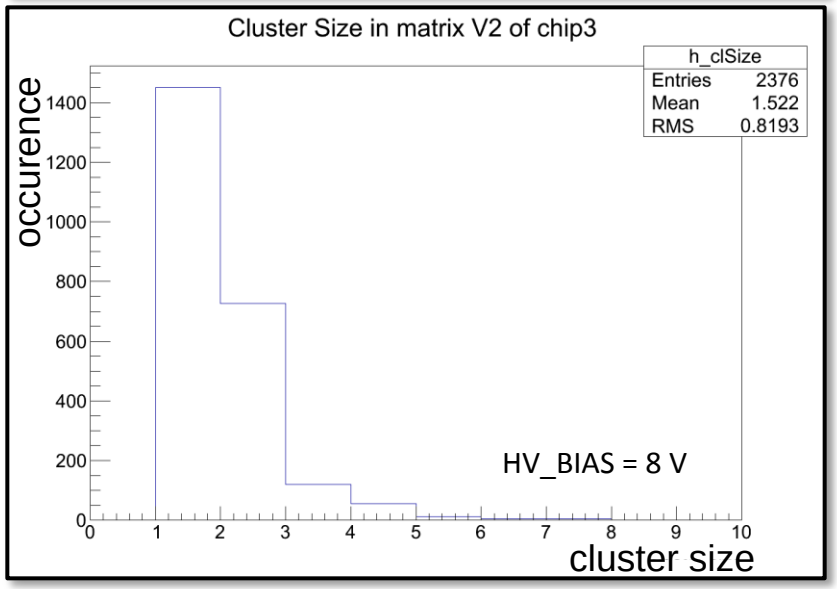


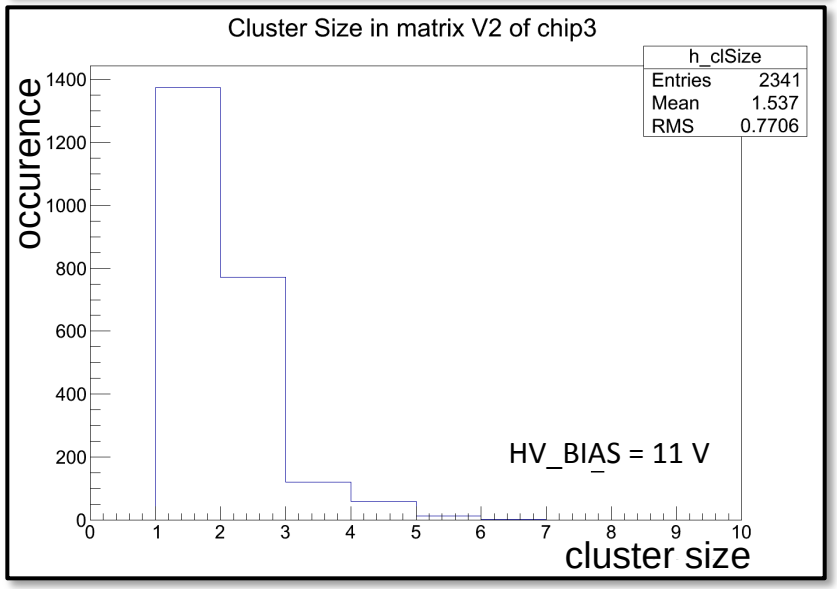
- Threshold set to 1 ke$^-$ and tuned
- Mostly single and double pixel clusters
- Long tail due to soft component of energy spectrum of Sr^{90}
- How the clusters change if we change bias voltage ??

Cluster size - bias voltage effects

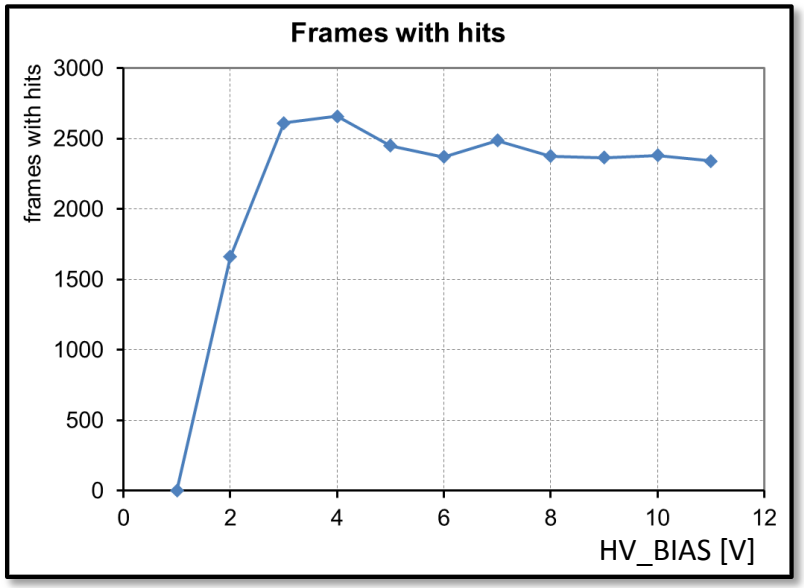


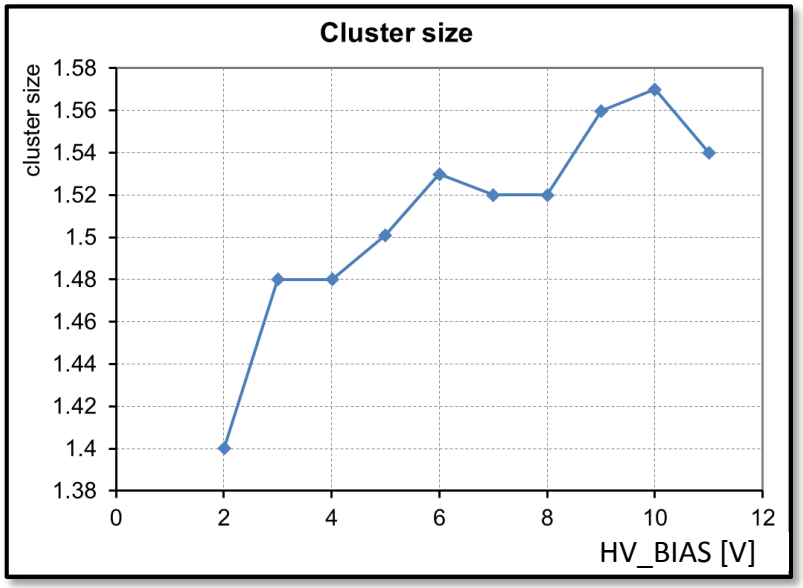




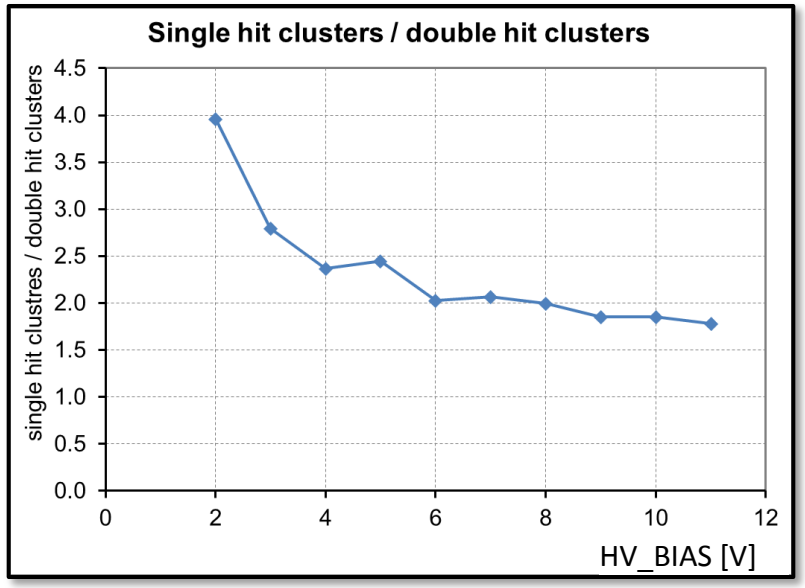


Cluster size - bias voltage effects

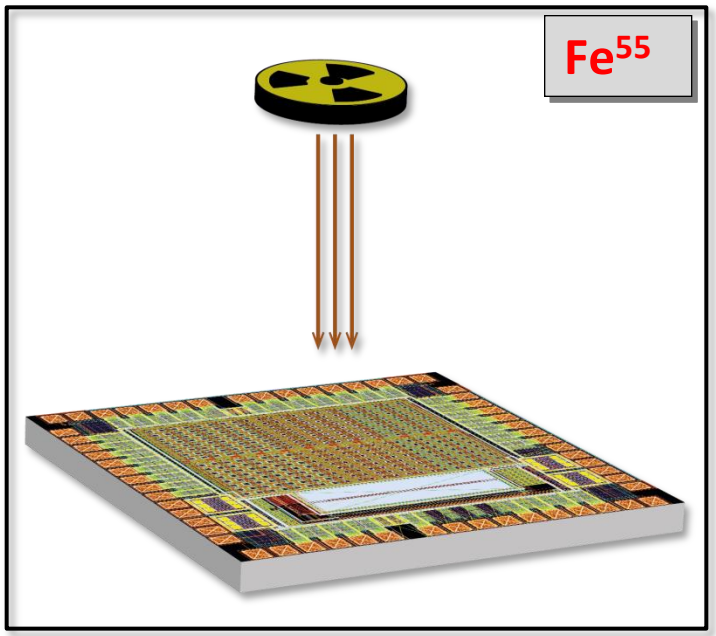


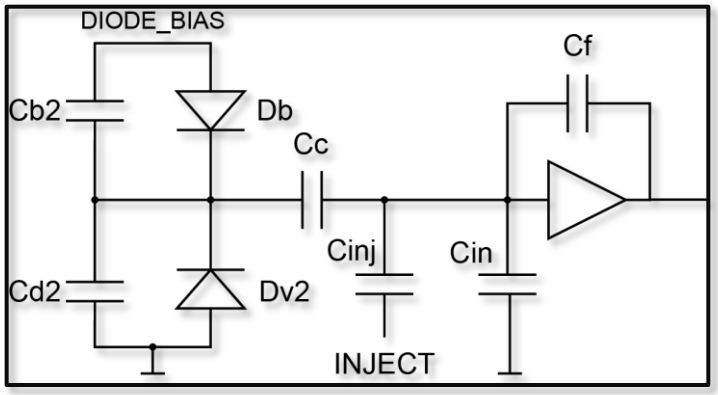


- Number of hits almost constant at HV_BIAS > 3 V
- Average cluster size increases with bias voltage
- Single hit / double hit clusters decreases with HV_BIAS and saturates at 6 V (full depletion)

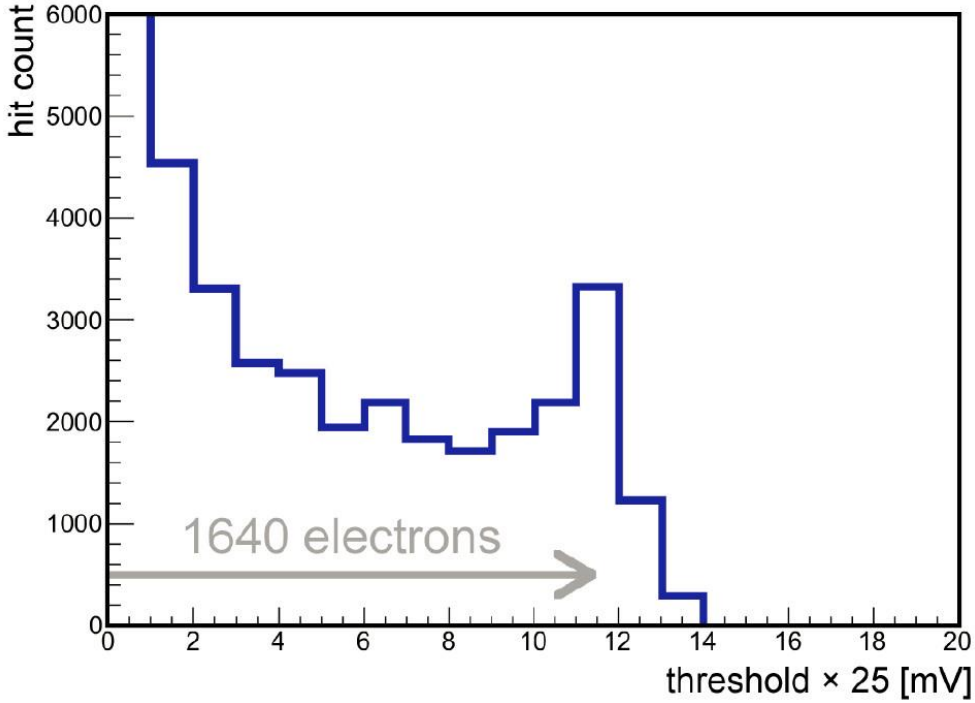


Gain determination with Fe^{55}

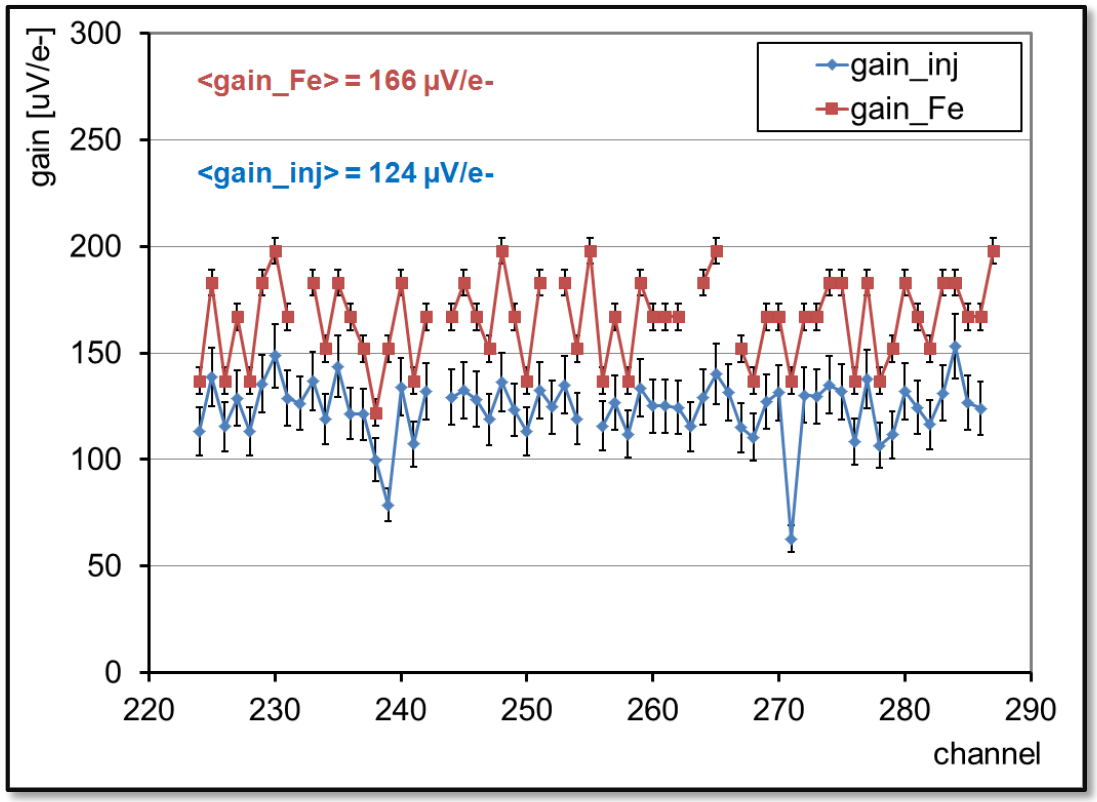




- DMAPS channel – single bit resolution
- Differentiating threshold scan we can get spectrum
- Enormous statistics needed:
  - data collection ~ 10 days
  - reconstructed spectrum at every pixel:



Gain comparison V2 (injection VS source scan)



- Gain from source scan is **34 % higher** than determined by charge injection
- **Gain variations between channels almost match in both cases**
- Systematic shift can be explained by increasing input capacitance when charge injection is enabled → gain decreases (see next slide)

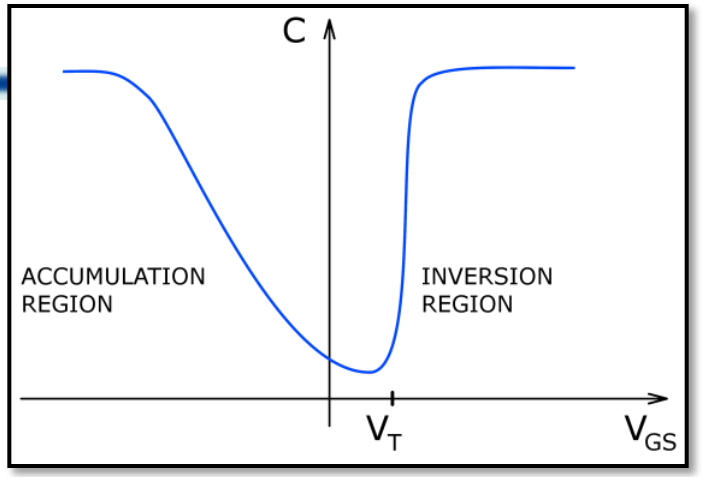
- **Determination of error bars:**

1.) Q injection method: uncertainty of injection capacitance 10 % (≈ typical process variation)

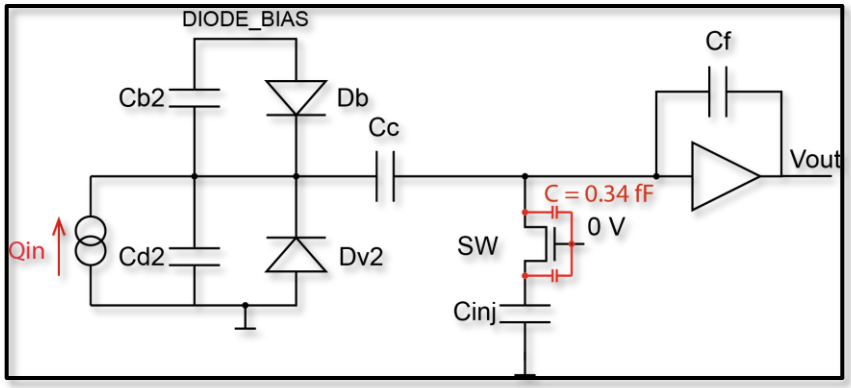
2.) ^{55}Fe source scan: error (1 std. dev.) comes from coarse binning of ^{55}Fe spectrum to see the peak

Explanation of gain difference

Capacitance of MOSCAP

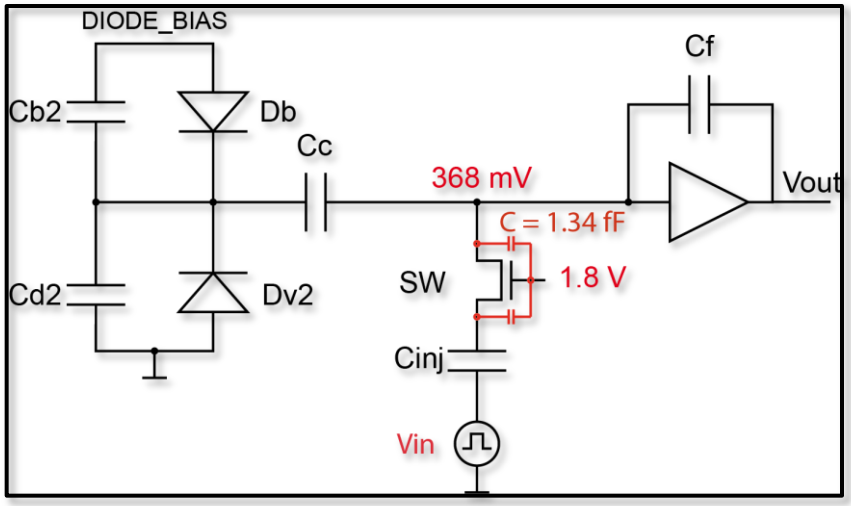


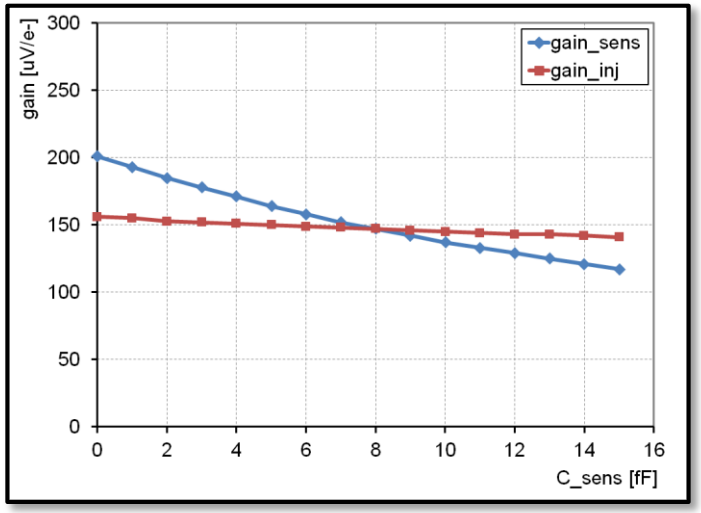
- Situation 1 (charge injected from sensor side):



- **When SW is ON, CSA sees higher input capacitance by ≈ 1 fF reducing gain when injection is enabled**
- Since capacitance of input transistor is 0.62 fF the additional capacitance of 1fF is significant
- **Simulation test – gain measured by both methods**

- Situation 2 (charge injected with injection circuit):





Lessons learned with EPCB01

- **General remarks**
  - Concept of DMAPS pixels works – but FE electronics needs improvements!!
  - Open loop gain of CSA needs to be large (at least several hundreds)
  - Closed loop gain has to be carefully adjusted by additional feedback capacitance (1-2 fF)
  - Use larger transistors to reduce danger of RTS noise

- **Designers remarks:**

  => every 100 aF capacitance matters!!

  => optimize routing of the CSA to minimize parasitic capacitances

  => design carefully injection circuit not to add too much parasitic capacitance

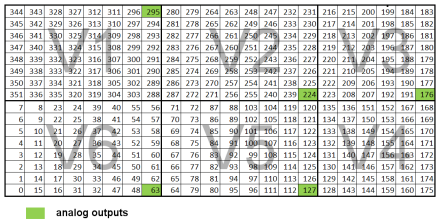
  => post-layout simulation and understanding influence of parasitics is important

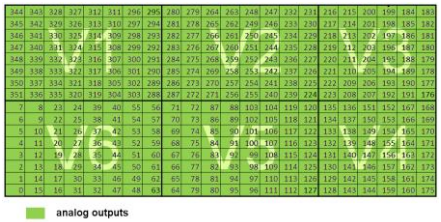
EPCB02

- **EPCB02 is evolution of EPCB01**

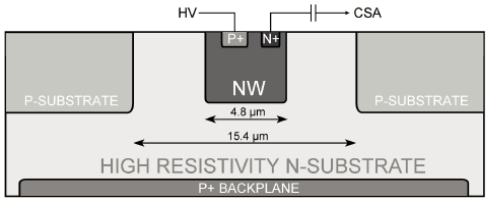
  - cascode amplifier with high open loop gain
  - added 2 fF feedback capacitor -> uniformity
  - both charge collection electrodes are custom
  - input transistors are larger
  - each pixel has analog output

  (multiplexed → unity gain buffer → IO pad)

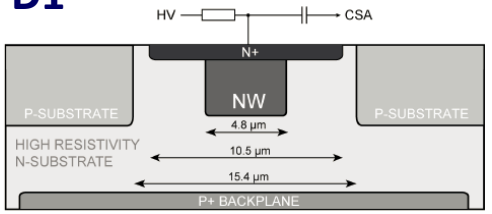




D2



D1



- **EPCB02 will allow to study independently:**

  V1 vs V2 – effects of biasing (RB/DB)

  V1 vs V4 – cont. vs switched FE

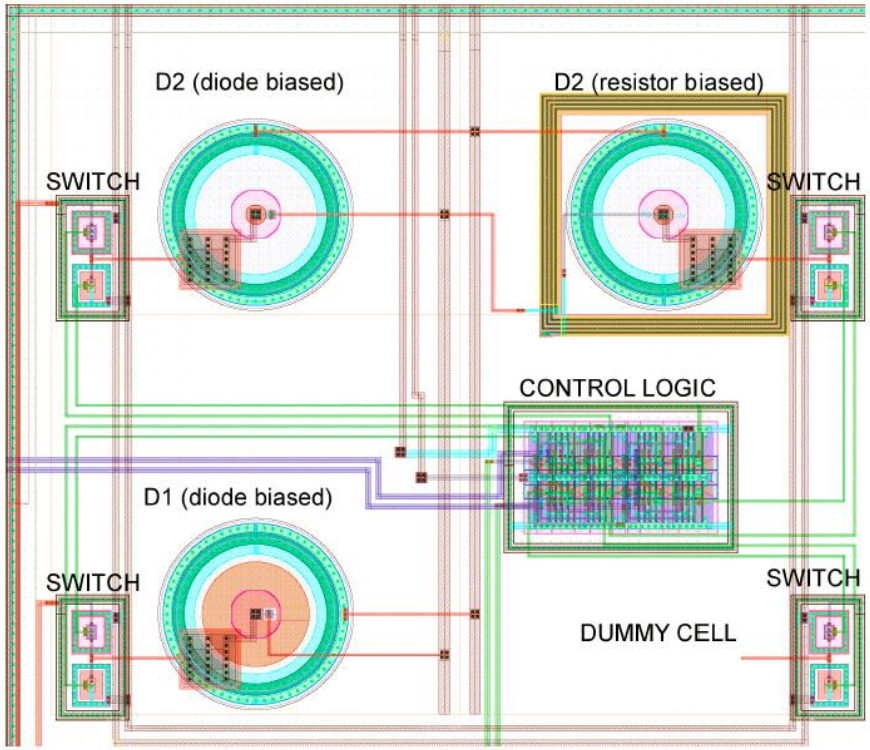
  V4 vs V5 – different sensor geom.

  V4 vs V6 – different transistor size

Variant	Sensor	Biasing	FE-type	M1 dim.
V1	D2	DB	CONT	1µ/300n
V2	D2	RB	CONT	1µ/300n
V3	D1	DC	CONT	1µ/300n
V4	D2	DB	SW	1µ/300n
V5	D1	DB	SW	1µ/300n
V6	D2	DB	SW	2µ/150n

Circuit for capacitance measurement in EPCB02

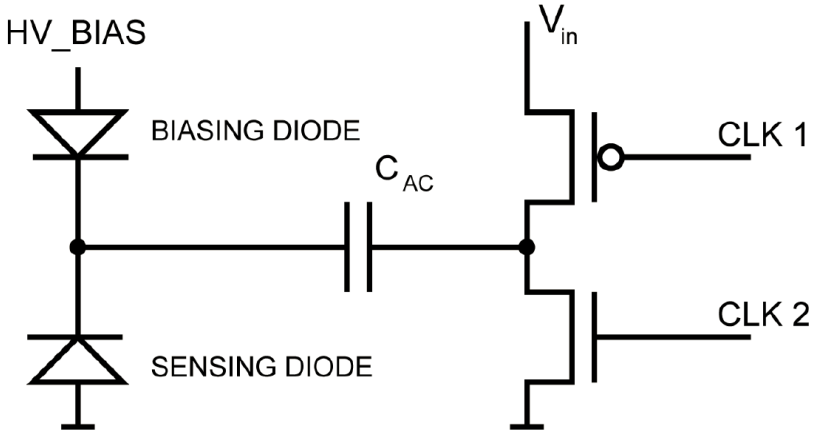
- Various layouts and biasing circuits can influence sensor capacitance
- C_d is important parameter for rise-time and noise optimization
- Charge-pump based circuit for capacitance measurement of DMAPS sensor



- **Two transistor charge pump:**

  - CV measurement => depl. voltage.

  - compare different geometries



Conclusions

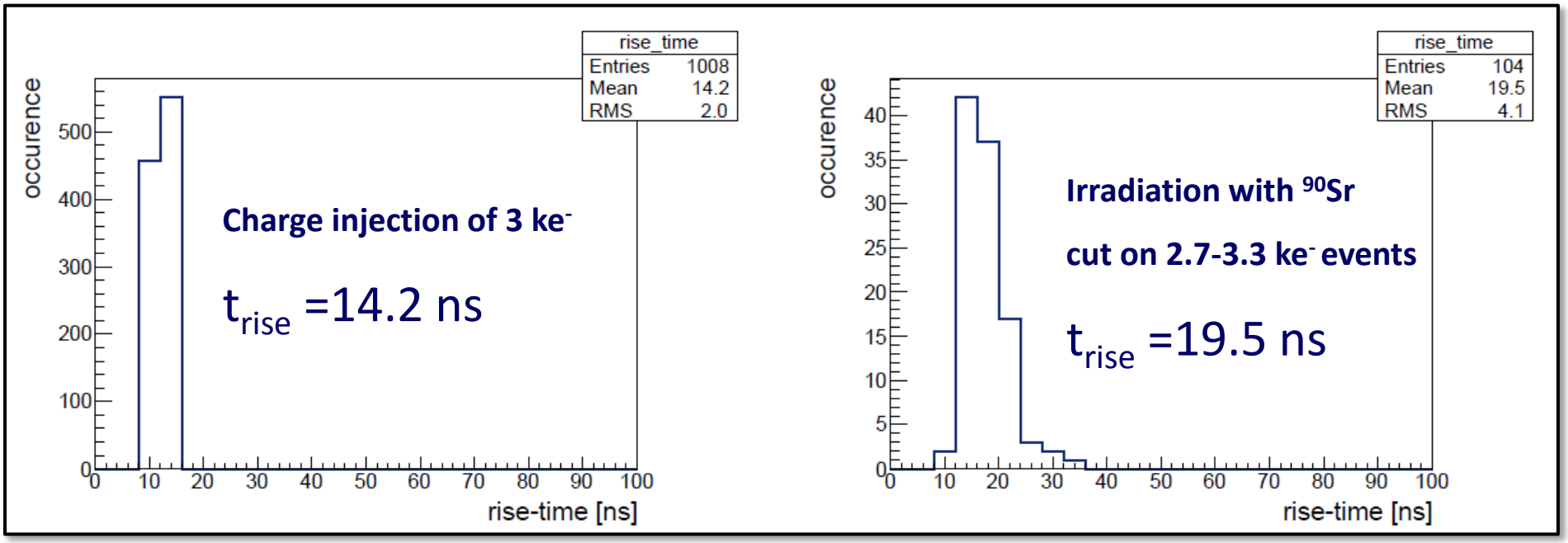
- **EPCB01 demonstrator of DMAPS sensor in ESPROS technology**
  - Depletion voltage ≈ 6 V (based on cluster size saturation)
  - Gain variation between pixels ≈ 20 %, significant threshold dispersion
  - RTS noise
  - New chip EPCB02 will allow more detailed studies of DMAPS pixels

- **Open questions for applications in HEP:**
  - Radiation hardness and effects of radiation damage
  - How to integrate complex digital logic (ToT, trigger logic, SEU latches …..)?

Thank you for your attention

Signal rise-time

- Rise-time => 25% - 75% signal amplitude
- Upper limit on charge collection time



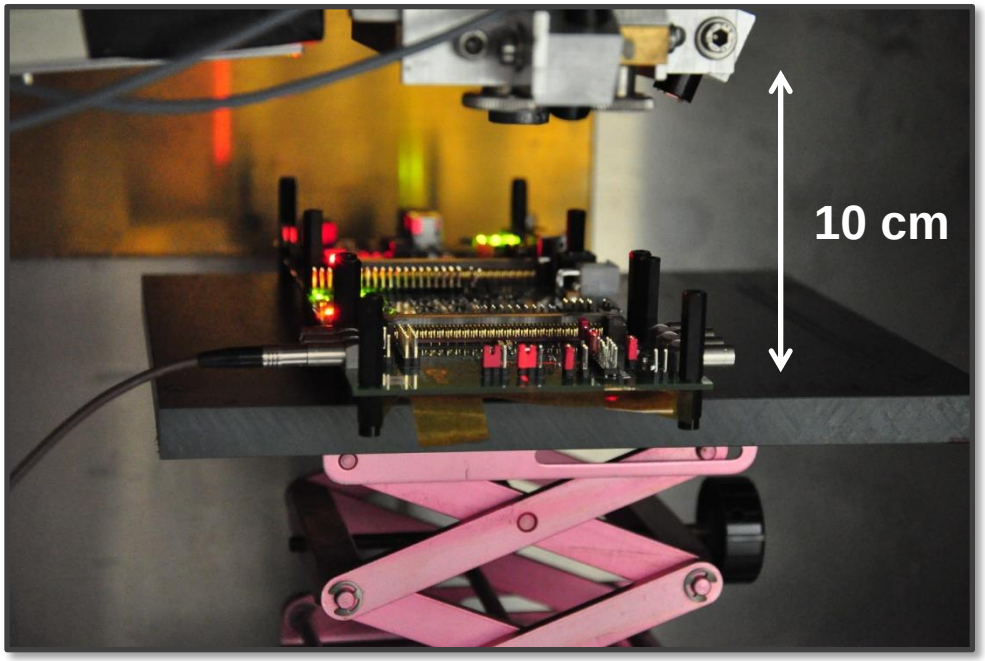
- Fast charge collection
- 50 % of the signal charge is collected for less than 19.5 ns

X-ray irradiation

X-ray irradiation
End-point energy 60 keV

Doses:
200 krad – 50 Mrad

Annealing:
100 min @ 80 °C

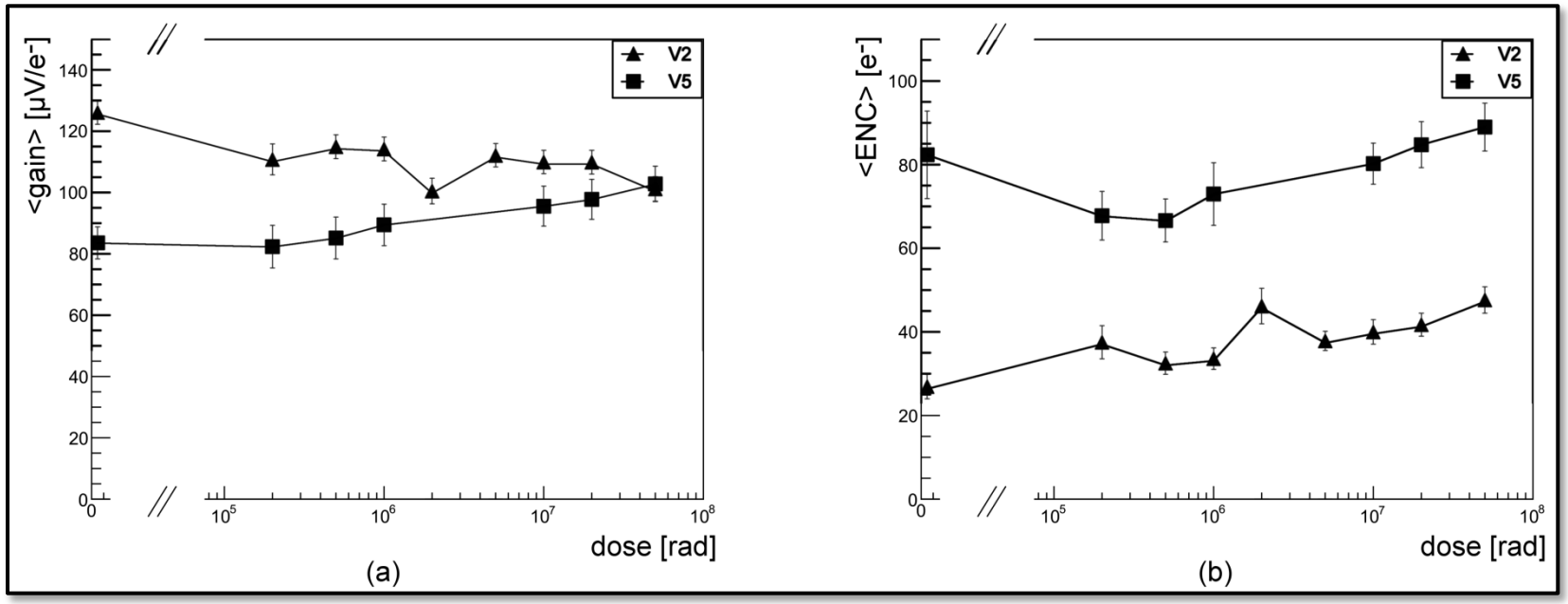


Tests:

threshold scan w/wo charge injection of 2ke -> fitting S-curve -> threshold
-> gain and ENC extraction

digital test: shift in / shift out data patterns: 0000…, 111…, 10101…
discharge curves of the CSA
IV-curves of the sensor

Radiation effects

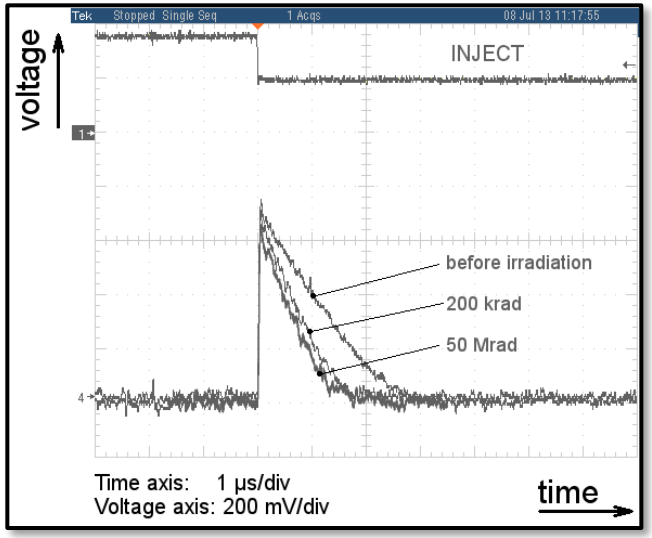


- Small radiation effects in analog FE:

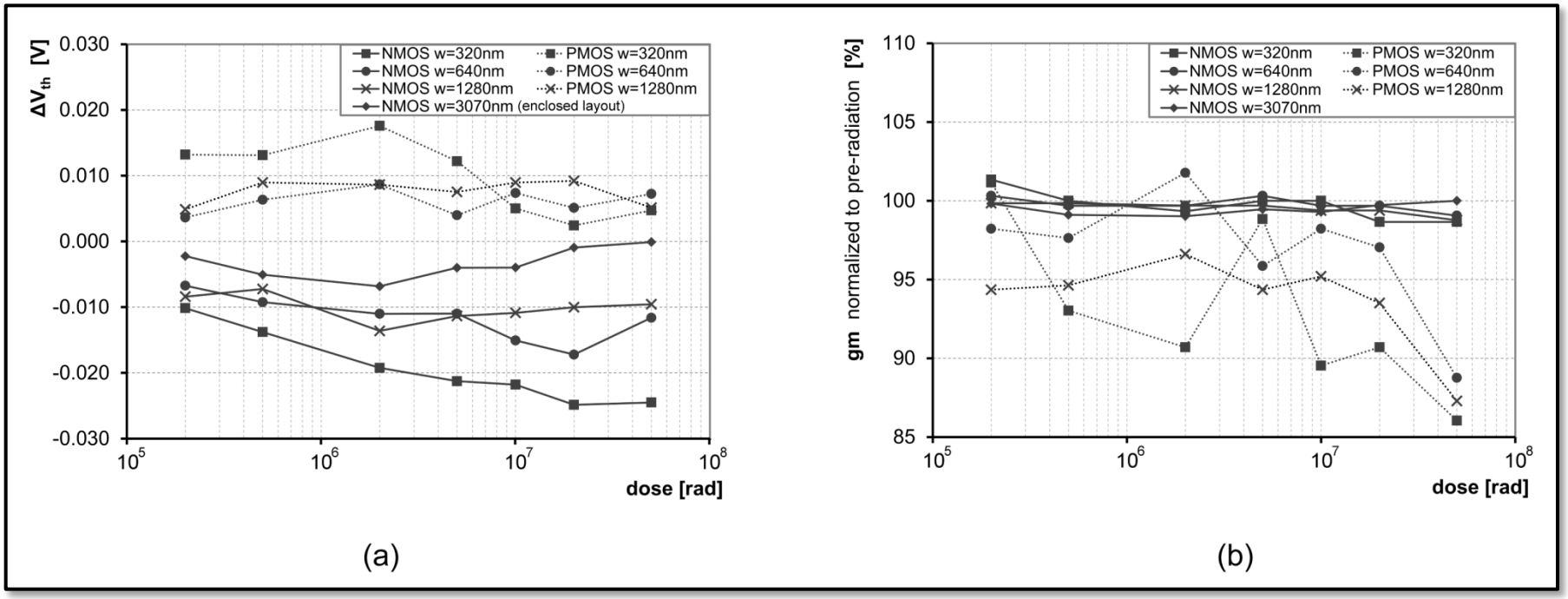
  - small changes of gain and noise

  - pulse shortening

- No effect on digital logic at all



Radiation effects - transistors



Measured by *L. Germic*

- Threshold voltage shift of all transistors
- gm degradation – mostly affects PMOS – narrow channel