APSEL Deep n-well and Deep p-well CMOS Sensors with ST and TowerJazz Technologies

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OUTLINE

- ✓Introduction
- ✓Deep n-well CMOS MAPS with ST technology
  - ✓APSEL Sensor
  - ✓SDR0 Sensor
- ✓Deep n-well CMOS MAPS with IBM technology
- ✓Deep p-well CMOS MAPS with TJ technology

Workshop on CMOS Active Pixel Sensors for Particle Tracking (CPIX14)

15th – 17th September 2014, Bonn, Germany

Motivations

- Experiments at the future high luminosity colliders and B-factories (ILC, SuperB) need fast, highly granular, low material budget particle trackers
- CMOS monolithic active pixel sensors (MAPS) may provide improved position and momentum resolution
  - based on collection of diffusing charge → may be thinned to a few tens of μm, low multiple scattering
  - minimal readout electronics → small pitch, high spatial resolution but no PMOS transistors
- Modern VLSI CMOS processes (180 nm and below) could be exploited to increase the functionality in the elementary cell -> design of MAPS with similar readout functionalities as in hybrid pixels (sparsification, time stamping)
  - A readout architecture with data sparsification could give some advantages with respect to standard, CIS-like MAPS implementations
- MAPS approach takes advantage of CMOS triple well structures to improve the readout speed of MAPS sensors through pixel level sparsification -> **APSEL family and SDR0 chip**
- A step toward full compliance with the experiment specs may be represented by vertical integration techniques → 3D DNW MAPS integrated in the first run of the 3D-IC collaboration

Talk V. Re this morning

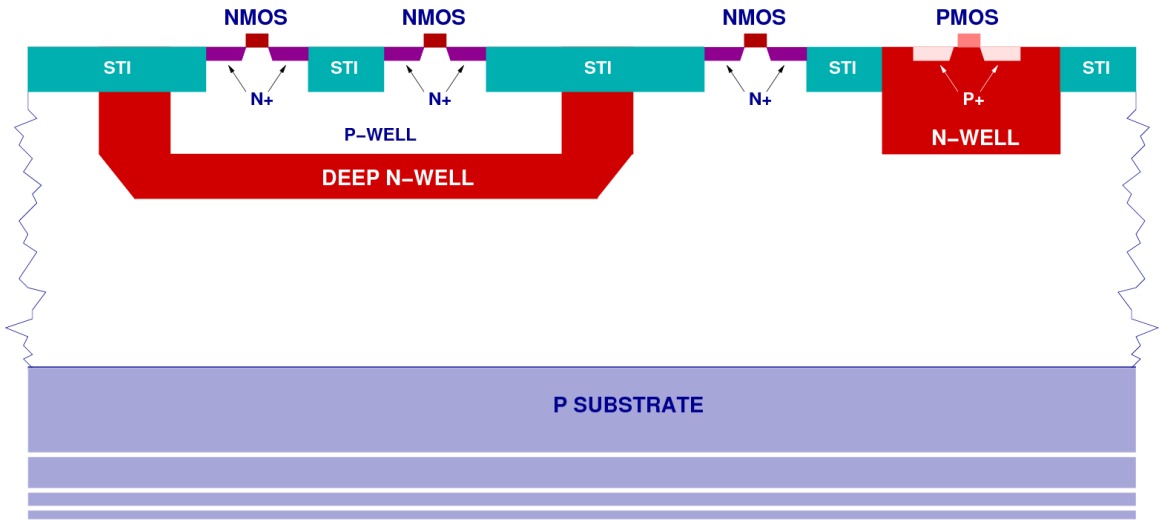
- Depending on the experiment characteristics, MAPS may be required to withstand a total ionizing dose from a few 10 krad to a few Mrad per year (e.g.: SuperB SVT Layer0 specs: 3 Mrad/yr and $5 \cdot 10^{12}$ 1 MeV neutron equivalent/cm^2/yr, challenging for CMOS MAPS)

Talk L. Ratti on Wednesday

- CMOS MAPS with sparsified readout in a high-resistivity epitaxial layer, deep p-well technology (INMAPS process provided by TowerJazz) -> **APSEL4WELL chip**

Deep n-well MAPS with the 130nm CMOS STMicroelectronics technology

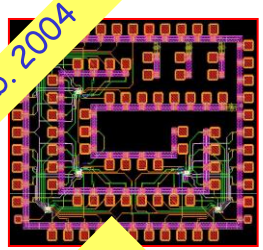
Deep n-well (Triple Well) Process

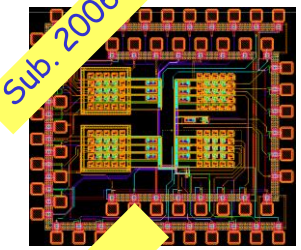


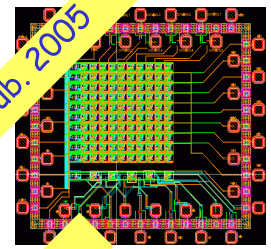
- In triple-well CMOS processes a deep N-well is used to shield N-channel devices from substrate noise in mixed-signal circuits
- DNW MAPS is based on the same working principle as standard MAPS

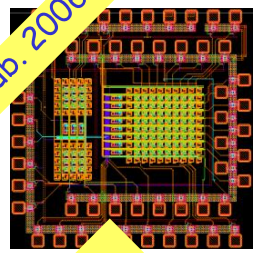
- Classical optimum signal processing chain for capacitive detector can be implemented at pixel level
- The collecting electrode (DNW) can be exploited to obtain higher single pixel collected charge
- A charge preamplifier is used for Q-V conversion → gain decoupled from electrode capacitance
- DNW may house NMOS transistors and using a large detector area, PMOS devices may be included in the front-end design → charge collection efficiency depends on the ratio between the DNW area and the area of all the N-wells (deep and standard)

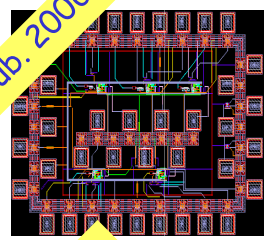
APSEL series chips

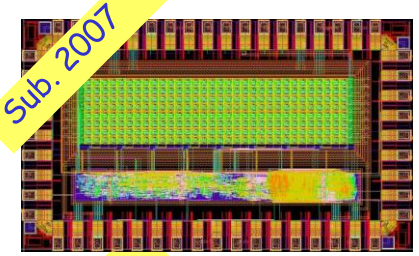


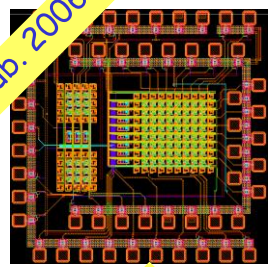


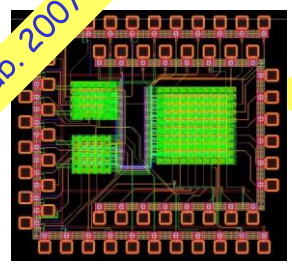


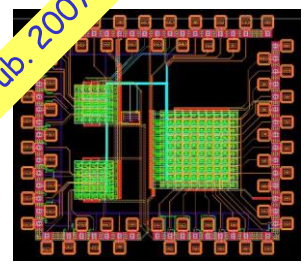


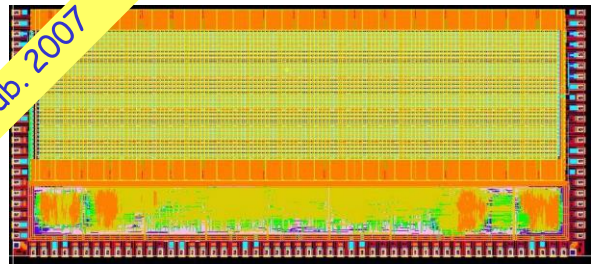




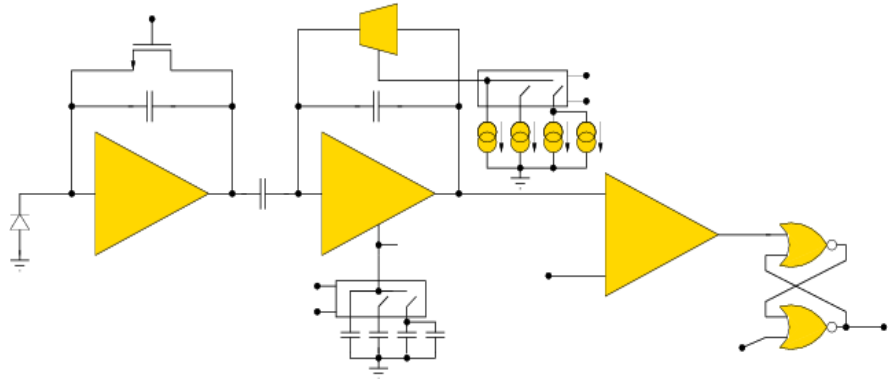








SuperB

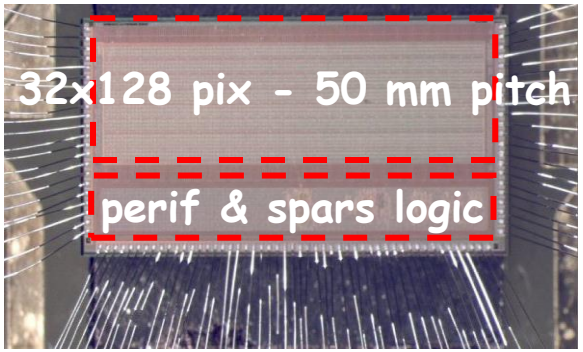


Full in-pixel signal processing:
PA + shaper + comparator + latch

- Prototypes fabricated with the STMicroelectronics 130nm triple-well technology
- High sensitivity charge preamplifier with continuous reset + RC-CR shaper with programmable peaking time
- A threshold discriminator is used to drive a NOR latch featuring an external reset
- Pixel size: 50um x 50um
- The first prototypes proved the capability of the sensor to collect charge from the substrate

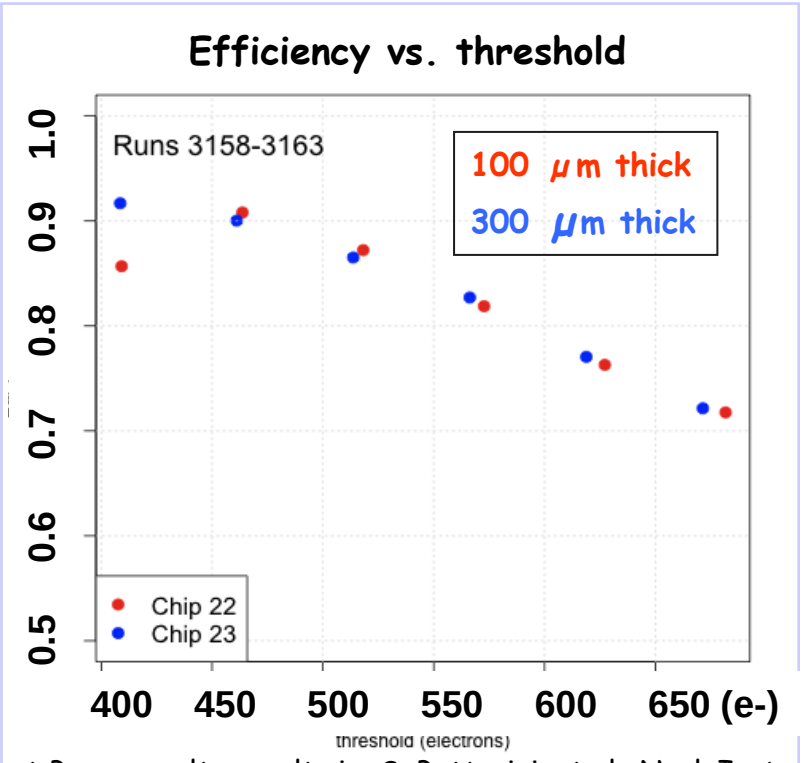
APSEL4D

4K(32x128) 50x50 μm^2 matrix subdivided in MacroPixel (MP=4x4) with in-pixel data sparsification and time stamping, continuous readout, tested with beams in September 2008



- MAPS hit efficiency up to 92 % @ 400 e- thr.
- 300 and 100 um thick chips give similar results
- Intrinsic resolution ~ 14 um compatible with binary readout

- Competitive N-wells (PMOS) in pixel cell steal charge reducing the hit efficiency: fill factor (DNW/tot N-well) ~90%
  - efficiency can be improved by optimizing the sensor layout -> APSEL5
  - even better using a deep p-well process (INMAPS) -> APSEL4WELL
  - MAPS in a vertically integrated technology -> APSEL5TC



Test Beam results results in: S. Bettarini, et al., Nucl. Instr. and Meth. A (2010), doi:10.1016/j.nima.2010.08.026

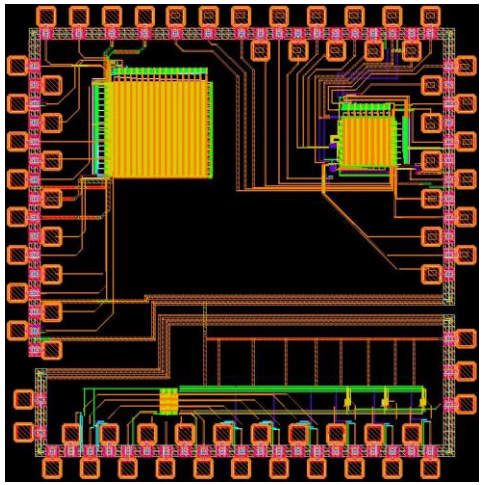
130nm CMOS DNW MAPS for the ILC vertex detector

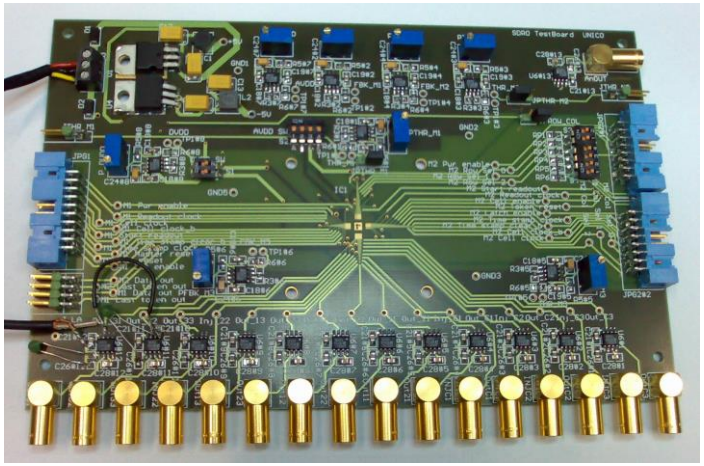
- INFN program (Milano, Pavia) started in 2006; design DNW MAPS according to ILC specifications
- Same concept as in the APSEL chips, but reduced pixel pitch and power dissipation
- Digital readout architecture with in-pixel sparsification logic and time stamping, taking into account the beam structure of ILC

The SDR0 chip includes:

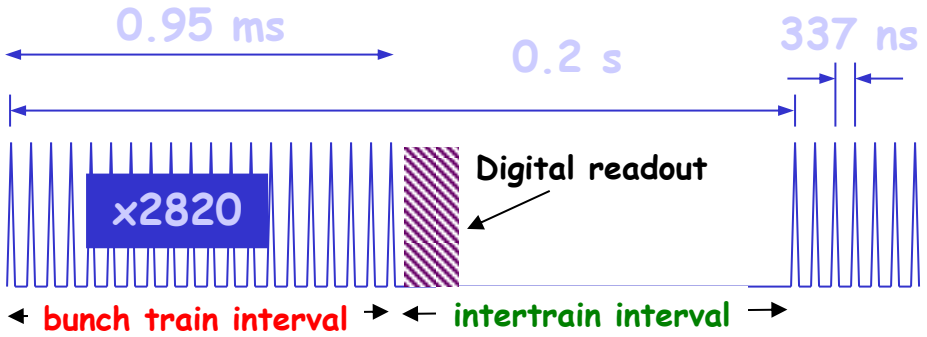
- a 16 by 16 MAPS matrix (25 μm pitch) with digital sparsified readout
- an 8 by 8 MAPS matrix (25 μm pitch) with digital sparsified readout and selectable access to the output of the PA in each cell
- a 3 by 3 MAPS matrix (25 μm pitch) with all of the PA output accessible at the same time
- 3 standalone readout channels with different C_D (detector simulating capacitance)

Delivered end of July 2007





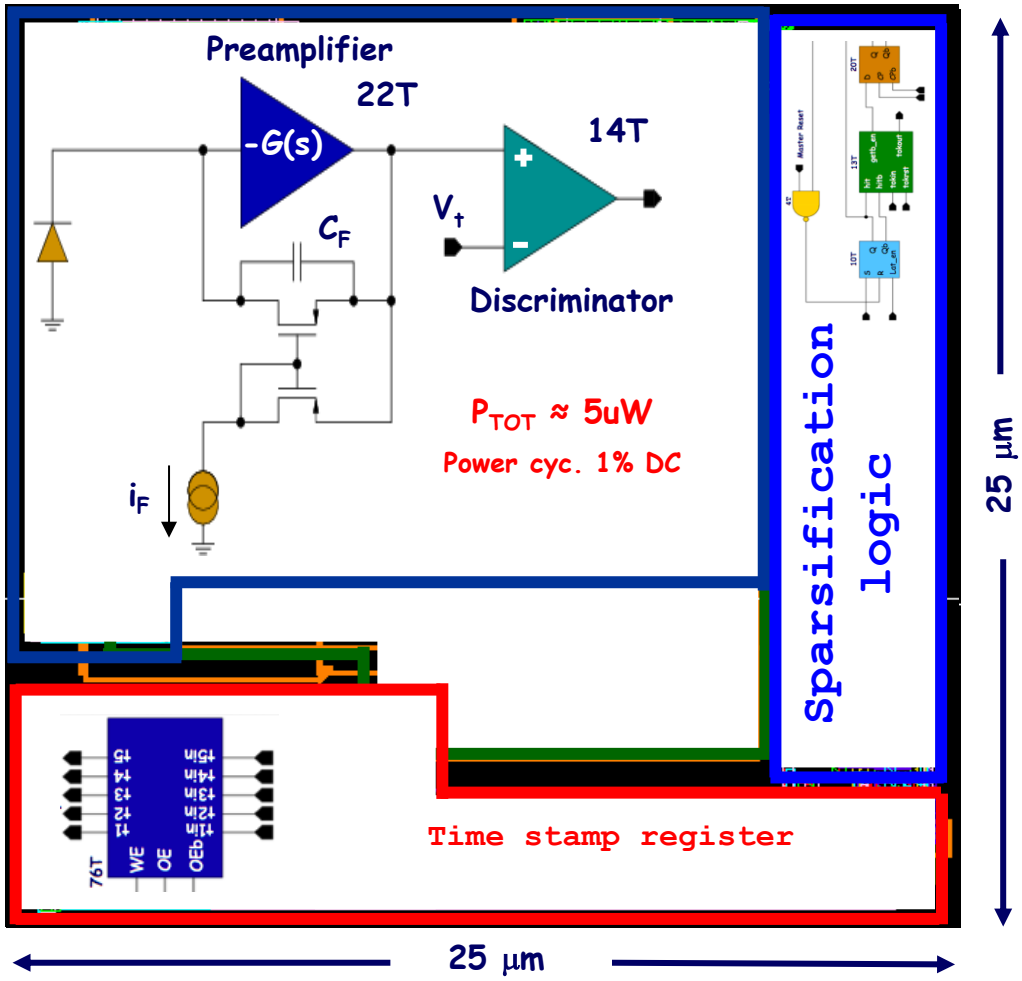
Design specifications for the ILC vertex detector



- The beam structure of ILC will feature 2820 crossings in a 1 ms bunch train, with a DC of 0.5%.
- Assuming:
  - maximum hit occupancy 0.03 part./Xing/mm^2
  - 3 pixels fire for every particle hitting → hit rate ≈ 250 hits/train/mm^2
  - digital readout adopted: 5um resolution requires 17.3 um pixel pitch

- 15 um pixel pitch → $O_c \approx 0.056$ hits/train → the probability of a pixel being hit at least twice in a bunch train period ≈ 0.0016 → there is no need to include a pipeline for storing more than one hit per pixel (more than 99% of events recorded without ambiguity)
- MAPS sensor operation is tailored on the structure of ILC beam
  - Detection phase (corresponding to the bunch train interval)
  - Readout phase (corresponding to the intertrain interval)
- Data readout in the intertrain interval → system EMI insensitive
- Sparsified readout based on the token passing scheme. This architecture was first implemented in the VIP1 chip (3-D MIT LL technology) by the ILC pixel design group at Fermilab

SDRO prototype elementary cell



analog front-end

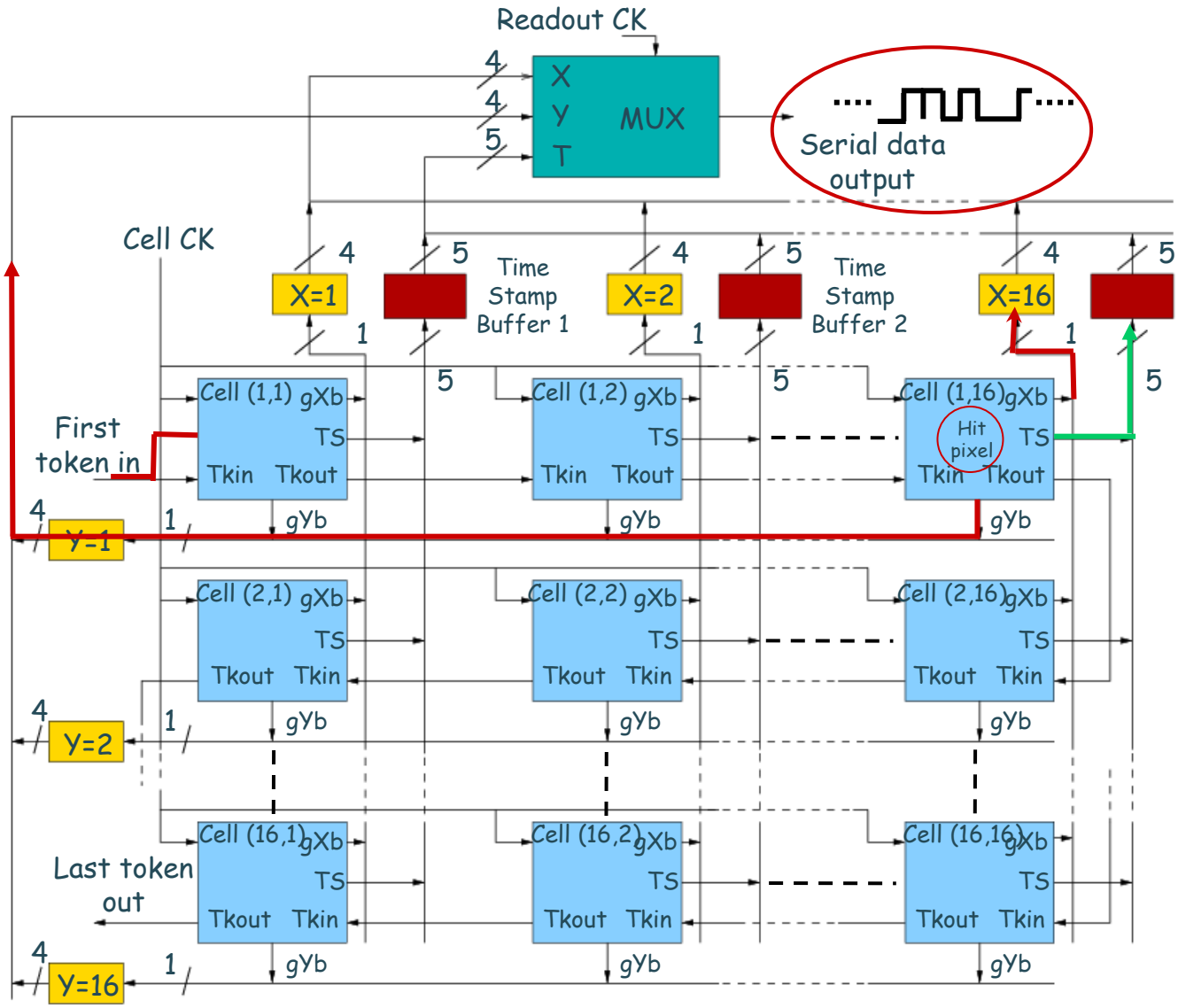
+

digital section

↓

164 transistors

Digital readout scheme



Readout phase:

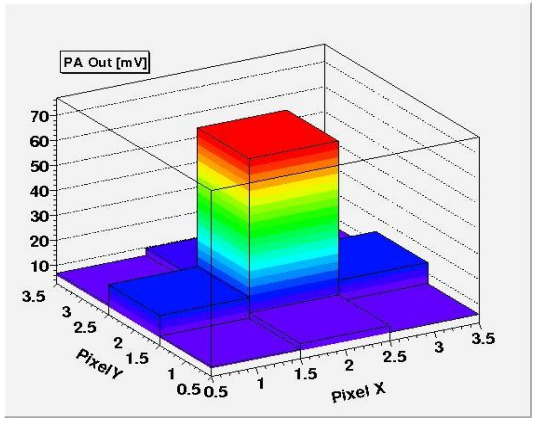
- token is sent
- token scans the matrix and
- gets caught by the first hit pixel
- the pixel points to the X and Y registers at the periphery and
- sends off the time stamp register content
- data are serialized and token scans ahead

The number of elements may be increased without changing the pixel logic (just larger X- and Y-registers and serializer will be required)

SDRO experimental results

- Tests on the analog section with injection of external calibration signals, with ^{55}Fe, and with an infrared laser scan (single channels, 3x3 pixel matrix)
- Charge sensitivity: 650mV/fC (mean value with ^{55}Fe)
- ENC ≈ 60 e- rms
  (PA input device: I_D = 1 uA, W/L= 22/0.25)
- Threshold dispersion ≈ 60 e-

Matrix response to infrared laser



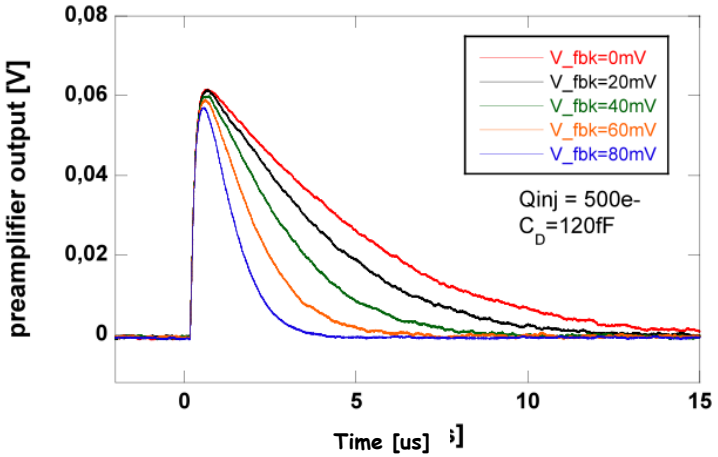
Laser on rear of sensor

λ=1064nm
(σ_{XY} ≈ 1.5 μm)

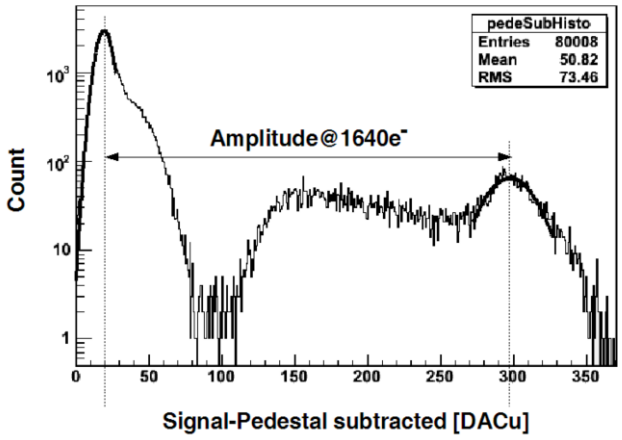
Laser focussed on the central pixel

Limited charge spreading

Preamplifier response to an external calibration signal

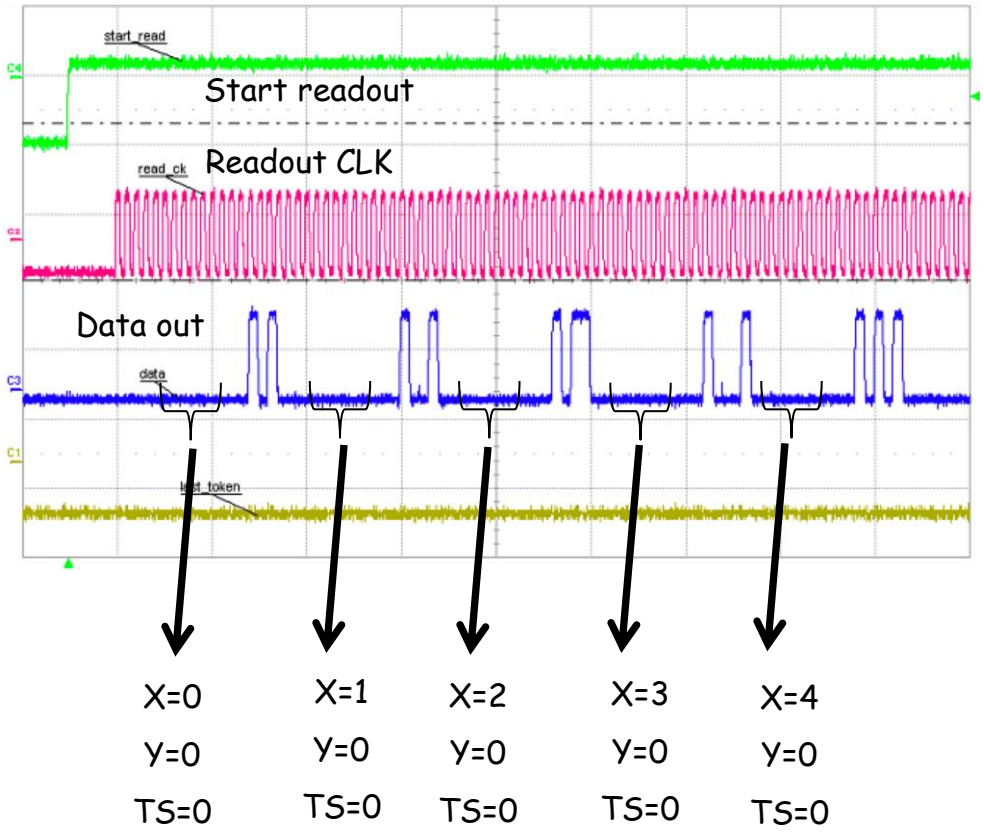


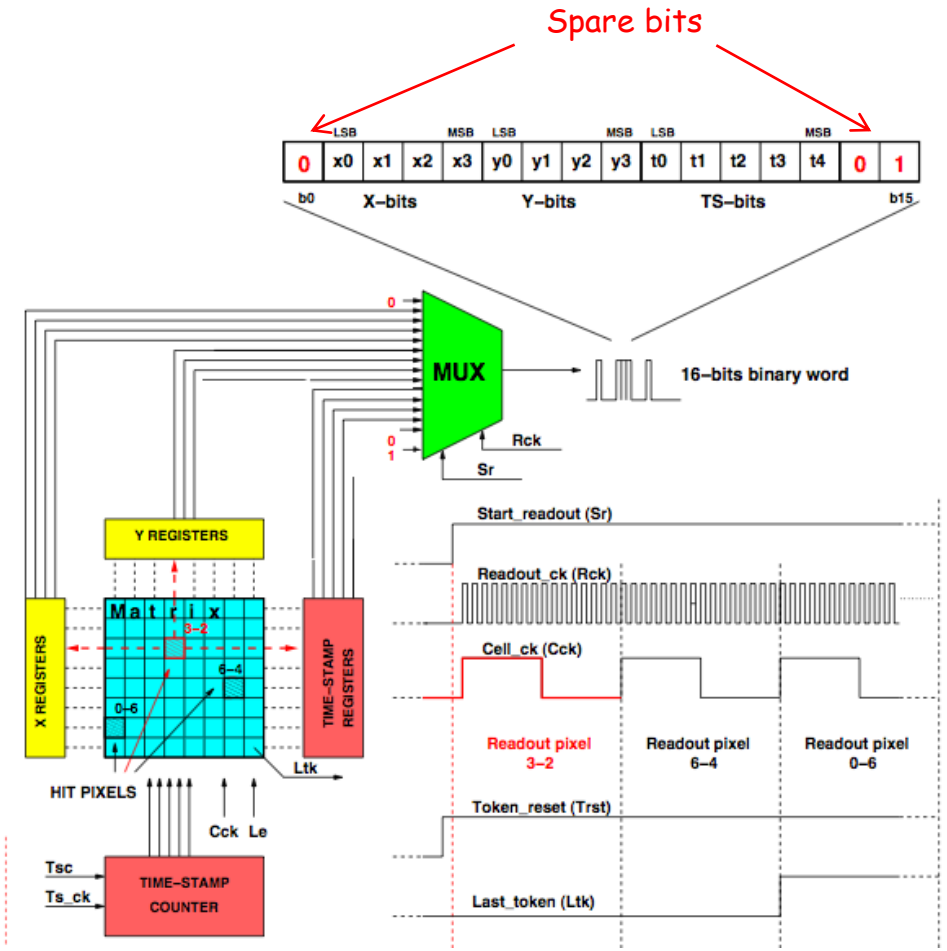
Test with ^{55}Fe



Digital readout test: pixel address

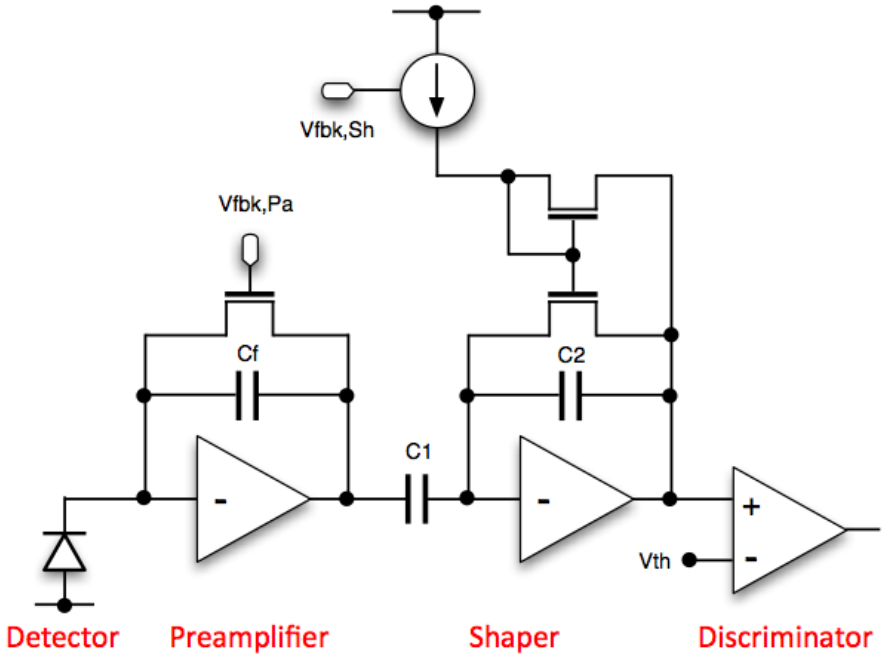
Vth < PA output DC level \ all the pixels are readout

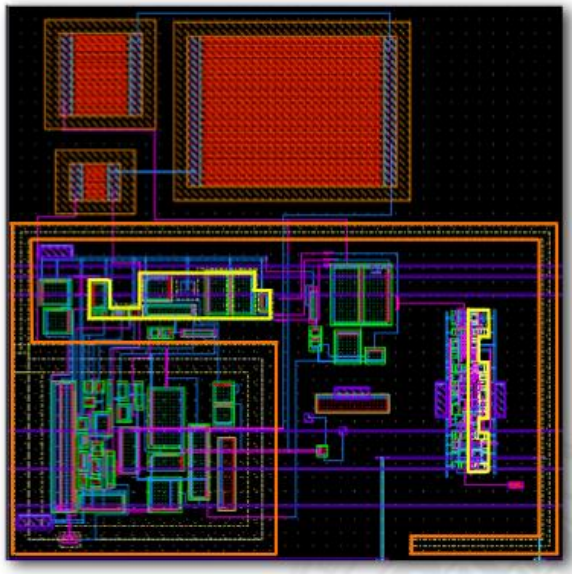




Deep n-well MAPS with 65nm CMOS IBM technology

APSEL65: a prototype DNW MAPS in 65nm



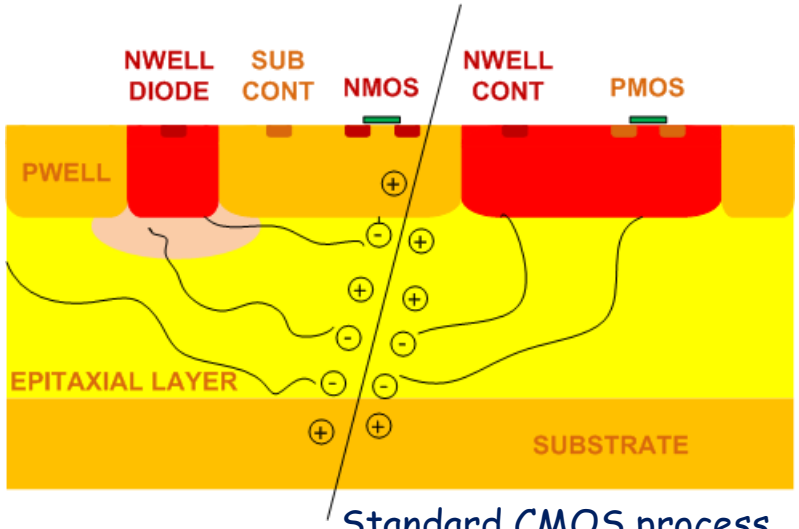


Main design features	
Chip Bias V_{DD}	1.2 V
PA input W/L	28/0.25
PA input I_D	14 μA
Power consumption	20 μW

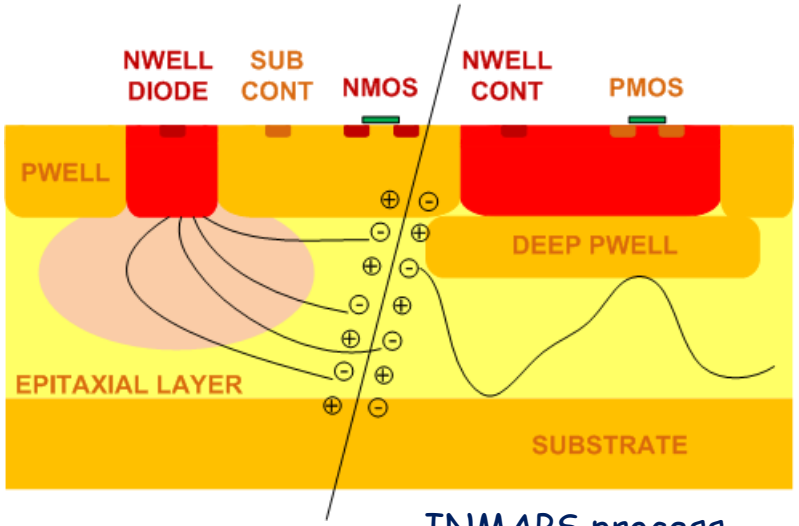
- Area: 40um x 40um
- DNW collecting electrode (orange)
  - Area: 360um^2
  - Capacitance: 340fF (estimated)
  - 99% efficiency @ 400 e- thr. (simulated)
- In this prototype the digital section is kept to the minimum (latch, OR gate, tri-state buffer)
- Sparsification and time-stamping logic at the pixel level in more advanced versions (room for this is available)

Deep p-well MAPS with 180nm CMOS TowerJazz technology

Deep p-well (180 nm CMOS INMAPS) process



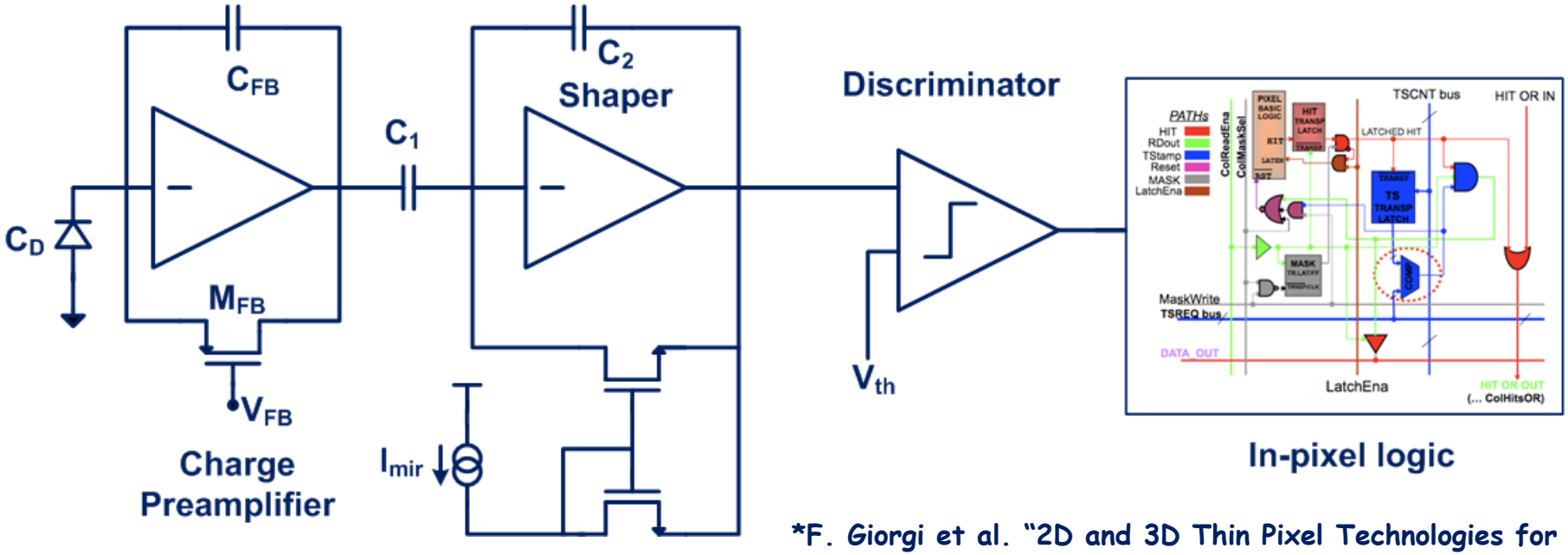
Standard CMOS process



INMAPS process

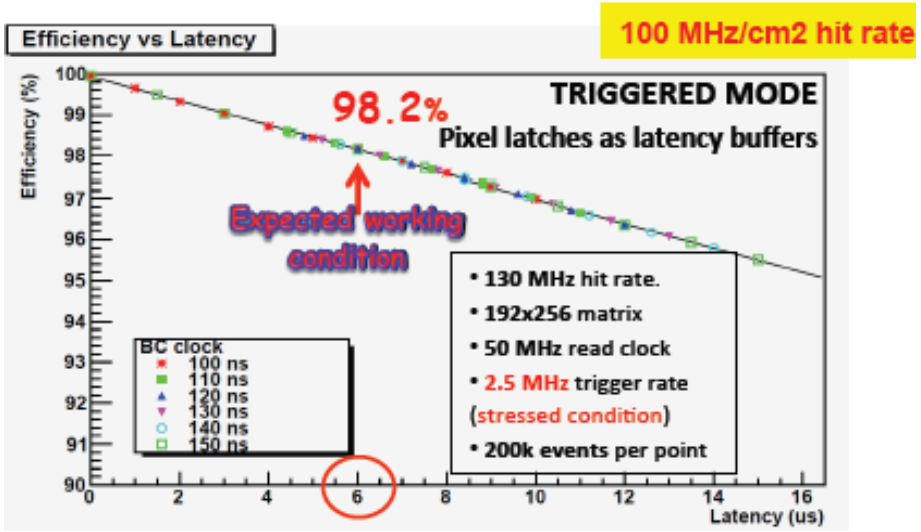
- Charge collection efficiency of MAPS structures developed in a standard CMOS process can be affected by the presence of competitive N-wells needed for in-pixel logic suited for a fast readout
- To overcome this issue a planar 180 nm CMOS process with quadruple well (INMAPS) has been considered
- An additional processing step deposits a deep P-well layer
- Advantages of a high resistivity epitaxial layer (featuring a resistivity higher than both the deep P-well and the substrate):
  - better charge collection properties (higher collected charge, charge collection speed)
  - higher bulk damage hardness expected
- The foundry provides different typologies of epitaxial layers. Three different versions of Apsel4well have been fabricated:
  - 5 μm standard resistivity (≈10 Ω·cm) epitaxial layer
  - 12 μm standard resistivity epitaxial layer
  - 12 μm high resistivity (≈1 kΩ·cm) epitaxial layer

Apsel4well front-end architecture



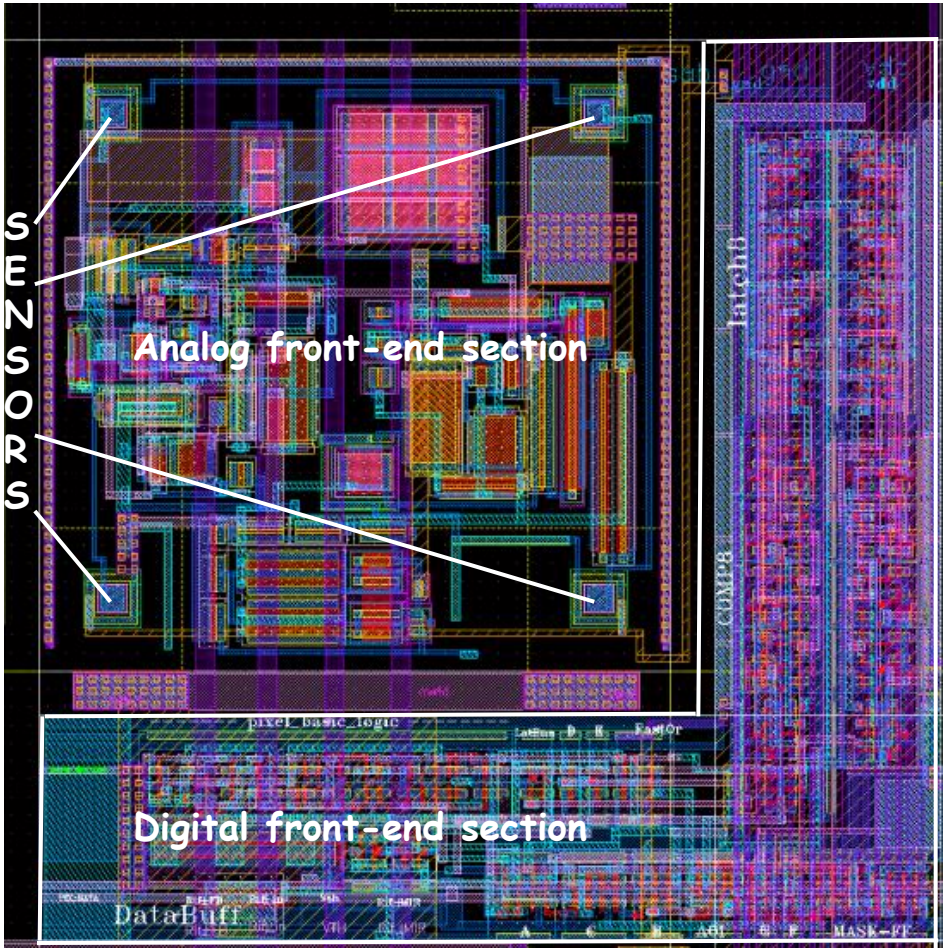
*F. Giorgi et al. "2D and 3D Thin Pixel Technologies for the Layer0 of the SuperB Silicon Vertex Tracker", NSS-MIC 2011

- 4 interconnected N-well diffusions as collecting electrode
- Charge PA, shaper and threshold discriminator
- In-pixel logic with time stamping capabilities, readout can be data-push or triggered
  - Readout efficiency >98% (triggered) and TS granularity down to 100 ns with 100 MHz/cm^2 target hit rate*

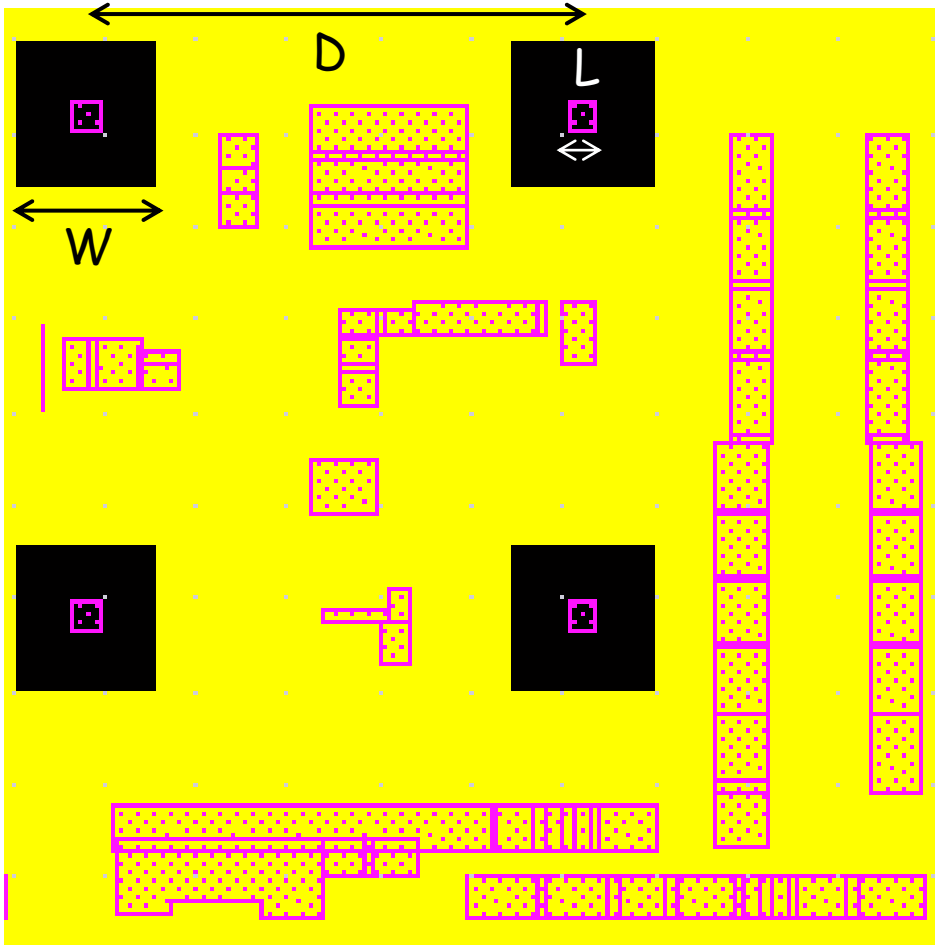


Apsel4well pixel layout

Pixel layout w/o DPW layer

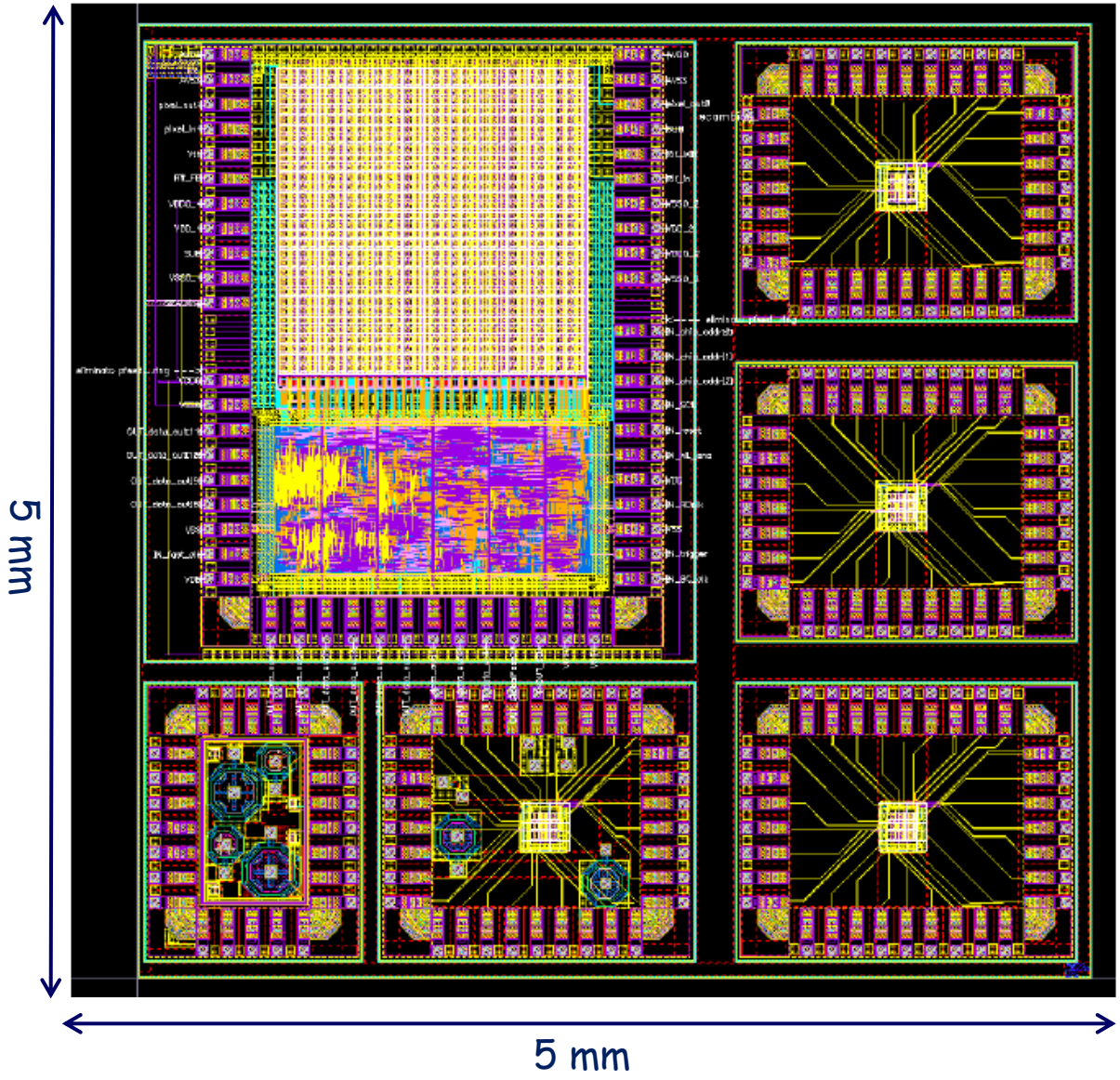


DPW (yellow) and NW (pink) layers



W=8 µm L=1.5 µm D=27 µm

Apsel4well chip layout

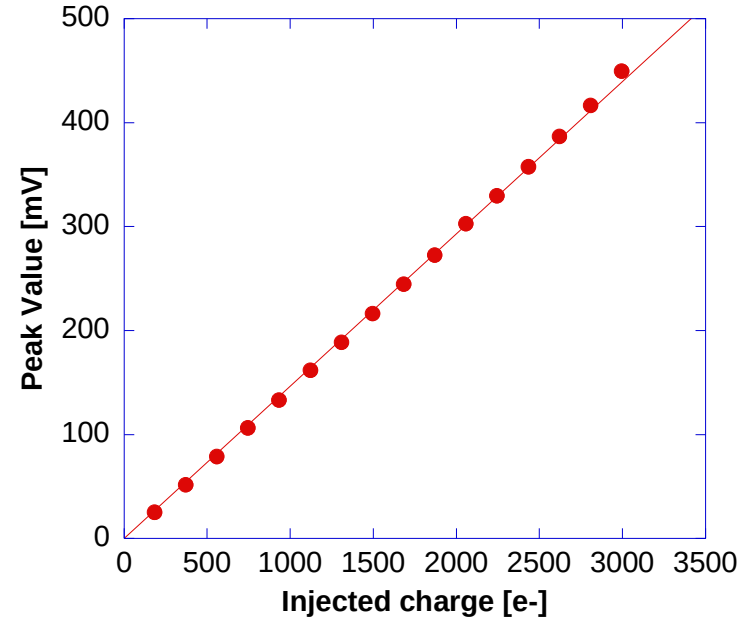


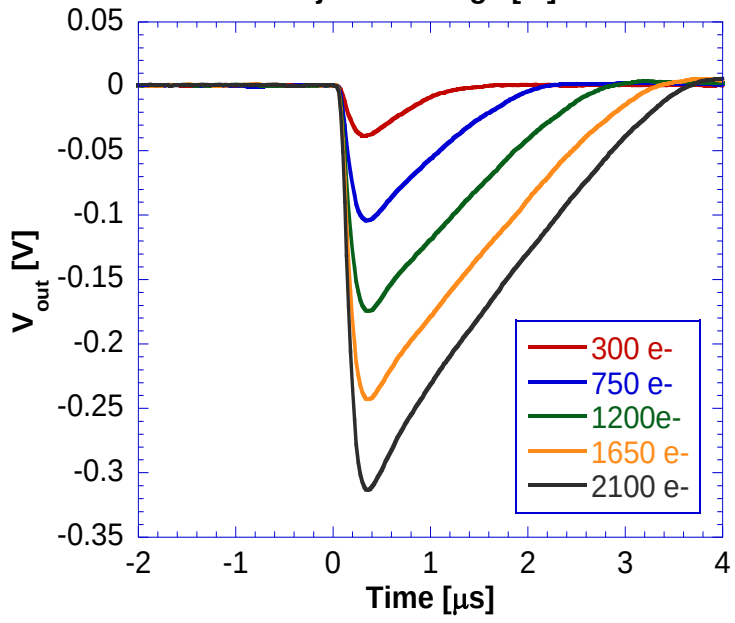
- Four 3x3 test analog matrices:
  - Enclosed layout PA input transistor, 4 collecting electrodes, DPW
  - Open layout PA input transistor, 4 collecting electrodes, DPW
  - EL PA input transistor, 2 collecting electrodes, DPW
  - EL PA input transistor, 4 collecting electrodes, no DPW
- Test structures:
  - Octagonal pn diodes
  - Accumulation capacitors
  - Single analog channels
- 32x32 matrix with peripheral readout logic

Apsel4well analog FE performance

Performance	3x3 matrix
Charge sensitivity	900-1100 mV/fC
t_p @ 800 injected electrons	290 ns
ENC (C_D = 30 fF)	38 e-
INL (@ 2000e-)	2%
Current consumption*	10 µA/pixel
Analog Power consumption*	18 µW/pixel 0.7 W/cm^2
Pixel pitch	50 µm

* Data from simulations



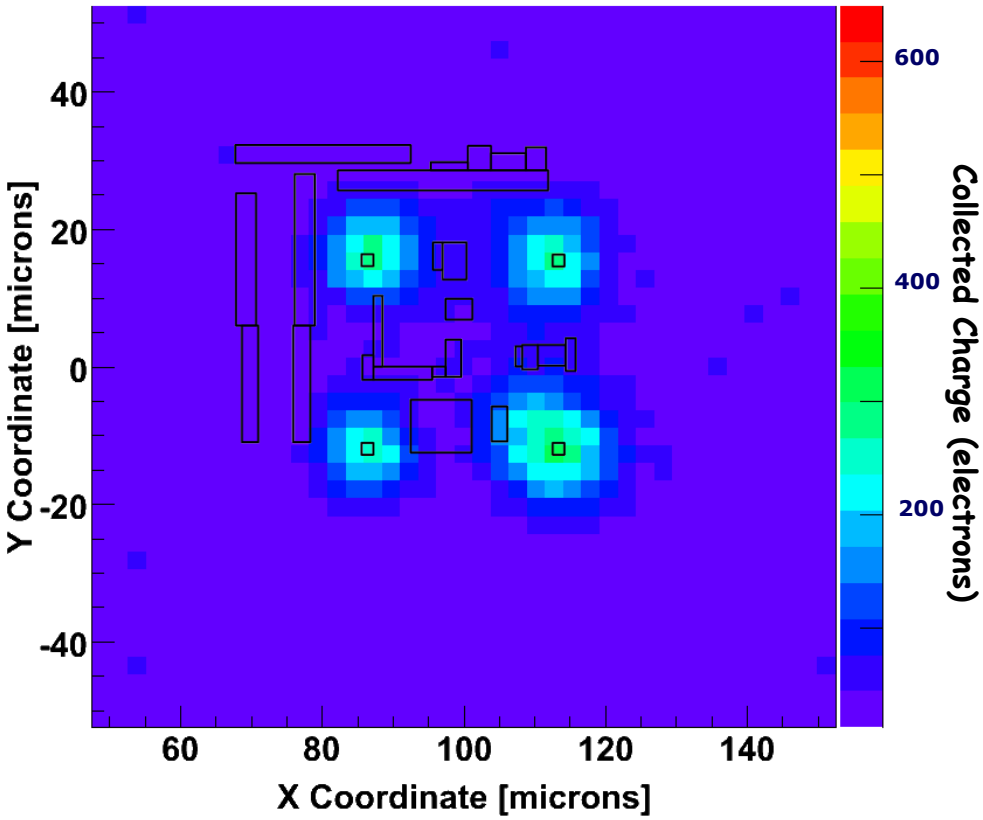


- Data in fair agreement with simulation results

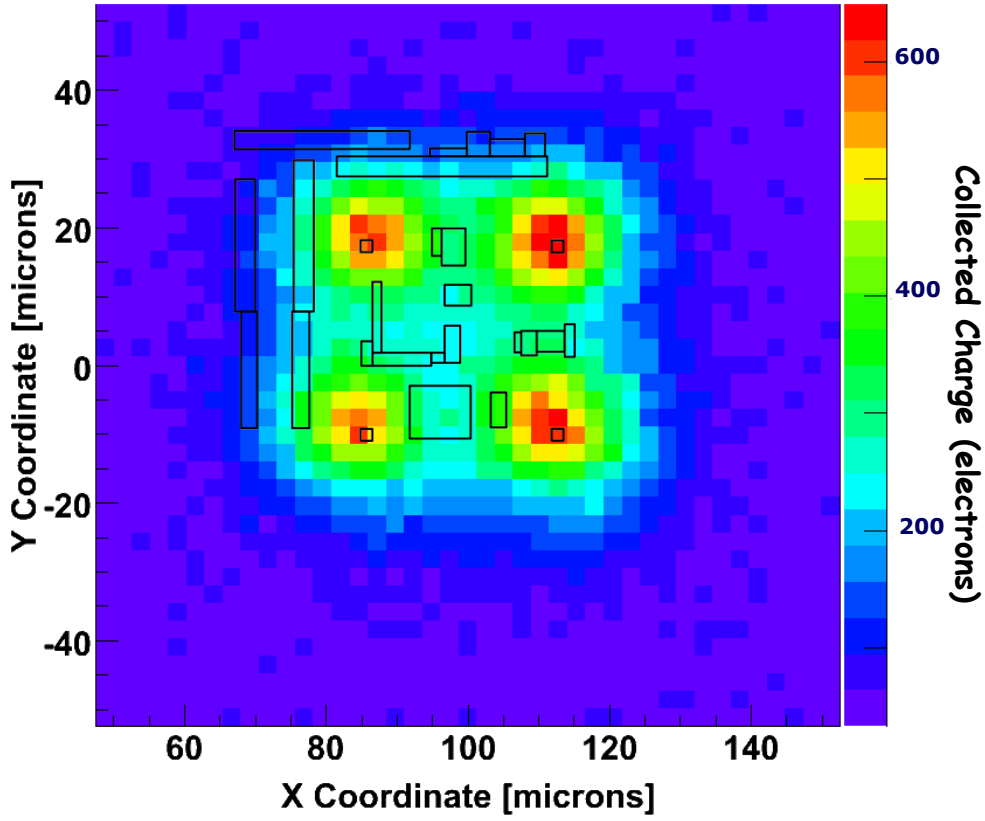
Advantages of deep P-well

- Comparison of charge collection properties performed by means of IR laser
- N-wells from layout have been superimposed to the charge collection plot

No Deep P-well, 5 µm std. res. epi layer



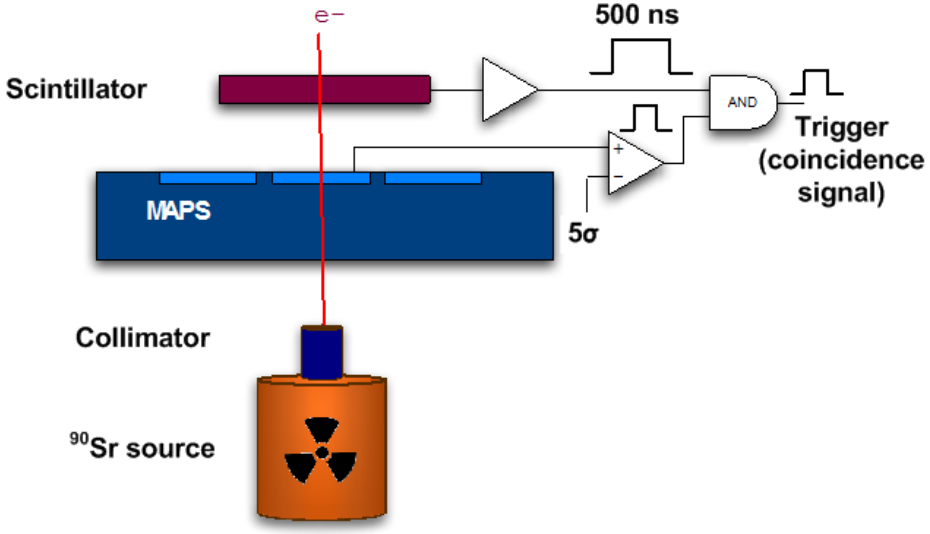
With deep P-well, 5 µm std. res. epi layer

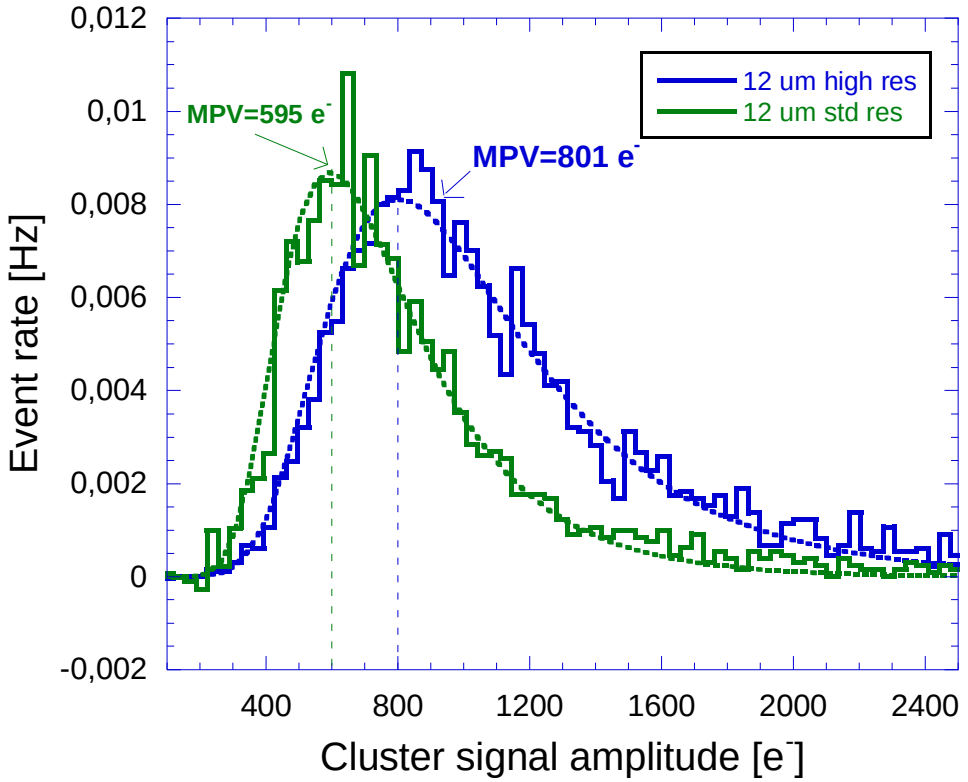


- In the pixel without DPW the charge is collected only around the electrodes.

Advantages of a high resistivity epitaxial layer

- Charge collection measurements performed by means of a ^{90}Sr radioactive source
- A waveform is acquired when the pixel analog output exceeds a given threshold (5σ) within a 500 ns gate signal from the scintillator



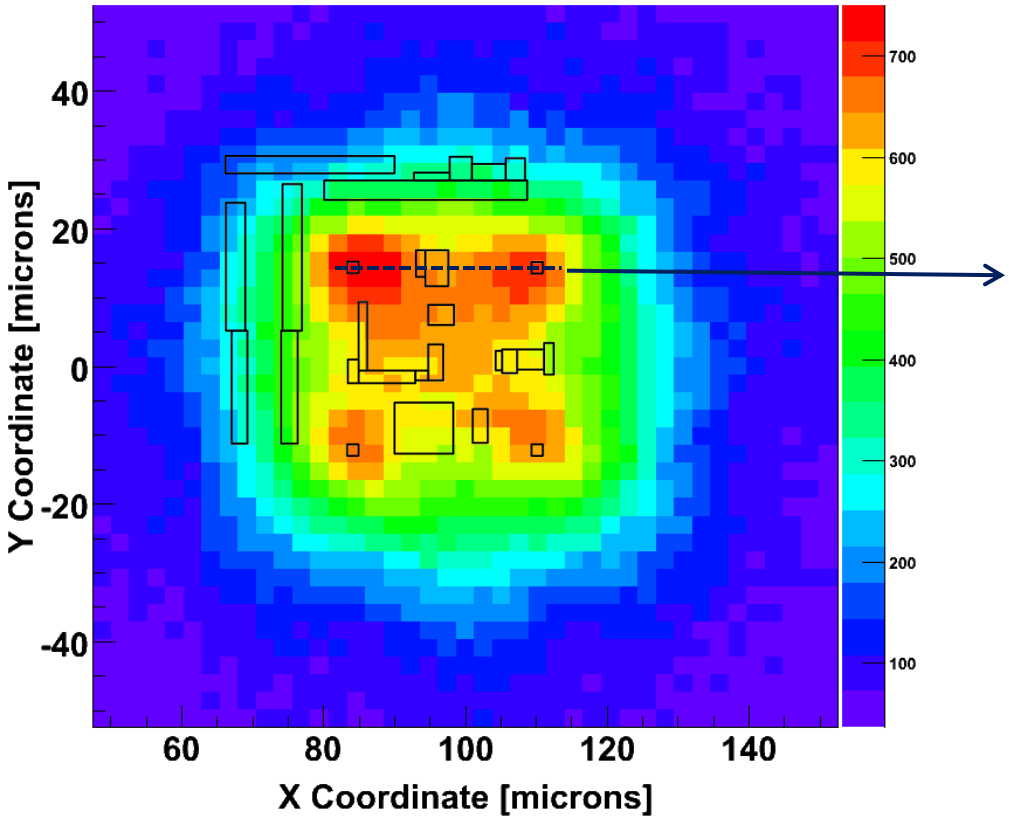


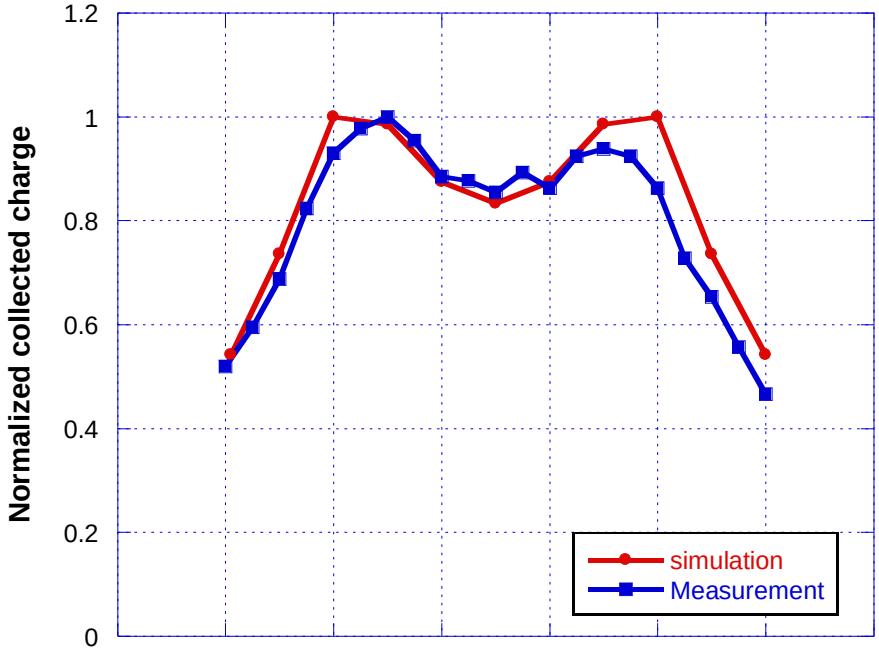
- The charge collected by adopting a high resistivity epitaxial layer (MPV≈800 e^-) is about 35% higher than in the case of the standard resistivity option (MPV≈600 e^-)

High resistivity epitaxial layer

- Pixel with 12 µm thick high resistivity epitaxial layer: higher charge collected and better uniformity

With deep P-well, 12 µm std. res. epi layer





- Good matching between TCAD simulations and measurement results

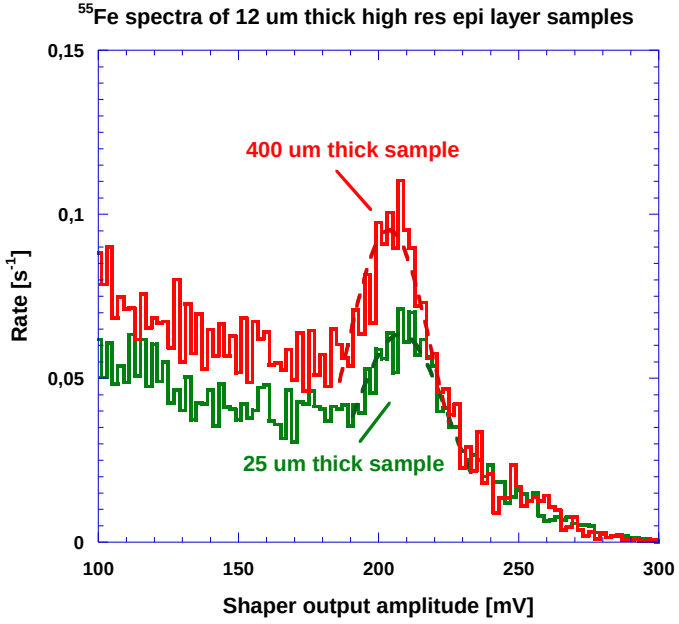
Charge collection performance of thinned Apsel4well

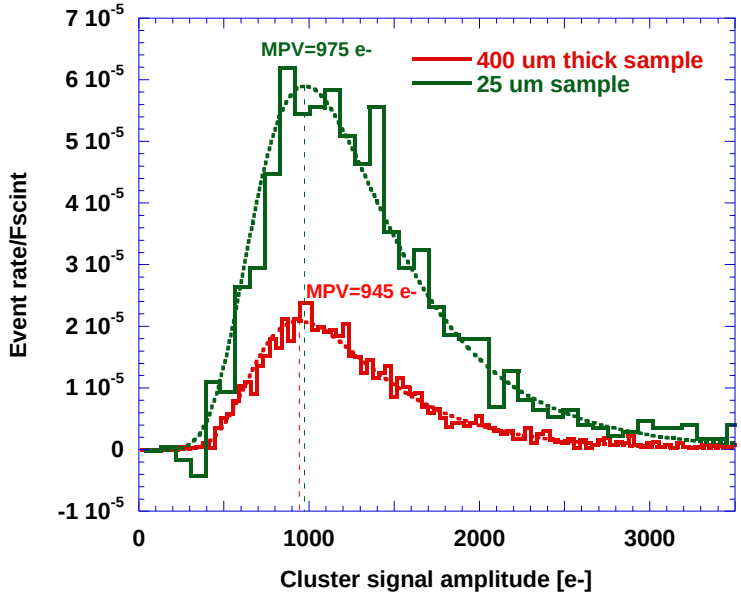
- Analog readout performance of thinned Apsel4well samples are similar to non-thinned chip ones -> all the discrepancies are in the range of statistical variations already observed in the measurements results relevant to non-thinned chips
- Measurements performed with ^{90}Sr do not exhibit any significant variation in terms of the amount of charge collected by the 3x3 cluster
- Charge collection measurements performed by means of IR laser and ^{90}Sr on Apsel4well samples 25µm and 400µm thick, both of them featuring the high resistivity epitaxial layer option

Comparison of the analog front-end performance

Performance	25 um thick	400 um thick
Charge sensitivity (C_{inj})	1120 mV/fC	1100 mV/fC
Charge sensitivity (^{55}Fe)	775-850 mV/fC	850-950 mV/fC
ENC (C_T = 42 fF)	43e-	38 e-
Analog Power consumption	18 µW/pixel	18 µW/pixel

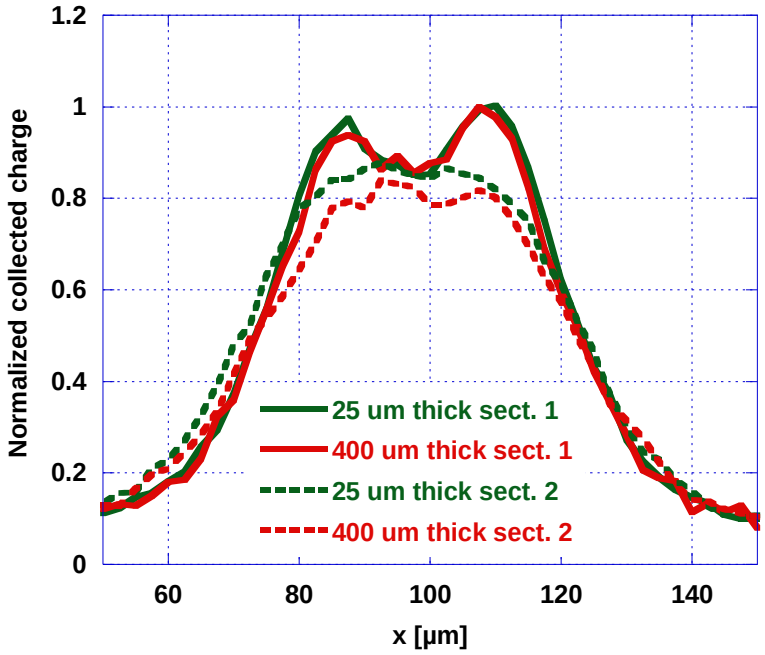
S. Zucca et al., "Effects of Substrate Thinning on the Properties of Quadruple Well CMOS MAPS", IEEE Trans. On Nucl. Sci., Vol. 61, (2) pp. 1039-1046.



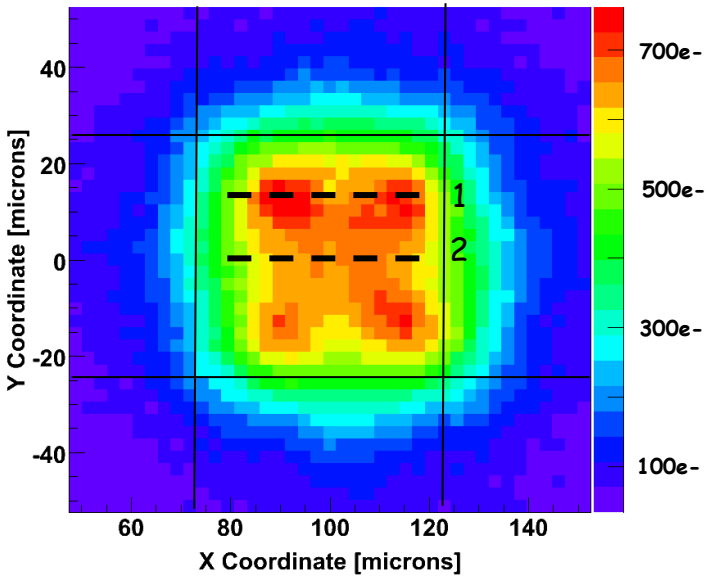


Charge collection performance of thinned Apsel4well

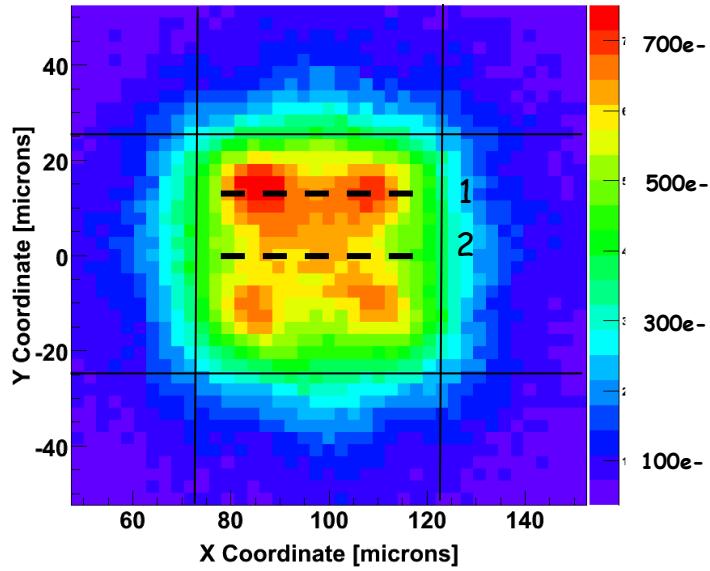
- Results from IR laser measurements show no significant changes in terms of charge collection uniformity



25 μm thick sample (chip 96)



400 μm thick sample (chip 41)



Conclusions

- Several **deep n-well MAPS** chip have been fabricated and tested with the **130nm CMOS ST technology**
  - **APSEL4D** (4096 pixels, 50um pitch) featuring in-pixel sparsification and time-stamp information has been characterized in laboratory and tested with beams
  - **SDR0**, a monolithic active pixel sensor for vertexing applications at the ILC has been fabricated and tested. Several issues (pitch, digital functionality, detection efficiency) had to be addressed in order to meet the ILC requirement -> SDR1 in 3D Tezzaron-GlobalFoundries process
- A test chip including **deep n-well MAPS** has been fabricated and tested in the **65nm CMOS IBM process**
- MAPS devices developed in the 180nm CMOS **INMAPS process (deep p-well)** can significantly improve the charge collection efficiency of DNW MAPS by preventing the parasitic collection action of n-well diffusions
- The high resistivity epitaxial layer option improves both the charge collection properties of the sensor and its bulk damage tolerance
- **APSEL4WELL** sensor was fully characterized by means of charge injection, infrared laser scan and radiation sources
  - Sensors fabricated in a 12um thick HR epi layer have been proven to be by far the best solution among the different available options in terms both of the amount of collected charge and of charge collection uniformity
- APSEL4WELL MAPS thinned down to about 25um have been tested and no significant changes in the performance of the thinned sensors have been detected with respect to non-thinned chips

Acknowledgments

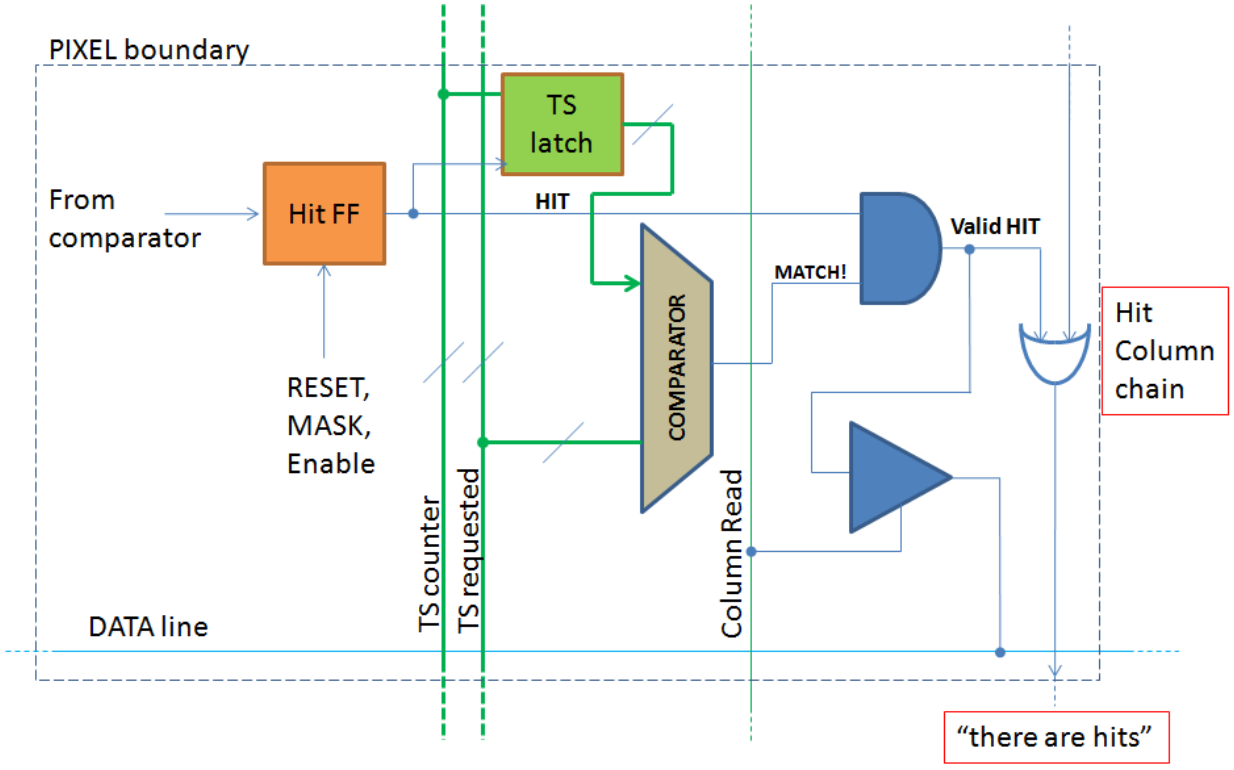
- L. Gaioni, M. Manghisoni, V. Re
  Università di Bergamo and INFN Pavia
- G. Bruni, M. Bruschi, R. Di Sipio, B. Giacobbe, F.M. Giorgi, A. Gabrielli, C. Sbarra, N. Semprini, M. Villa, A. Zoccoli
  Università di Bologna and INFN Bologna
- M. Caccia, A. Bulgheroni, F. Risigo, M. Jastrzab
  Università dell'Insubria e INFN Milano
- L. Ratti, A. Manazza, V. Speziali, S. Zucca, E. Pozzati, C. Andreoli
  Università di Pavia and INFN Pavia
- G. Batignani, S. Bettarini, G. Casarosa, M. Dell'Orso, F. Forti, P. Giannetti, M.A. Giorgi, F. Morsani, N. Neri, E. Paoloni, M. Piendibene, G. Rizzo
  Università di Pisa and INFN Pisa
- L. Bissi, P. Ciampolini, A. Marras, G. Matrella, P. Placidi, E. Pilicer, D. Passeri, L. Servoli, P. Tucceri
  Università di Perugia and INFN Perugia
- E. Bernieri, G. Conte, M.C. Rossi, G. Assanto, L. Colace, E. Spiriti
  INFN Roma III
- G.F. Dalla Betta, A. Repchankova, V. Tyzhnevyi, G. Verzellesi
  Università di Trento and TIFPA INFN
- L. Bosisio, L. Lanceri, L. Vitale, I. Rashevskaya
  Università di Trieste and INFN Trieste
- R. Yarema, F. Fahim, G. Deptuch, T. Zimmerman, A. Shenai, J. Hoff, M. Trimpl
  Fermi National Accelator Laboratory
- R. Turchetta, J. Crooks, R. Coath
  Rutherford Appleton Laboratory

Backup slides

In-pixel logic

- Complex in-pixel logic can be implemented without reducing the pixel collection efficiency. Readout can be data push or triggered (only selected time stamp are read out)

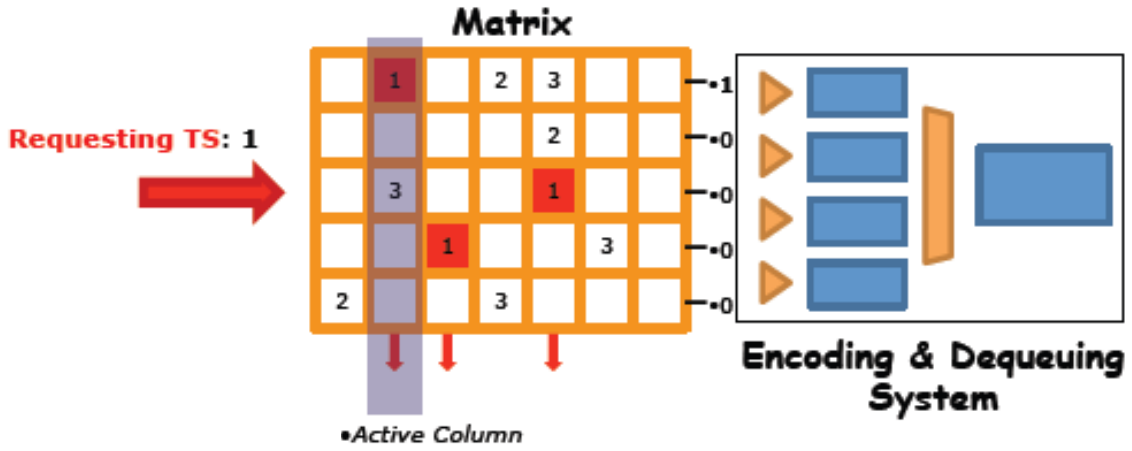
- Timestamp (TS) is broadcast to pixels and each pixel latches the current TS when fires
- Matrix readout is TS ordered
  - A readout TS enters the pixel and a HIT-OR-OUT is generated for columns with hits associated to that TS
  - A column is read only if HIT-OR-OUT=1
  - DATA_OUT is generated for pixels in the active columns with hits associated to that TS.



In-pixel logic

- In-pixel Hit & Time Stamp Latch
- **TS request** to the matrix
- Pixel **FastOR** activates if:

  Latched TS==TS request
- 1 Column sparsified in 1 clk cycle (whatever the occupancy)
- Only active-**FastOR** columns are enabled in sequence (i.e. active column FastORs → 10 clk cycles readout)



- Module area: 8 cm^2
- Hit rate: 100 MHz/cm^2
- Hit encoding: 30 bit/hit
- TS: 1 μs
- Trigger frequency: 150 kHz → rate/module: 3.5 Gb/s

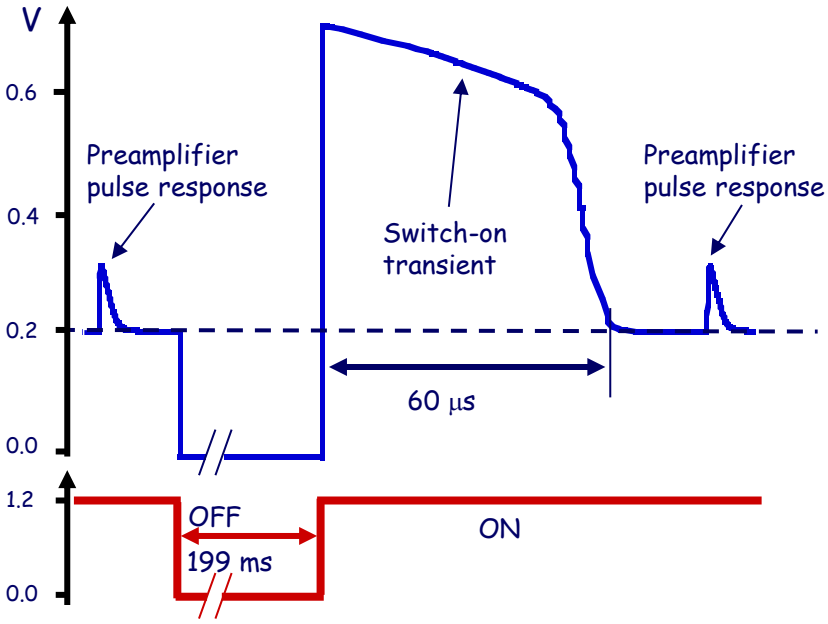
Power cycling simulations

Power cycling can be used to reduce average dissipated power by switching the chip off when no events are expected

Example:

- ✓ ILC bunch structure

The analog section in the elementary cell can be switched off during the intertrain interval in order to save power (analog power is supposed to be predominant over digital)



Based on circuit simulations, power cycling with at least 1% duty-cycle seems feasible