# CMOS MAPS in Planar and 3D Technologies: TID Effects and Bulk Damage Study

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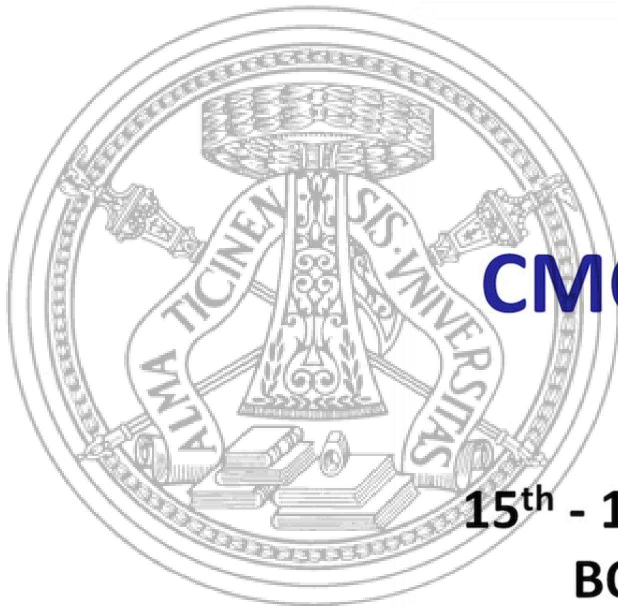


**CPIX14**

Workshop on

**CMOS Active Pixel Sensors**

for Particle Tracking

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# Motivation

- Experiments at the future particle colliders (B-Factories, ILC) or upgrade of present colliders (HL-LHC) will set severe requirements for silicon vertex trackers
- CMOS monolithic sensors have some attractive features to offer
  - full integration (in a CMOS technology) of the front-end electronics and the sensitive part in the same substrate
  - the sensitive region is limited to a few tens of microns ➔ substrate can be thinned down with negligible signal loss and improved impact parameter resolution
- Design/layout (DNW monolithic sensors) and/or technological (SOI, HV CMOS, quadruple well) solutions may help overcome some limitations in the use of PMOS devices and design circuits with the required complexity for data sparsification an time stamping
- One weak point of MAPS devices is their moderate radiation hardness
  - ionizing radiation may degrade the analog performance (noise, gain) in the front-end channel and increase the sensor leakage
  - bulk damage may deteriorate the charge collection properties and again increase the leakage in the sensor
- Radiation tolerance study is of paramount importance both to qualify the devices for the foreseen applications and to improve the design

# Content

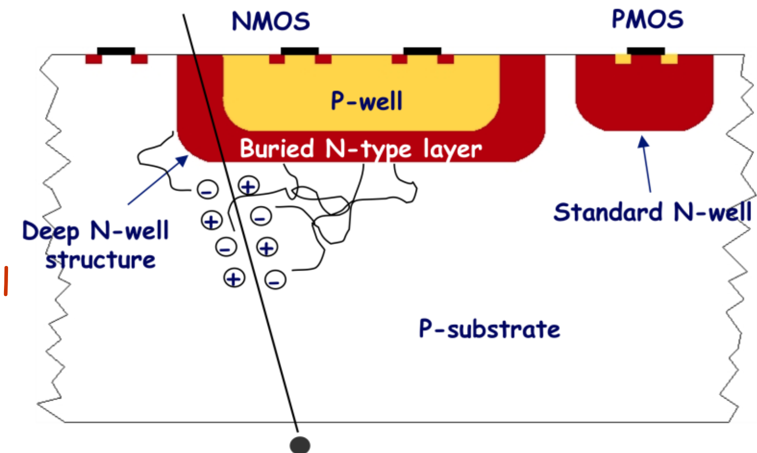
- DUTs and irradiation sources and procedures
  - DNW MAPS in planar and 3D, 130 nm CMOS technology
  - MAPS in a quadruple well, 180 nm CMOS technology
  - $^{60}$Co $\gamma$-rays up to 10 Mrad($SiO_2$), 1 MeV eq. neutrons from a nuclear reactor up to $10^{14}$ cm$^{-2}$, annealing (100° C/168 h)

See the talks by V. Re and G. Traversi on Monday

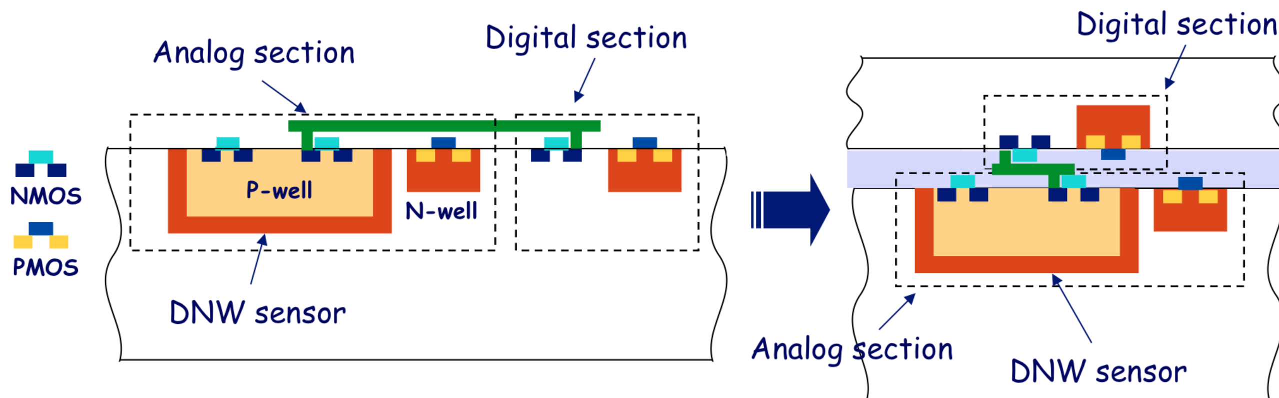
- Total ionizing dose tests
  - Effects on the front-end electronics (noise, gain), dependence on design and technology
  - Effects on the collecting electrode (leakage current)
- Bulk damage tests
  - Effects on the collecting electrode (charge collection, leakage current), dependence on resistivity
  - Indirect effect on front-end electronics (gain)
- Lessons learned and conclusion

# Planar and 3D DNW MAPS

- Deep N-well monolithic pixels
  - A large DNW is used to collect the charge released in the substrate
  - A classical readout channel for capacitive detectors is used for Q-V conversion → gain decoupled from electrode capacitance
  - NMOS devices of the analog section are built in the deep N-well
  - Full CMOS for high performance analog and digital blocks → charge collection inefficiency depending on the relative weight of NW with respect to DNW




- From planar to 3D
  - sensor and analog front-end can be integrated in a different layer from the digital blocks
  - less PMOS in the sensor layer → improved collection efficiency
  - more room for both analog and digital power and signal routing

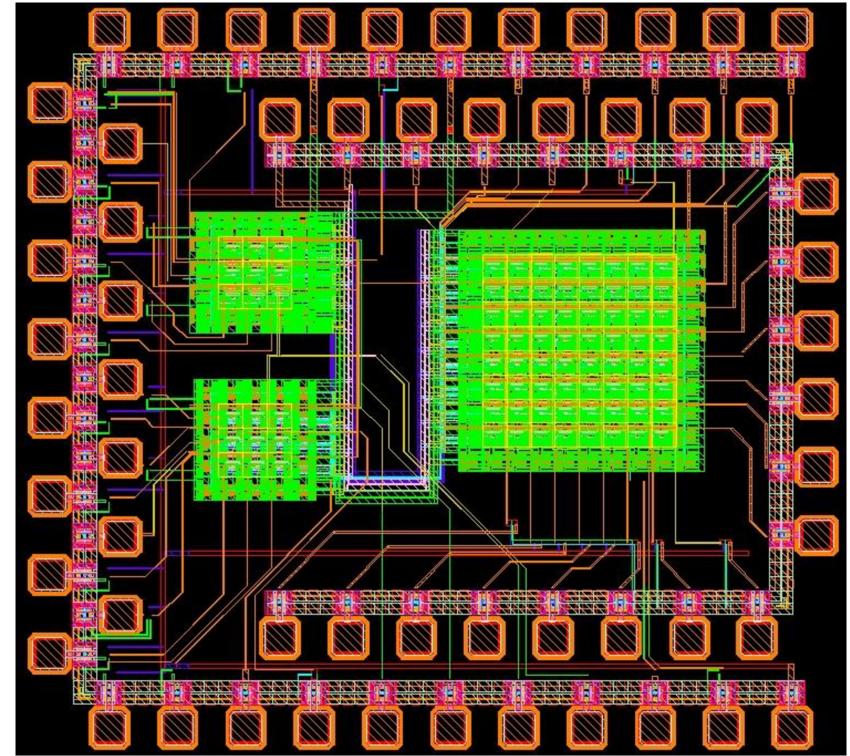



- Tier 1: collecting electrode and NMOS parts of the analog front-end (and a few PMOS)
- Tier 2: discriminator PMOS parts, digital front-end and peripheral digital readout electronics

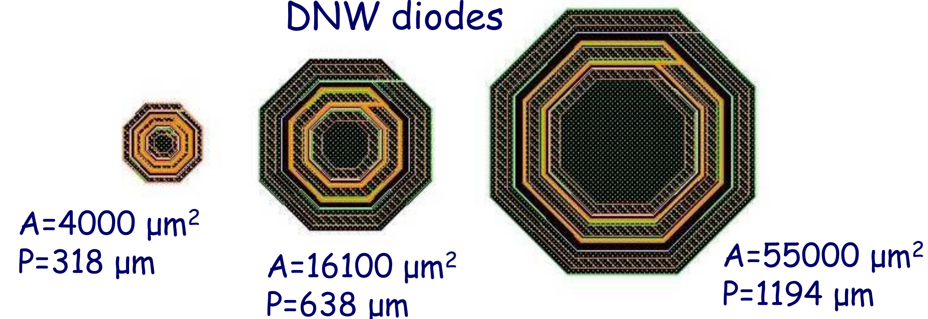
# Planar DNW MAPS

- 130 nm CMOS DNW-MAPS
  - Matrices with different size (3x3, 8x8) and layout of the collecting electrode
  - Up to 9.7 Mrad($SiO_2$), 9 rad/s dose rate, 100°C/168 h annealing cycle, DUTs biased as in the real application
  - Charge sensitivity, ENC, $^{55}$Fe and infrared laser characterization
- Single 130 nm NMOS devices
  - Narrow channel transistors
  - Up to 9 Mrad($SiO_2$), gate at 1.2 V, all other terminals grounded
  - Static characterization
- DNW diodes
  - Three devices with different size
  - Up to 3.3 Mrad($SiO_2$)
  - Leakage current

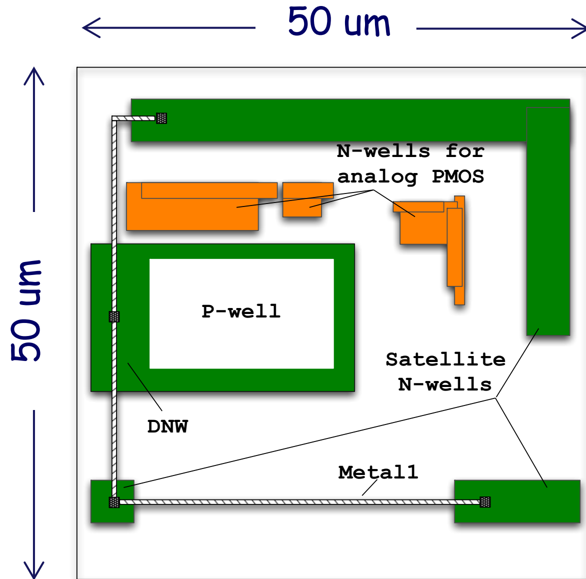
Apsel3T1 test chip



DNW diodes



# Front-end channel




Elementary cell (M1 type)

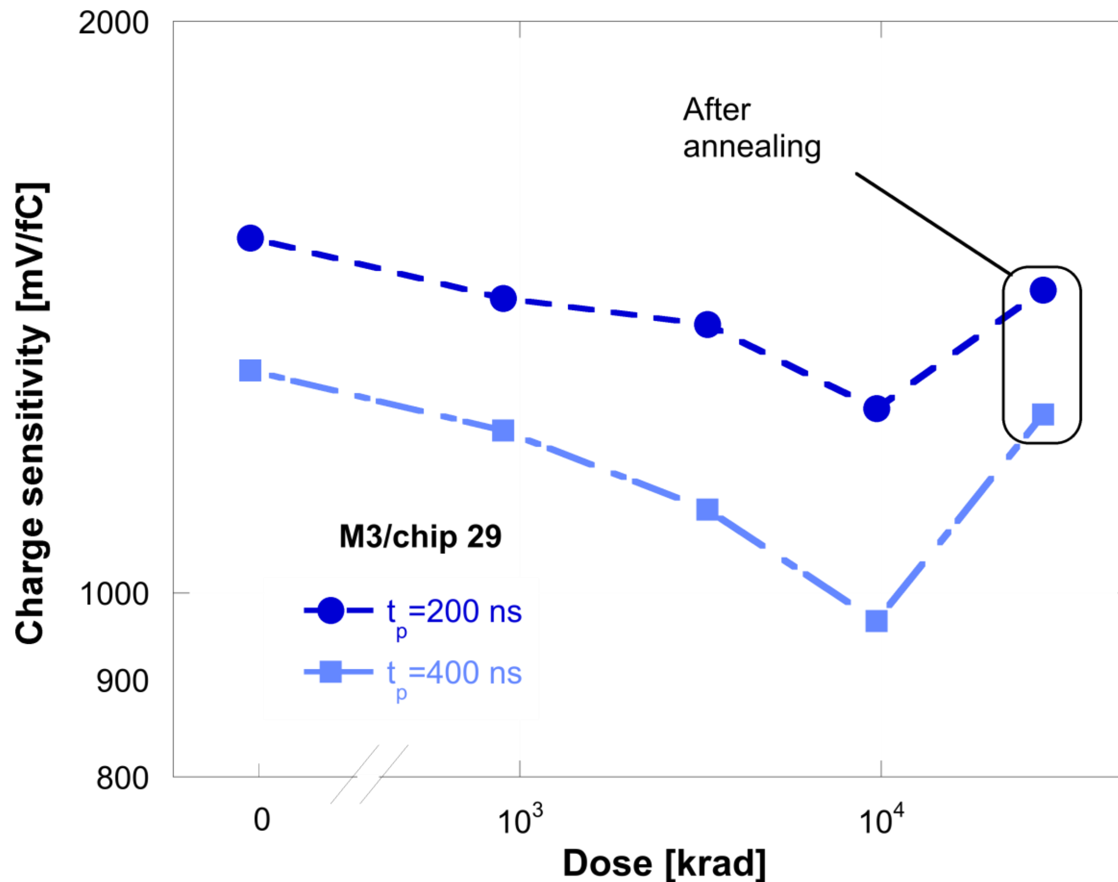
Thoroughly described in IEEE TNS., vol. 56, no. 4, pp. 2360-2373, Aug. 2009.

$V_F$ $M_F$ $e_n$ $C_F$ $C_1$ $G_m$ $A(s)$ $C_2$ $V_t$ $Q\delta$ + $I_{leak}$ p n+ p

- Sensor and front-end (analog and digital, not shown) electronics integrated in a 50 µm pitch pixel
- Selectable peaking time (200 and 400 ns), 30 µW/channel power dissipation, $C_D$≈300 fF, W/L=14 um/0.25 um for the preampli input device

# Charge sensitivity

Planar DNW MAPS

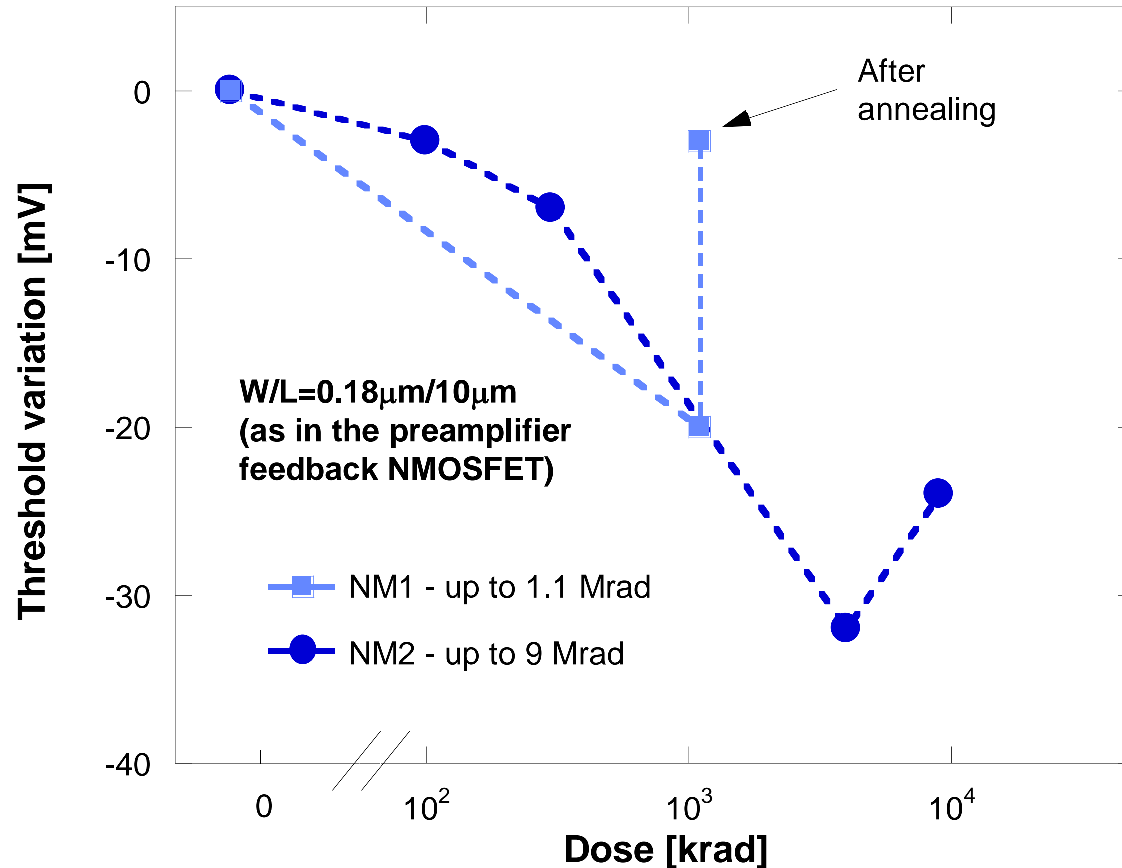



Radiation damage mechanisms discussed in IEEE TNS., vol. 56, no. 4, pp. 2124-2131, Aug. 2009.

- About 20-25% decrease after the last irradiation step (9700 krad)
- Sizeable recovery after annealing
- Change in charge sensitivity results from:
  1. Threshold shift in the preampli feedback MOSFET (RINC effect)
  2. Increase in leakage current in the detector (partially compensating the first effect)
  3. Change in the feedback transconductance and gain-bandwidth product in the shaper

# RINC effect



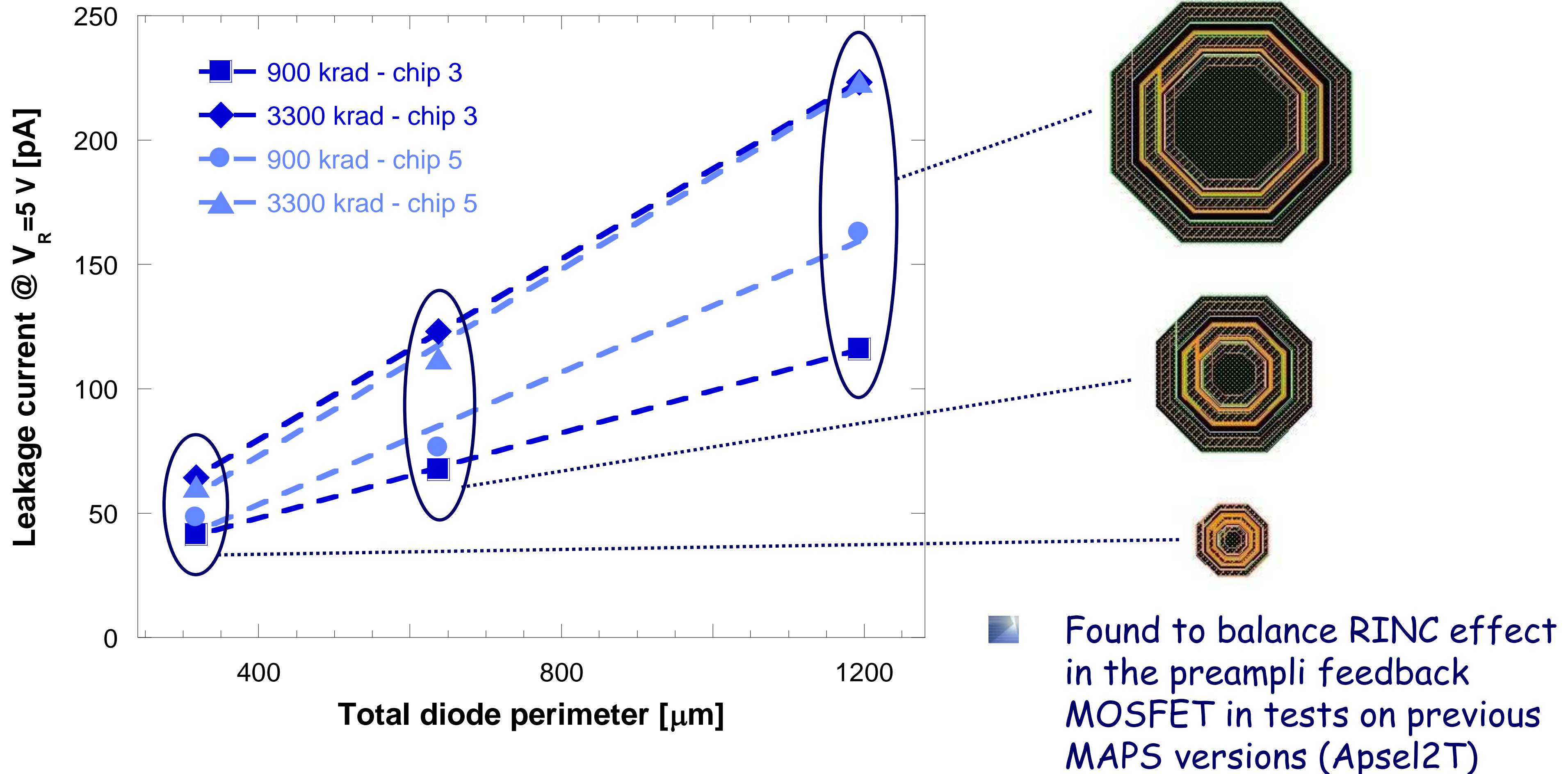



RINC effect discussed for the first time by F. Faccio and G. Cervelli in IEEE TNS., vol. 52, no. 6, pp. 2413-2420, Dec. 2005.

- Radiation Induced Narrow Channel (RINC) effect ➔ significant change in threshold voltage and drain leakage current in N- and PMOSFETs with narrow (<1 um) channel
- Due to charge trapped in the shallow trench isolation (STI) affecting electric fields in the main channel
- Responsible for threshold shift in the preampli feedback MOSFET (W/L=0.18 um/10 um)
- Shift of tens of mV in irradiated narrow channel devices (to be compared with a few mV in wide channel MOSFETs)

# Sensor leakage



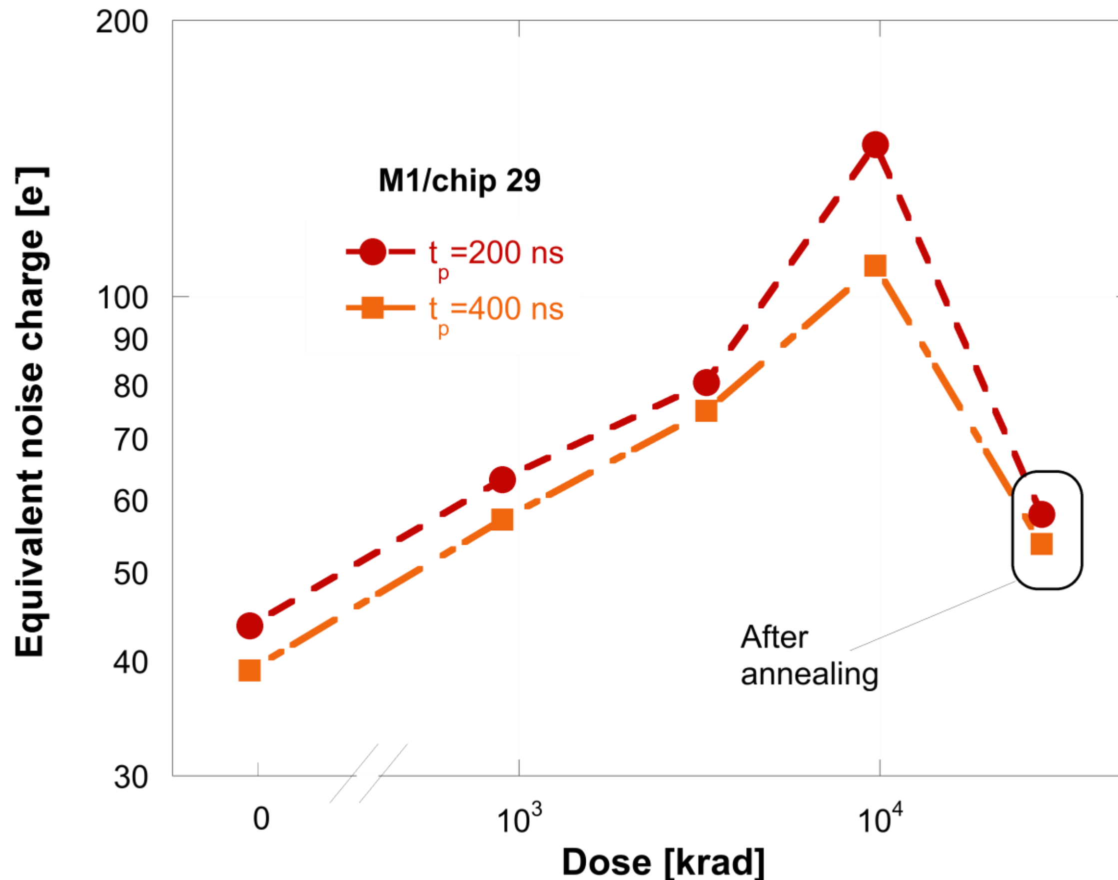



- Found to balance RINC effect in the preampli feedback MOSFET in tests on previous MAPS versions (Apsel2T)

- Leakage current proportional to the diode perimeter → compatible with charge buildup in the field oxide and/or creation of traps at $SiO_2$/Si interface, accounting for surface generation current increase

# Equivalent noise charge






$$ENC^2 = C_T^2 A_1 S_w^2 \frac{1}{t_p} + C_T^2 A_2 A_f t_p^{\alpha_f - 1}$$

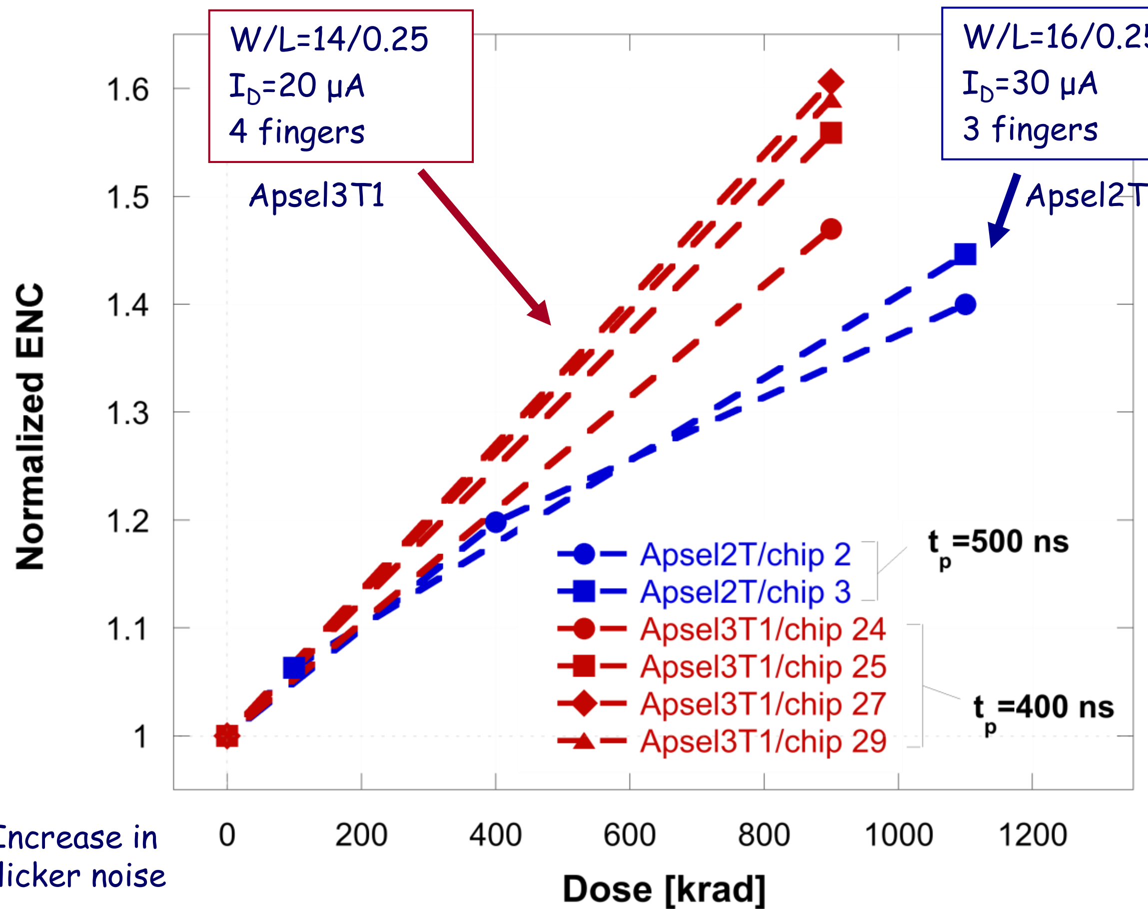
channel thermal noise — flicker noise

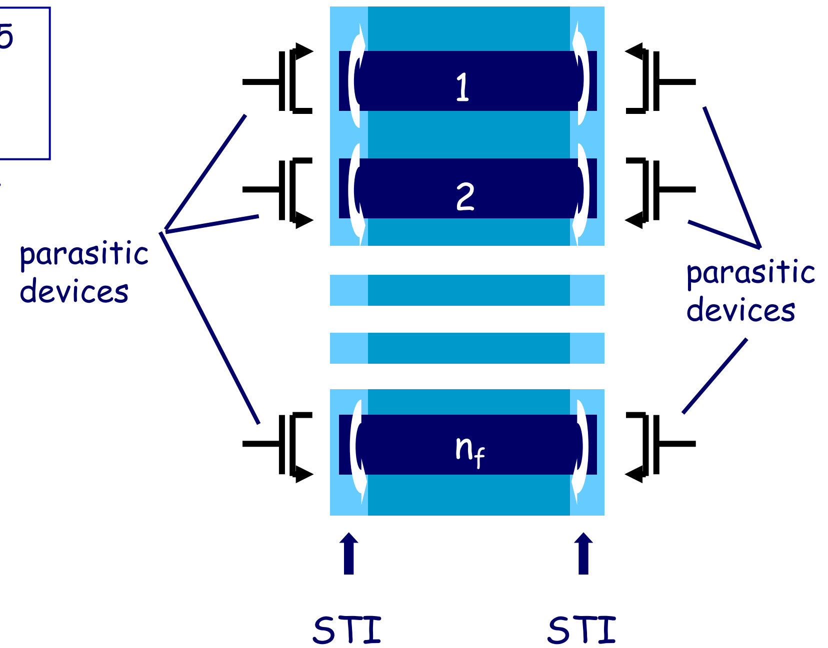
- Main contributions from the preampli input device (channel thermal and flicker noise)
- Other, low frequency (parallel) noise terms negligible at the considered peaking times
- Increase in excess of 100% in equivalent noise charge (ENC) after the last irradiation step
- Sizeable recovery after the annealing cycle
- Main contribution to noise degradation likely to come from flicker noise increase

Radiation induced increase in flicker noise is discussed in IEEE TNS., vol. 54, no. 6, pp. 1992-2000, Dec. 2007.

# Equivalent noise charge: hole build-up in the STI






Increase in flicker noise

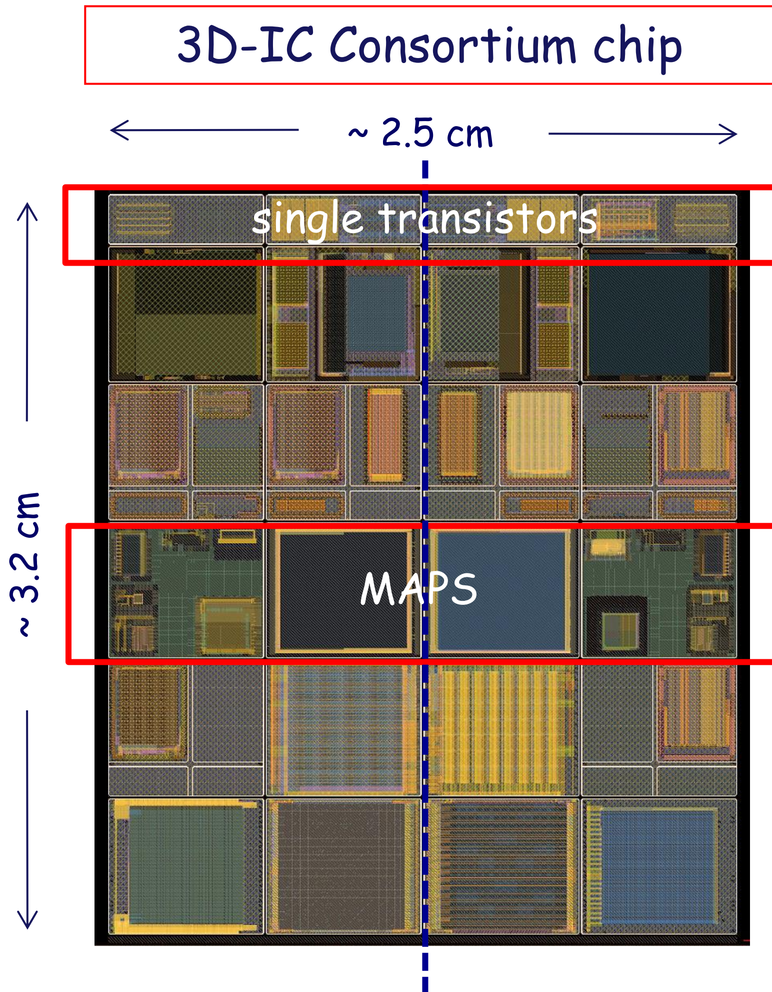
$$\frac{A_{f,post}}{A_{f,pre}} \approx \frac{K_{f,m,post}}{K_{f,m,pre}}\left(1+2n_f\frac{K_{f,lat}}{K_{f,m,post}}\frac{nI_z^*}{L}\frac{1}{I_{D,m,post}/W}\frac{I_{D,lat,s}}{I_{D,m,post}}\right)$$

Finger number

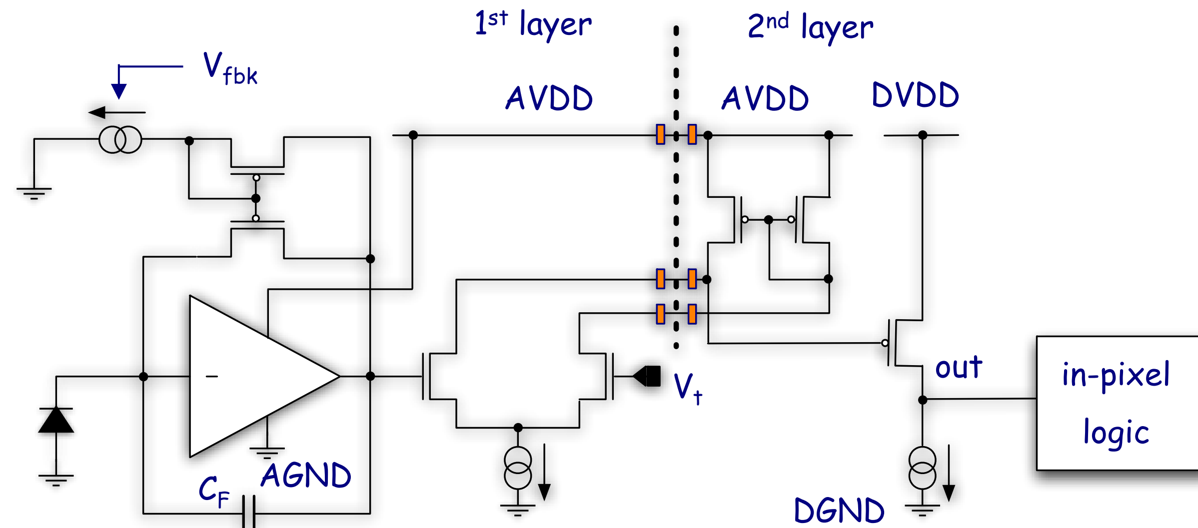
Current density

- Parasitic devices turned on by positive charge trapped in the STI
- Each parasitic device (two per finger) provides its contribution to the overall noise
- Flicker noise degradation is worse in devices with larger number of fingers and smaller drain current density

# Vertically integrated DNW MAPS



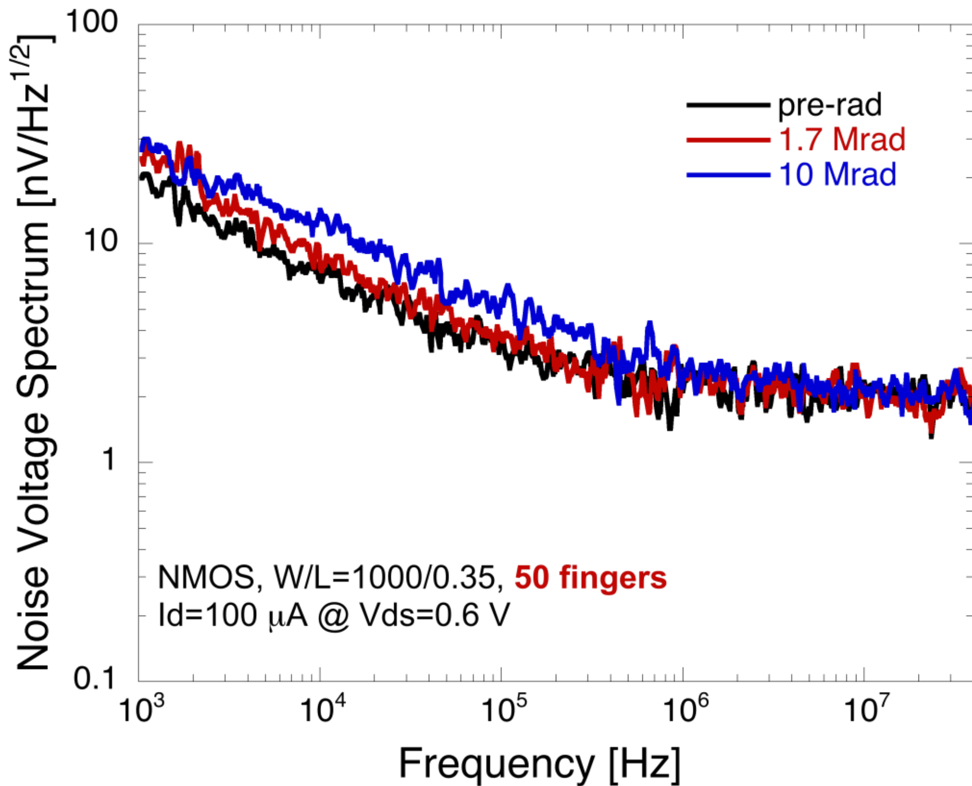

- A couple of different solutions (sharing the same analog front-end architecture) for different experimental environments
  - Apsel5T-TC, B-factory experiments – 40 um pitch, triggerless digital readout
  - SDR1, ILC experiments – 20 um pitch, token passing readout scheme
- Single transistors irradiated up to 10 Mrad($SiO_2$), MAPS up to ~800 krad($SiO_2$) with $^{60}Co$

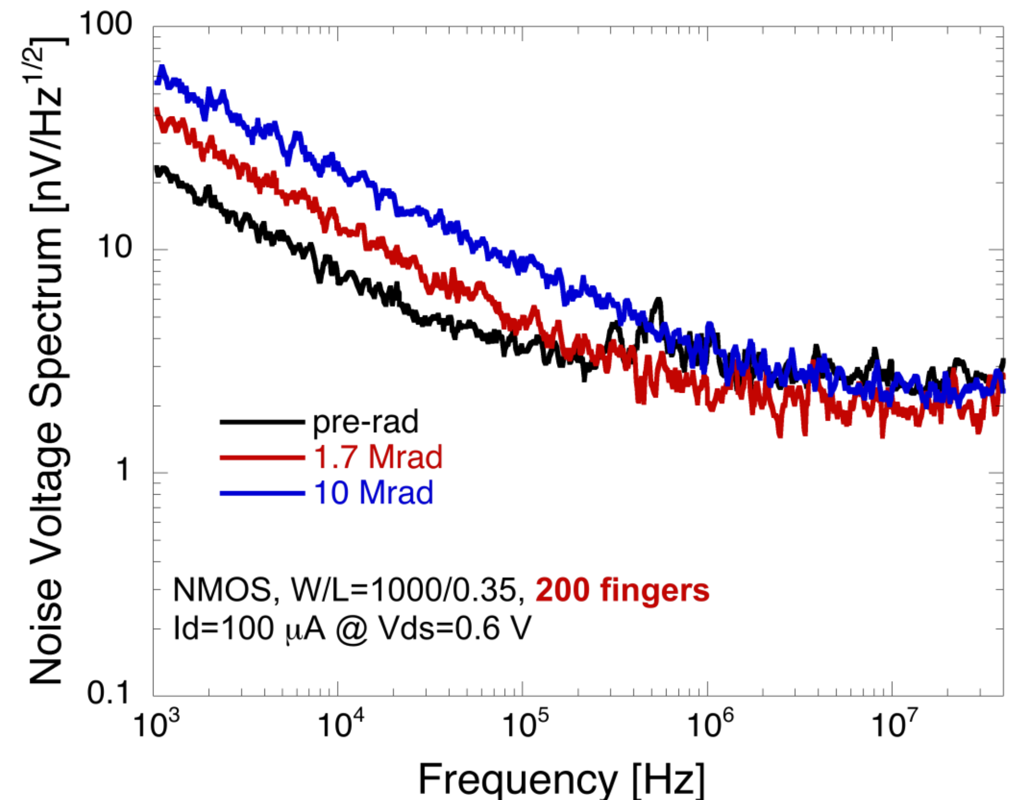


# Single transistors in 3D technology



- Single devices biased in the worst case condition (NMOS gate at VDD, all the other terminals grounded)
- Noise increase at low frequency in irradiated devices is related to excess noise contributions from lateral parasitic MOSFETs turned on by positive charge build-up in STI oxides

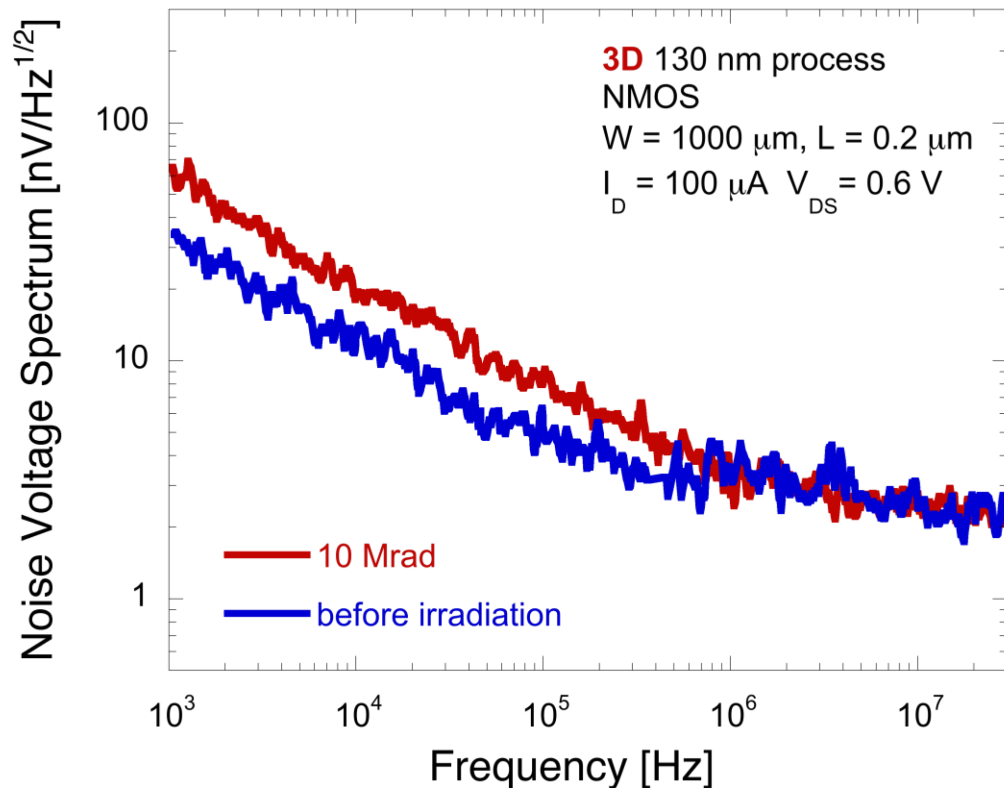


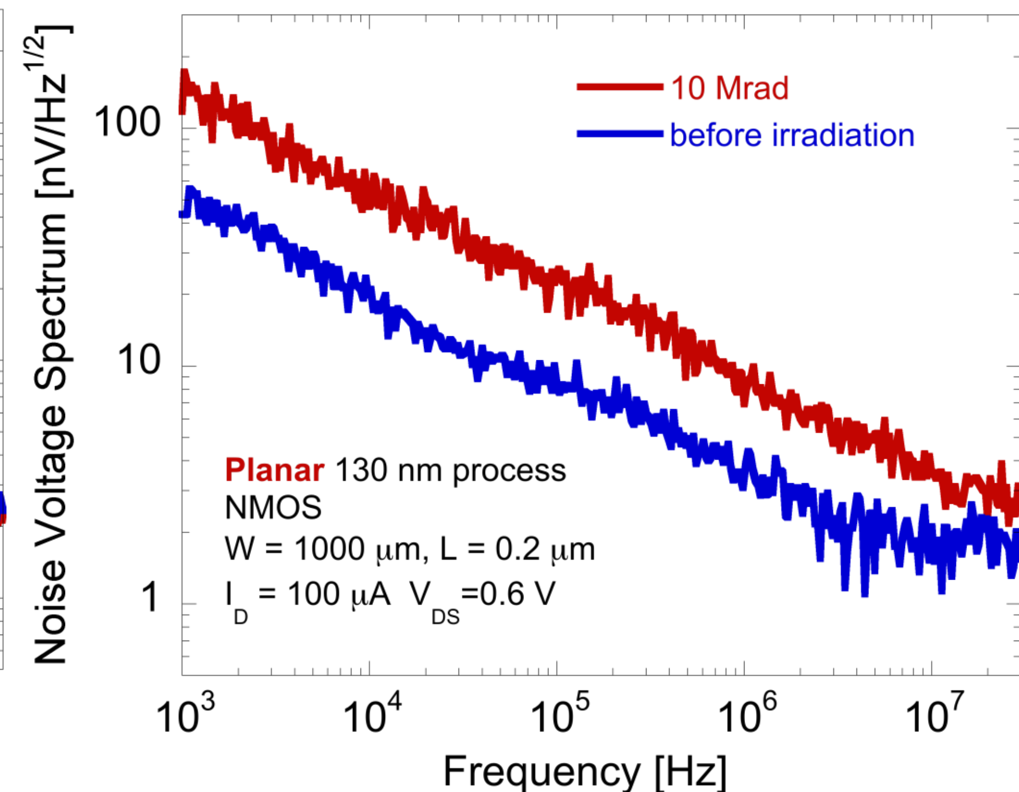



# Comparison with planar technology



- 3D processing steps do not result in any significant degradation of the radiation tolerance features
- Smaller sensitivity to ionizing radiation than planar devices from the same CMOS generation – likely due to oxide processing details and different bulk doping levels

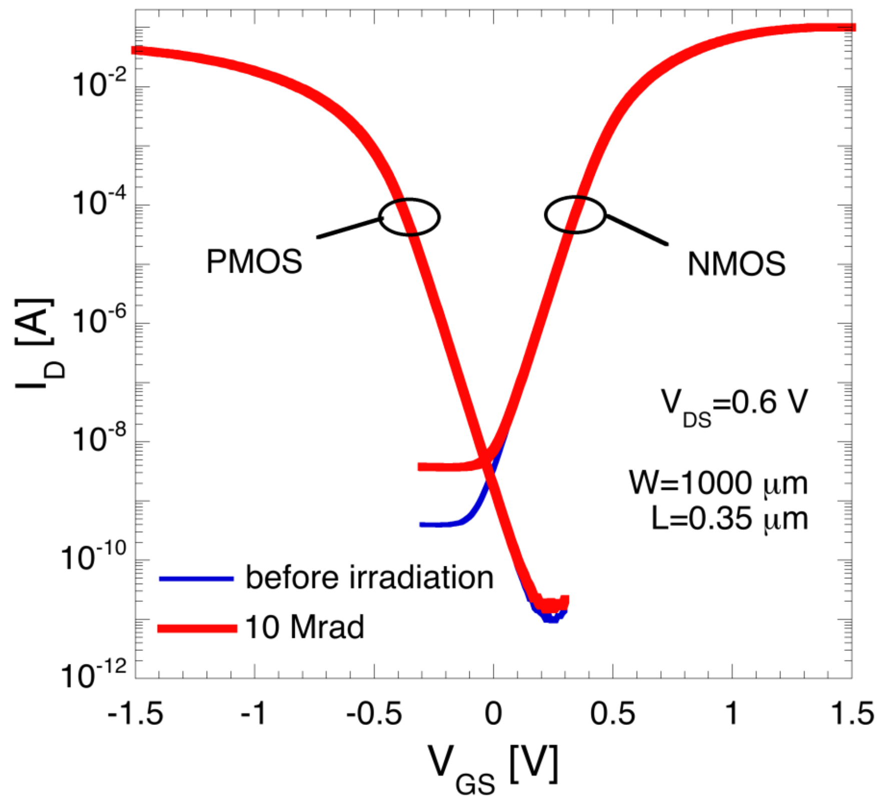


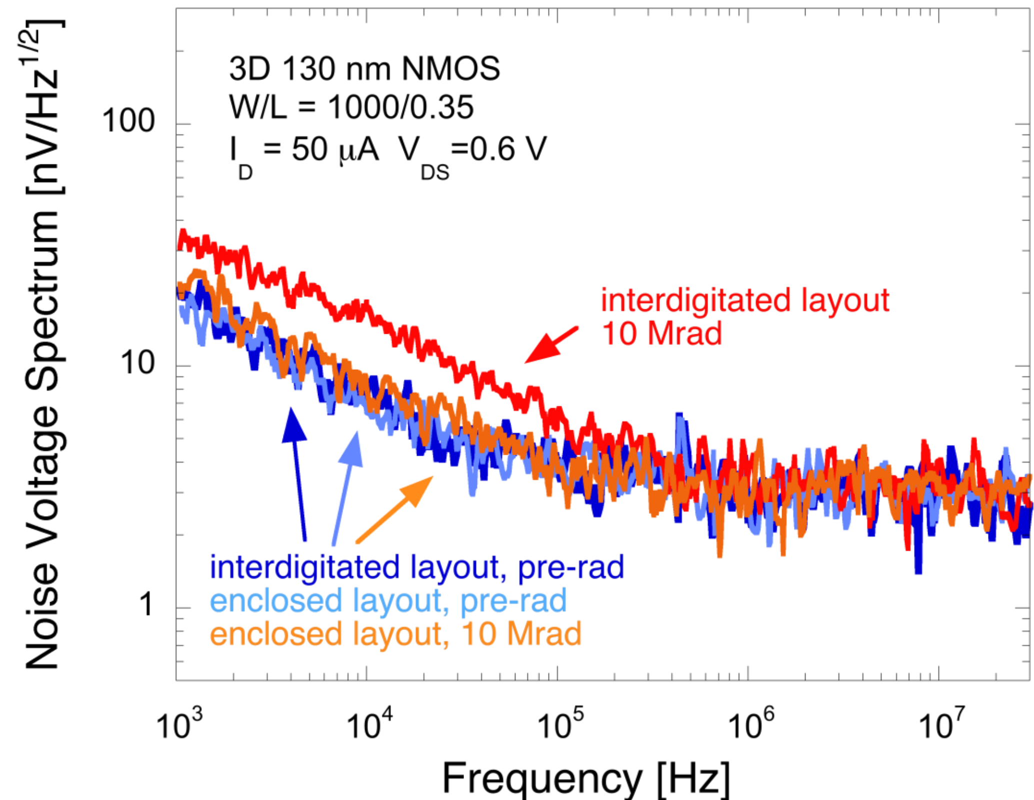



# Enclosed layout



- Increase in the off-state current for NMOS transistors, negligible change in PMOS transistors
- Use of enclosed layout techniques, as in other technologies in the same and other nodes, improves the tolerance to ionizing radiation

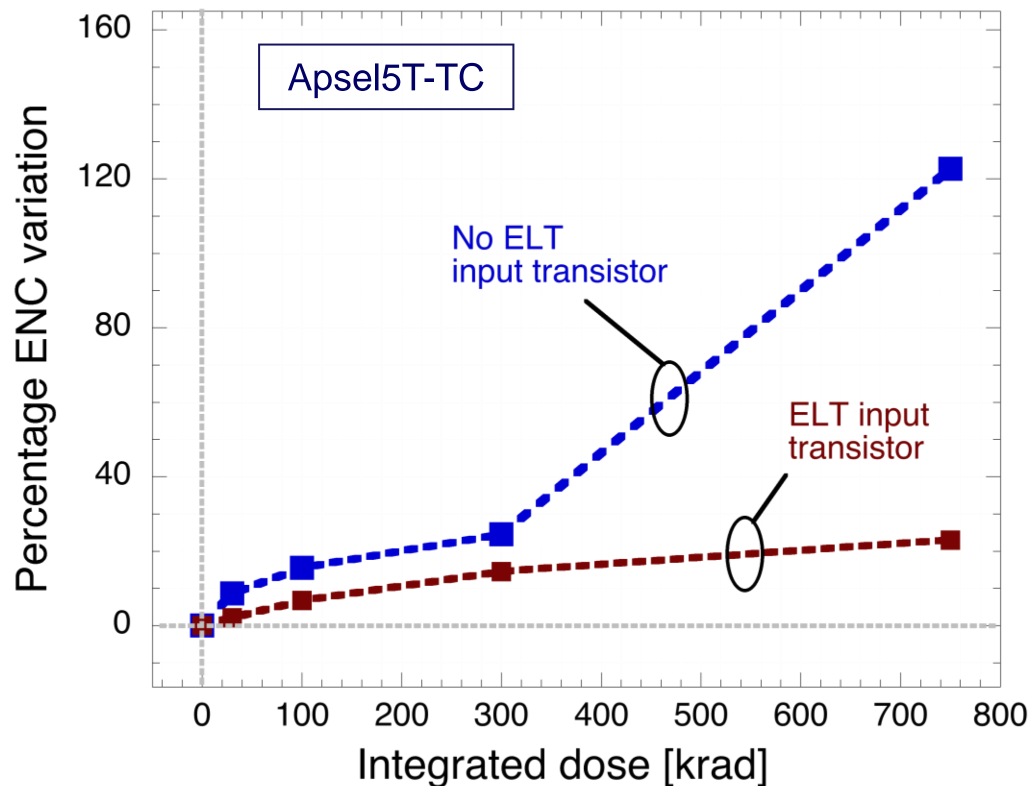


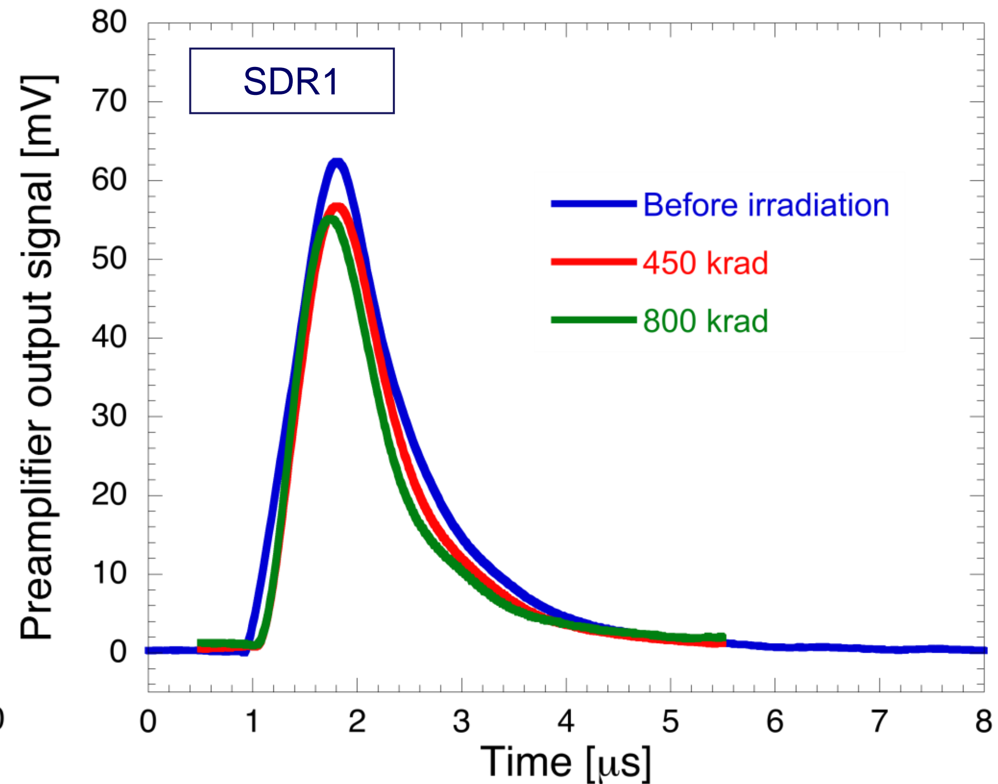



# Monolithic sensors

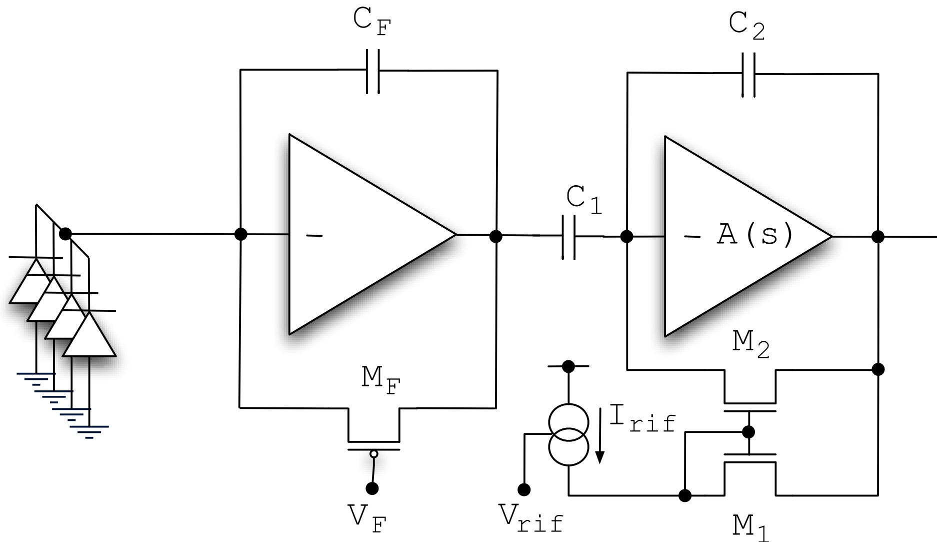


- Radiation tolerance improvement provided by enclosed layout techniques is confirmed by 3D MAPS characterization – smaller ENC increase detected in devices with enclosed layout input transistors
- Charge sensitivity found to decrease by 10% at about 800 krad TID



# Quadruple well MAPS




- Deep P-well used to avoid parasitic collection by the N-wells containing PMOS devices
- Starting wafers with different epi-layer resistivity available, ~10 Ωcm (std res) or ~1 kΩcm (hi res)
- 3x3 matrices with different epi-layer resistivity, 12 um in thickness (also 5 and 18 um options available)
- Test structures irradiated up to
  - $10^{14}$ 1 MeV n/cm$^2$ with intermediate steps at 2x$10^{12}$, 7.2x$10^{12}$ and 2.7x$10^{13}$ n/cm$^2$
  - ~11.5 Mrad($SiO_2$) $\gamma$-rays TID, with intermediate steps at 1 and 3 Mrad($SiO_2$)
- DUTs biased as in the real application during gamma-ray irradiation

50 um

50 um

A

A'

Collecting electrodes

N-well

P-well/Deep P-well

A

A'

DPW

DPW

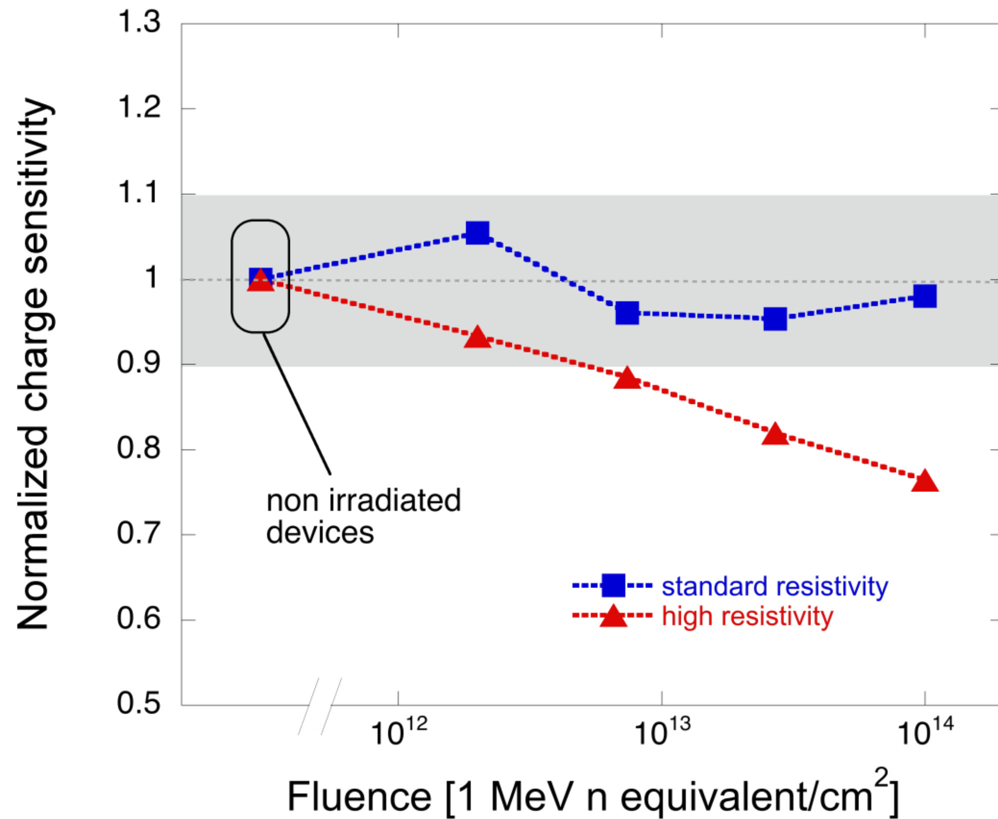
epi-layer

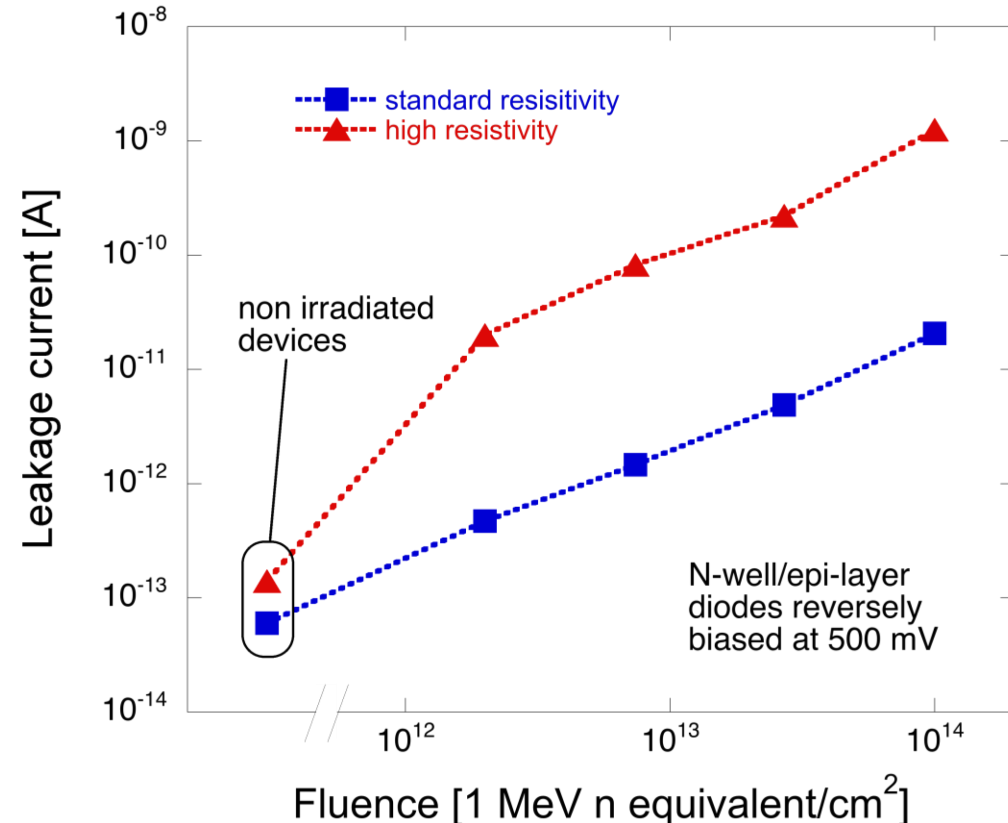
substrate

# Bulk damage: gain degradation vs epi-layer resistivity



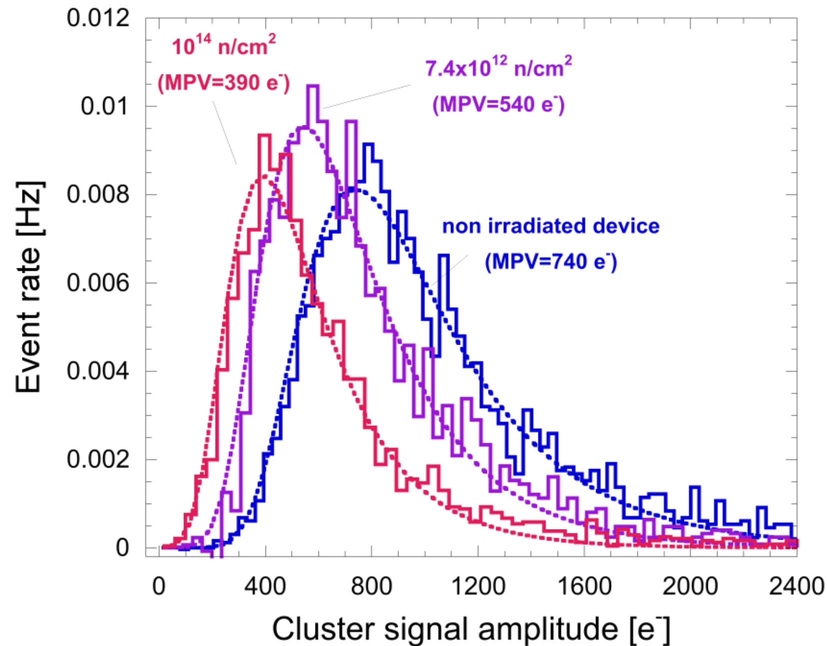
- Non negligible charge sensitivity decrease in the samples with high resistivity epitaxial layer – likely due to an increase in the leakage current from the collecting electrodes → increase in the preamplifier feedback conductance



# Bulk damage: charge collection degradation






non irradiated devices

small electrodes (4-well CMOS, epi-layer)

large electrodes (130 nm CMOS, no epi-layer)

Normalized MPV

1
0.8
0.6
0.4
0.2

$10^{12}$ $10^{13}$ $10^{14}$

Fluence [1 MeV n equivalent/cm$^2$]

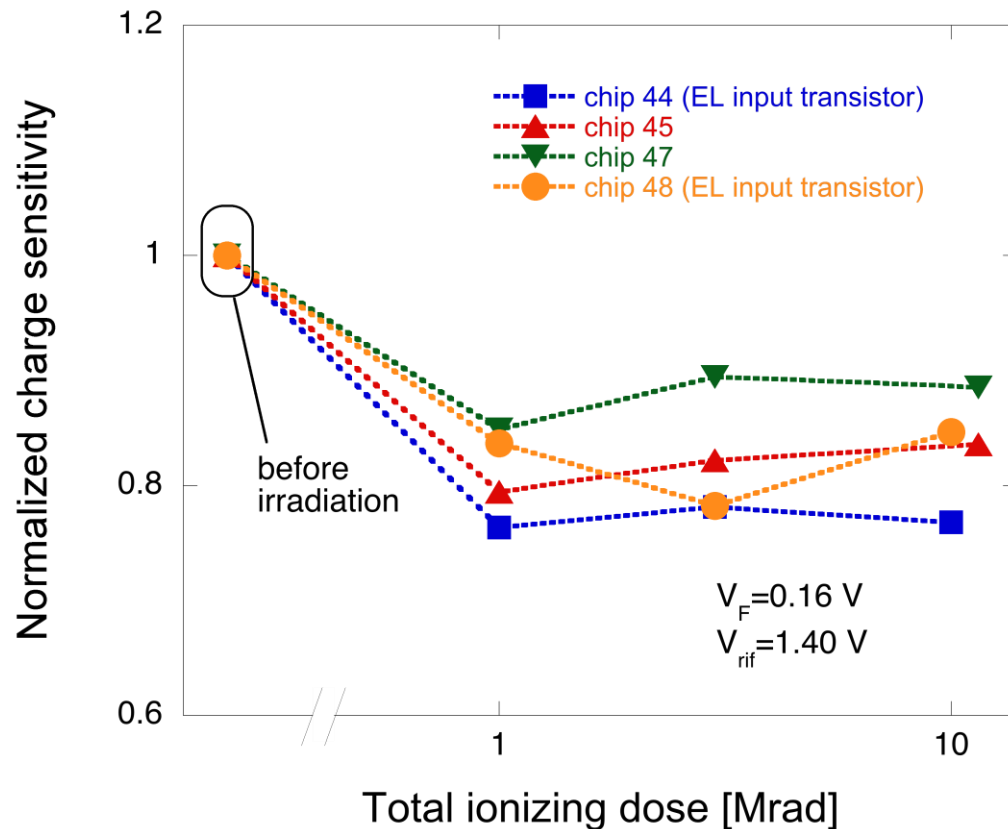
4well MAPS - 1kΩ cm
4well MAPS
DNW MAPS - M1
DNW MAPS - M2
10 Ω cm

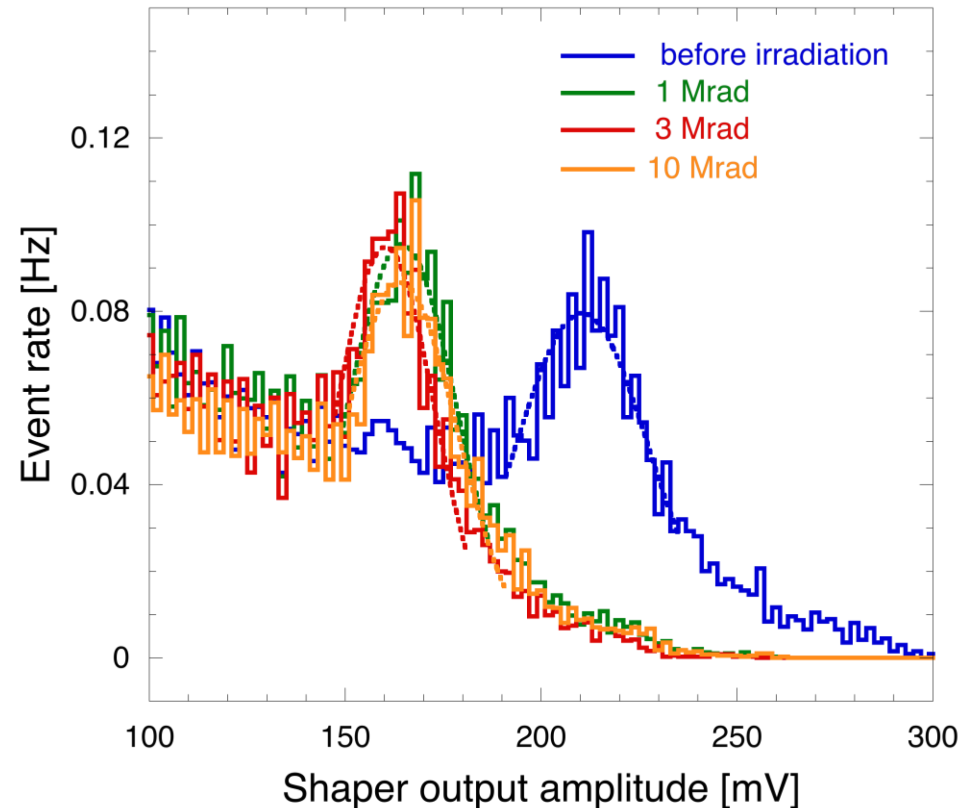
- Charge collection degradation evaluated through $^{90}$Sr spectrum measurements
- Significantly higher tolerance detected in samples with smaller doping concentration in the sensitive layer – larger electrodes also help at relatively small fluences

# TID effects: gain degradation

Quad. well MAPS

- Charge sensitivity decreases with the first step, no significant change at higher doses (direct charge injection measurements confirmed by $^{55}Fe$ spectra) – likely due to effects taking place both in the charge preamplifier and in the shaper



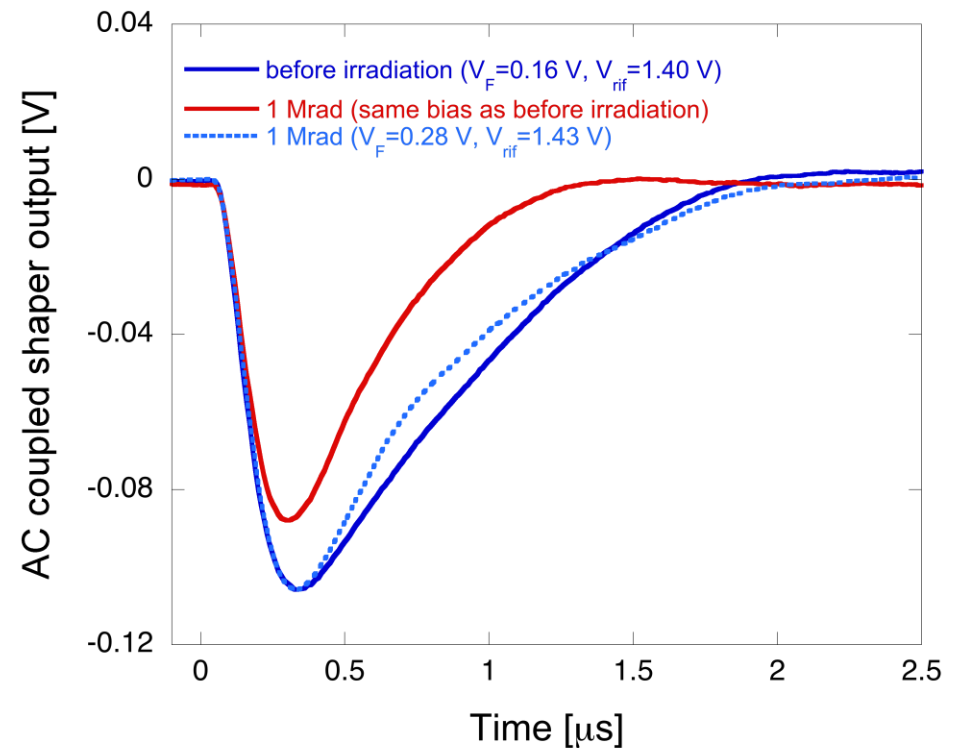



# TID effects: shape change in the channel response

- Change in the response peak, peaking time and slope after the first step – due to detector leakage increase and radiation induced narrow channel effects in the shaper feedback network
- Virtually complete recovery in slope and peaking time after the final step

$C_F$ $C_2$ $C_1$ $-A(s)$ $M_F$ $M_2$ $I_{rif}$ $V_F$ $V_{rif}$ $M_1$

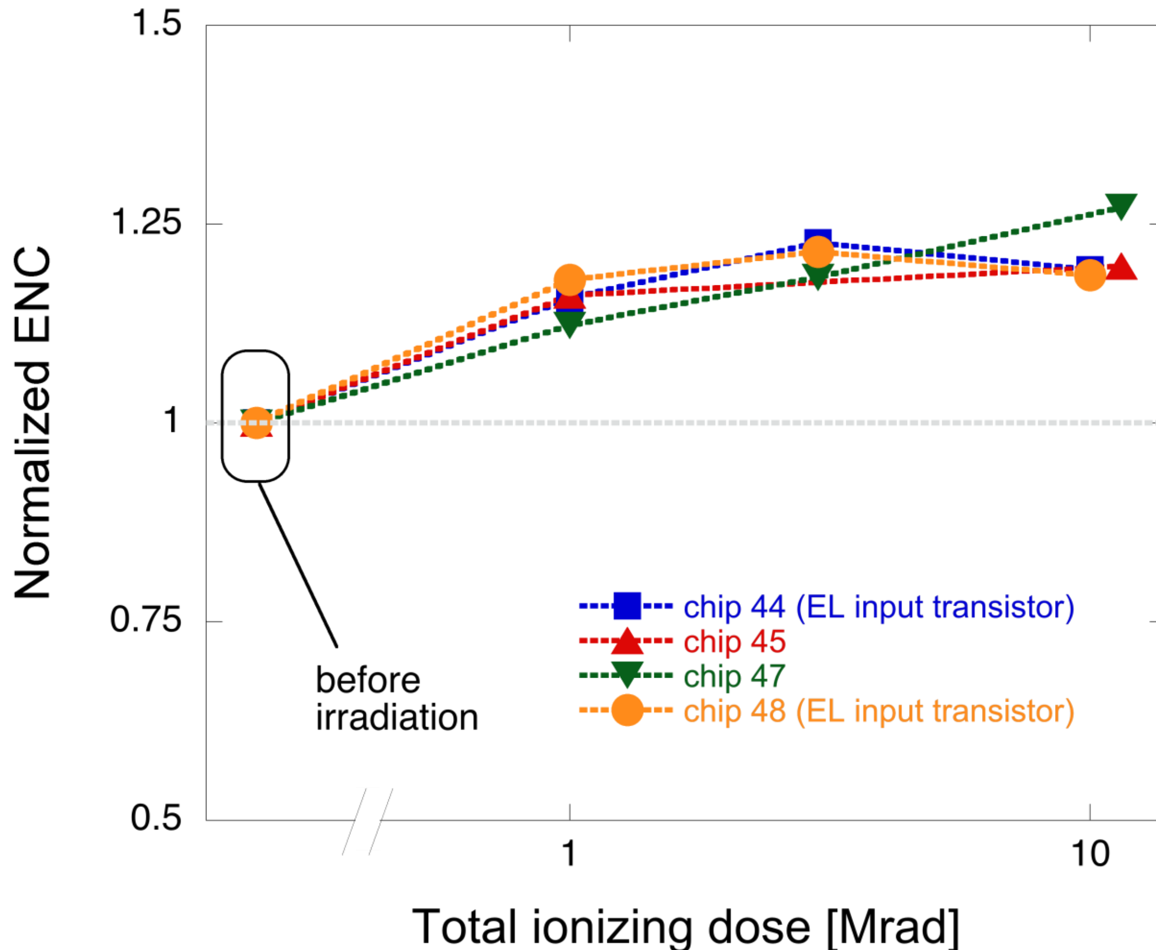
AC coupled shaper output [V]
0.04
0
-0.04
-0.08
-0.12
0
0.5
1
1.5
2
2.5
Time [μs]
before irradiation
1 Mrad
3Mrad
10 Mrad
$V_F$=0.16 V
$V_{rif}$=1.40 V



# TID effects: noise degradation



- Equivalent noise charge increases by 20% after 1 Mrad($SiO_2$), small increase after the subsequent steps up to about 25%




- Increase probably due to 1/f noise increase in the preamplifier input device (induced by border traps density increase in the gate oxide)
- Use of an enclosed layout input transistor in the charge preamplifier makes no significant difference

# Lessons learned and conclusion

- Careful design is needed to minimize performance degradation in CMOS monolithic sensors exposed to radiation (while complying with the limited amount of area and power available, especially in a pixel sensor)
  - minimize finger number and/or use enclosed layout to avoid noise increase in the preampli input device particularly when peaking times well in excess of 100 ns are used
  - avoid using narrow channel transistors in critical front-end points (e.g., feedback network, current sources)
  - use compensation networks to counteract the increase in the sensor leakage current
  - large area collecting electrodes help (compromise with noise/power dissipation needed)
- Some technology options may substantially improve the tolerance to bulk damage
  - use a sensitive layer with a low doping concentration (but beware of the possible higher sensitivity to radiation in terms of leakage current)
- Characterization of carefully planned test structures may be extremely helpful in understanding what is going on in relatively complex devices such as hybrid pixel-like MAPS when they are exposed to radiation