Design and Performance of Fully Depleted Backside Illuminated CMOS Sensors

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CPIX14 Workshop, September 15 - 17 2014

Outline

- About SCI
- SCI’ deep depletion process
- Results from 640x512 imager
- SCI camera

Sensor Creations

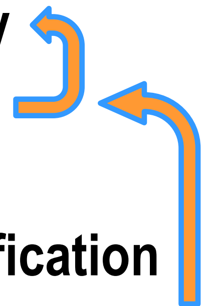
About Sensor Creations

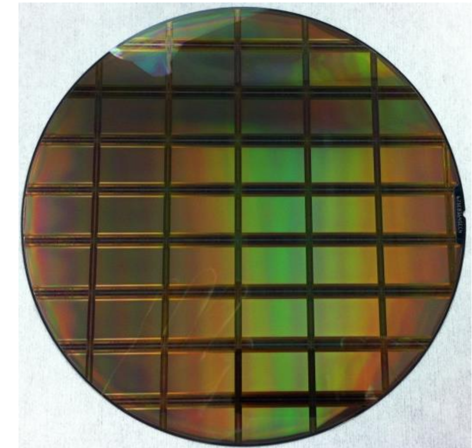
- Founded by Stefan Lauxtermann in 2010
- Located in Southern California
- Affordable, ROIC and image sensor design
  - Design (in house)
  - Fabrication (through CMOS fab partner)
  - Test (in house)
  - Prototype and low volume packaging (in house)
- Extensive suite of silicon proven IP blocks available today
  - Low noise snapshot shutter pixels with multi frame storage
  - Low noise readout chain programmable
  - Serial interface (SPI)
  - 14bit high speed, low power column parallel ADC (measured)
  - High speed I/O port with 1Gbit/sec (measured)
- Fully depleted backside illuminated CMOS imagers
  - Custom designs
  - Products
- Prototype Cameras

Sensor Creations

SCI uses Tanner EDA Design System

1. Schematic entry
2. Simulation
3. Layout
4. Block level verification
5. 2D/3D parasitic extraction
6. Top level verification

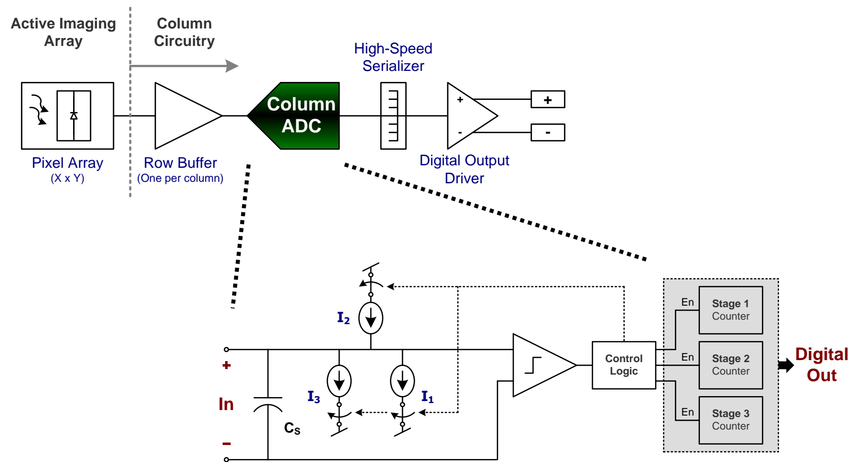




8” wafer with large format ROIC designed by SCI, (MacDougal et al, DSS 2012)

Designs with > 45M Transistors and Layout Area >22 x 32 mm^2 have been realized successfully

Low Power – High Pixel Rate Single-Ramp Multi-Slope ADC



- **Low power**
  - < 120 μW per column
- **Small size**
  - 10 μm x 1000 μm
- **Resolution: 14b**
  - Adjustable from 10b – 14b
- **High speed**
  - 500 kS/sec (=> to 2μsec line time)

Power efficient architecture

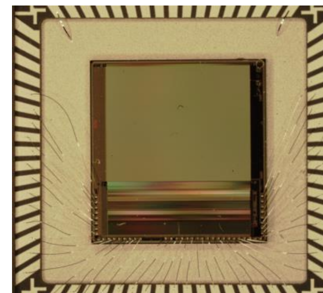
- Lower power/pix/sec than analog equivalent
- Expl.: 1 MPix sensor, 30 fps, P_{ADC}= 7.2 mW

ADC for IR image sensors

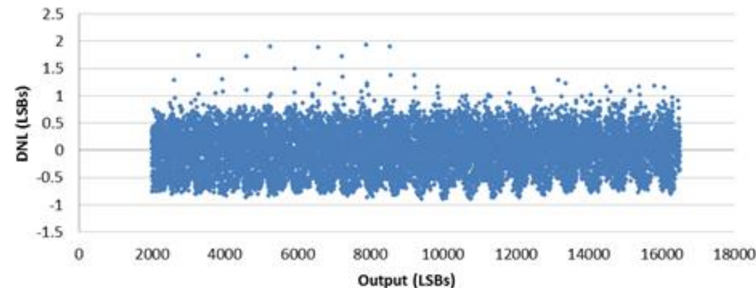
- Some fixed pattern noise acceptable

Status

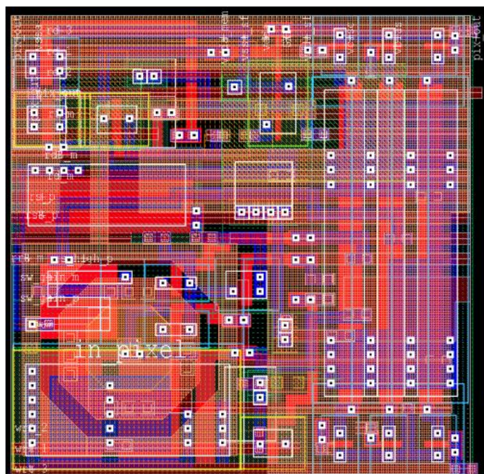
- Tested and available



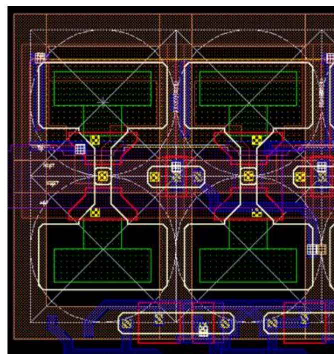
640x512 ROIC with 10μm pitch and digital output



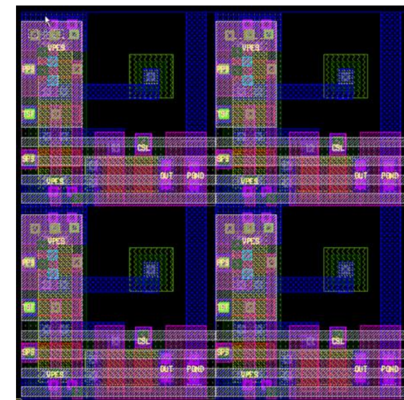
Pixel IP for Monolithic and Hybrid Imagers



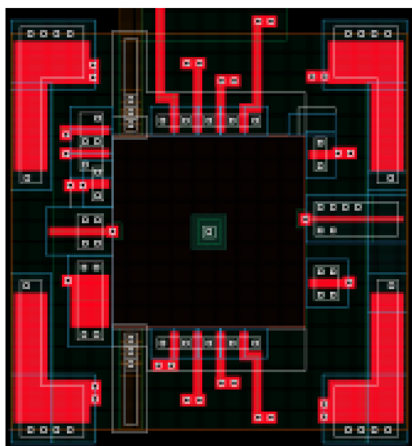
15 µm ROIC Pixel



2.7 µm 4T pixel with CFA and micro lens (FSI, 2x2)

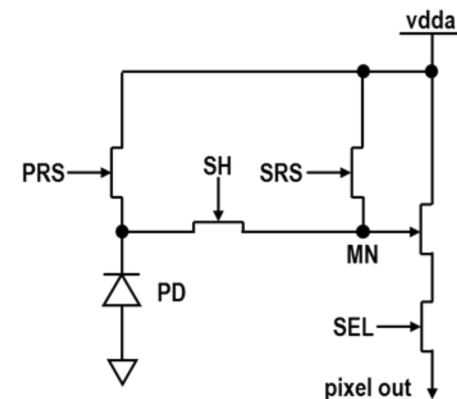


5.8 µm 5T pixel (BSI, 2x2) Test array

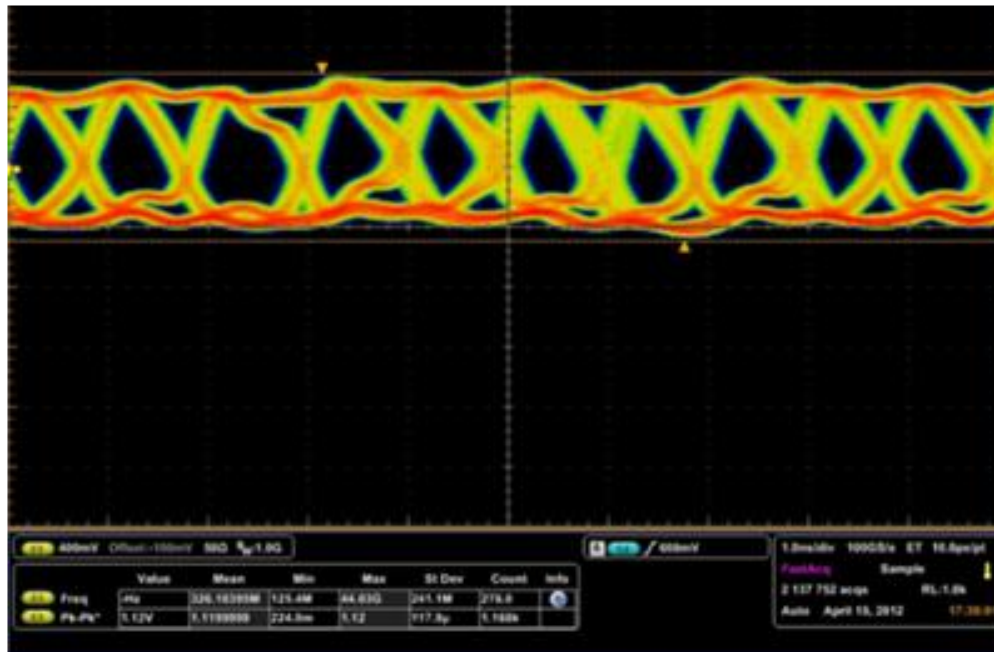


15 µm Mutiframe BSI Pixel

All Pixels are proven on silicon



High Speed LVDS I/O Port

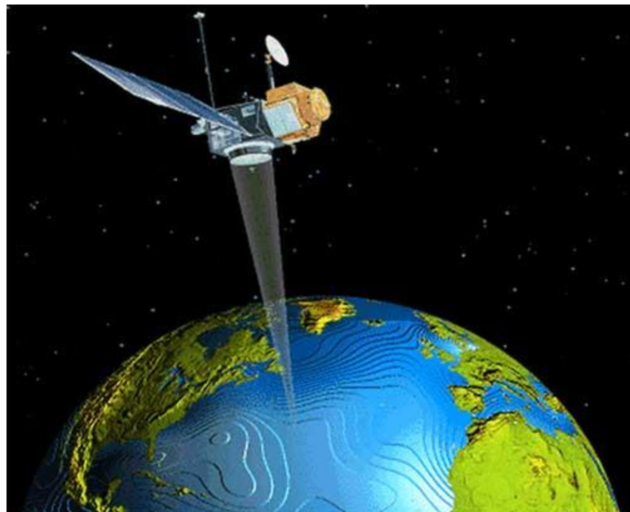


Measured on standard low resistivity silicon

- **1GHz, 16b serializer**

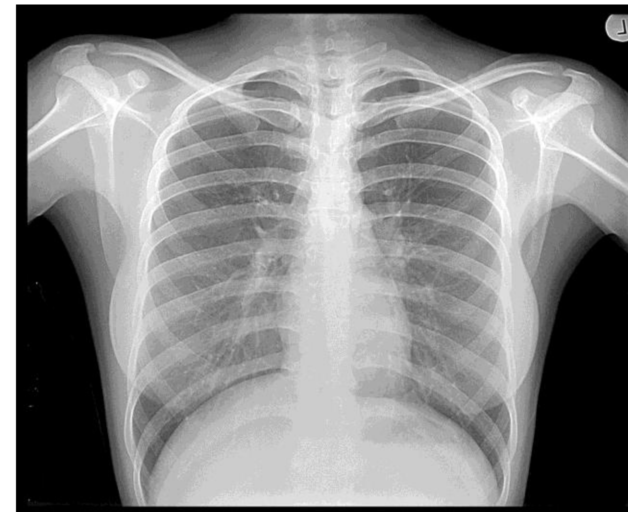
In high rho silicon transistor have a slightly higher transit frequency

Application for Deep Depletion CMOS Imagers

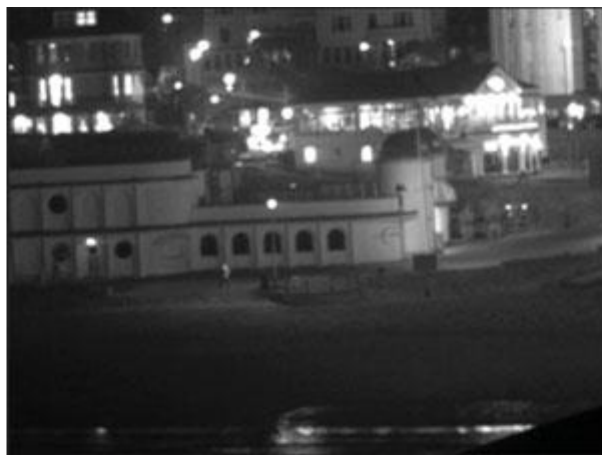


Hyperspectral Imaging in Remote Sensing Applications

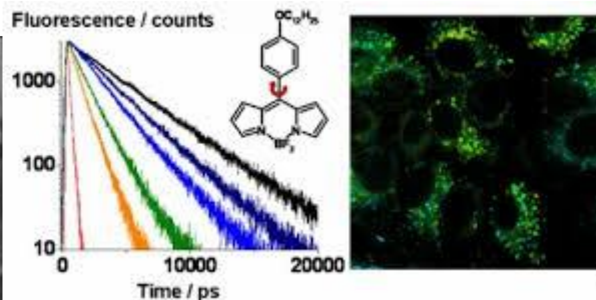
NIR Laser Ranging



Direct X-Ray Detection



NIR Night Vision



Nsec Fluorescence Lifetime imaging

Benefits of DD-CMOS

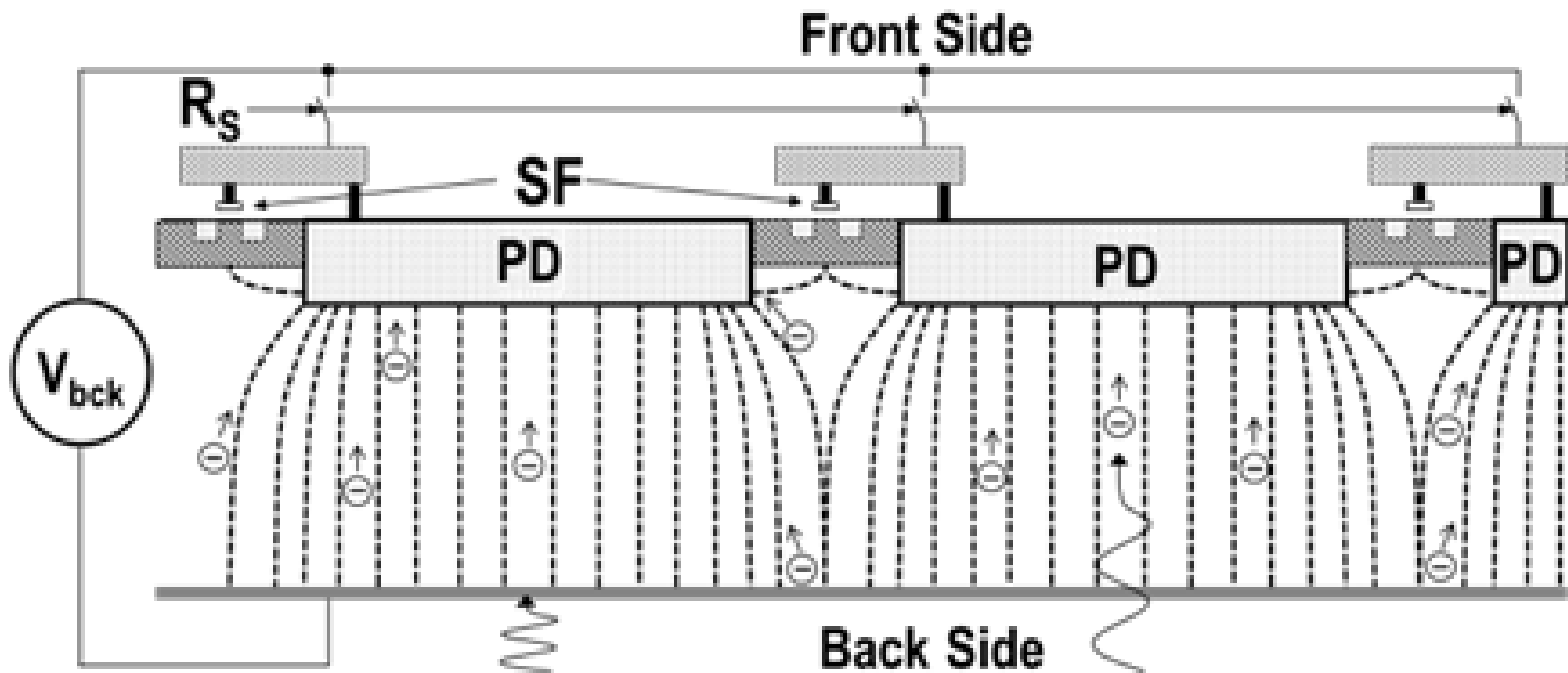
- High NIR sensitivity
- nsec response time
- High X-ray sensitivity
- Low noise at high speed

Advantages of Deep Depletion CMOS Technology

- High NIR response
  - Up to 40% at λ = 1069 nm (with 500µm thick silicon)
- High UV response
  - > 30% at λ = 300nm
- High broad band response
  - peak QE > 90%
- Direct detection of high energy radiation
  - X-ray < 20k eV
  - MIP for tracking
- Suited for very large format arrays
  - High yield compared to Hybrid FPAs
  - High data rate compared to CCD
  - Small pixel pitch (Nyquist MTF: 200µm thick silicon, 100V bias: 4.5µm)
- High Snapshot shutter efficiency
- Manufactural in standard CMOS foundry

Deep depletion CMOS provides unprecedented performance for single imager

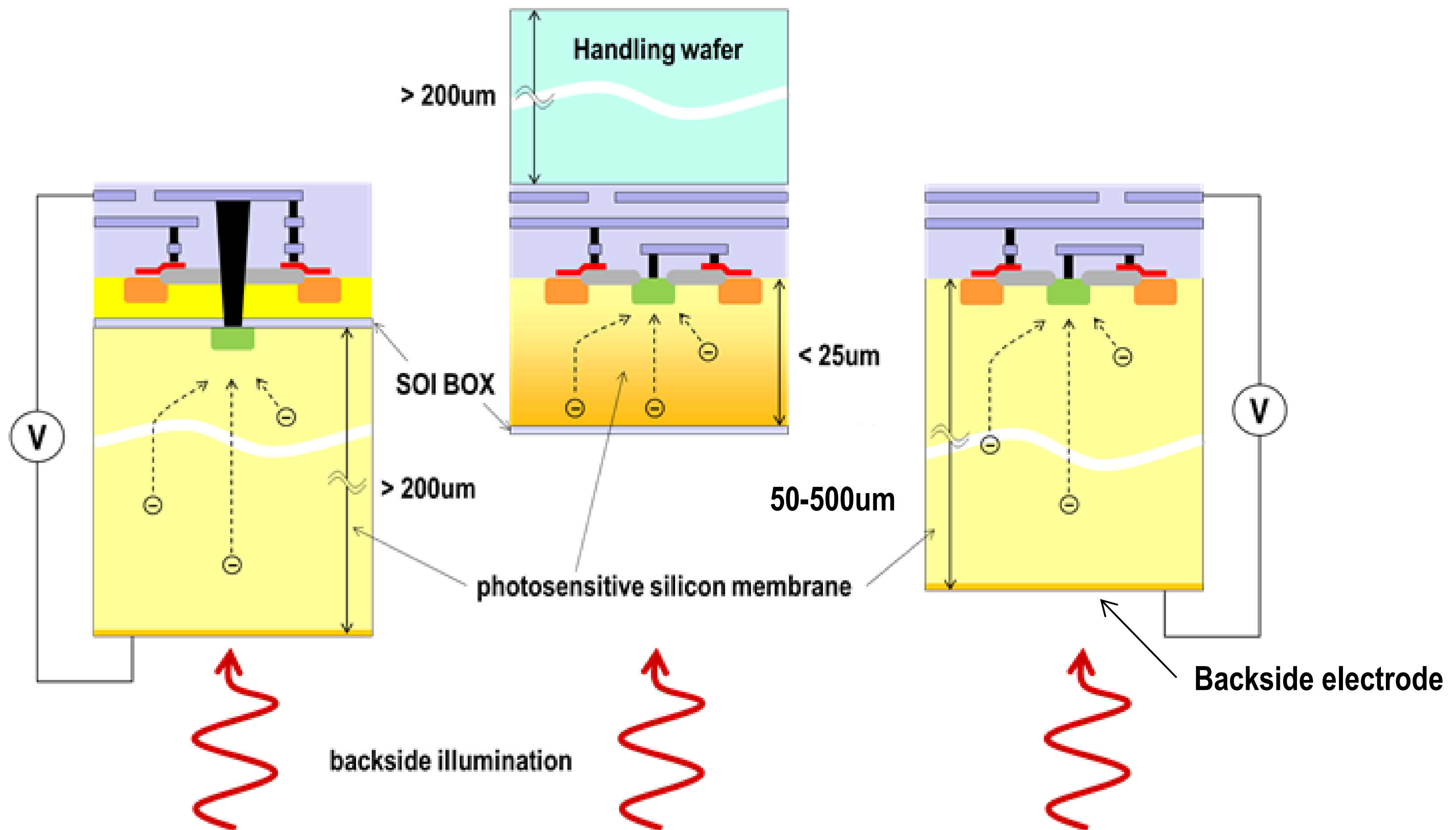
Cross Section of Fully Depleted CMOS Technology



Charge Collection Region Defined by Lateral and Vertical Depletion

Sensor Creations

Comparison of CMOS Deep Depletion MAPS



High rho silicon with TSV and 3D IC interconnect technology

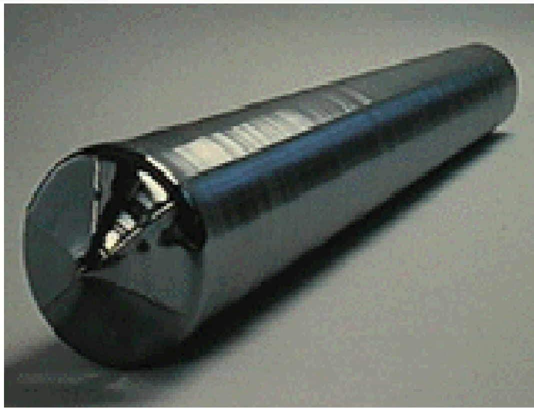
SOI with custom EPI layer (no backside contact)

This presentation

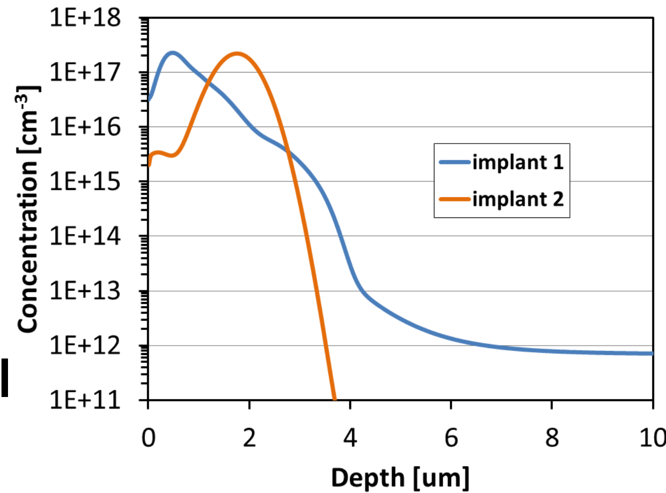
Our Approach Combines Excellent Performance with Highest Manufacturability

Pre-Processing of 640x512 Sensor

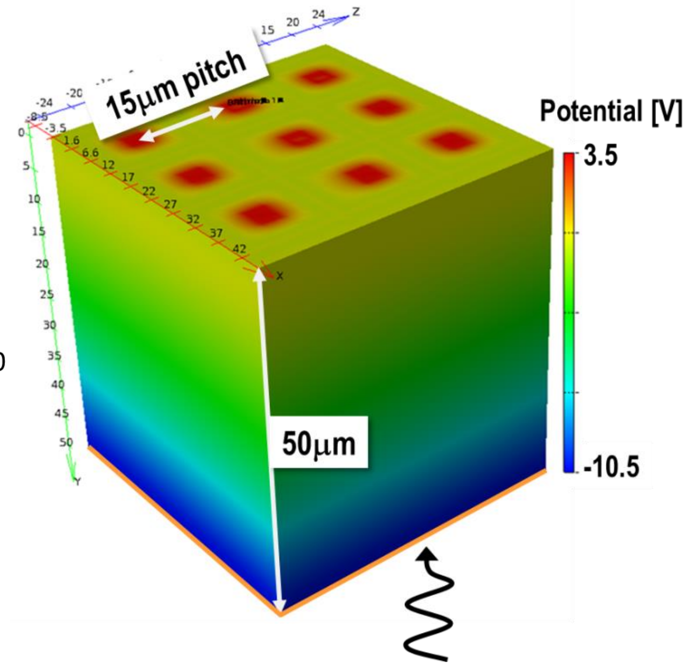
Sensor Creations



Selection of high purity silicon as starting material



Implantation Profiles for deep depletion PD



3D device model based on simulated

Process and Device Models were Confirmed with SIMS Profiling and Device Characterization

Potential Distribution Throughout Detector

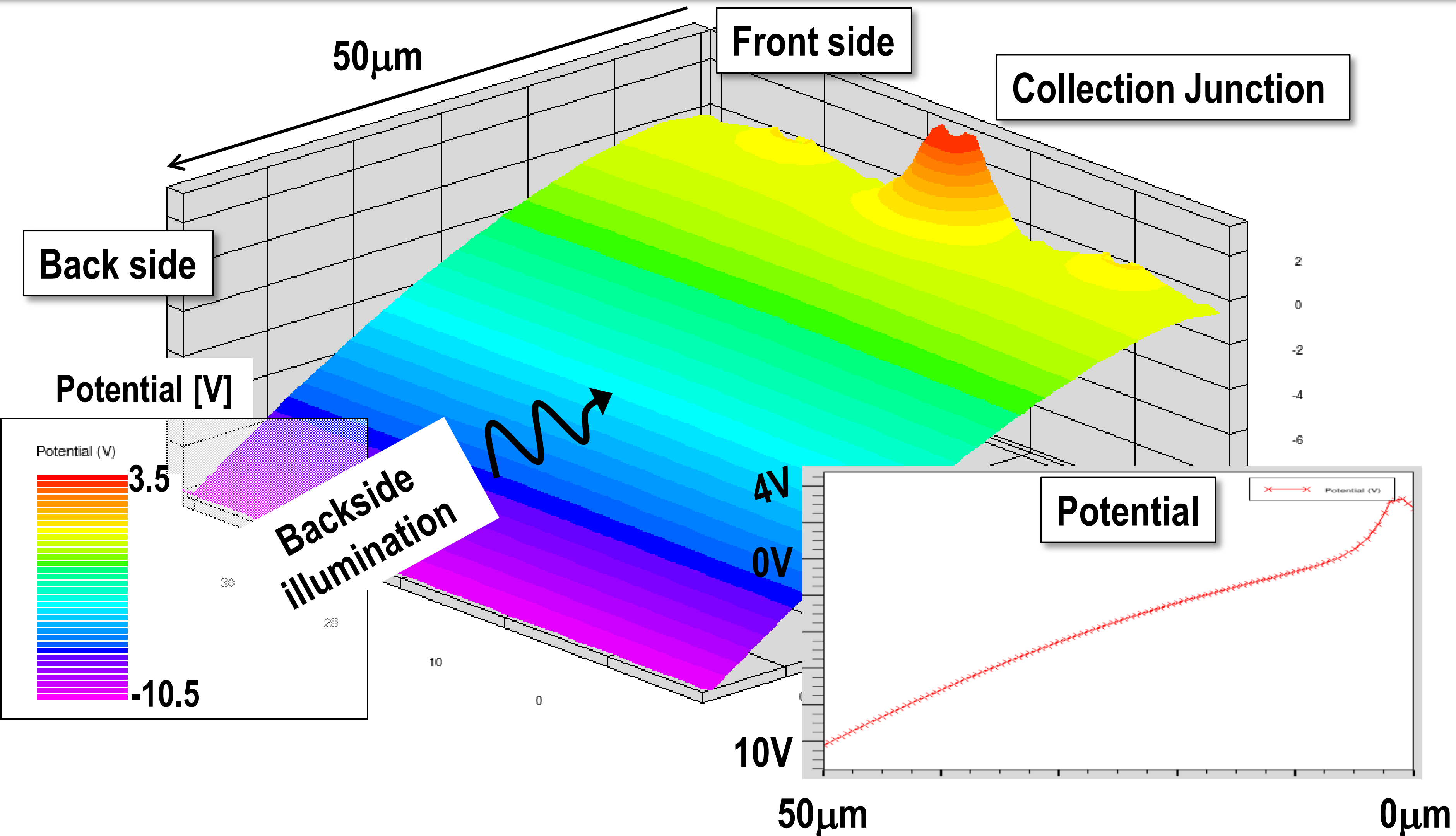
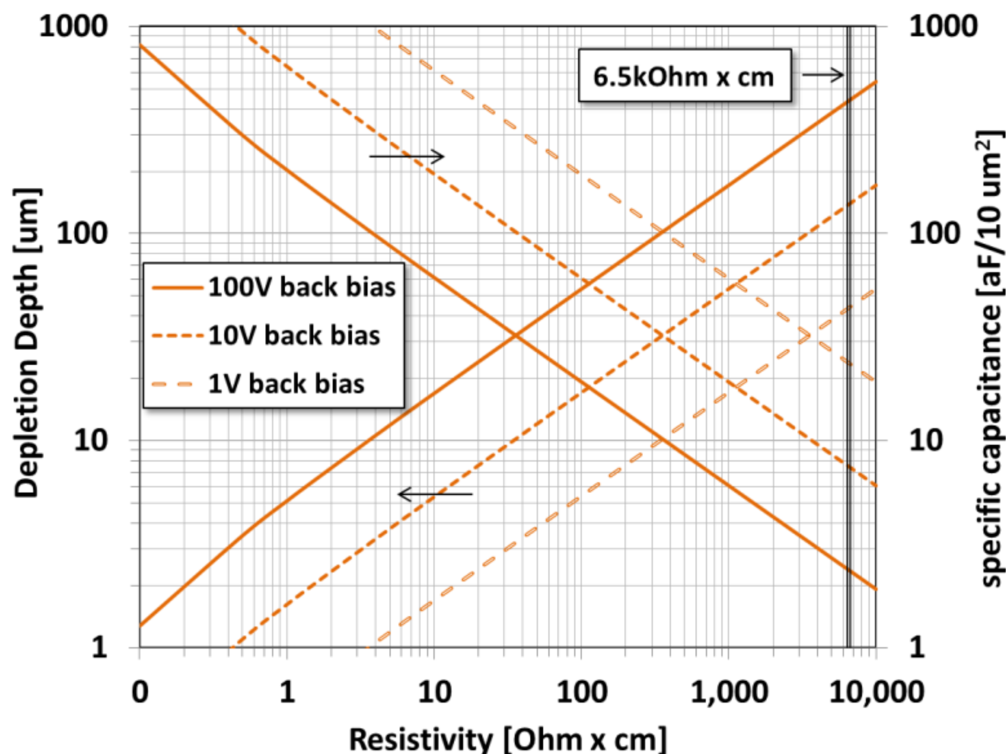


Photo Generated Charge Carriers are Gathered by Fast Drift Process (instead of slow diffusion) in Front Side Collection Junction

Estimate of Depletion Layer Versus Si Resistivity



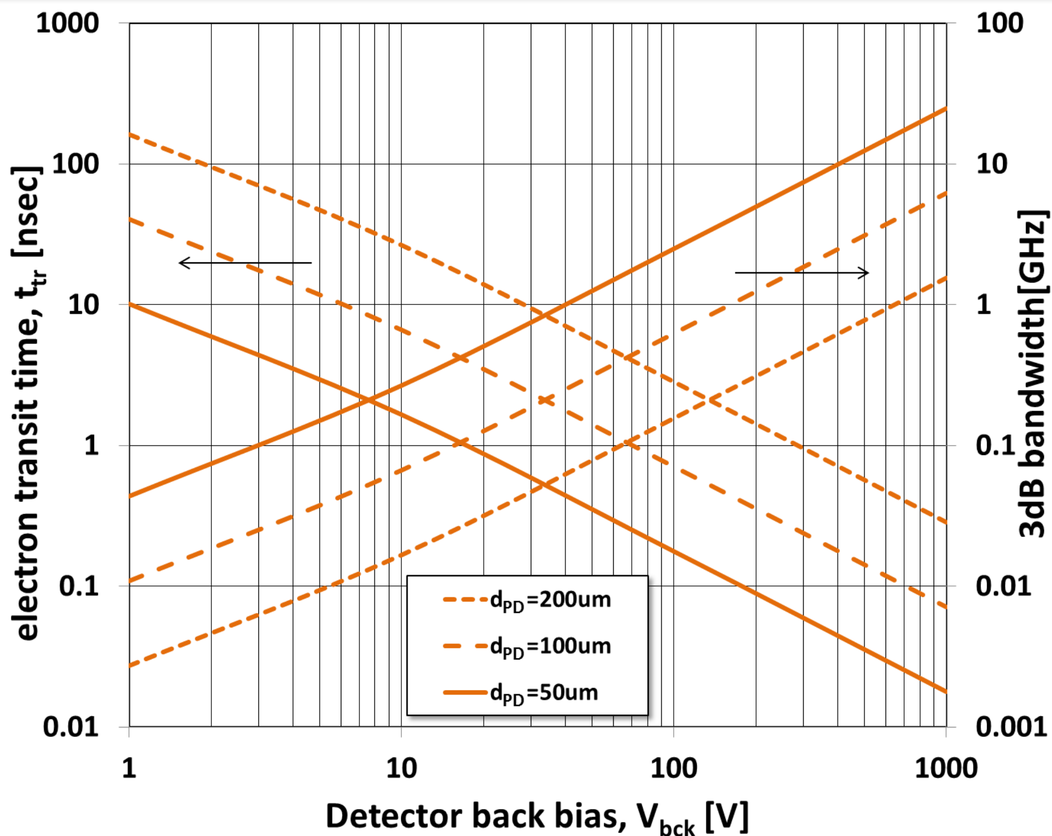
For best performance a backside bias must be applied

➡ Our 6.5 kOhm x cm material can be depleted to a thickness of 50um with a backside bias of less than 5V

High Resistivity Silicon Must be Used to Achieve Deep Depletion

Sensor Creations

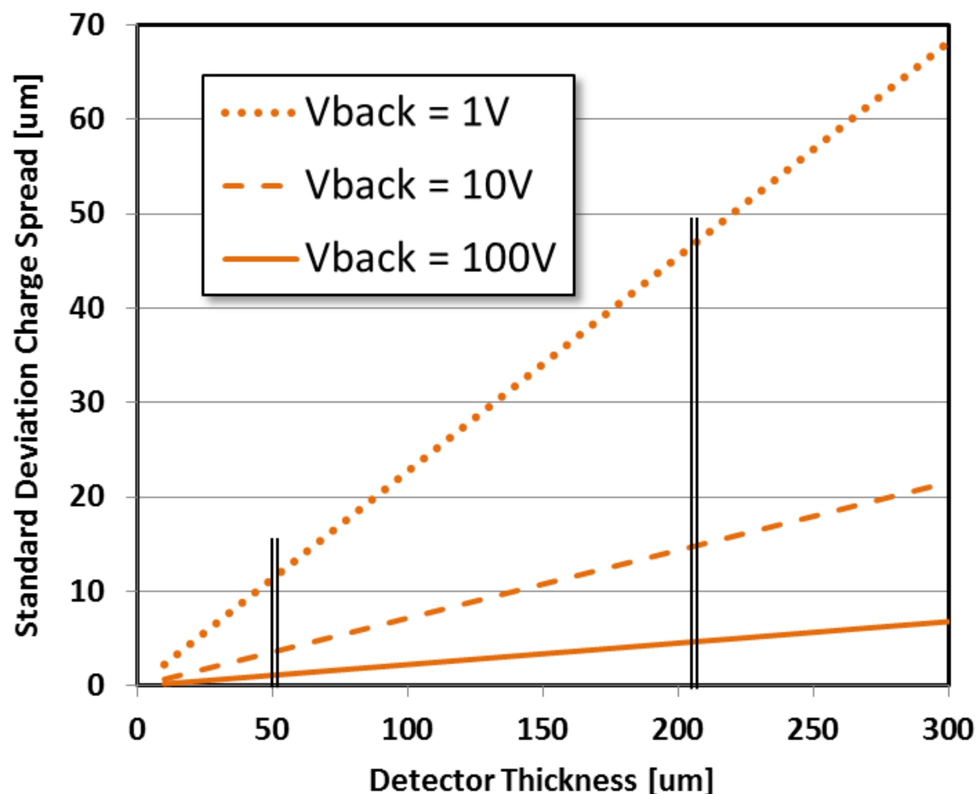
Predicted FD PIN Diode Response Time



Transit time of photo generated charge carriers in 100um FD CMOS imager with 100V backside bias < 1nsec, corresponding to a 3dB bandwidth > 1GHz

Fully Depleted Imager is Suited to Support Nanosecond Integration Time Windows

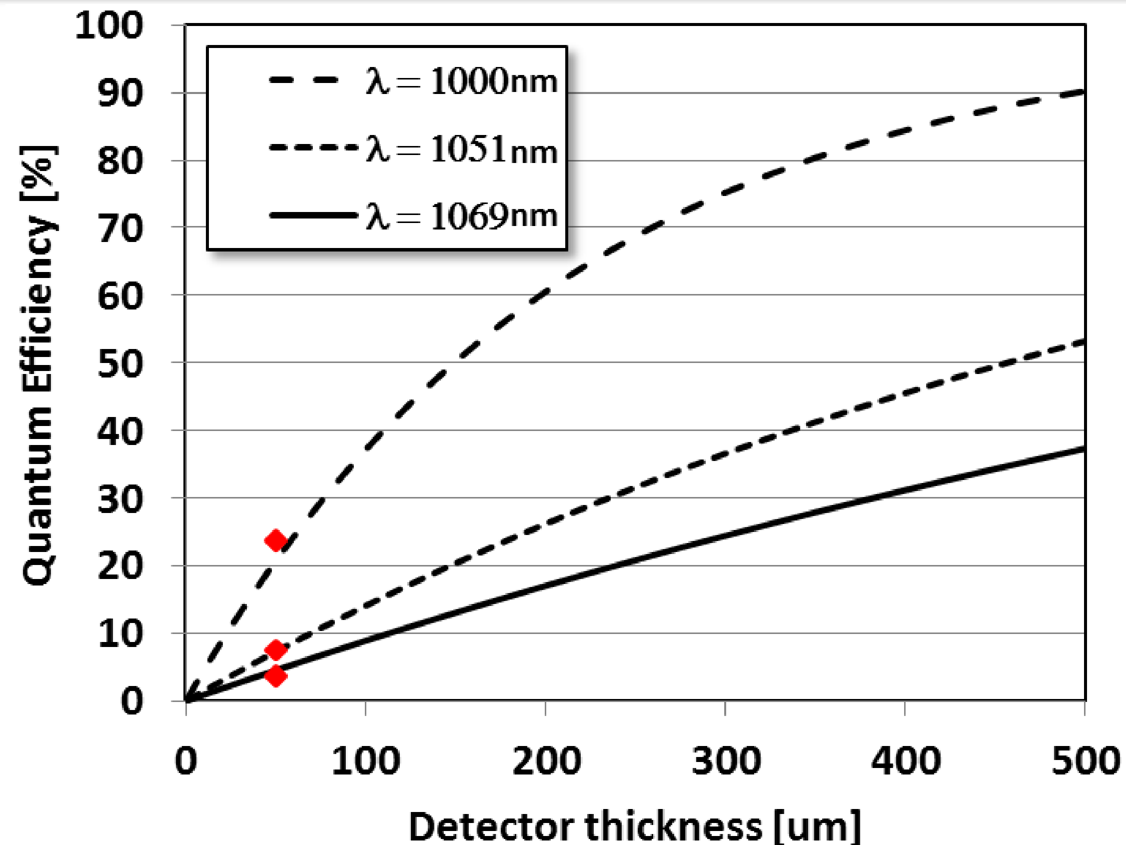
Predicted Charge Spread Versus Detector Thickness

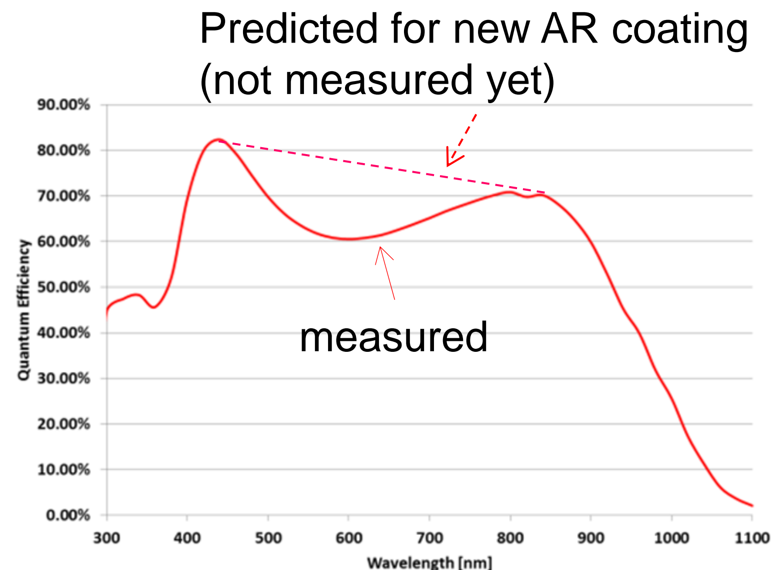


For a 200um thick FD CMOS imager with 100V backside bias, photo generated charge carriers can spread up to 4.5 um before reaching the front side collection junction

MTF Performance Limited Pixel Pitch of FD imager: < 4.5um

Quantum Efficiency

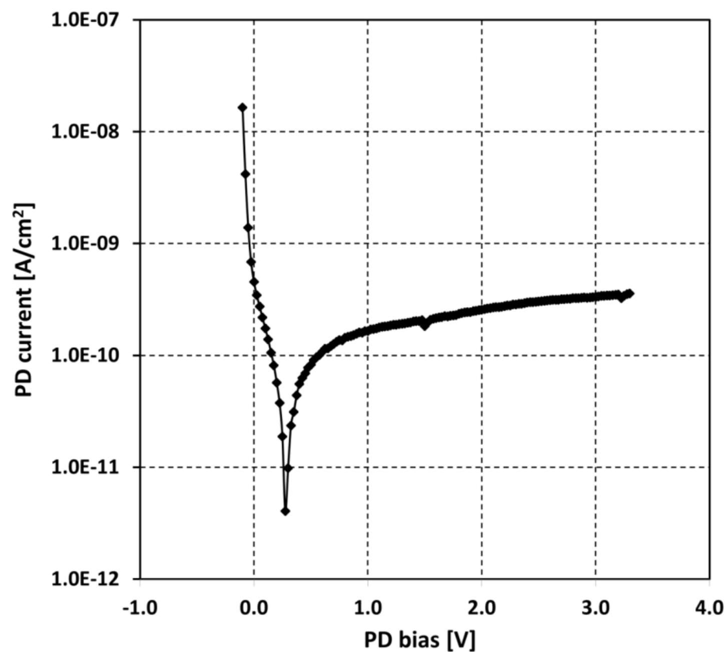


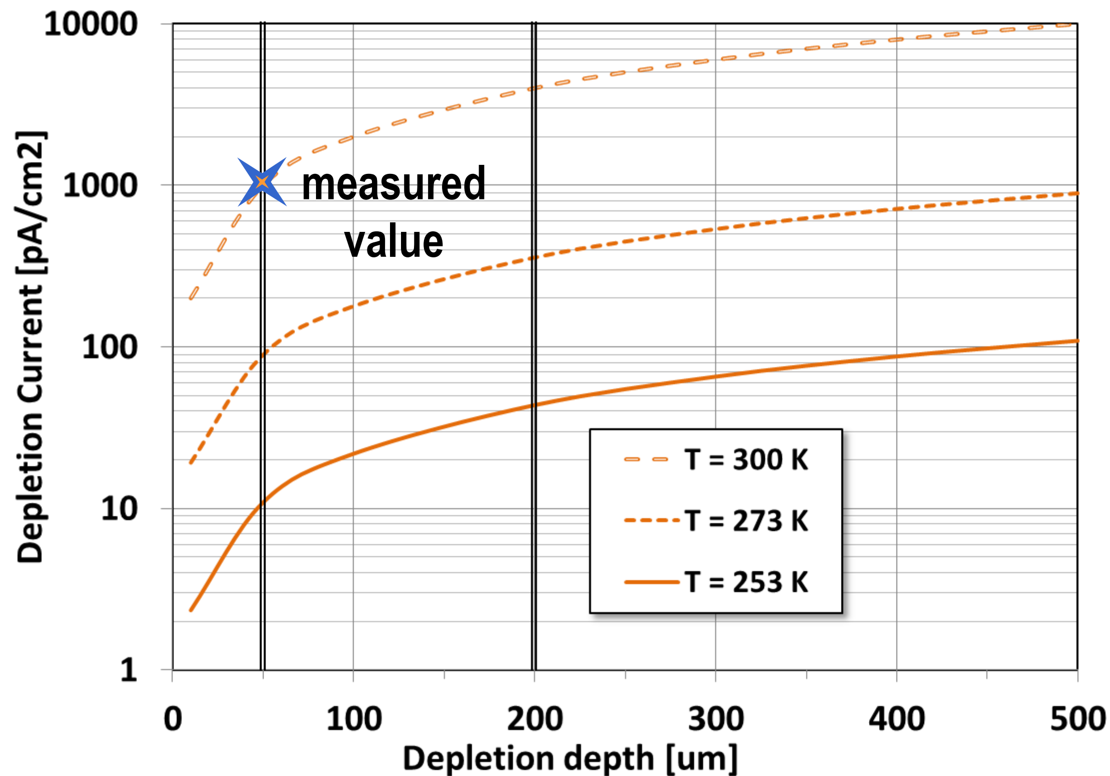


- High Broadband response
- High and stable UV response
- Peak QE > 90% can be customized with AR coating

Quantum Efficiency Comparable to that of Fully Depleted BSI CCDs

Dark Current on 50um Thick Silicon



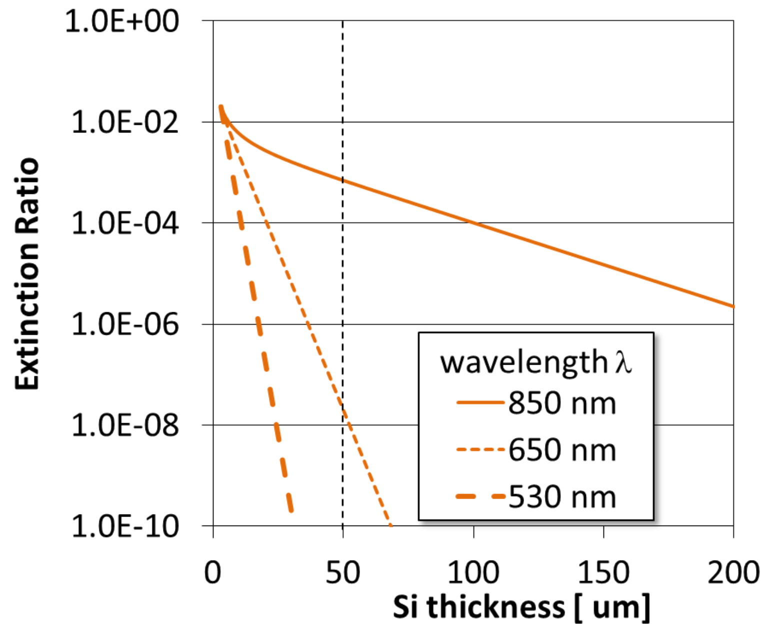


- Measured on $1mm^2$ large test pixel arrays, on wafer level, at room temperature
- 1V back bias was applied

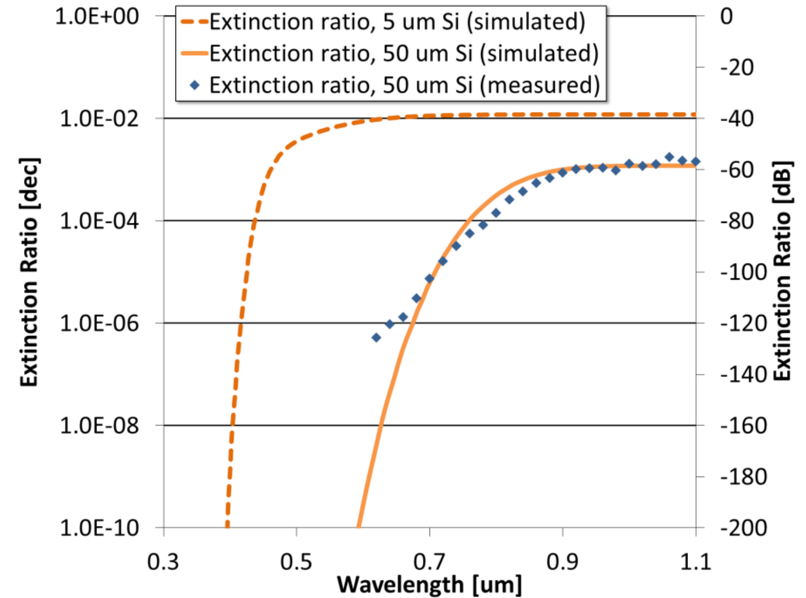
Measured Dark Current is Close to Predicted Depletion Current

Predicted and Measured Snapshot Shutter Performance

Extinction Ratio as a function of detector thickness (simulated)



Extinction Ratio as a function of wavelength (simulated + measured)



>120dB Extinction Ratio in Visible Domain for $\lambda \leq$ 640nm

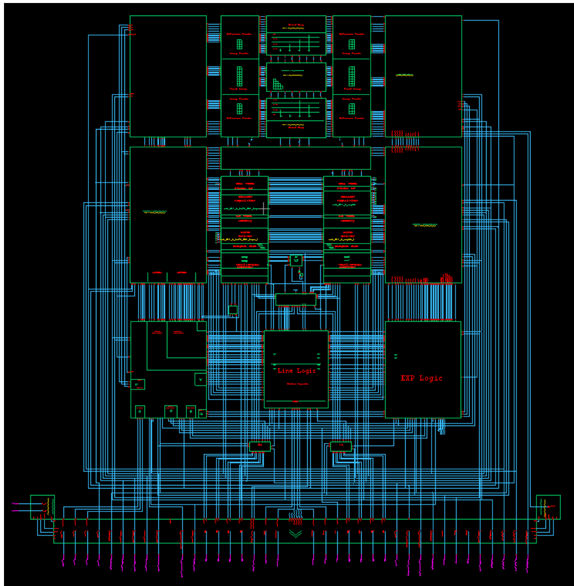
Deep Depletion Sensor Fabrication Flow

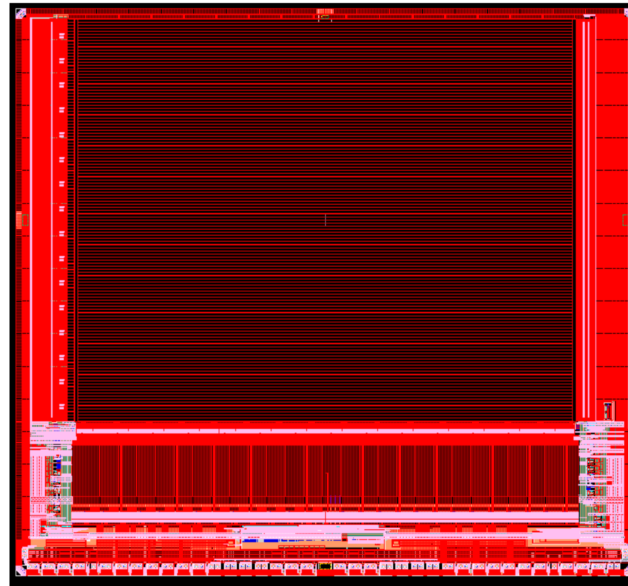
- Pre-Process steps
  - Deep depletion photodiodes
- CMOS Process
  - Standard wafer fab
- Backside Process
  - Thinning, Passivation, AR coating

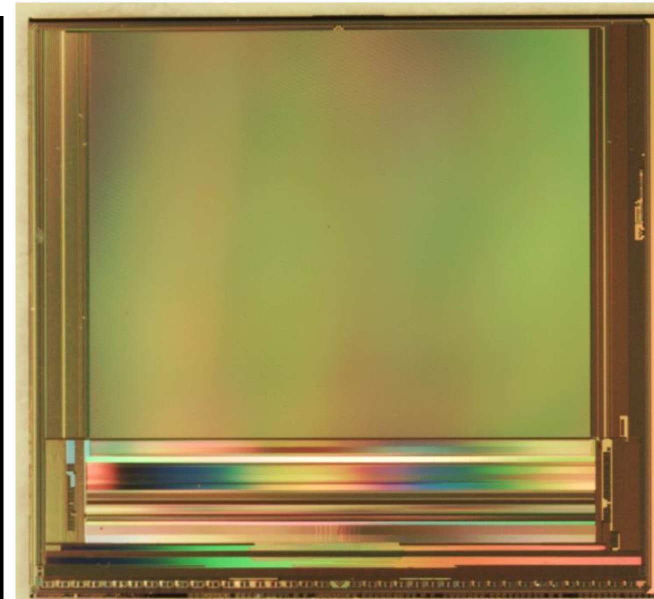
DD – CMOS development requires strong collaboration between process device and circuit design

Sensor Creations

Front Side Design of 640x512 Imager


schematic


layout


chip micrograph

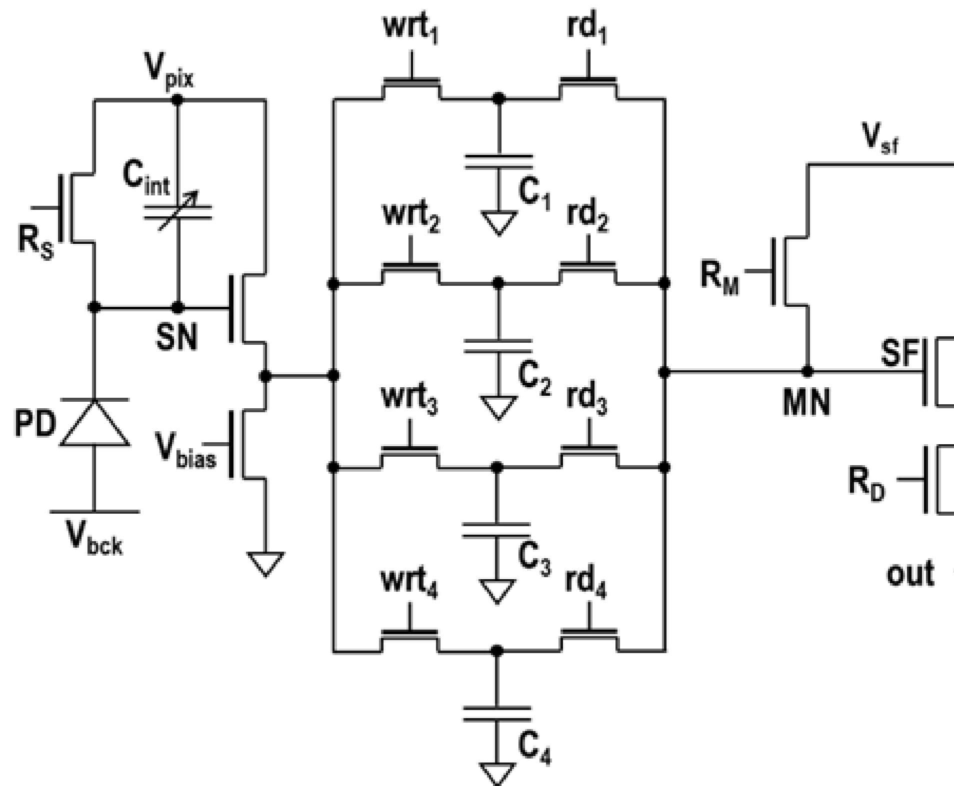
Implementation into SCI's EDA environment

- **New simulation models for optoelectronic devices**
- **Definition of design rules for non-standard process steps**
- **Programming of rule deck into verification tools (DRC + LVS)**

Custom Process Design Kit (PDK) was Used for IC Design of 640x512 Sensor

Sensor Creations

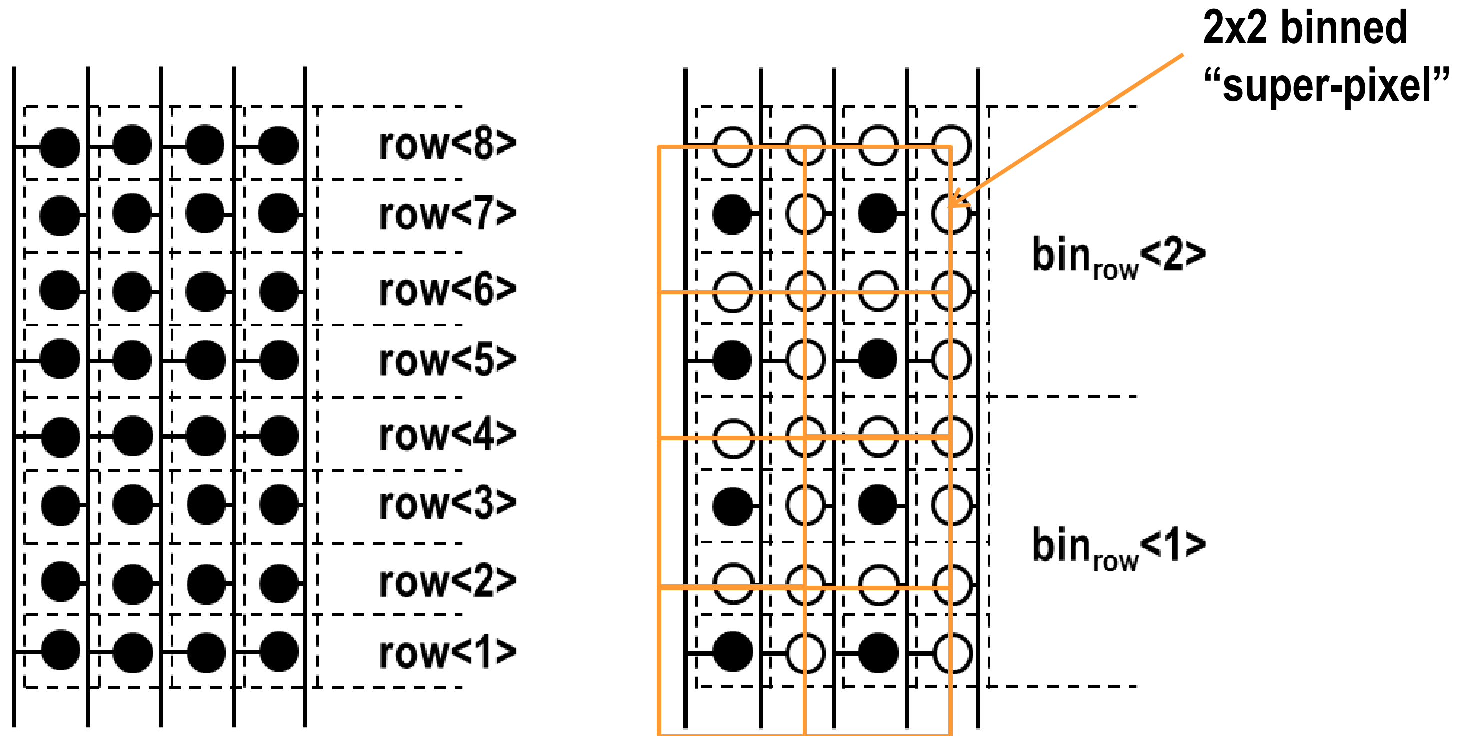
Pixel Schematic



- Programmable Full well capacity (row individual)
- Integrate while Read (IWR) snapshot shutter
- Correlated Double Sampling readout with IWR snapshot shutter functionality

Pixel Schematic Supports Low Noise Readout for < 100 nsec Integration Time Windows

2x2 Charge Domain Binning



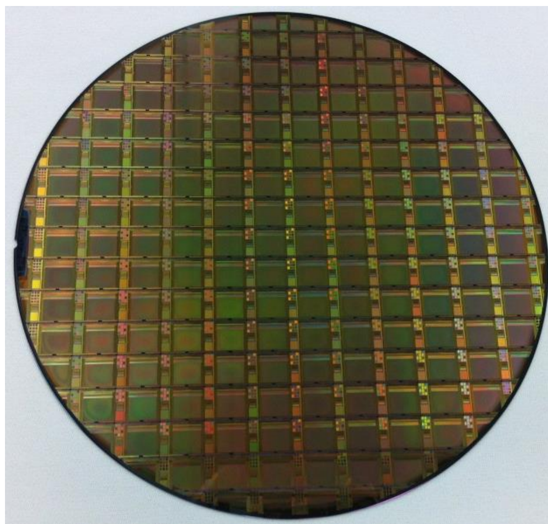
- **Potential well of charge collecting junction is turned off in skipped pixels (white circles)**

SNR Increase in Readout Noise Limited Domain: 4x → Same as CCDs

Frame Rate Increase: 4x → 2x Faster than CCDs

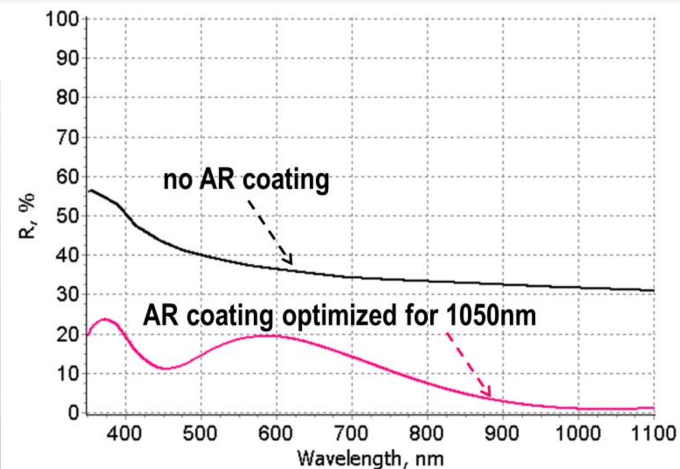
Sensor Creations

Backside Processing of 640x 512 Imager



High rho silicon wafer with completed CMOS process

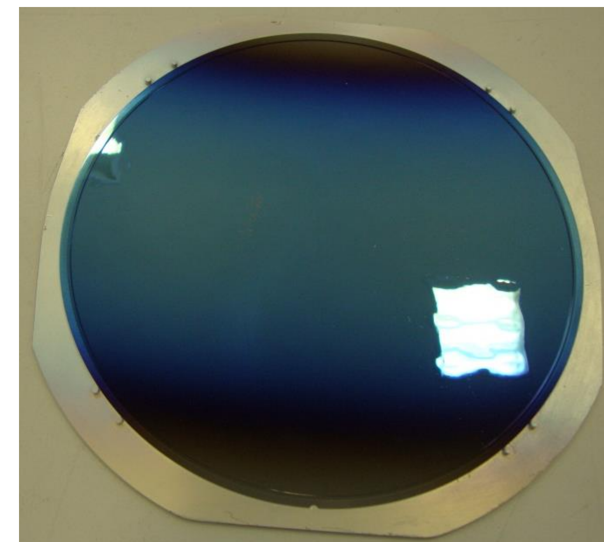
Wafer thinned to 50um



Thin film simulation of AR coating

Backside Process defines Optoelectronic Device Characteristics and can be Optimized for Different Applications

in-house backside processing



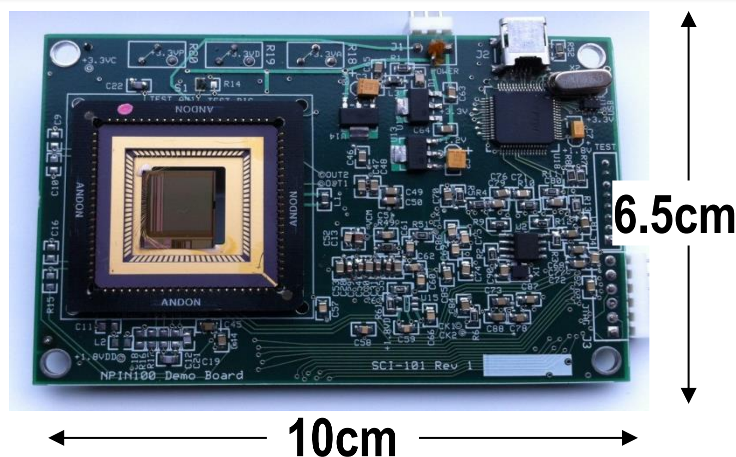
50um thick wafer with AR coating

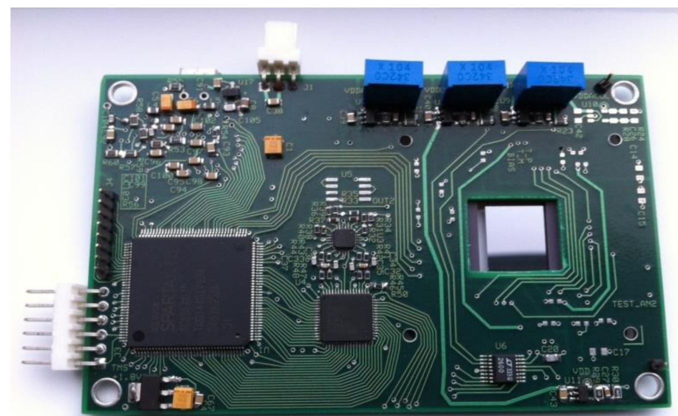
Sensor Creations

In-House Characterization, Test and Packaging

8” wafer probe station

Manual Ball Bonder





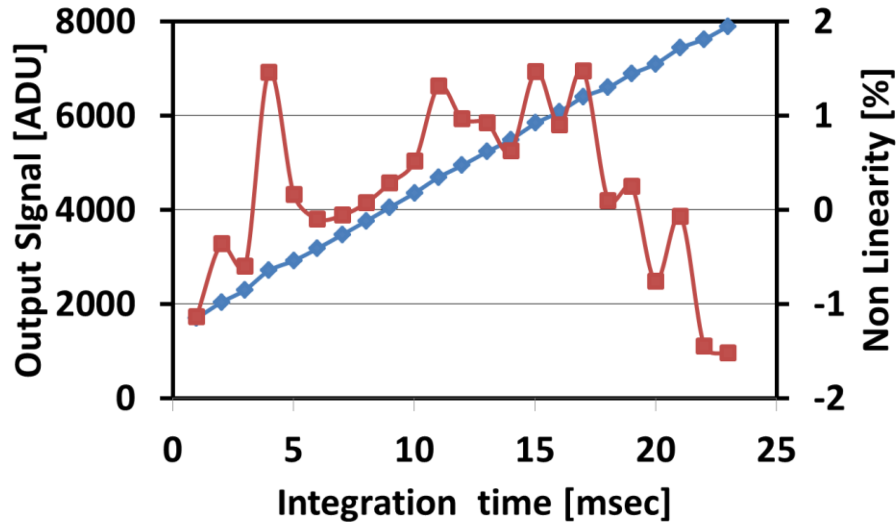
Front- and back-side of evaluation board for BSI Imager

- Probe station
  - Dark current characterization
- Packaged test structures
  - QE measurement
- Test boards
  - Camera operation

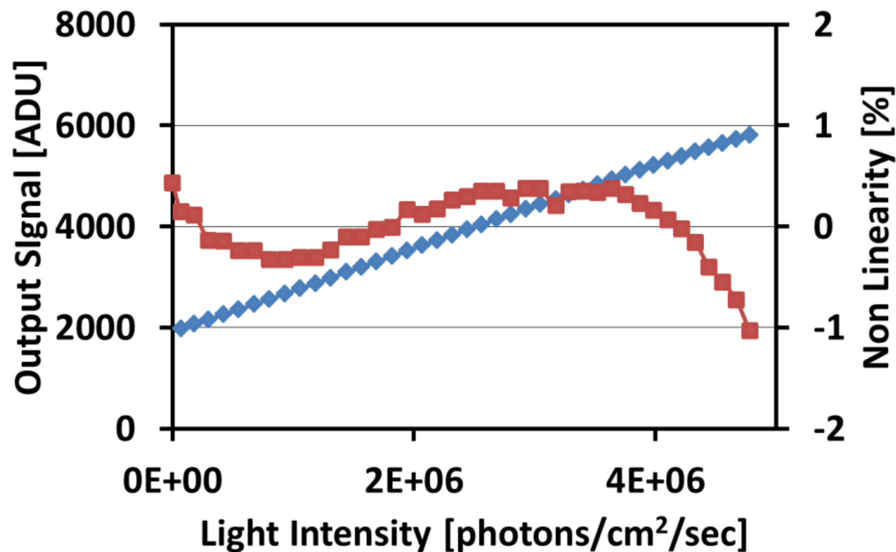
In-house test capabilities critical for efficient development of new sensor technology

Sensor Creations

Linearity in Mid Gain



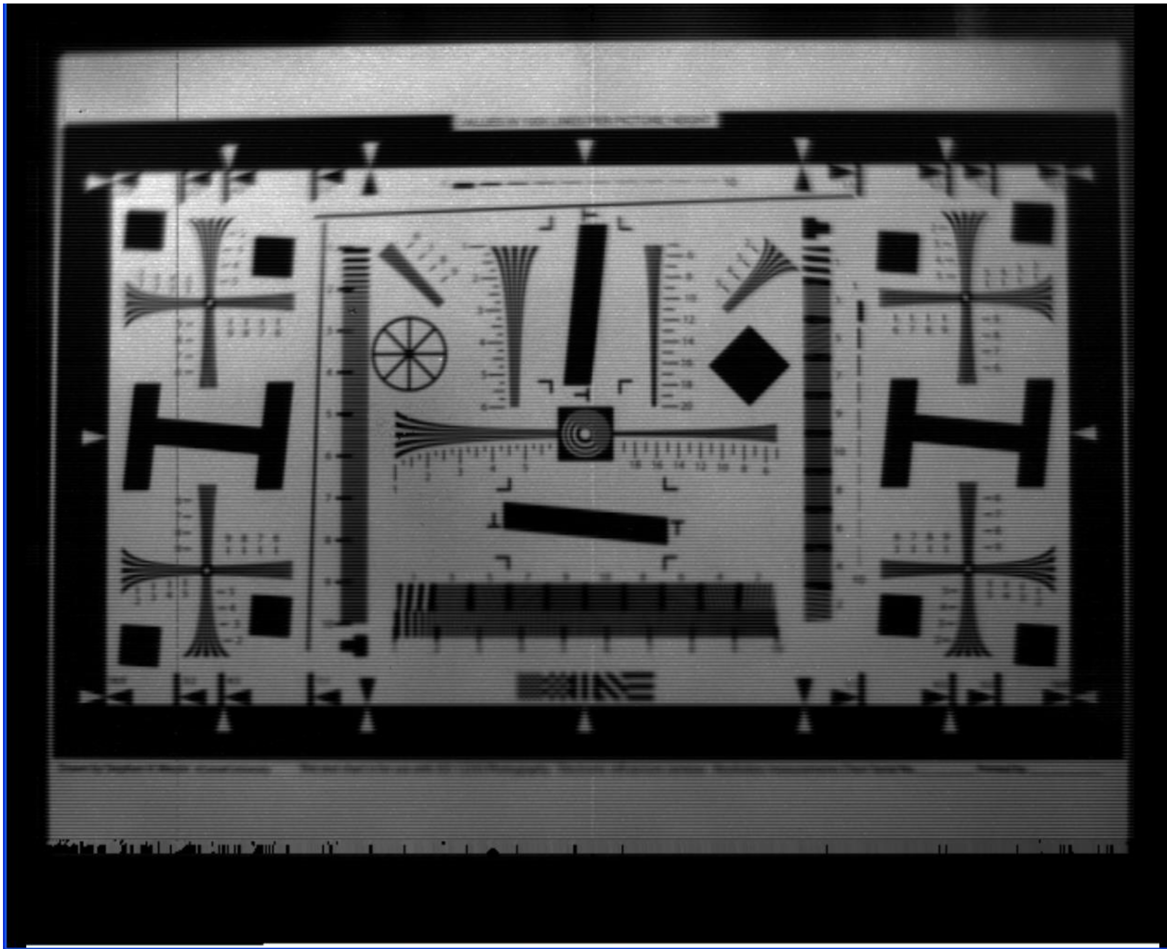
- **Wavelength:** 940 nm
- **FWC:** 60,000 e^-
- **Gain:** ~0.102 ADU/e^-



Linearity is < +/- 2%

… which is standard for a floating diffusion type pixel

First Images, 50um thick sensor – Example 1



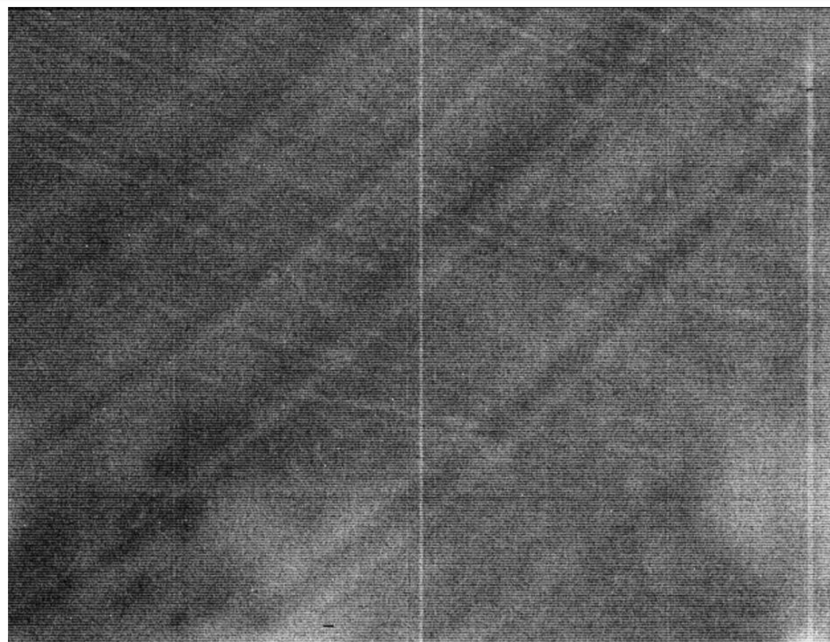
- Correction : 2 point NUC
- Integration time: 15.11 msec (66Hz frame rate)
- F/#: 5.6

Sensor Creations

First Images, 50um thick sensor – Example 2

- Correction : 1 point NUC
- Illumination: : ambient office (incandescent) light
- Integration time : 10msec
- Lens has NIR cut-on filter at ~900nm

Phenomenon in Deep Depletion Silicon Sensors



- **Curved line pattern under flat field illumination**
  - **Reported before in deep depletion CCDs → tree rings**
    - **Steve Holland et al., LBNL**
- **Caused by inhomogeneity in silicon resistivity during crystal growth**
  - **Phenomenon in all deep depletion sensors**

Tree Rings Disappear when Reverse Bias is Increased

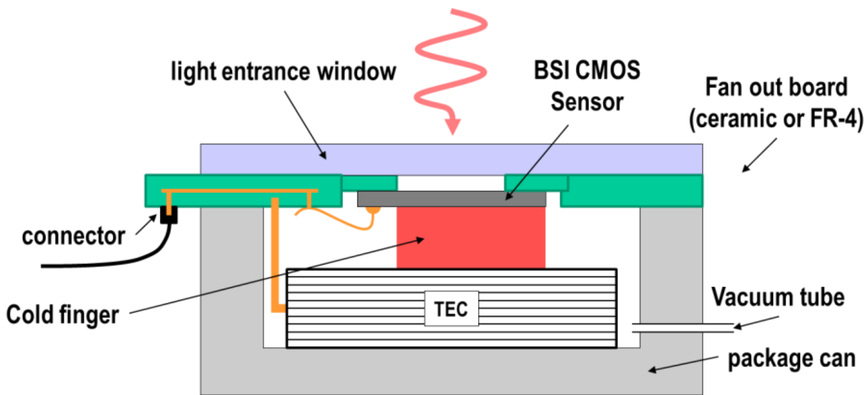
Sensor Creations

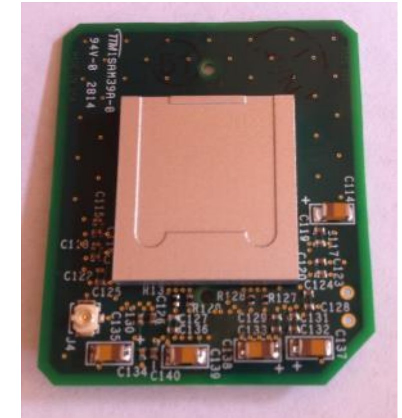
Summary of Specifications

Parameter	Value
Array Format	640 X 512
Pixel Size	15 µm
Die Size	11.2 X 12.2 mm^2
Die Thickness	50 µm, 100 µm, 200 µm
Exposure time control	snapshot shutter: ITR, IWR, NDR
Charge Capacity	programmable
minimum	10k e^- (high gain)
medium	60k e^- (high gain)
maximum	500Ke (low gain)
Input Referred Noise	
high gain	$10e^-$
medium gain	$30e^-$
low gain	$130e^-$
Windowing	horizontal center to outsides, bottom to top
minimum	1 rows x 24 columns minium
increments	1 rows, 24 columns
Integration Time range	100nsec to 30 msec
Output	analog (through 1,2, 4 or 8 output ports)
Frame Rate	1000 Hz (when using all 8 output ports)
Output data rate	5MPixel/sec - 41MPixel/sec
Number of output channels	1, 2, 4 or 8 (programmable)
Master Clock	2.5 - 20.5 MHz
Binning	2x2, 2x1, 1x2
Power (120Hz, 60Hz, 30Hz)	60mW @ 60Hz frame rate
Supply voltage	3.3/1.8
Logic I/O levels	0.0V/3.3V
Serial Interface	3 wire (multiple long word of different length)
Operating Temperature	300K

Sensor Creations

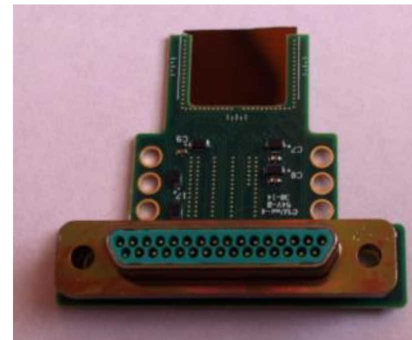
SCI Packaging Approach

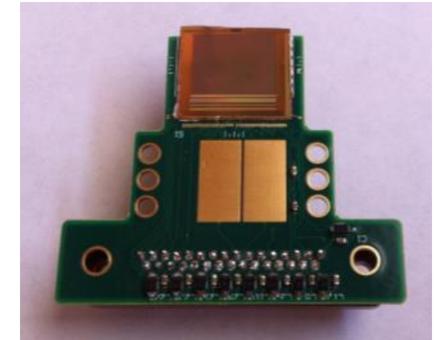




Package 1: Cold finger directly attached against CMOS circuits

- Wire bonding
- Chip on board
- Cold finger attached
  - Also guarantees planarity
- Backfill or vacuum seal
  - With ceramic board



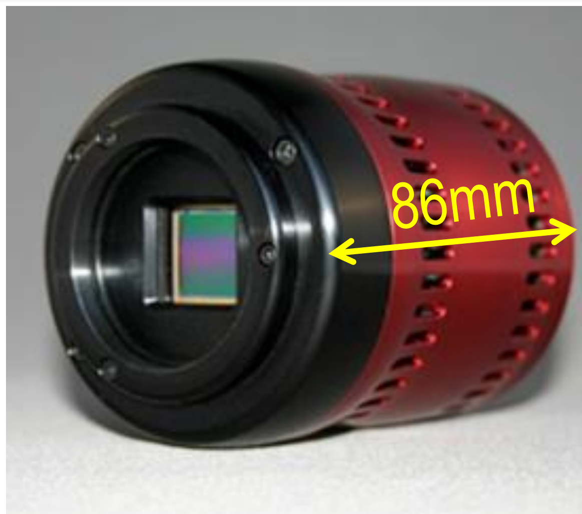


Package 2: Sensor freely suspended with support on sides only (⇒ only 50µm thick silicon membrane in beam path)

Low cost Package for High End Applications with Low Volume

Sensor Creations

SCI Deep Depletion BSI Camera



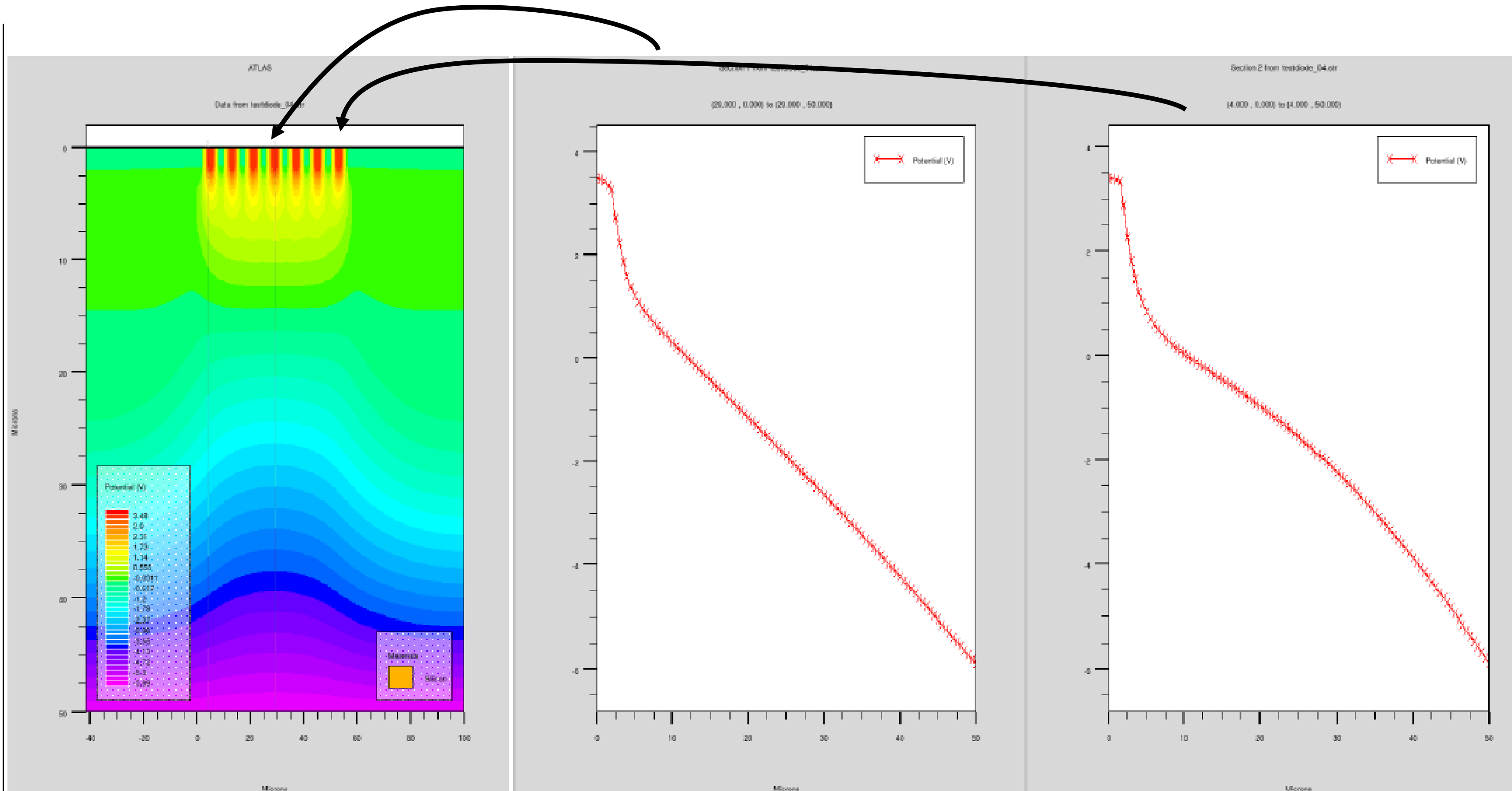
- GigE or WiFi Interface
- C- or F- mount
- CameraLink available upon request
- Internet browser for display and camera control
  - No driver installation required

Camera provides easy access to this new image sensor technology for early adopters

Sample image taken with this camera (raw data)

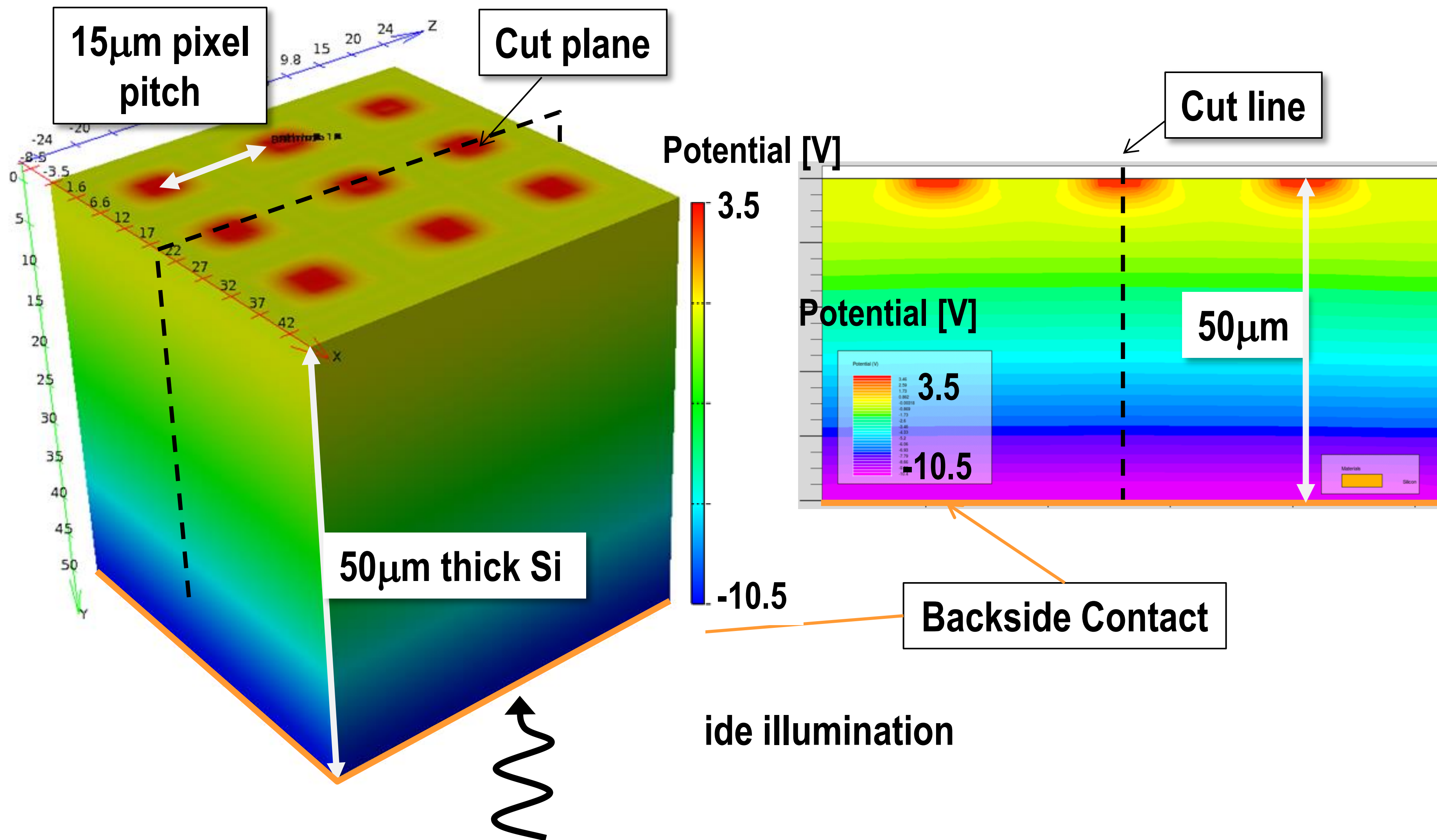
Thank You for your attention!

Potential Underneath 50 micron thick Photodiode Array



- **Full Depletion and Pixel isolation on front side achieved**

3D Simulation of FD CMOS Pixel on 6.5 kΩ x cm Si



3D Device Simulations were Used to Optimize Pixel Structure

Sensor Creations

Pixel Timing