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Chapter 1

Introduction

This document sets out the organisation, cost estimate and time schedule of the ALICE Muon Chambers (MCH) Detector, Muon Identifier Detector (MID), the Fast Interaction Trigger Detector (FIT) Upgrade, the common read-out ASIC SAMPA and the common read-out (CRU) Projects as described in the TDR (CERN-LHCC-2013-019, April 15, 2014).

Within the ALICE upgrade program two common hardware developments are pursued. The SAMPA detector read-out ASIC will be used by the MCH and the Time Projection Chamber (TPC). The common read-out unit (CRU) is a hardware read-out platform used TPC, MCH, MID, Inner Tracking System (ITS), Zero Degree Calorimeter (ZDC) and Transition radiation detector (TRD).

Chapter 1 describes the MCH, chapter 2 the MID, chapter 3 the SAMPA ASIC, chapter 4 the CRU and chapter 5 the FIT. All chapters are organised in a similar manner where section 2 lists the participating institutes and shows the organisational chart for the management of the corresponding Upgrade Project. Section 3 provides explanations and justifications of cost estimates for the main cost items. The work breakdown structure (WBS) of the Upgrade projects is explained in detail in section 4, starting with an overview of all cost items and a responsibility chart for the allocation of funding. Then, for each level 1 cost item, details of the cost estimates are given in summary tables together with explanations of the underlying basis for

estimates. Section 5 describes the resource loaded schedule and section 6 deals with the manpower requirements necessary for the execution of the corresponding upgrade projects. An evaluation of the most relevant project risks is given in section 7.

Chapter 2

Muon Chambers - MCH

2.1 Project Organisation

The MCH Project Leader (PL) heads the Muon Chamber Project. He/she is assisted by the MCH Deputy Project Leader (DPL) and the MCH Technical Coordinator (TC). The MCH PL, DPL and TC are all members of the ALICE Technical Board and thus can assure the coherence of this project within the ALICE experiment in general. Issues of a financial, managerial and organizational nature are discussed and decided by the MCH Institute Board. This board also endorses technical matters recommended by the MCH Technical Board (see below) and proposed by the MCH Project Leader or Deputy Project Leader. All Institutes participating in the MCH Upgrade Project, shown in Tab. 2.1, are represented by their Team Leader in the Institute Board. The Project Leader, Deputy Project Leader and Technical Coordinator are ex-officio members of the Institute Board.

As shown in Fig. 2.1, the MCH Upgrade Project is organised into xx Work Packages. The Work Package Coordinators are nominated by the Project Leader and endorsed by the MCH Institute Board. They are members of the MCH Coordination Board. The Project Leader, Deputy Project leader and Technical Coordinator are ex-officio members of the ITS Coordination Board. Other scientists with dedicated technical expertise are also nominated “ad personam” by the PL to be members of the MCH Coordination Board.

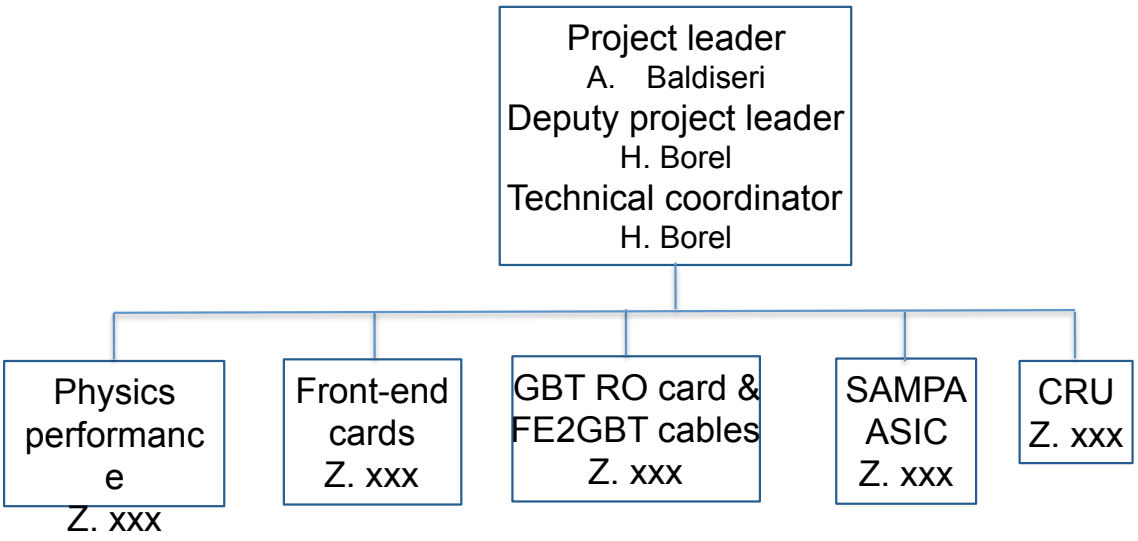

Figure 2.1: The MCH Coordination board.

Country	City	Institute
France	Eurodisney	Walt Disney
Austria	Nordpol	Christmas

Table 2.1: Institutes participating in the MCH Upgrade Project.

2.2 Budget Explanation and Justification

This chapter addresses important design choices and their possible impact on the project cost and schedule.

2.2.1 GBT Read-out card and existing infrastructure

In order to minimise the overall upgrade effort on development and cost the MCH upgrade design is designed to reuse the existing chamber design including the infrastructure such as data transmission via printed circuit boards and data cables, cooling, mechanics and power supply systems. These considerations have been taken into account for the front-end electronics data interface, power consumption and the the on-detector read-out architecture. As a result the front-end cards are designed to be compatible with the existing infrastructure. The MCH read-out architecture follows the ALICE common approach shared with a majority of upgraded detectors. The standardised front-end links use the versatile link and GBT components. This

optical and electrical, redaction tolerant serial transmission link set is developed by the CERN Electronics Design Group and is targeted are and the off-detector read-out

2.2.2 Front-end cards & SAMPA

The presently used front-end ASIC is inappropriate for the upgrade operation conditions due to the increased interaction rate. The same situation applies for the ALICE TPC front-end electronics. In order to reduce the overall effort the MCH and TPC projects develop a common read-out ASIC, called SAMPA. The differences in specifications, such as the different signal polarity and dynamic range are taken into account by the implementation of programmable parameters in the ASIC. For the MCH application the SAMPA specifications on noise or data bandwidth provide a comfortable margin.

2.2.3 Common Read-out Unit

The MCH detector upgrade design has adopted the ALICE common read-out architecture, which standardised the front-end links with versatile link and GBT components and offers common read-out units (CRU) to multiplex the data and provide a connection to the ALICE standard link to the online systems (DDL3) and the standardised timing and trigger distribution link (TTS). This approach reduces the overall development by benefiting from centralised versatile link component developments and the development of the common read-out unit used by a large number of upgraded ALICE detectors.

2.3 Cost Chart

Table **??** shows the Work Breakdown Structure (WBS) chart for MCH Upgrade Project. The tasks of the WBS have been broken down in xx level 1 subgroups

Activity	Material Cost	Manpower Cost	Total Cost/item
1. Front-end cards	**x**	**x**	**xx**
1.1. Design & Prototyping	x	x	xx
1.1. Qualification	x	x	xx
1.2. Production	x	x	xx
1.2. Test	x	x	xx
1.2. Installation	x	x	xx
2. SAMPA ASIC	**x**	**x**	**xx**
3. GBT Read-out Cards	**x**	**x**	**xx**
3.1. Qualification	x	x	xx
3.2. Production	x	x	xx
3.2. Test	x	x	xx
3.2. Installation	x	x	xx

Table 2.2: Cost breakdown structure of the ALICE MCH upgrade, divided into material cost and cost for externally hired manpower.

Table 2.3: Exchange rates used in the cost estimates.

1 EUR	1.23 CHF
1 USD	0.9 CHF

referring to either main detector subcomponents or to the most essential parts and services foreseen to be installed in the MCH.

Cost estimates are provided for each level 2 task and are understood as to be CORE costs, including detector components and production costs, as well as industrial or outsourced manpower for production, but not costs for personnel and basic infrastructures of the participating institutes. In addition, costs for R&D are not included in the estimate. The aforementioned cost for outsourced manpower has been estimated with 100 kCHF per man year (220 working days). All estimates based on offers or quotes in foreign currency have been converted into Swiss francs using the exchange rates of February 2014 (cf. Table 3.3).

More detailed information on the cost estimate for the level 1 items are given in the following sections. The expected spending profile, based on the detailed cost estimates and the project planning, is shown in Fig. **??**. Figures **??** and **??** finally show the cost breakdown structure together with the expected funding contributions.

Year	2014	2015	2016	2017	2018	2019
Spending [kCHF]	xx	xx	xx	xx	xx	xx

Table 2.4: Expected spending profile for the ALICE MCH upgrade.

Activity	Country or Inst	Country or Inst	Country or Inst
1. Front-end cards	**x**	**x**	**xx**
1.1. Design & Prototyping	x	x	xx
1.1. Qualification	x	x	xx
1.2. Production	x	x	xx
1.2. Test	x	x	xx
1.2. Installation	x	x	xx
2. SAMPA ASIC	**x**	**x**	**xx**
3. GBT Read-out Cards	**x**	**x**	**xx**
3.1. Qualification	x	x	xx
3.2. Production	x	x	xx
3.2. Test	x	x	xx
3.2. Installation	x	x	xx

Table 2.5: Cost breakdown structure of the ALICE MCH upgrade, including expected funding from the different contributors.

	#FEC	**x% Spares**	**Total**
Station 1	xx	xx	xx
Station 2	xx	xx	xx
Station 3	xx	xx	xx
Station 4	xx	xx	xx
Station 5	xx	xx	xx
Total	xx	xx	xx

Table 2.6: Quantities of Front-end cards needed for the different detector parts.

	#ROC	x% Spares	Total
Station 1	xx	xx	xx
Station 2	xx	xx	xx
Station 3	xx	xx	xx
Station 4	xx	xx	xx
Station 5	xx	xx	xx
Total	xx	xx	xx

Table 2.7: Quantities of GBT read-out cards needed for the different detector parts.

	#SAMPA	x% Spares	Total
Station 1	xx	xx	xx
Station 2	xx	xx	xx
Station 3	xx	xx	xx
Station 4	xx	xx	xx
Station 5	xx	xx	xx
Total	xx	xx	xx

Table 2.8: Quantities of SAMPA ASICs needed for the different detector parts.

2.3.1 Front-end cards

2.3.2 GBT read-out cards

2.3.3 Front-end cables (FE2GBT)

The unit prices are based on an offer by xx. Cables are standard, acceptance criteria,..

2.3.4 SAMPA

Section **??** deals is in detail with the SAMPA project. The cost estimate for the SAMPA is based on 33000 SAMPA plus 10% spares for a total of 37000 ASICs. Table **??** gives an overview of the quantity of chips needed for the MCH stations. It is planned to build 10% spare ASICs. If a production yield of 70% is assumed, this results in a number of 53000 ASICs to be produced. The number of chips per wafer is approximately xx, which leads to a number of xx wafers. Section **??** shows the cost estimate for the SAMPA ASIC manufacturing, packaging and testing.

2.3.5 Common read-out unit

number of channel calculation

2.3.6 fiber installation

2.3.7 Power Distribution and Cooling

old stuff reused

2.3.8 Detector Control System

2.4 Schedule

Microsoft Project or similar.

2.5 Man Power

The estimated manpower available in the collaboration institutes, which is needed for the different activities, is shown in Fig. **??**. The numbers are divided into physicists (PH), mechanical engineers (ME) and technicians (MT), electronics engineers (EE) and technicians (ET) and others (OT). The manpower available from the different participating institutes is shown in Fig. **??**.

2.6 Risk Register

SAMPA otherwise technically no risk

SAMPA :
see section @.

Activity	Contact Person	PH	EE	ET	Ot
1. Front-end cards	**x**	**x**	**xx**	**xx**	**xx**
1.1. Design & Prototyping	x	x	x	x	x
1.1. Qualification	x	x	x	x	x
1.2. Production	x	x	x	x	x
1.2. Test	x	x	x	x	x
1.2. Installation	x	x	x	x	x
2. SAMPA ASIC	**x**	**x**	**xx**	**xx**	**xx**
3. GBT Read-out Cards	**x**	**x**	**xx**	**xx**	**xx**
3.1. Qualification	x	x	x	x	x
3.2. Production	x	x	x	x	x
3.2. Test	x	x	x	x	x
3.2. Installation	x	x	x	x	x
Total	**x**	**x**	**xx**	**xx**	**xx**

Table 2.9: Available man power per institute and year.

Funding risks:

General schedule risks

SAMPA, 17000 Front-end card production & test.

Chapter 3

SAMPA

3.1 Project Organisation

The organization of the SAMPA project reflects the close relation between physicists and engineers that is necessary in order to successfully achieve the new ASIC that will be able to respond to the demands of the ALICE experiment after LS2. It also reflects the several tasks that need to be accomplished in order to reach this goal. The leadership is shared by a engineer (W. A. M. Van Noije) and two physicists (M. G. Munhoz and M. Bregant) from Universidade de São Paulo, Brazil. Figure 3.1 shows the organizational structure of the SAMPA project with all tasks and the contact people for each of them. Table 3.1 shows the institutions that are participating in the SAMPA project.

Country	City	Institute
Brazil	São Paulo	Instituto de Física da Universidade de São Paulo
Brazil	São Paulo	Escola de Politécnica da Universidade de São Paulo
Brazil	Campinas	Universidade Estadual de Campinas
Norway	Oslo	University of Oslo
Norway	Bergen	University of Bergen
France	Paris	Centre d'Etudes de Saclay
Italy	Cagliari	Universita degli Studi di Cagliari
Sweden	Lund	Lunds University

Table 3.1: Institutes participating in the SAMPA Upgrade Project.

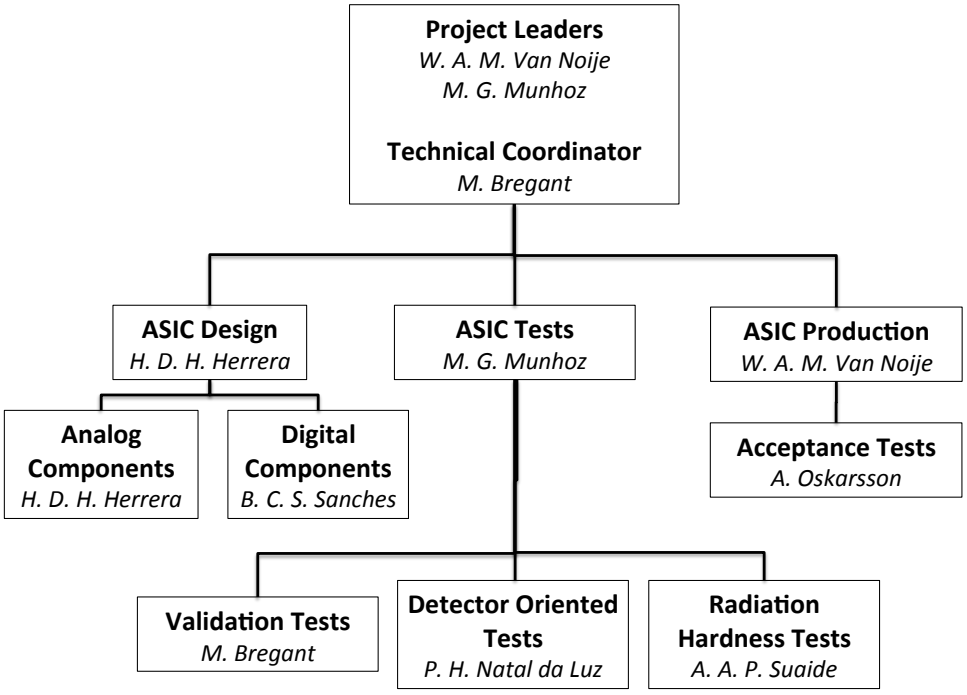

Figure 3.1: The SAMPA organization structure with the contact persons.

3.2 Budget Explanation and Justification

This section presents the costs of the SAMPA production divided in the several components of the project.

3.2.1 ASIC Design

Prototyping runs of Multi-Wafer Prototypes (MPW) is a powerful tool during the design process of a ASIC. It allows to perform tests on several choices and solutions adopted during the chip design in order to achieve the best result for the final object. In this project, 3 MPW runs are foreseen in order to solve all the challenges involved in the SAMPA design. The first prototype is aimed to study the basic principles of the chip. It will consist of 3 main blocks, where the first block is composed of 5 front-ends circuits (analog circuit and shaper PASA) and the bias circuit; the second block will consist of 10-bit ADC and a special differential digital driver that allows the output operating at 320 Mbit/s; a third block with 3 complete front-end channels (PASA, Shaper, ADC and bias circuit) and the DSP (Digital Signal Processor) circuit, i.e., almost three full channels of the TPC (only an additional memory unit for each channel will be missing).

The second MPW aims a full chip with 32 channels very close to the final one. It will allow a very detailed test of the SAMPA chip before fabrication. A third MPW is basically a contingency of the project foreseen just in case major changes in the chip design become necessary as a result of the tests performed after the second round.

3.2.2 ASIC Tests

Validation Tests

The SAMPA chip design and production presents several challenging points, like the addition of a high sensitivity/low noise amplifier and the Digital Signal Processor

in the same die. An accurate evaluation of all the main parameters is required to validate the chip performance before its usage in the ALICE experiment. The proper measure and evaluation of a ASIC chip which includes the evaluation and validation of pre-amplifier, shaper, ADC and digital signal processing represents a challenge for itself. An ad hoc test system will be developed and it represents a core part of the project. The test system will allow to power, program, inject signals, read out and access all the registers, buffer, and memories.

A low noise test system, which includes custom design electronics cards and high performance laboratory instrumentation, will be constructed. This system will consist of two boards in order to emulate the final ALICE electronics approach. The first board will support the chip and the necessary structures to power, input and output the signals. A second board will consist of a commercial FPGA that will control all the chip functions, emulating the future ALICE CRU (Common Readout Unit).

The main goal of such test system is to give access to all the main parameters that characterize the chip. The final aim is:

- to be able to completely evaluate the chip;
- to be able to use of the chip in long-term stability runs in order to evaluate the stability of the chip as well as the stability and performance of the system formed by the chip reading a detector (TPC and MCH chambers);
- to allow the test of the chip for radiation sensitivity. Since we are mainly concern in Single Event Effects, having the chip powered on and operational during the irradiation is a requirement;
- to measure with sufficient precision several parameters which are of capital importance for the chip integration with the TPC and MCH readout chains. Among these parameters wed like to stress the importance of the dynamical current absorption during data taking.

Detector Oriented Tests

The specification of the SAMPA chip defined a high performance chip, which is relatively general purposed. Nevertheless, the main goal of the SAMPA project is to provide a chip which permit to get the best performance in the ALICE detector (namely from TPC and MCH). For this reason, it is very important to test the chip with realistic signals, i.e., those coming from a real detector, since the early stages of the MPW prototypes. Therefore, a test setup that includes GEM prototypes and MCH chambers are forseen. The full-time availability of a real detector will allow a true understanding of possible interplay between chip and the detectors.

Radiation Tests

The establishment of radiation hardness assurance programs is a very important issue at the Large Hadron Collider (LHC), as the number of collisions generated is very large and part of the signal and data processing electronics is located on the sensors to maximize signal to noise and to reduce the size of cables. For the radiation hardness assurance of electronics components, radiation tests need to be performed to address the different effects. In this case, the use of radiation testing facilities is necessary. When performing radiation hardness tests it is very important to adopt well defined procedures, as it is difficult to reproduce the real time dependence of the damage during the irradiation. Usually the total dose expected to irradiate the sensors during their life time is deposited in a short period, which can be even more damaging. It is important to mention that no radiation hard structure will be used in the SAMPA chip due to international agreements. Our aim is only to test whether the regular structures are tolerant to the level of radiation present in the ALICE experiment.

The radiation tolerance tests for the SAMPA chip represent a major challenge given the complexity of the device. The mixture of analog with digital components demands very complex tests since there is the possibility of the occurrence of different effects simultaneously. The first step in order to perform these tests corresponds

to a detailed knowledge about the environment where the ASIC will be mounted . Calculations that take into account recent measurements of multiplicity in pp collisions, PbPb and pPb were performed to estimate the levels of radiation expected in the ALICE detector that electronic components are exposed. Fluency in terms of 1 MeV neutrons (1 MeV neutron equivalent - NEQ) and TID are the main quantities that must be considered to assess radiation damage in the long term for the detectors and the electronics. The TPC electronics should receive a dose of 2.1 and 3.4 krad kHz/cm2 of high energy hadrons . For the MCH, radiation levels are similar. Therefore , these numbers can be used to guide the radiation tolerance tests for the SAMPA chip .

These tests will be carried out basically in two steps :

- The first tests will be conducted at the Open Laboratory of Nuclear Physics (*Laboratório Aberto de Físic a Nuclear* - LAFN) from University of São Paulo and Laboratory of Medical Physics from the Institute of Physics Gleb Wataghin (IFGW) at State University of Campinas. Proton and heavy ion beams in the LAFN and X - rays of high intensity in IFGW will be used. A multi-purpose scattering chamber of 1 m in diameter located in the experimental area of the LAFN will be used. The device under test (DUT) is initially placed in air without encapsulation. Special flanges will be constructed to allow the beam passage outside the chamber. In order to better control the flow, the DUT will be placed at a given angle to the proton beam that hits a thick target of Au (approximately $1 mg/cm^2$) . Since the scattering cross section is well known, the flow of protons in the DUT can be calculated and hence the dose.

- In a second step, tests with high-energy protons (above 100 MeV) in a European laboratory, as Svedberg Laboratory (TSL) in Uppsala , Sweden will be performed. These tests will serve mainly to study Single Event Effects.

3.2.3 Production

In terms of cost, the production can be divided in an engineering phase and a construction phase. The SAMPA chip will be produced by TSMC (Taiwan Semiconductor Manufactory Company) in the 130nm CMOS technology that was evaluated as the best cost/benefit balance. In order to supply the ALICE experiment needs, 56.000 chips must be produced. Assuming a conservative yield of 70%, 80.000 chips will be produced. The SAMPA production will use 8-inches wafer, and since SAMPA size is estimate to be $90mm^2$, about 280 chip will fit in one wafer. The production of 80000 chip will therefore require making about 285 wafers. The production of the masks for the chosen technology costs about 275kUSD, while the production of each wafer will then cost about 1.5kUSD (see table 3.2 for the full cost figure). For this reason, the production will be split in two runs. First the engineering run (pre-production) where just 12 wafers will be produced in order to fully validate the process and the mask (masks are different between MPWs and production, even if no single detail is modified in the chip design). Once these mini-batch has been verified, the second batch with the mass production of remaining 270 wafer will start.

The reasonable yield (better than 70%), the small number of wafers, and the high number of pins of the chips make the test of the chips on the wafer economically not convenient. Indeed the cost of setting up such a test (including the fabrication of the probe cards) will be significantly higher than packaging, without doing any preliminary test, all the produced chips including the 30% of chips that will not be validated in the final test (see next section). In addition it should be considered that some chips are damaged during the cut, bonding, and packaging processes, and they represent a fraction not negligible of the not working chips.

Acceptance Tests

The SAMPA chip will be installed in the Front End Electronics (FEE) board of the ALICE detectors, namely TPC and MCH. Given the complexity involved, the

replacement of a defective chip once it is already mounted on the FEE, even if feasible, is not the most preferable option. In addition, it is well known that chip production is characterized by an intrinsic spread of the parameters, due to the natural variations in the processes. Therefore, a complete test and characterization of each single chip is necessary. The aim of such a complete and exhaustive test will allow the certification of good chips and their classification in groups with uniform characteristics (especially in terms of gain).

The accessible quantities for the (final) chip testing are:

- Static and dynamic power consumption, for each power domain;
- Working on all the possible configuration;
- Noise, gain and dynamical range of the full chain;
- Correct operation of the DSP unit;
- Integrity of register, memories and buffers;
- Correct operation of the communication unit.

The total number of required chips counts for more than 56.000 certified good chips, which in the hypothesis of a 70% yield, requires testing at least 80.000 chips. This amount of pieces calls for a fast and full automatic test, where the human intervention is very reduced. The number and the sequence of the tests should be optimized to allow a complete evaluation of the chip in the shortest time. One key point of the test procedure is the definition of the criteria that should be used to define a chip as good or as rejected. In first approximation a simple threshold and/or an interval of allowed values would be sufficient for the tests involving the power consumption, while the evaluation of the quality of a channel (full chain) for sure will require a more complete set of variable.

At the moment, two possibilities are being considered: a test in the company that will build the chips and a test performed within an ALICE collaboration institute.

The test of each single chip in a company will require to fully define a set of automatic test and the list of acceptance criteria before the mass production starts. The chip is a heavily dedicated object, for a very peculiar application. That makes it (quite) different from the usual consumer or b2b (industrial) electronics. Therefore, also for its characterization, some kind of test are not commonly in use and the protocol of measurement and result interpretation should still be developed. In this context, the in-house option looks preferable, since it allows refining the protocol in a interactive way. In addition, making the complete test in an external company will make more difficult to trace and log the full chip history (including the complete outcome of the test measurements) in the unified ALICE detector database. Therefore, the tests in a external company is considered a contingency in the SAMPA project, but it will included in the core budget.

3.3 Cost Chart

Table 3.2 shows the costs of each component of the SAMPA project in kCHF, both in terms of material cost and human resources that corresponds to fellowships (therefore it excludes salaries costs of the participating institutes). The funds for the ASIC design has already already been granted (335,00 kCHF) by the Brazilian funding agency FAPESP (*Fundação de Amparo à Pesquisa do Estado de São Paulo*). The project for the full production is currently in the submission phase for the same agency. The contingency of 20% is granted by the funding agency as default. The validation and detector oriented tests costs consist mainly of infrastructure. The radiation hardness test is mostly beam time cost while the acceptance test regards the TSMC test procedure cost.

The expected spending profile, based on the detailed cost estimates and the project planning, is shown in Table 3.4.

Activity	Material Cost	Manpower Cost	Total Cost
ASIC Design	**255,00**	**80,00**	**335,00**
Validation Tests	**75,00**	**45,00**	**120,00**
Detector Oriented Tests	**130,00**	**115,00**	**245,00**
Radiation Hardness Tests	**50,00**	**35,00**	**85,00**
Production - Engineering	**280,00**	**-**	**280,00**
Production - Construction	**465,00**	**-**	**465,00**
Acceptance Tests	**185,00**	**-**	**150,00**
Contingency (20%)	**365,00**	**-**	**365,00**

Table 3.2: Cost breakdown structure in kCHF of the ALICE SAMPA project, divided into material cost and cost for externally hired manpower.

Table 3.3: Exchange rates used in the cost estimates.

1 EUR	1.23 CHF
1 USD	0.9 CHF

3.4 Schedule

Figure 3.2 shows a Gantt chart with the schedule foreseen for each of the activities of the SAMPA project. This a 3 years project aiming the delivery of all chip units in the middle of 2016 in order to allow sufficient time for integration with the ALICE experiment.

3.5 Man Power

The estimated manpower available in the collaborating institutes, which is needed for the different activities through the years, is shown in Table 3.5. The number of physicists, engineers, post-docs and graduate students through the years is show in Table 3.6.

Year	2014	2015	2016
Spending [kCHF]	537,50	247,50	895,00

Table 3.4: Expected spending profile for the ALICE MCH upgrade.

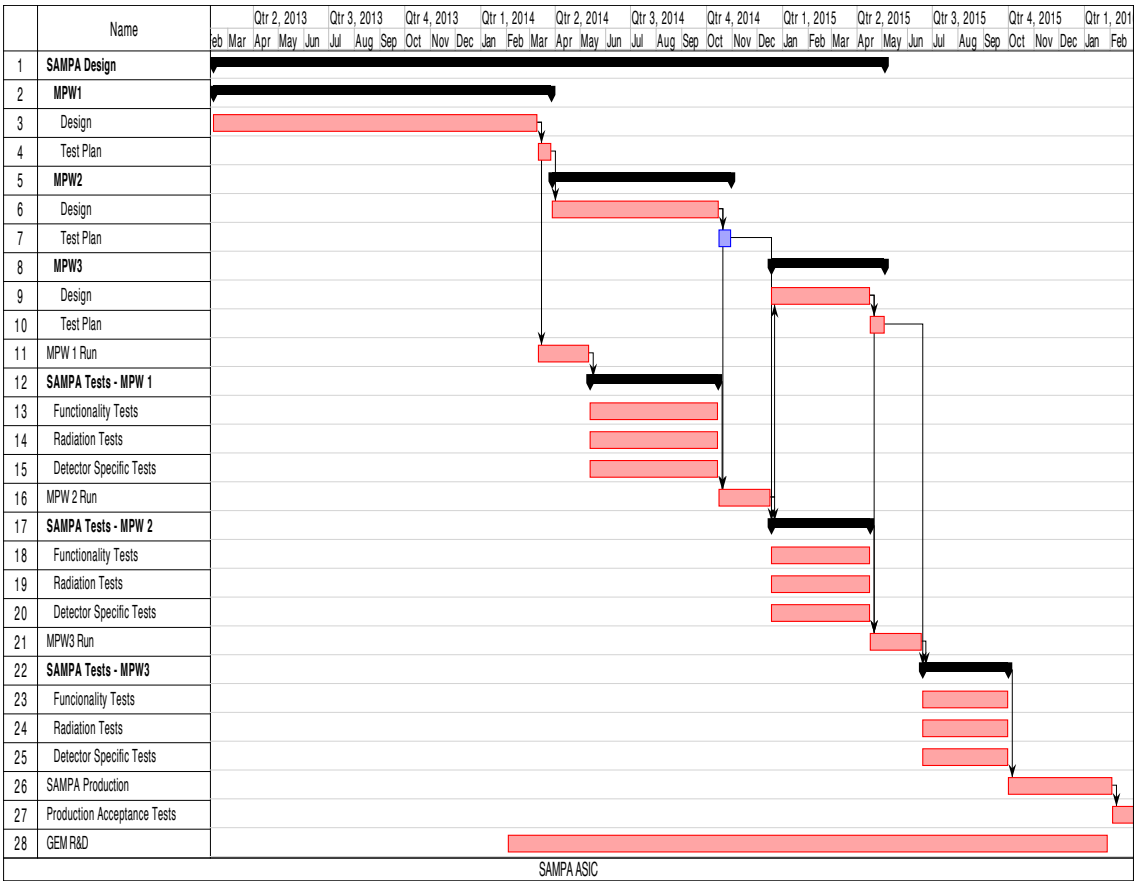

Figure 3.2: The SAMPA Time Table

Activity	2014	2015	2016
ASIC Design	**3.1**	**3.1**	**-**
Validation Tests	**2.8**	**1.5**	**-**
Detector Oriented Tests	**1.9**	**2.4**	**-**
Radiation Hardness Tests	**1.7**	**1.7**	**-**
Acceptance Tests	**-**	**-**	**2.8**

Table 3.5: Available man power in FTE per task and year.

Occupation	2014	2015	2016
Physicist	**1.8**	**1.8**	**1.7**
Engineer	**4.0**	**2.7**	**1.1**
Post-doc	**1.5**	**1.5**	**-**
Graduated Student	**1.9**	**2.4**	**-**

Table 3.6: Available man power in FTE per occupation and year.

3.6 Risk Register

Funding risks As mentioned before the funds for the ASIC design has already already been granted by the Brazilian funding agency FAPESP and the project for the full production is currently in the submission phase for the same agency. Its approval is very likely, but not guarantee. In the case of a denial of FAPESP, new sources of funding must be tried. A possibility would be the Brazilian national funding agency, CNPq (*Conselho Nacional de Desenvolvimento Científico e Tecnologógico*. The contingency included in the project should cover any additional prototype run (MPW) in case of any technical problem.

General schedule risks The schedule for the SAMPA design and production is relatively tight. There are mainly two type of risks:

- complete failure of one of the MPWs (either due to design or foundry problems) that could delay the project between 3 to 9 months, depending on the cause
- departure of one of the main designers. The project is well documented, nevertheless this would lead to a delay of at least 3 to 6 months