Data Acquisition System for HF Radiation Monitors

S. Dugad, T. Grassi, A. Kaminsky, S. Lokhandwala, R. Shukla

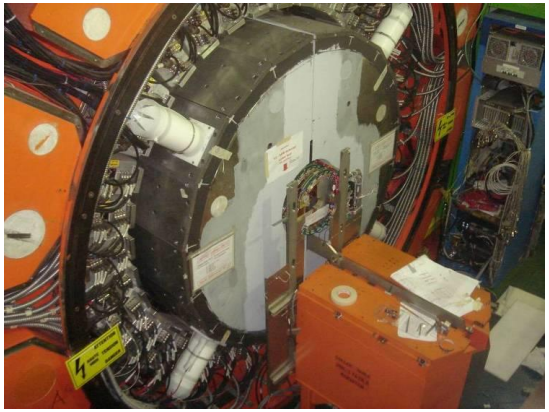
HF Radiation Monitors

❖ OBJECTIVE:

- Long term monitoring of the absorbed dose and neutron flux to estimate the expected degradation of fibers, electronics, PMTs and to measure the shielding efficiency.

- Additional monitoring of the HF itself performance for future re-calibration etc.

- Background (beam losses) monitoring.



System for a radiation monitoring in the CMS HF area

❖ CONTENTS:

- Introduction of HF Radiation Monitor Detectors
- Present System
- Proposal and requirements for upgrade
- Summary of components
- Firmware Development
- Course of action

*Ref: http://test-kaminsky.web.cern.ch/test-kaminsky/cooling_upg/HCAL/hcal/HF_RAMON_Safety.pptx

HF Radiation Monitors – neutron detectors (NRM-14)

16 neutron monitors: NRM-14 for neutron flux measurements

- 4x2 monitors inside every HF shielding
- 4x2 monitors outside every HF shielding

Physics properties	NRM-14 (neutrons)
Rank of measured energies	0.5eV… 15MeV
Measured parameter	Fluence (flux) rate
Rank of measured values	1e-2… 1e+5 n/(cm²/sec)
Sensitivity	1.3… 2.3 (n/cm²)/count
Isotropism	50%
Size (with capsule & moderator)	dia155x330 mm
Weight (with moderator)	5 kg

Power requirements	NRM-14
Power supply	20… 24 V
Current (DC)	<25 mA
Signal amplitude	70 mA
Pulse duration	0.5e-6 sec

Counters specification

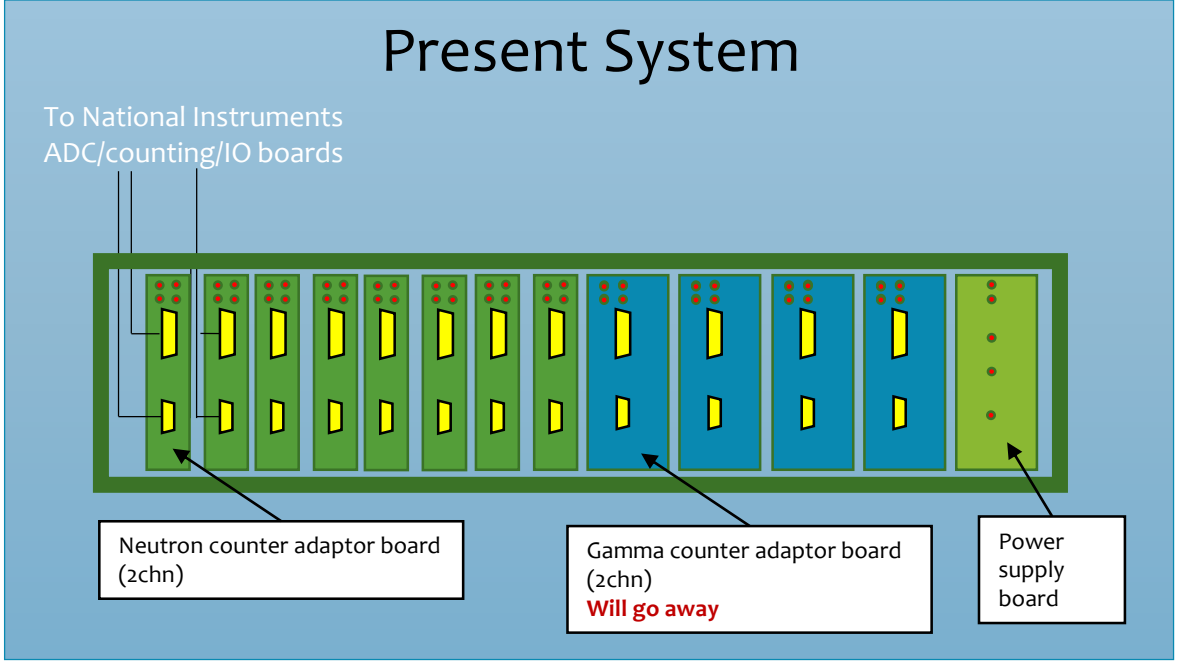
*Ref: http://test-kaminsky.web.cern.ch/test-kaminsky/cooling_upg/HCAL/hcal/HF_RAMON_Safety.pptx

Requirements of DAQ for monitoring of Neutron Counters

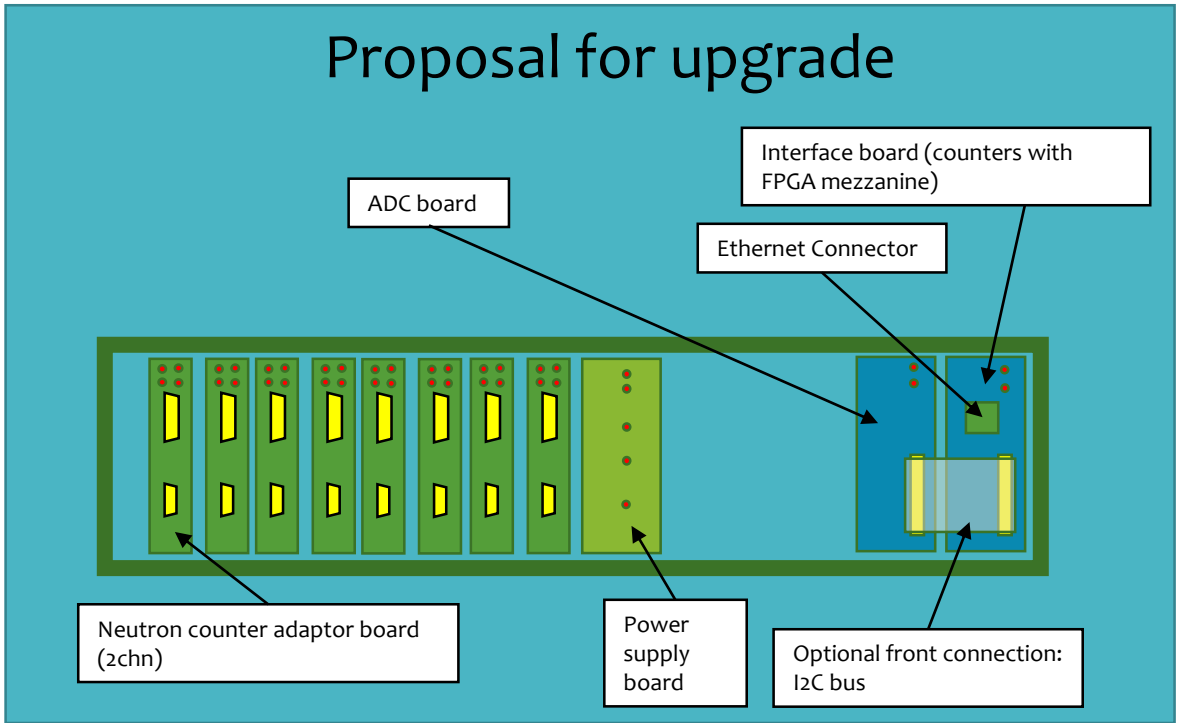
- 16 channels:
  - Control ON/OFF signaling (TTL)
  - 32-bit count of asynchronous pulses (TTL), rate 1MHz
  - Voltage and Current Monitoring (Range: 0-10V)
- Readout: Ethernet (low luminosity the readout rate : 1/10s, at high luminosity : 1/sec)

- ➢ Present system is monitored through NI-DAQ cards with PCI interface.
- ➢ PCI is phased out at CMS (moreover, NI cards are 5V PCI) and drivers are only 32bits.
- ➢ The new FPGA based system aims to provide more flexibility along with an Ethernet interface.

Present System



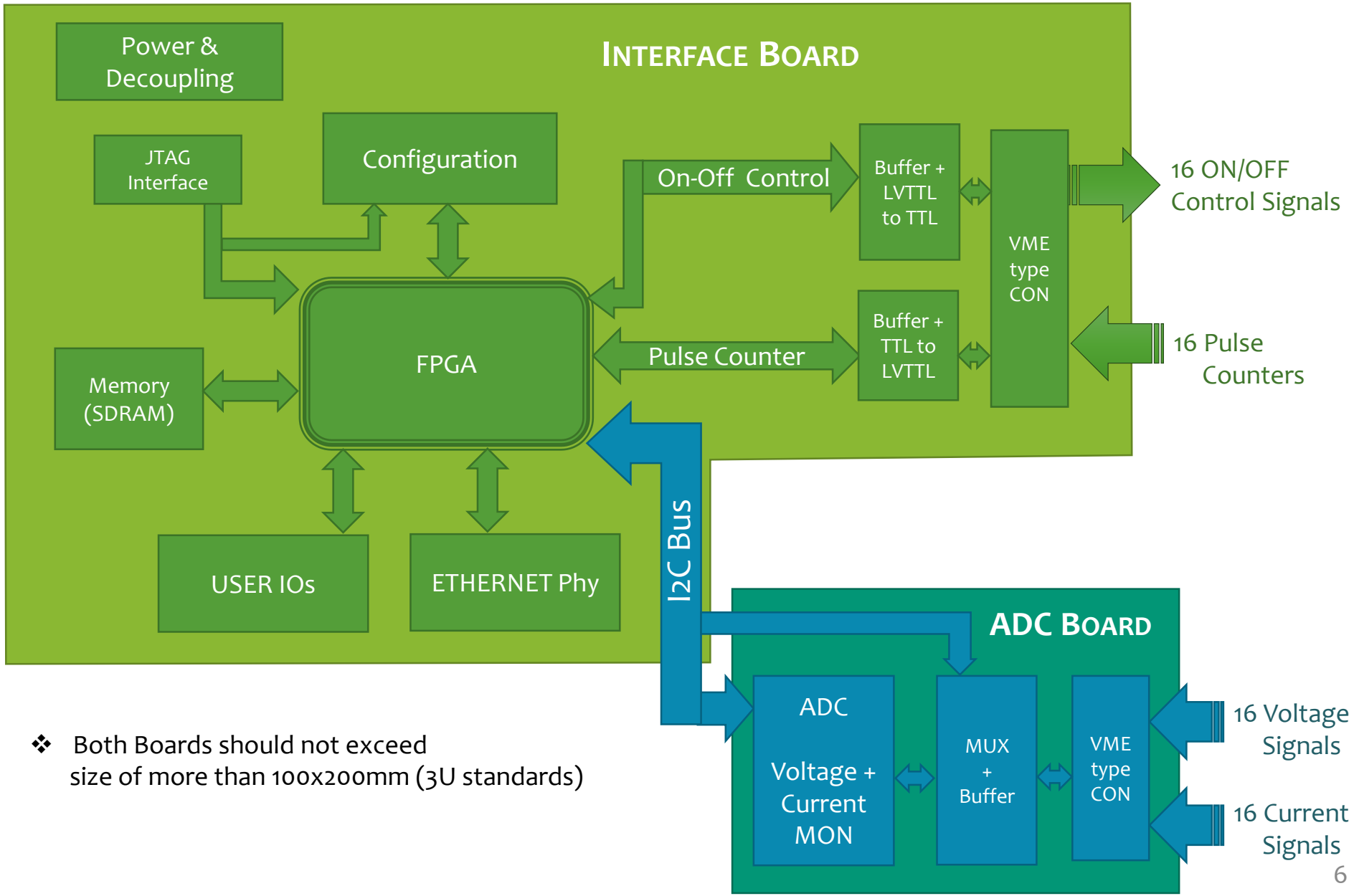
Proposal for upgrade



- Removal of Gamma counter boards frees 4 double slots in the crate. This allows us to place the new interface board(s) directly to the crate.
- Digital signals from/to neutron adaptor boards will be routed to new backplane board connector using single wires.
- Analog signals from neutron adaptor boards will be routed to new backplane board using single wires.
- ADC board is connected to Interface board via backplane lines (carrying I2C signals) (optionally: by the flat cable)

*Ref: http://test-kaminsky.web.cern.ch/test-kaminsky/cooling_upg/hfradmon/NR_HFRM_2.pptx

Block Diagram of Proposed DAQ



- Both Boards should not exceed size of more than 100x200mm (3U standards)

Interface Board: Summary of Components

Components specifications:

- FPGA : **Xilinx SPARTAN 6 LX16**
- Flash PROM:
  - **XCF04S**: 4M-bit Platform FLASH PROM *(Xilinx Recommended)* and/or
  - **NP5Q128A**: 128-Mbit, Phase Change Memory (PCM) with 66MHz SPI Bus Interface
- Ethernet LAN Phy: **LXT971A**: MII interface, 10/100 Ethernet Transceiver
- Digital Buffers: **74LVC245**: 8-channel TTL-LVTLL Buffer, Propagation time: 4ns
- Power Modules for FPGA : 3.3V, 2.5V, 1.8V, 1.2V (Linear Technologies: **LTC3633, LTC3619**)
- Connectors:
  - **VME based** for backplane connection : 96 contact connectors (ERNI 533402)
  - Ethernet : **RJ-45 with Magnetics** : HALO Electronics HFJ11-2450E-L12
  - I^2C Header
  - GPIO Connector
- SDRAM: ISSI's **IS42S16160G**: 16Mx16bits (256Mbit), up to 166MHz clock. .
- I^2C Buffer: **P82B96**: I^2C -bus logic signals levels convertor, improves noise immunity on longer bus lengths.

ADC Board: Summary of Components

- ***Requirements:***

  Each of 16 neutron adapters produces 2 analog signals: "detector voltage" and "detector current".
  - Both signals are voltages in range 0 to 7 volts, output resistance ~kΩ
  - ADC accuracy should be not worse then 0.1 V

  The need for separate ADC board is mainly due to arrangement of connections from the backplane.

- ***Components specifications:***

  - ADC: **MAX127** : 8-channel, 12-bit SAR-ADC, +10V compatible analog input signals, I^2C controlled
  - Analog Multiplexers: **LTC1380:** 8-channel, CMOS analog MUX, max analog input 15V, I^2C controlled
  - Analog Buffer
  - I^2C Buffer: **P82B96:** I^2C -bus logic signals levels convertor, improves noise immunity on longer bus lengths.

- All components on ADC board will be controlled by I^2C protocol by the FPGA on Interface board acting as Master
- Optionally, a micro-controller can be provided on the ADC board which will handle the control of ADC and analog mux. on one side and communicate to FPGA on other (*acting as bridge*).

  This functionality can also provide room for expansion of multiple such cards.

Firmware Development

❖ Main modules required for Interface board DAQ:

- 16 channel , 32-bit, Scalar asynchronous counters ✓
- 16 channel on/off and interlock control
- I^2C Master core for ADC board control
- Ethernet MAC core with UDP ✓
- SDRAM memory control core ✓

✓ We have already implemented the following cores for different applications with SPARTAN 6 FPGA

Course of Action

1. Circuit Schematic Design : Estimated time 2 – 3 weeks
2. PCB Design : Estimated time 3 weeks
3. PCB Manufacturing : Estimated time 4 weeks (Usual time taken by PCB manufacturing company)
4. Firmware Development: Estimated time 2 weeks (Can be done during PCB Manufacturing)
5. Implementation & Testing : Estimated time 2 – 3 weeks (After arrival of PCB)

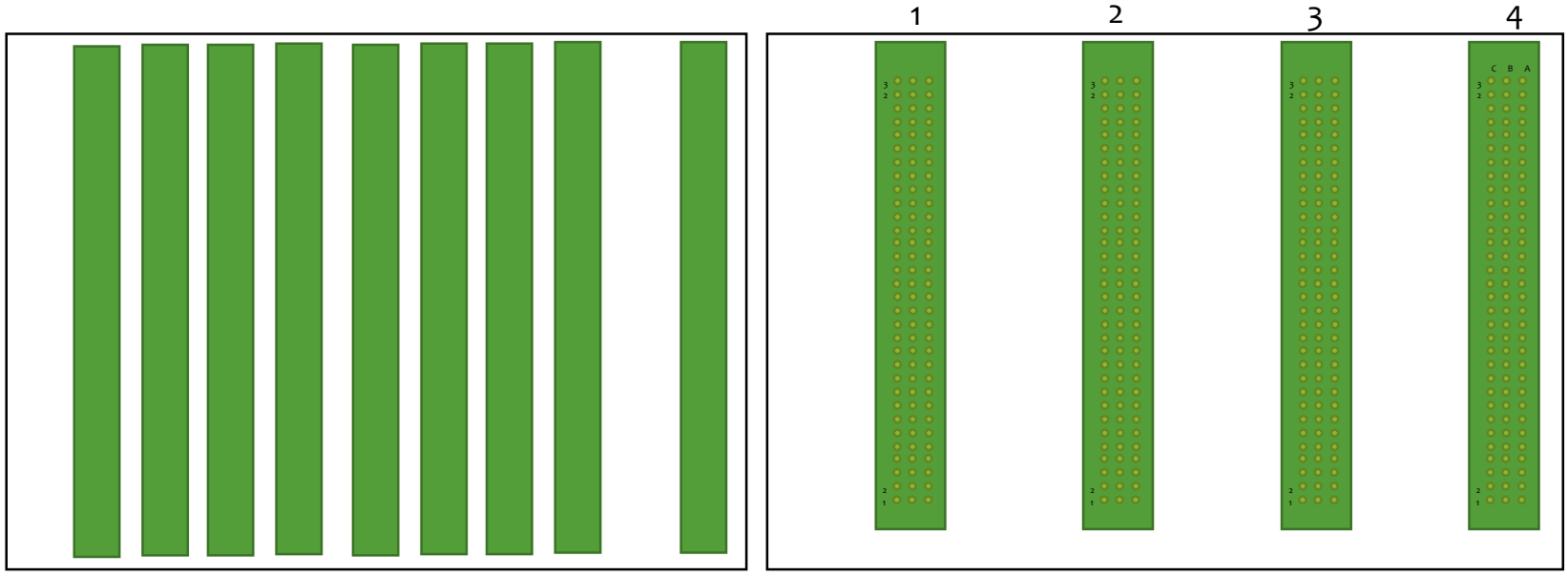
Approx. time for completion of Project : 3 Months

Thank You

BACK-UP SLIDES

New backplane boards

BP1 is a "shortened" version of existing backplane. BP2 is to be produced (by CERN/MSU)
BP2 will be equipped by 4 "VME type" 96 contact connectors (for example ERNI 214836). The corresponding connectors for interface board is ERNI 533402
Voltage at backplane2: +5V and +12V.
Digital signals from the neuron counters will be routed to BP2/4, the analog ones will go top BP2/3



BP1 BP2

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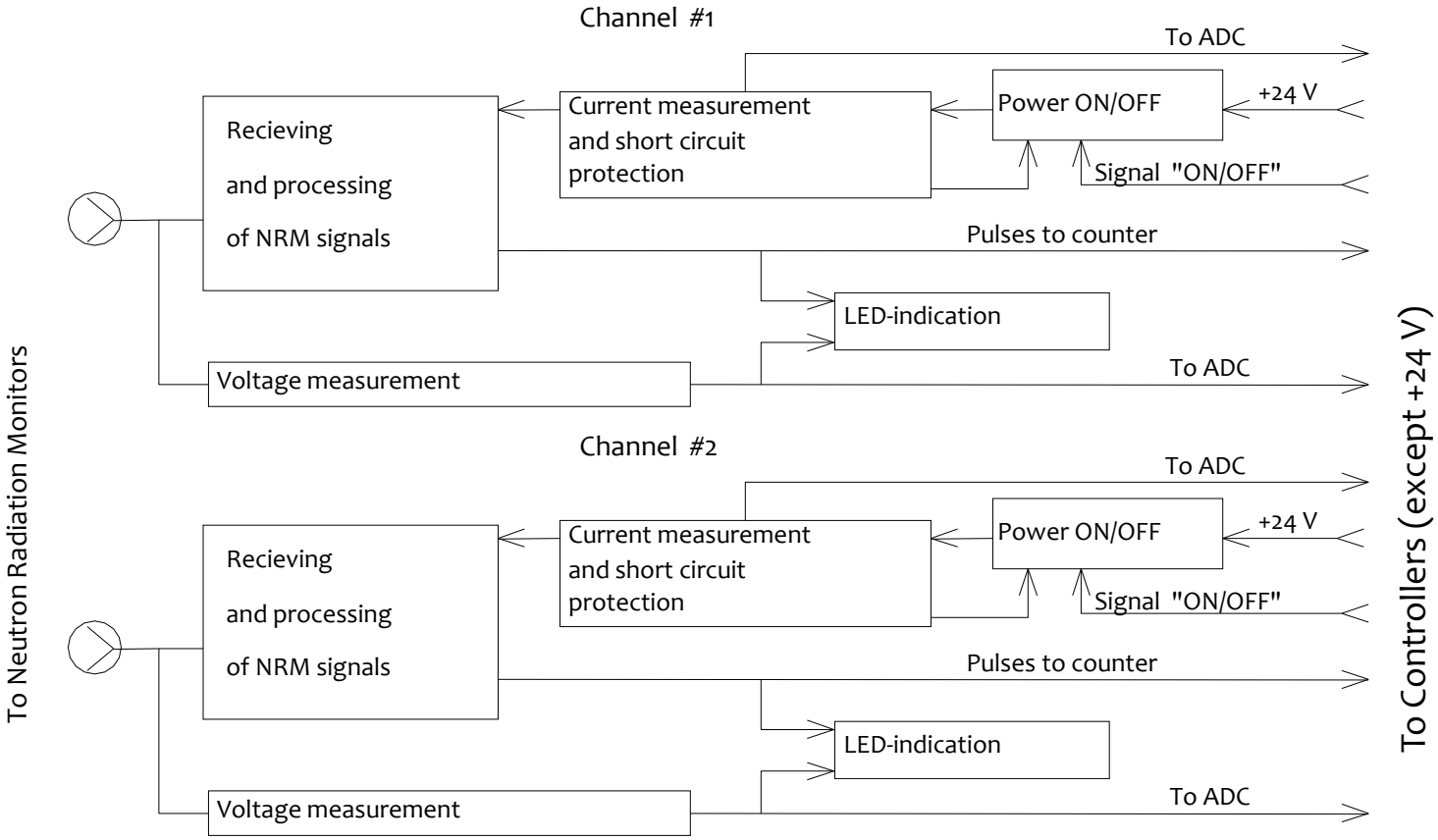
HF Radiation Monitors – Electronics



Structural scheme of the NRM adapter

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