# Calibration Module Firmware Development

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For the Rio de Janeiro group

**August 21, 2014**

# Current work on the Calibration Module Development

## What the firmware of the Calibration unit needs to do

1) **Select the time of the abort gap for the trigger**
2) **Additional pulse phase adjustment (and may be width control)**
3) **Receive the LED feedback from the PIN diodes and send them to the VTTX**

In principle, information from steps 1 and 2 can be generated at the Bridge FPGA and passed to the mezzanine board, or they can be generated at the mezzanine itself.

We will see in this talk that one implementation at the Bridge level has already been made by Nicolo Tosi.

# QIE Board Interface

- **Signals at the mezzanine connector:**
  - **Clk, TrA, TrB – LVDS signal levels**
    - ✓ Clk – 40 MHz
    - ✓ TrA/TrB – 25ns wide positive pulse
  - **SCL – 3.3V compatible I2C clock input**
  - **SDA – 3.3V compatible I2C data line (open collector/drain)**
  - **Power:**
    - ✓ +3.3V
    - ✓ +5V
    - ✓ Vbp – unregulated backplane power, +7 to +8V
    - ✓ Vcal – additional power from a tab on backplane

- **Mezzanine board connector installed on the QIE10 board:**

  **Panasonic: AXN330038**

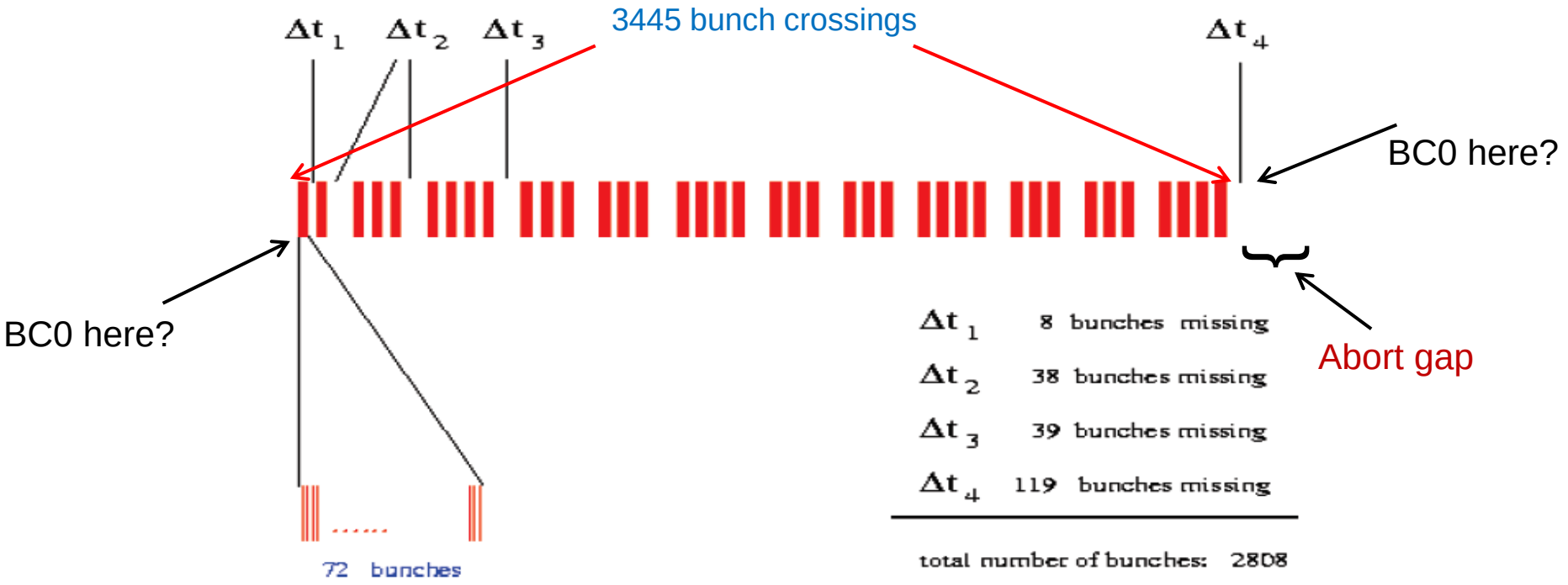
| +3.3 | +3.3 | +5V | +5V | Vcal | Vcal | Vbp | Vbp | +TrA | -TrA | +TrB | -TrB | +Clk | -Clk | SCL |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 3 | 5 | 7 | 9 | 11 | 13 | 15 | 17 | 19 | 21 | 23 | 25 | 27 | 29 |
| 2 | 4 | 6 | 8 | 10 | 12 | 14 | 16 | 18 | 20 | 22 | 24 | 26 | 28 | 30 |
| gnd | gnd | gnd | gnd | gnd | gnd | gnd | gnd | gnd | gnd | gnd | gnd | gnd | gnd | SDA |

Sent by bridge FPGA

# 1) Trigger

- We need to trigger in the abort gap ($\Delta t_4$ below)
- We understand that the BC0 signal (RESET_QIE?) is sent by the backplane, from which the FPGA must calculate the timing for this gap.

**Question 1: What information gives this BC0?, is the beginning of the abort gap, or the crossing of the first bunch?**



**Question 2:** **How many time will need to be pulsed within the abort gap?.**

**Assumed just once, according to Jane Nachtman.**

**Question 3:** **In case the BC0 is not present in every orbit (as Tullio**

**Pointed us), will the LED be pulsed in every orbit, or**

**only when the BC0 is present?.**

# 2) Timing for the pulse generator

## Initial requirements for timing

1. Pulse timing is programmable to any bunch crossing number within

   LHC orbit

2. An additional fine tuning from 0 to 25ns in 1ns increments → (?)

3. Pulse width is programmable between 5 and 25 ns in 5ns increments

4. Trigger signals can be enabled / disabled independently

Recencently, these requirements were implemented in the new firmware version for the QIE Bridge FPGA designed by Nicolo Tosi, as we will see next.

# Bridge firmware for the QIE

## cms-firmwsrc - Rev 2095

Subversion Repositories: cms-firmwsrc

(root)/hcal/

Rev: HEAD Go

| Revision Information | |
|---|---|
| Last modification: | Rev 2095 - nicko - 2014-08-18 11:23:35 - Rev 2090 |
| Log message: | HF_RM_Bridge: Creating branch for prototype card, trunk will continue to preproduction (FPGA package changes) |

Last modification - Compare with Previous - View Log - RSS

| Path | Last modification | | | View Log | Download | RSS |
|---|---|---|---|---|---|---|
| amc13/ | 2094 | 1d 00h | ehazen | Log | | RSS |
| cms_tcds/ | 2093 | 3d 07h | hansenm | Log | | RSS |
| csc/ | 1579 | 96d 22h | bylsma | Log | | RSS |
| ecal/ | 108 | 1648d 04h | cschwick | Log | | RSS |
| fec-css/ | 108 | 1648d 04h | cschwick | Log | | RSS |
| hcal/ | 2095 | 5h 12m | nicko | Log | | RSS |
| Castor-HTR/ | 633 | 560d 03h | beaumont | Log | Download | RSS |
| ctr2/ | 2031 | 10d 21h | drew | Log | Download | RSS |
| FanoutV4/ | 78 | 1780d 23h | | Log | Download | RSS |
| fefpga10/ | 159 | 1505d 04h | mansj | Log | Download | RSS |
| fefpga12/ | 531 | 654d 22h | tgrassi | Log | Download | RSS |
| HCAL_GLIB_ngFEC/ | 2090 | 3d 21h | msahin | Log | Download | RSS |
| HF_ngCCM/ | 2080 | 4d 16h | sdg | Log | Download | RSS |
| HF_RM_Bridge/ | 2095 | 5h 12m | nicko | Log | Download | RSS |
| HF_RM_FPGA/ | 1724 | 68d 18h | nogima | Log | Download | RSS |
| HF_RM_igloo2/ | 2050 | 5d 05h | nicko | Log | Download | RSS |
| HTR/ | 438 | 792d 00h | tgrassi | Log | Download | RSS |

# Question: What is the file pulser.v (bridge firmware) doing?

- Coarse pulse timing is programmable to any bunch number **config_a[31:16]**.
- An additional pulse timing fine tuning **config_a[13:2]**.
- Pulse width is programmable **config_a[13:2]**.

In principle, the bridge FPGA needs to send positive pulses 25 ns wide to the mezzanine, according to Mike Miller.

In the current version, with a 120 Mhz fast clock in the FPGA, the smallest time step that is achievable is 8 ns..

**QUESTION: why do we need the 1ns fine tuning?.... Is it woth?**

**Nicolo' Tosi, pulser.v, cms-firmwsrc - Rev 2095, HF_RM_Bridge.r2089/trunk/hdl**

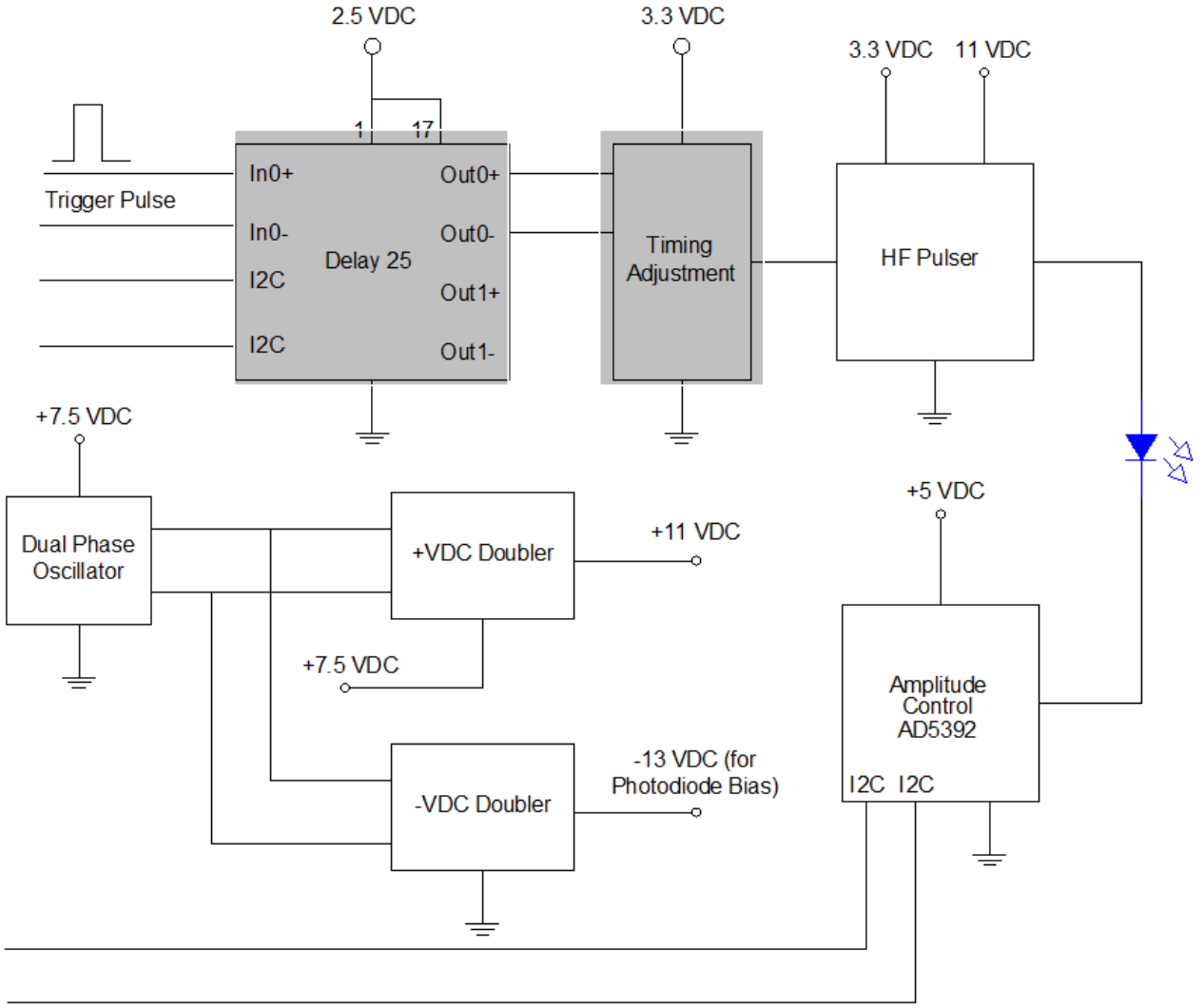
# Amplitude of the pulse

The amplitude of the pulse must be programmable from control room through the I2C protocol.

This is managed by the ngCCM module that transmit I2C commands through the backplane to the bridge FPGA, which in turn will pass it to the mezzanine.

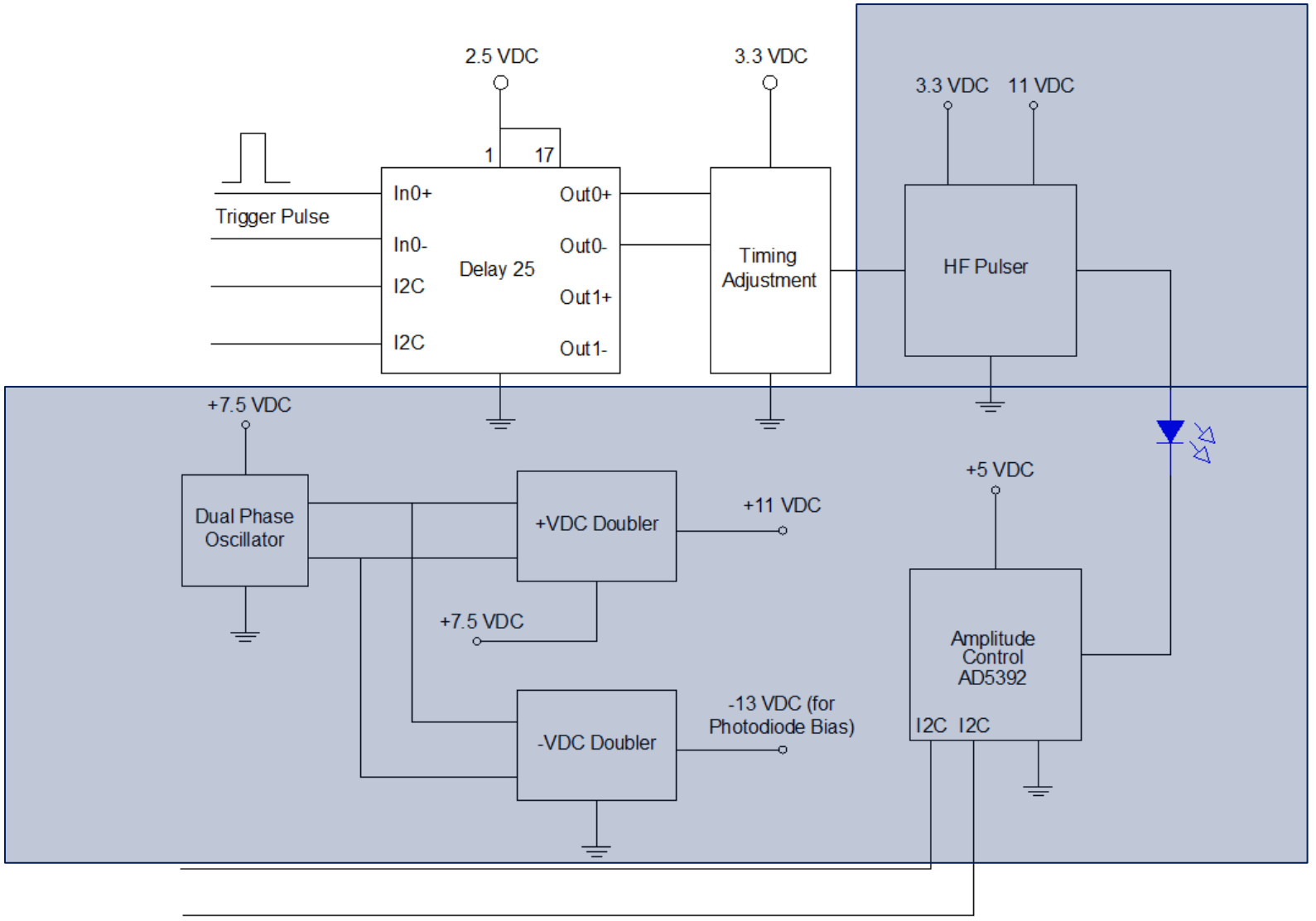
Question: should the FPGA make any change to this connection?, or just pipeline it to the mezzanine connector?

# Currently being developed in the Bridge FPGA




**Presentation from Michael Miller 24/07/14 showing the HF pulser circuitry**

# Already included in the mezzanine



# 3) Feedback

The PIN diodes information must be processed by the QIE chips.

In principle the same output format used for the QIE cards can be used for the calibration unit.

According to Jane Nachtman, the DAC value could also be included on top of the normal QIE output information sent to the VTTX. This represents a minor change in the firmware of the QIE FPGA for the calibration unit.

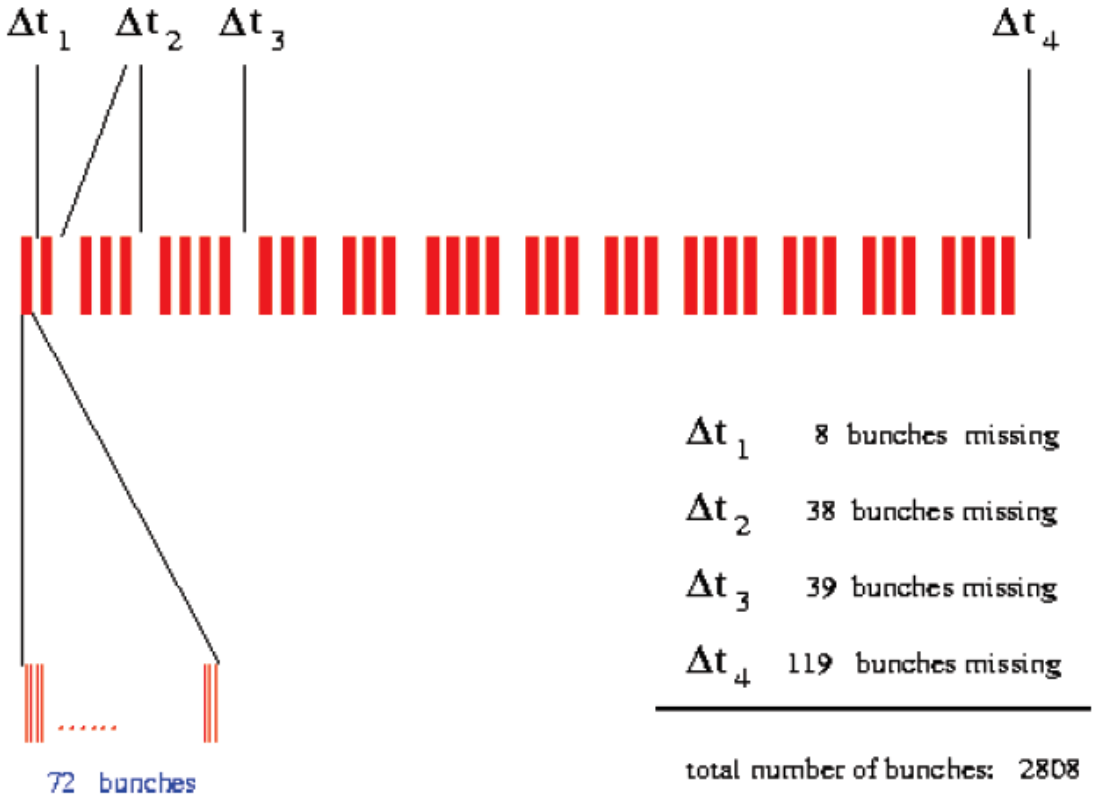
# Conclusions

**Most of the work that the Bridge FPGA needs to do is now being developed by Nicolo Tosi.**

1. Need to understand what the BC0 signal represents
2. Apparently no change in the bridge FPGA is needed for the I2C signal
3. Minor changes need in the format to include the DAC signal in the reading chain
4. Need to think about the testing of the boards once they are approved and constructed.

# Backup slides

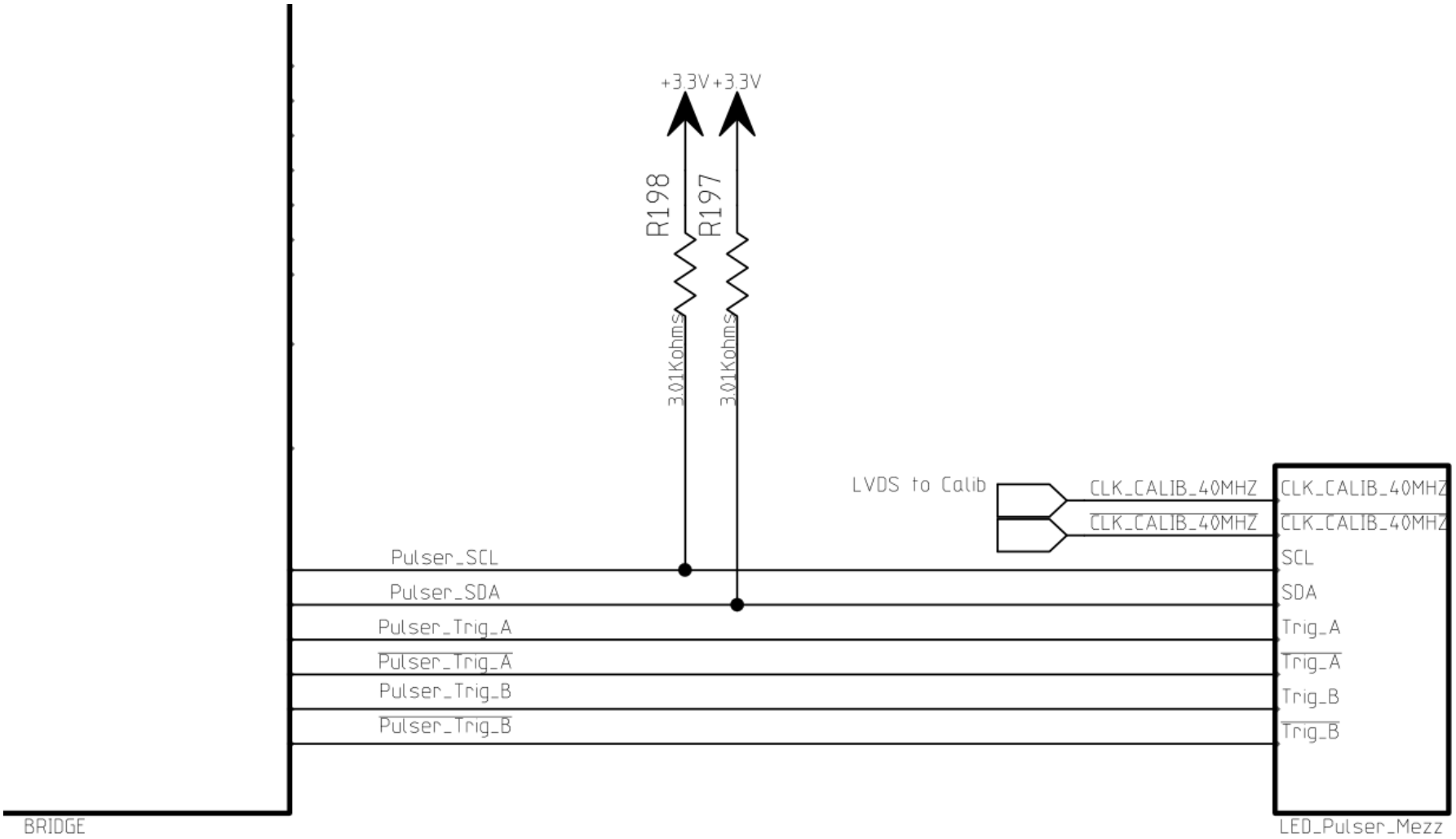
# LHC beam structure




| | | | |
|---|---|---|---|
| 2808 | Bunches | → | 2808 |
| 27 x 8 | $\Delta t_1$ | → | 216 |
| 38 x 8 | $\Delta t_2$ | → | 304 |
| 39 x 3 | $\Delta t_3$ | → | 117 |

3445 bunches until the abort gap

If we add the 119 bunchs of the abort gap we end up with the 3564 bunches

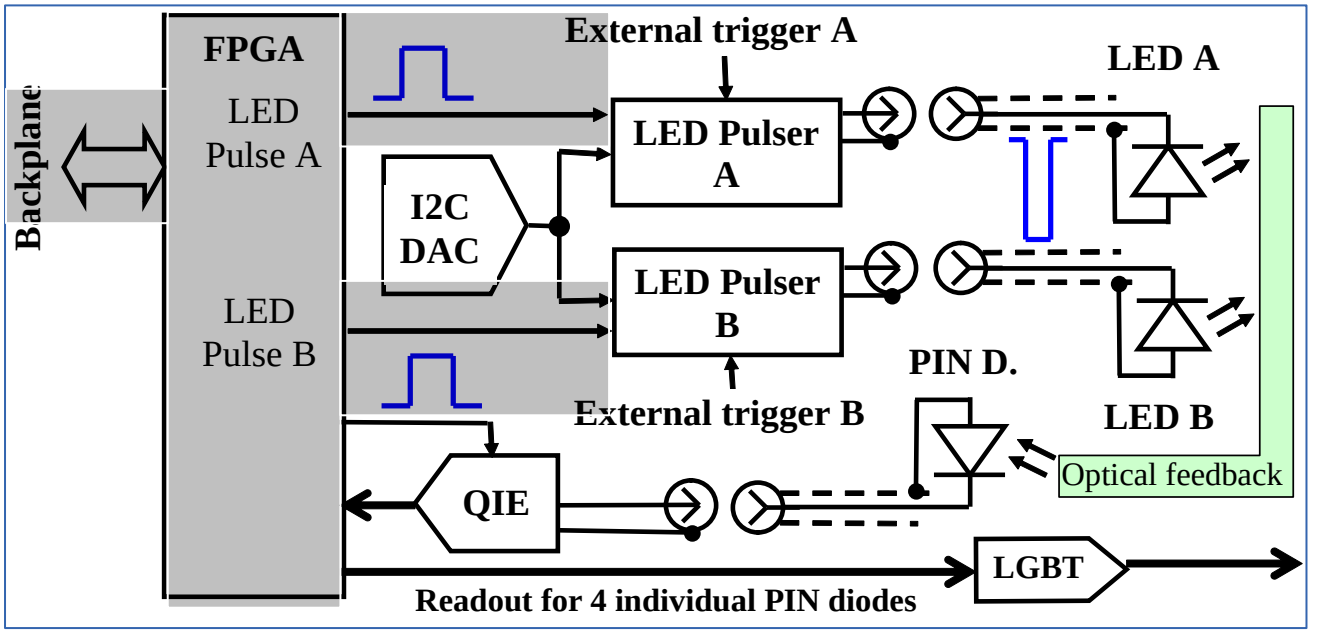



**CMS-doc-11974-v24, Theresa Shaw, HF_Prototype_HF_24Channel_Schematic.pdf**

# Current work on the Calibration Module Development

**FPGA provides timing for the programmable amplitude pulse generator**

- **Selection of bunch crossing (with respect to BC0)**
- **Additional pulse phase adjustment (and may be width control)**



# Timing flow chart proposal