LLRF FOR THE SPS 800 MHZ CAVITIES *UPDATE*

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September 10th, 2014

Status & strategy

- Cavity 1
  - Old LLRF Installed but not commissioned (like before LS1)
  - New LLRF will be installed & tested on Cav1 first
- Cavity 2
  - Old LLRF Installed and commissioned for start-up (like before LS1)
  - Old LLRF used for operation for 2014 run, mid 2015 run () (backup solution)
  - New LLRF will be installed after commissioning on cavity 1
- Old LLRF:
  - amplitude & phase loop
  - no beam loading compensation

Status (new LLRF)

HW: Hardware
FW: Firmware (FPGA)
NR: not relevant
NA: not available

Module Name	Nb of Module/cavity	HW Status August 2014 Cavity 1	HW Status August 2014 Cavity 2	Spares	Software
Linux Front-end (CPU)	1	**Installed**	**Installed**	OK	NR
CTRV (timing)	1	**Installed**	**Installed**	OK	OK
CMM (Crate Management)	1	**Installed**	**Installed**	OK	OK
RFFG (Function generator)	1	**Installed**	**Installed**	OK	OK
Switch&Limit	1	**Ready to be installed**	**Ready to be installed**	To be tested	To be designed (migration from L4 ?)
Clock Distributor	1	**HW Ready, FW to be finalized**	**NA (fabrication need to be launched)**	NA	To be designed (migration from L4 ?)
200MHz Quadrupler	1	**Ready to be installed**	**HW Ready, to be tested**	To be tested	NR
Cavity Loops (RF Feedback)	1	**HW Ready, FW to be finalized**	**NA (used for L4 RFQ)**	NA	To be designed (migration from L4 ?)
Antenna Vector Sum	1	**Installed**	**Installed**	NA	NR

Plans

1: chopper project from 6.10.2014 to 27.02.2015
2: chopper project from 16.02.2015 to 26.06.2015

	Power chain	Beam	Date[1] (Cavity 1)	status	Date[1] (Cavity 2)	status	Date[2] (Cavity 1)	MD	Fesa class ready by…
Clock Distribution module			By 1.10.2014		By 2.03.2015		By 1.10.2014		22.10.2014
1. Clock generation (phase noise, PLL locking,…)	No	No							
2. RF Ramp test	No	No							
Switch&Limit module									
1. Gain&Limiting level calib	yes	no	By 1.10.2014		By 1.04.2015		By 10.2014		22.10.2014
RFFG module									
1. Function generation tests	No	no	By 1.11.2014		By 1.04.2015		By 11.2014		06.10.2014
Cavity-loops module									
1. Open loop tests *(delay, phase, gain adjust)*	Yes	No	By 1.10.2014		By 1.05.2015		By 1.10.2014		29.09.2014
2. Close loop test *(1-T fdbk)*	Yes	No	By 1.10.2014		By 1.05.2015		By 1.10.2014		"
3. Function reception	No	No	By 1.11.2014		By 1.05.2015		By 1.11.2014		"
4. Beam loading comp. *(25ns, low intensity)*	Yes	Yes	8.10.2014		-		08.10.2014	MD1	"
5. Beam loading comp. *(25ns, high intensity)*	Yes	Yes	26.11.2014		-		26.11.2014	MD2	"
6. RF ramp test	Yes	No	By 1.04.2015		-		11.2014		16.03.2015
7. Beam acceleration	Yes	Yes	04.2015		06.2015		26.11.2014	MD3	"
			04.2015		-		12.2014	MD4	"
8. Polar loop tests	Yes	No	06.2015		06.2015		12.2014		01.06.2015
9. Feedforward tests	Yes	yes	07.2015		07.2015		01.2015	MD5	"

TWC800 Cavity 1 & Vector Sum