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Time Interpolator Mapping from IBM 120nm to TSMC 65nm

Moritz Horstmann
PH-ESE-ME

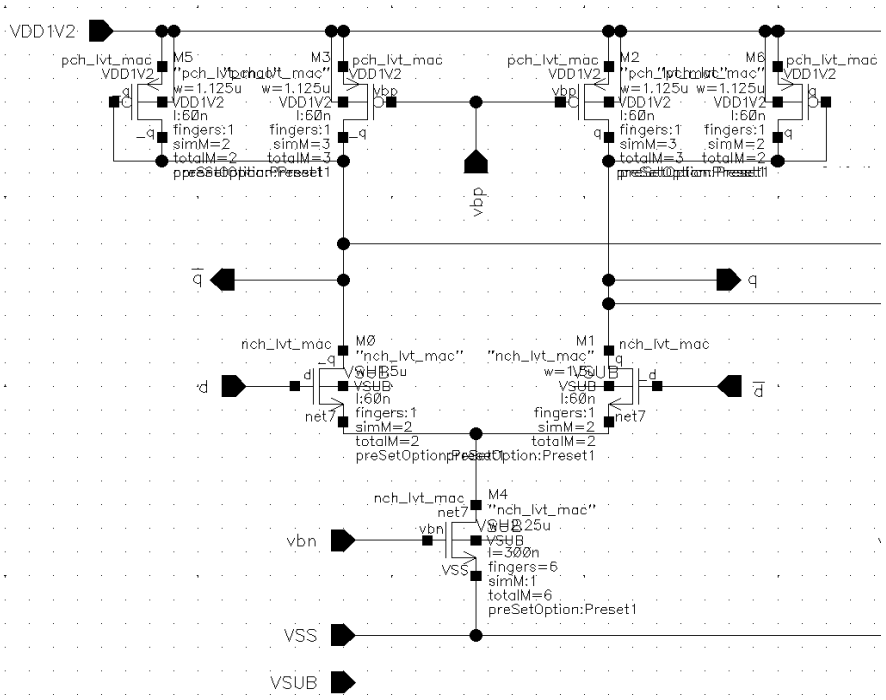
Differences of the Technologies

- CERN uses the TSMC 65nm low power technology, resulting in higher threshold voltages
- Threshold of IBM Low VT MOS is around 200mV;
  of TSMC Low VT MOS around 400mV
- TSMC provides Shallow Trench Isolation (STI) in 65nm, enabling better isolation between different modules

Mapping

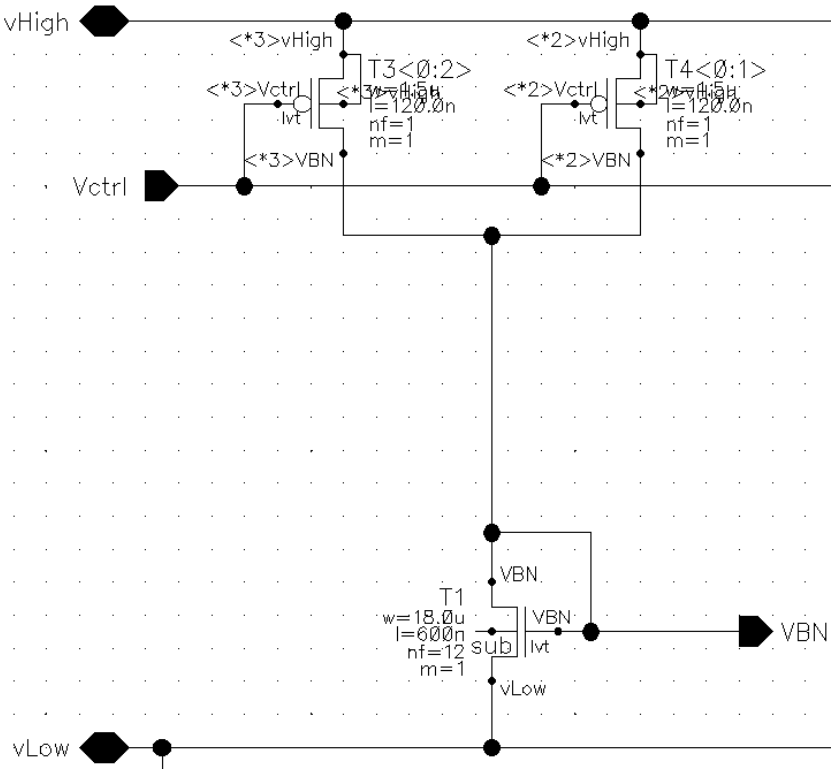
- First approach: Direct mapping by scaling all dimensions to 50%
- Cell runs at more than double the speed
- Higher threshold results in small operation region in which the delay can be controlled
- Matching is worse, especially in the dual- to single-ended buffer

Maneatis Delay Cell

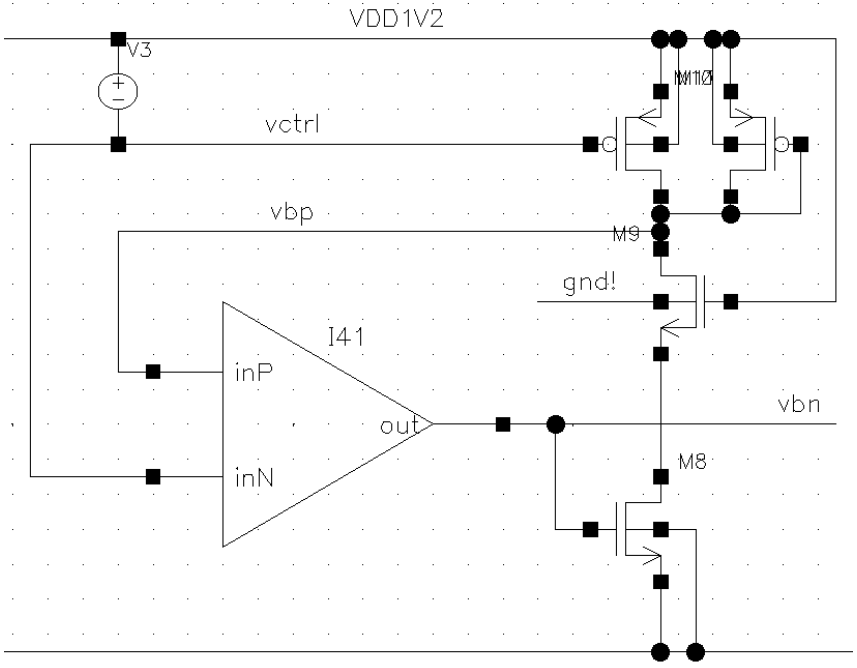


- Length is kept at 50%
- Width of all transistors is scaled to around 75%
- Higher threshold and matching is only partly compensated
- Optimized biasing increases the operating region
- No resistive peaking

Optimized Biasing



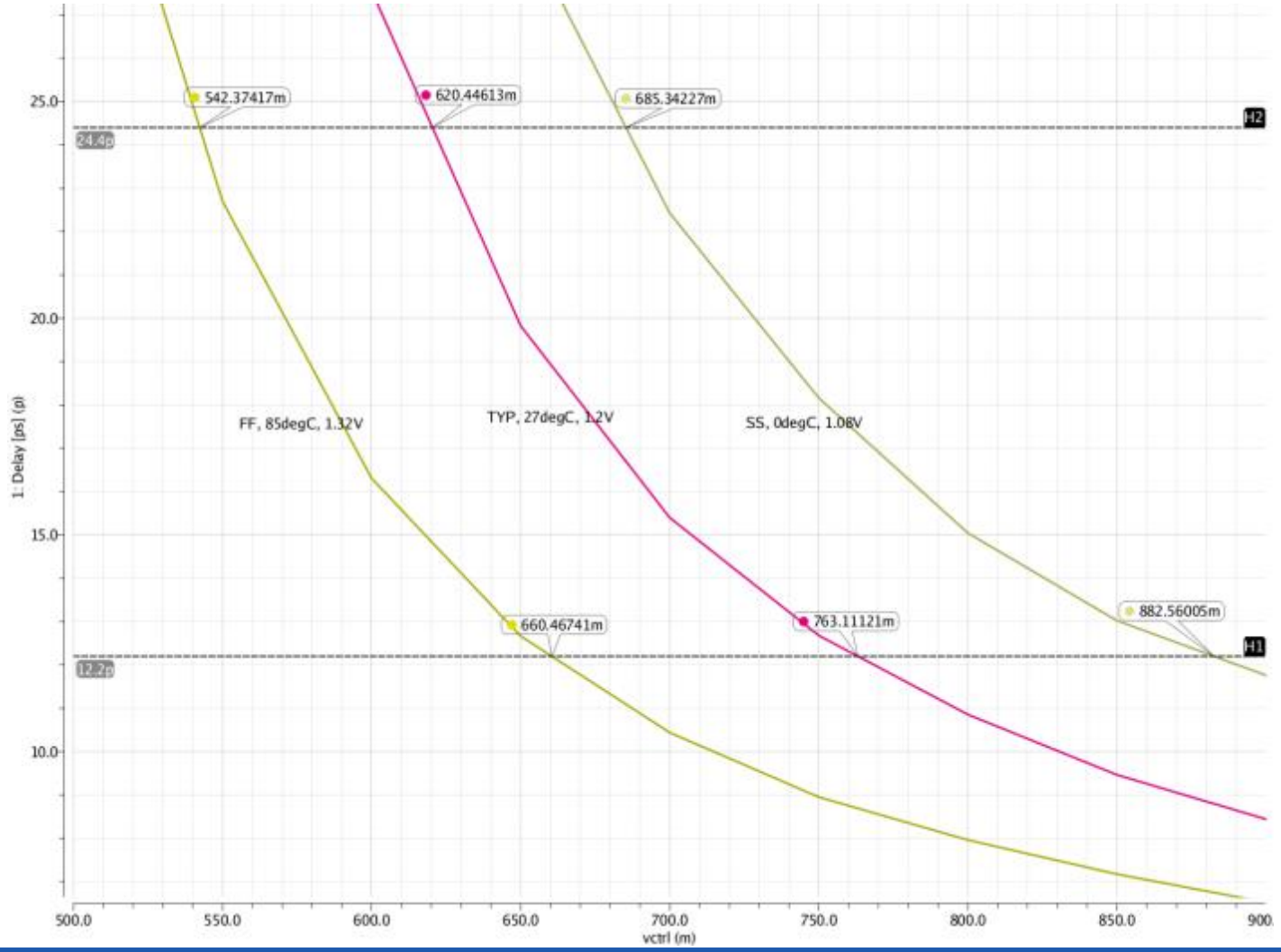
Original Biasing Circuit



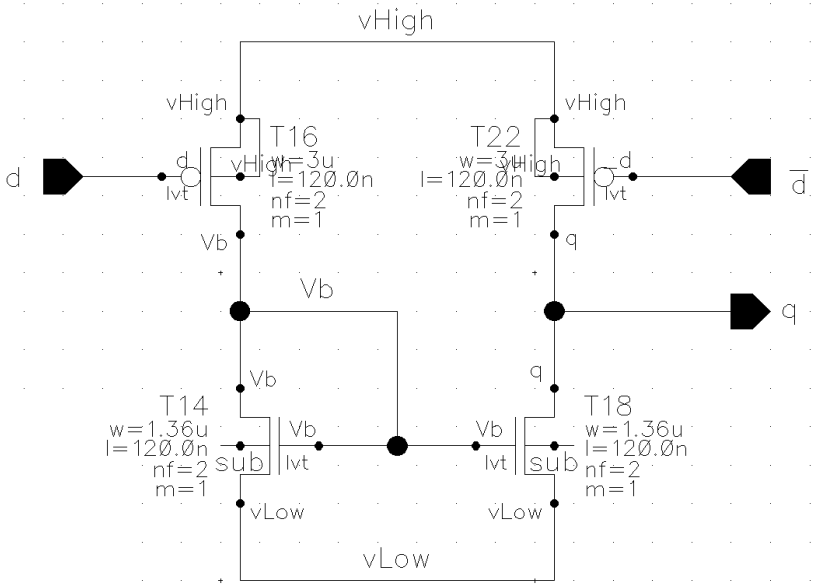
Biasing with Copy of a Branch of the Delay Cell

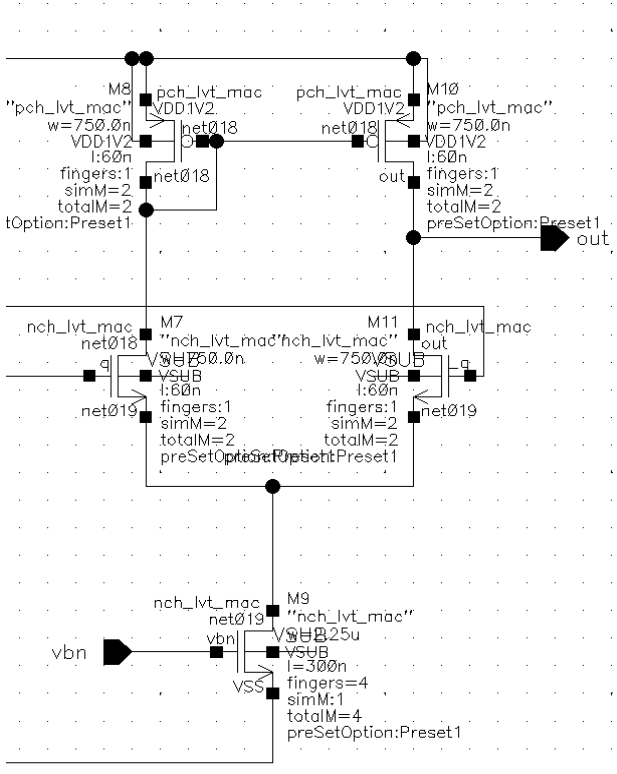
-> vbn can reach VDD1V2

Operation Region (Post Layout)



Faster DE to SE Buffer



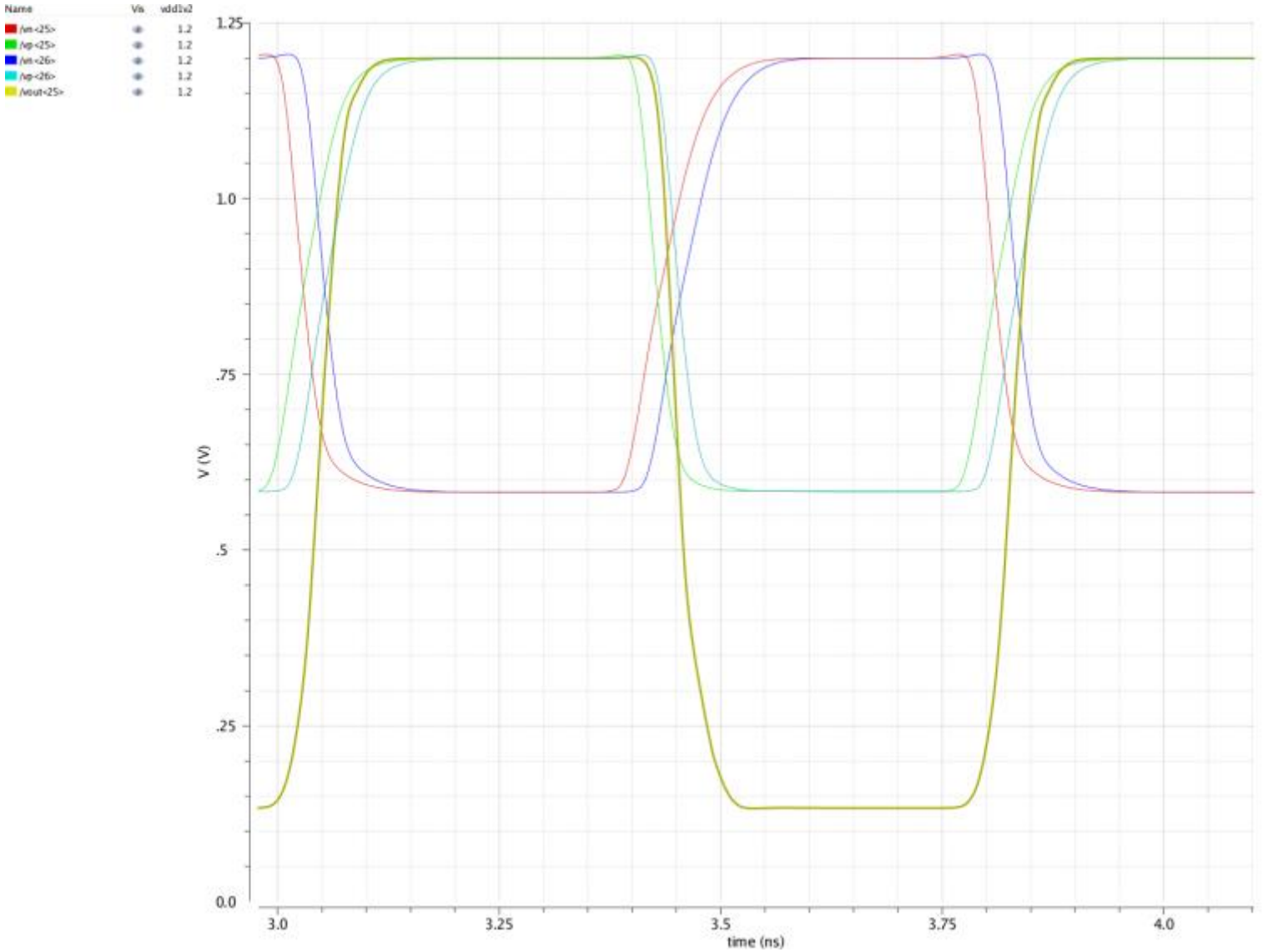


Original Dual- to Single-Ended Buffer

Optimized Design

Much faster, resulting in lower mismatch

Simulation Results



Results Comparison

	TSMC, 12ps	TSMC, 24ps	IBM, 20ps
Absolute Mismatch Delay Element	0.30ps	0.78ps	0.49ps
Relative Mismatch Delay Element	2.4%	3.2%	2.5%
Absolute Mismatch After DE2SE Buffer	0.72ps	1.75ps	2.43ps
Relative Mismatch After DE2SE Buffer	5.9%	7.2%	11.2%
DE2SE Buffer Delay	13ps	17ps	47ps
Power Consumption	38mW	13mW	28mW

Mismatch: 1-sigma variation
Power: 32 delay cells + DE to SE buffers + drivers
TSMC simulations include extracted parasitics, IBM simulations not

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