PLL

PLL architecture and LC-tank

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Content

- PLL architecture

- VCO LC-tank

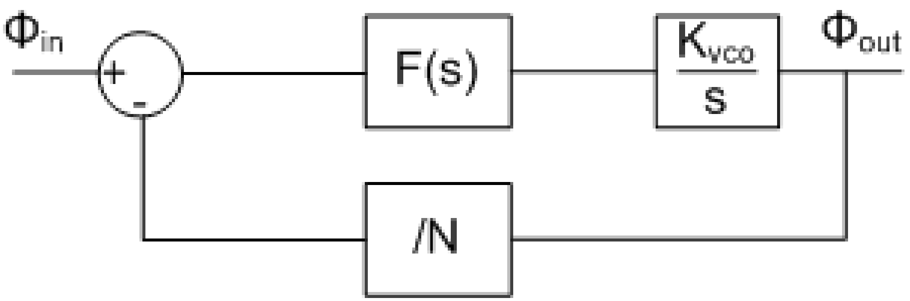
PLL architecture

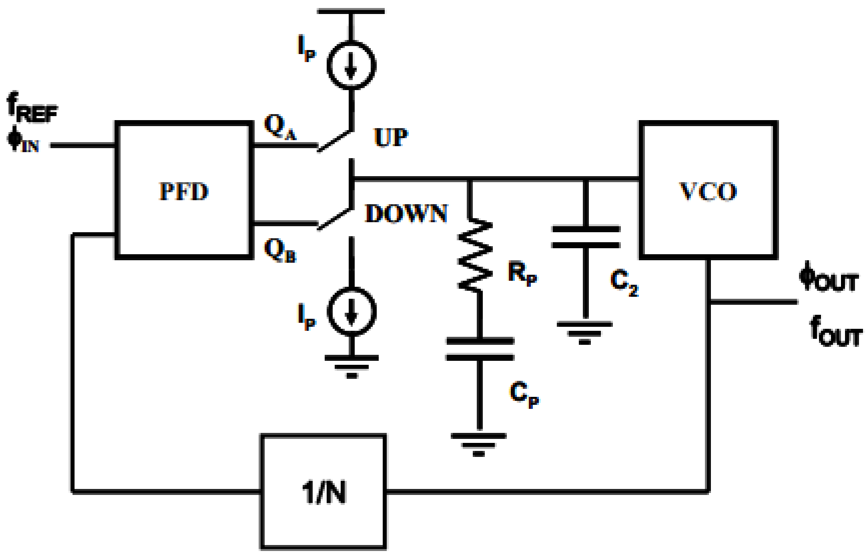
- Architecture choice
  - 3rd order PFD charge-pump PLL
    - Reference spur, CP-noise X N, Divider noise
  - Subsample PLL
    - CP-noise not multiplied, No divider
  - Sampled loop-filter
    - Low reference spur
  - Multiplying DLL
    - Only for high bandwidth, low reference jitter

- With low bandwidth, reference spur is less severe.
- More complex = more radiation sensitive

PLL architecture

- 3rd order optimal PLL system





$$F(s) = \frac{K_{pd}\left(1+\frac{s}{\omega_z}\right)}{s\left(1+\frac{s}{\omega_p}\right)}$$

$$\omega_n = \frac{\omega_{-3dB}}{\sqrt{1+2\zeta^2+\sqrt{(1+2\zeta^2)^2+1}}}$$

$$\omega_z = \frac{\omega_n}{2\zeta}$$

$$\omega_p = \omega_z\,(2\zeta)^4$$

$$K = \omega_n^2\,N$$

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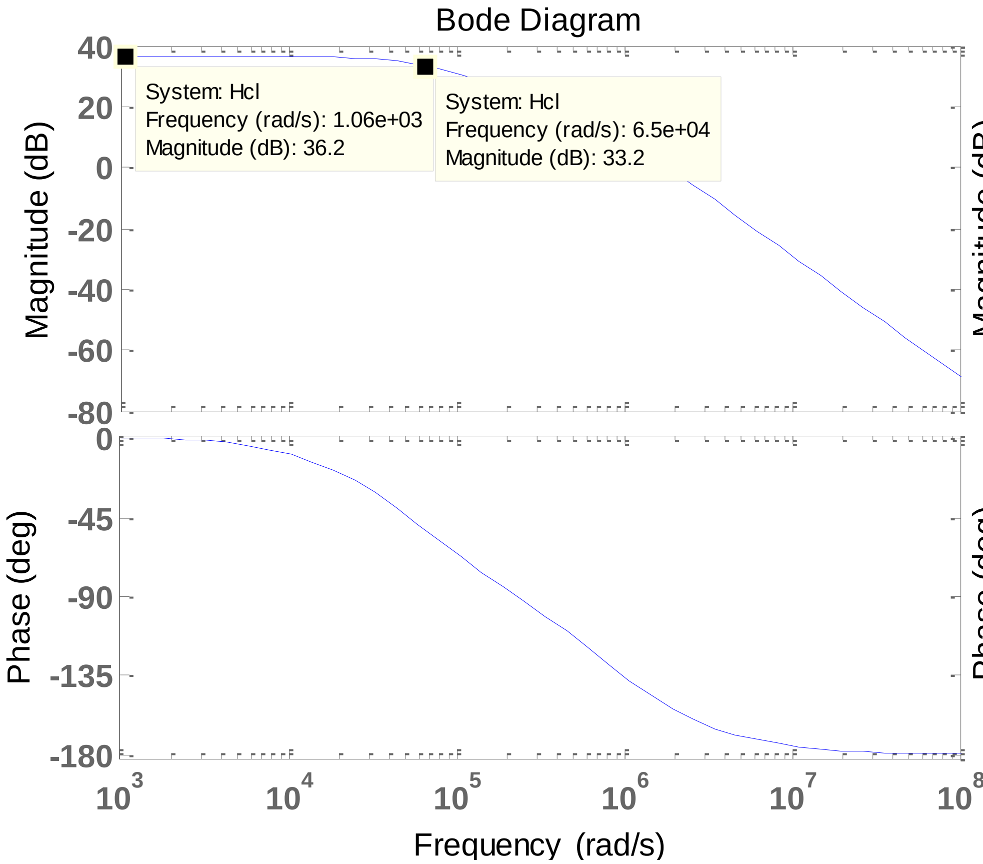
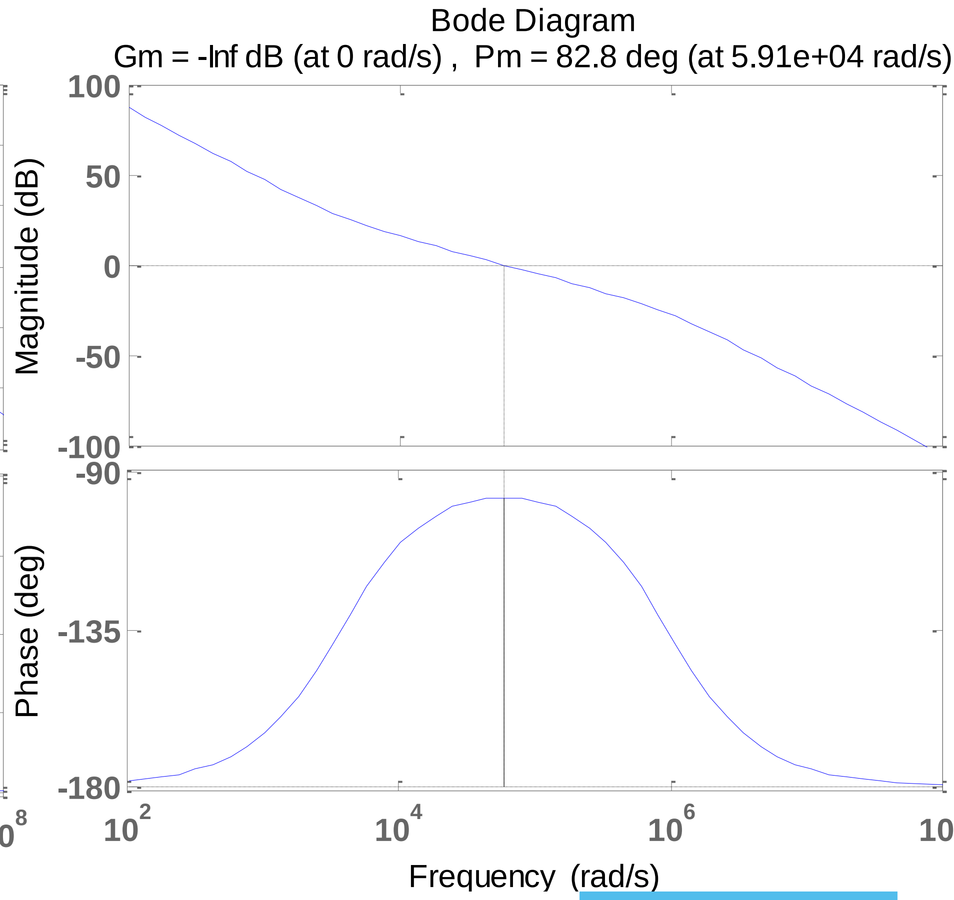
PLL architecture

- E.g. 10 kHz (62.8 krad/s) closed loop bandwidth





PLL architecture

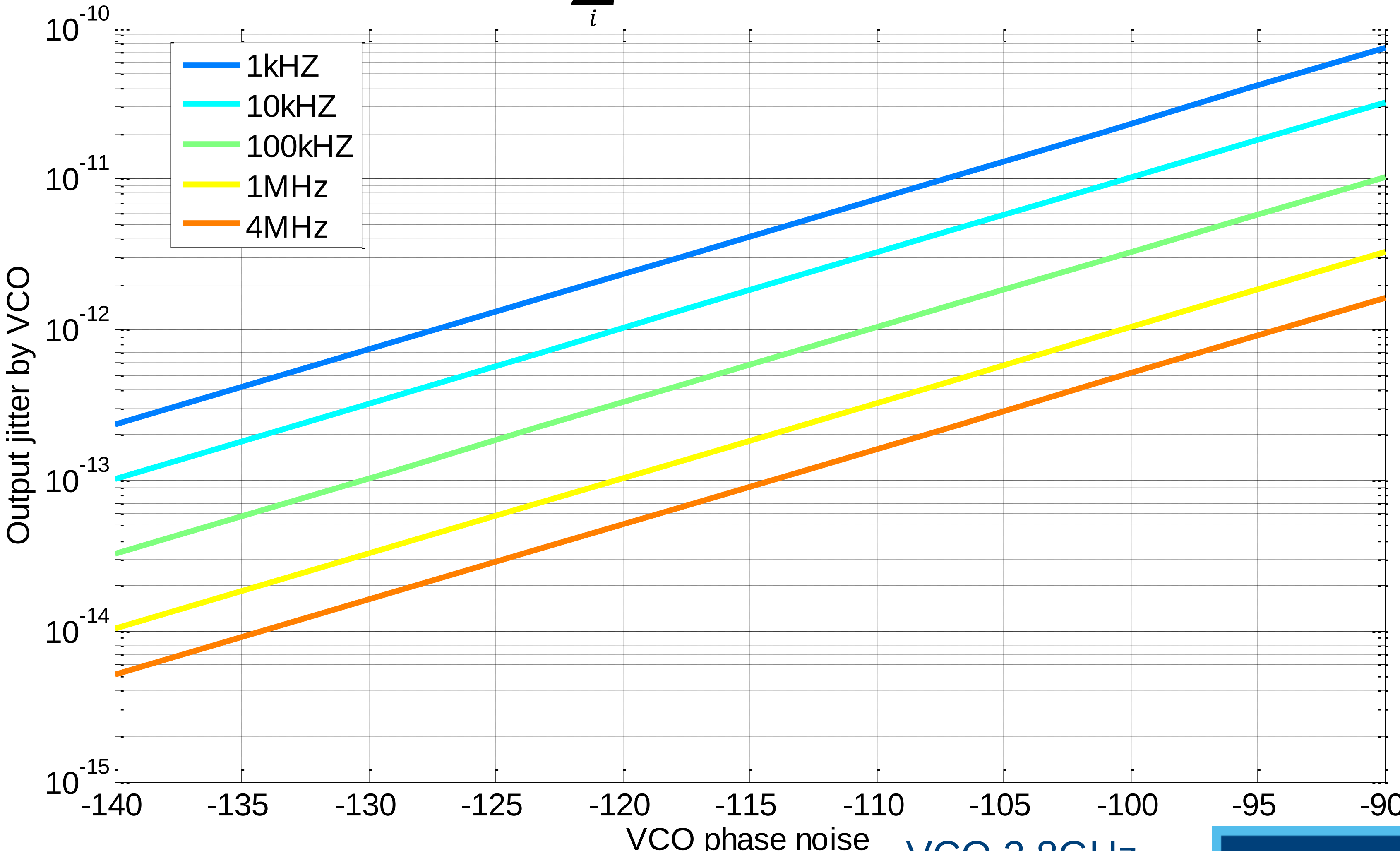
- Matlab model is ready
  - Noise calculations
  - System generation
- For low bandwidth PLL, VCO is most important
- Master thesis is working on rad-hard lock detector
- To be determined
  - Frequency range
  - Bandwidth range
  - Type of programming, how to tune BW
    - # of steps , constant damping …
- Components in AMS kit?

Jitter

$$Jitter = \sqrt{\frac{1}{\omega_0^2}\int_{fmin}^{fmax} S_{\emptyset}(f)\,df}$$

$$where\ S_{\emptyset}(f) = \sum_i \emptyset_{noise,i}(f)\,H_i(f)$$

Better VCO = Lower BW allowed!



VCO 2.8GHz

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Phase noise

- LC-tank phase noise sources
  - Inductor's Rs
  - Active -1/gm element (equivalent A.Rs noise)
  - Capacitor less important at this frequency

$$v_n^2(f) = kTR_s(1+A)\left(\frac{\omega_0}{\Delta\omega}\right)^2$$

- LC-tank amplitude

$$v_{tank}^2 = \frac{4}{\pi} i_{tail} R_p \quad or \quad v_{sat}$$

- Phase noise depends on noise AND signal power

$$S_\phi(f) = \frac{v_n^2(f)}{v_{tank}^2}$$

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Phase noise

- Rs and current determine the phase noise
- What L gives best phase noise?
  - Depends on power consumption and maximum swing

- For given power, take smallest L with best Q that places the VCO near voltage limited region

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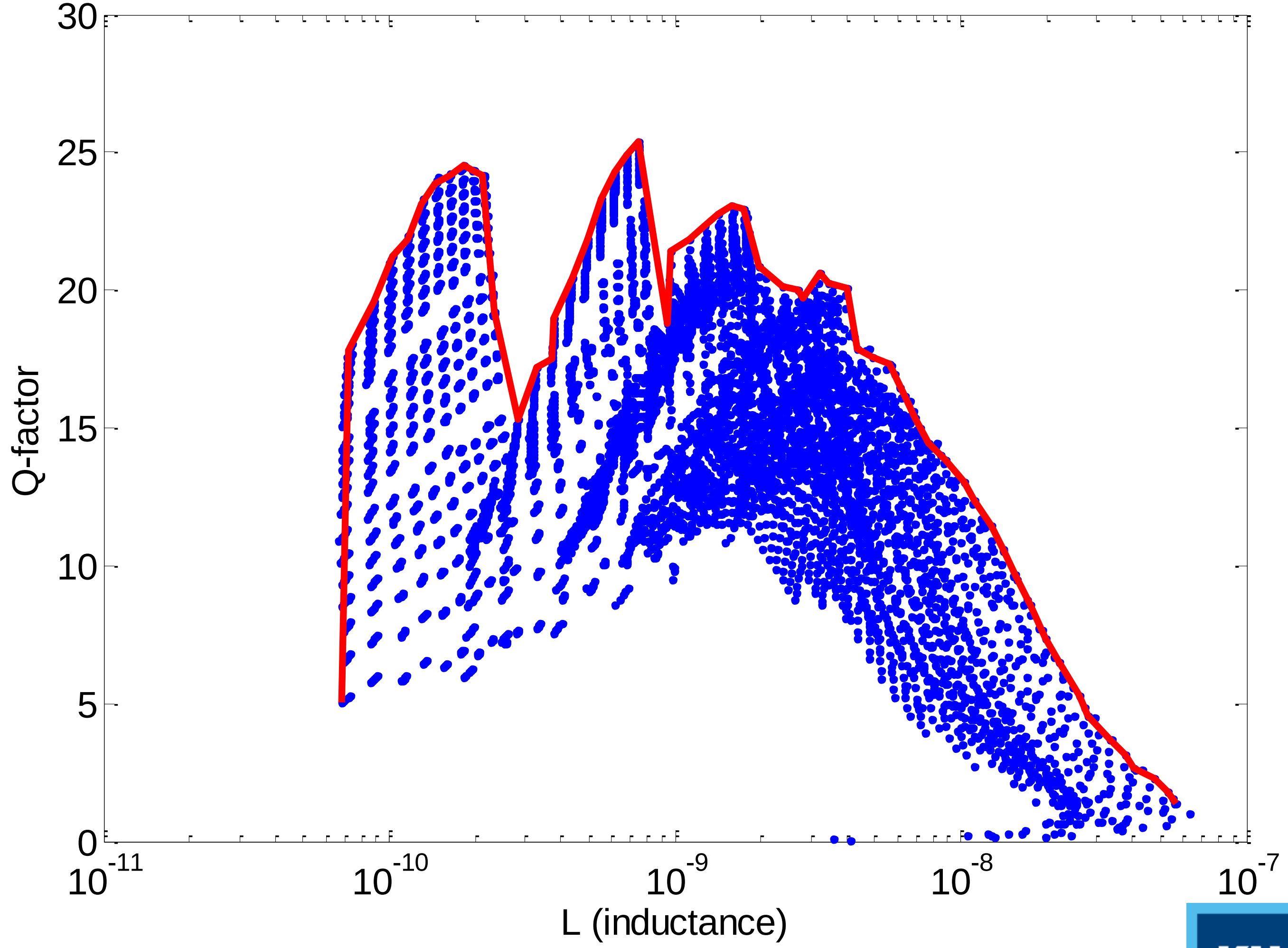
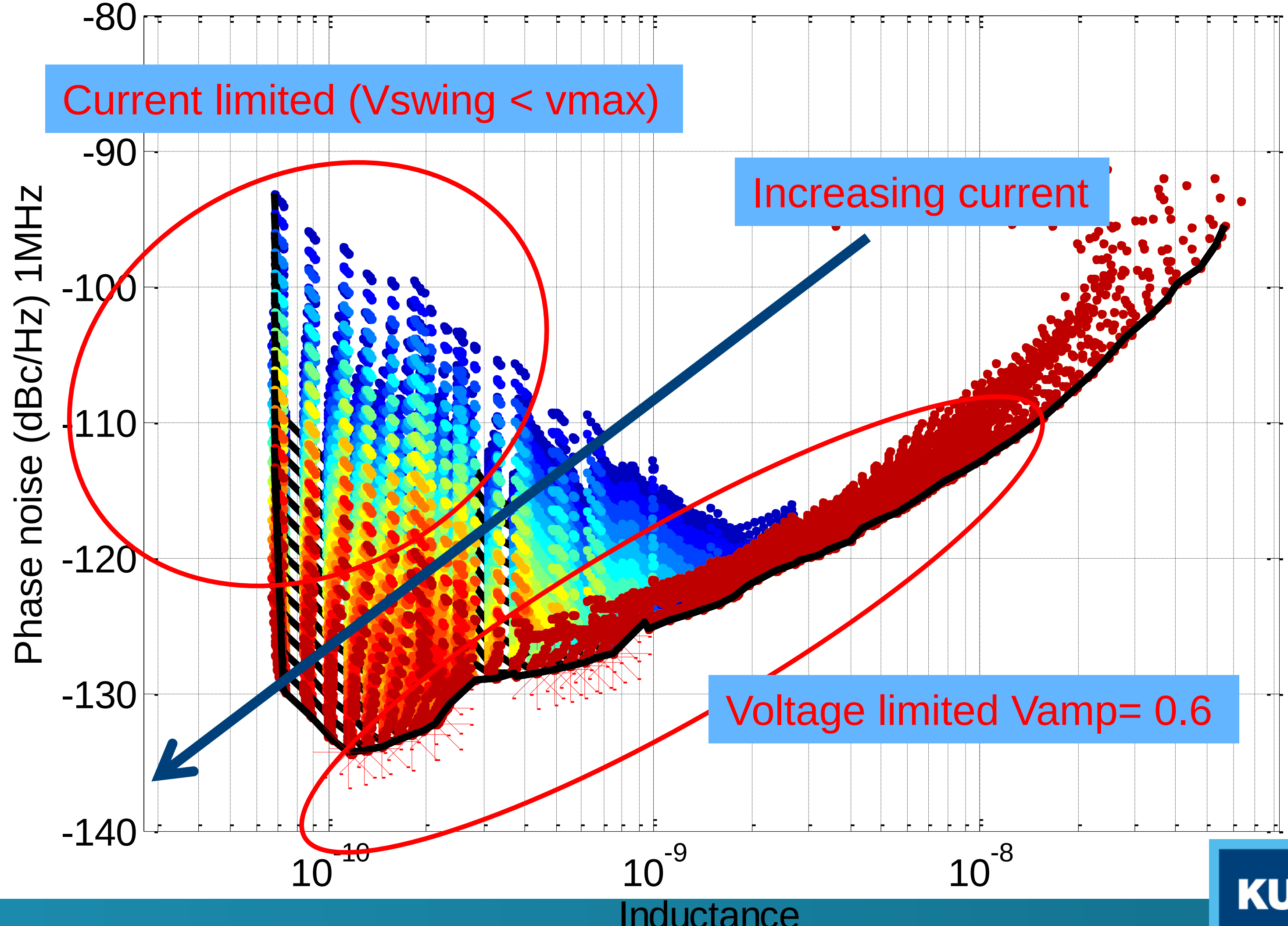
Q-factor



Phase noise



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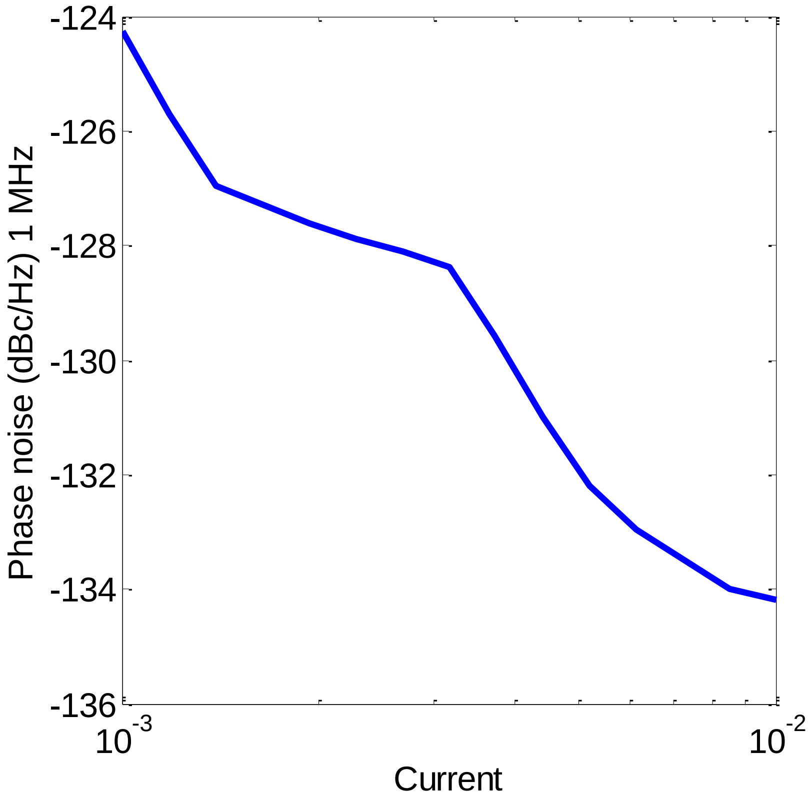
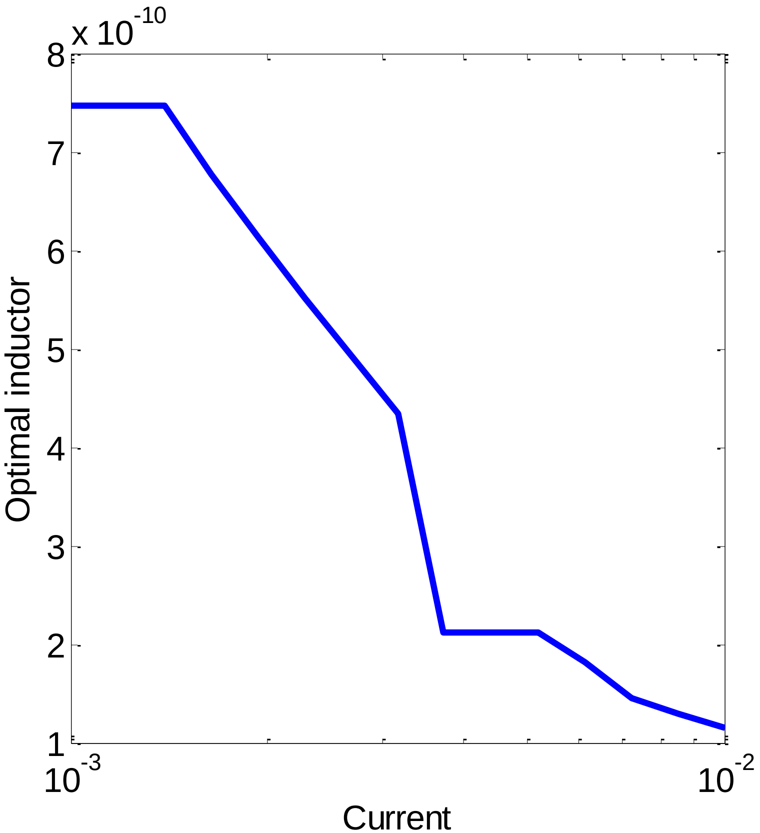
Phase noise



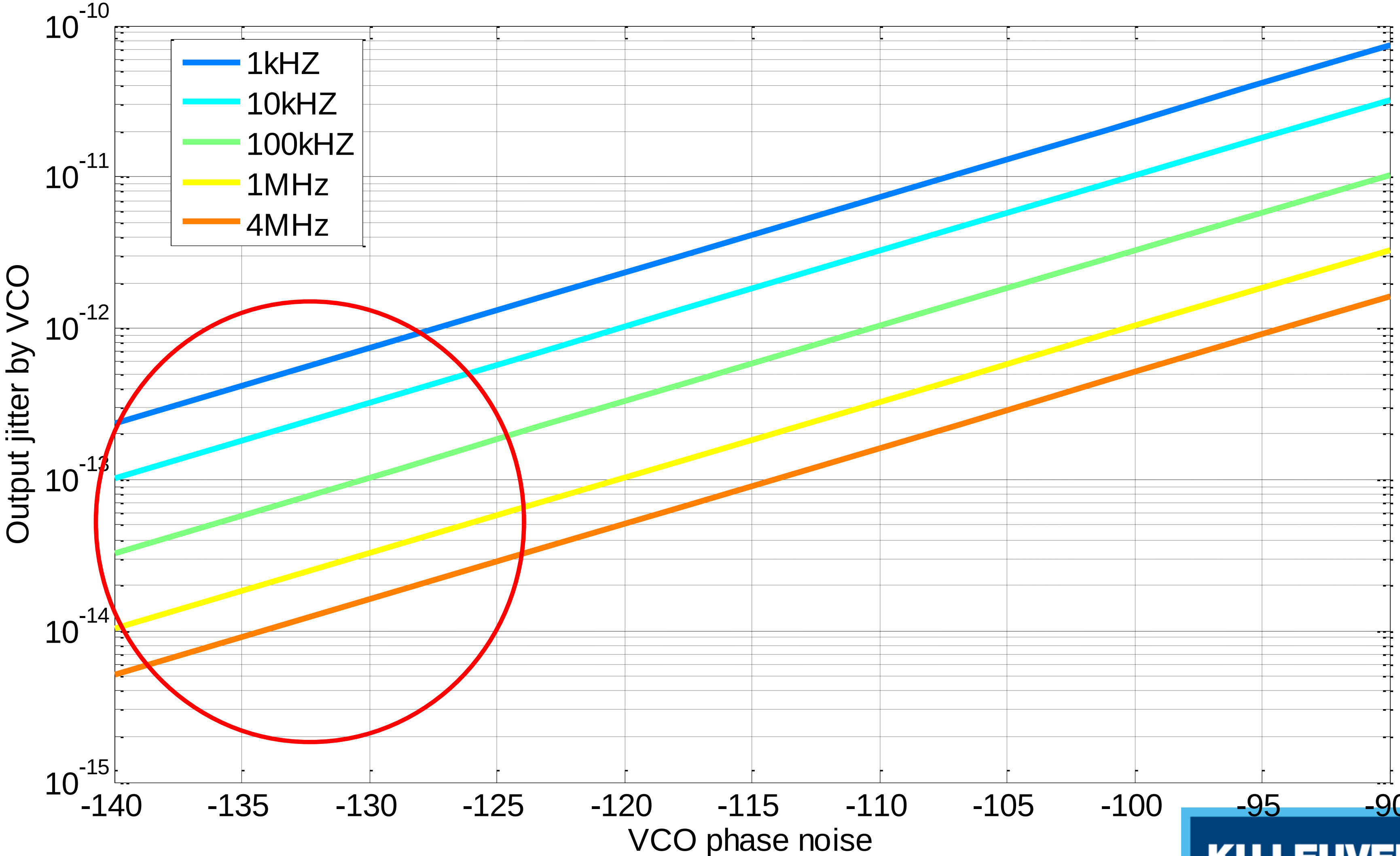


For given power consumption, best phase noise for L that gives largest swing.
-> larger L above voltage limited range = worse PN (more noise at the same signal power)
-> lower L has less noise but also les Rp so lower amplitude and more PN.
-> Optimal L depends on power consumption.
-> Higher power = smaller inductor = less Rs = less voltage noise

Discussion of LC usage

- VCO FOM
  - 20log(f0 / P df) – PN(@df)
  - +-223 dB
  - This number can compare different VCOs at different frequencies!
  - Indicates the phase noise relative to power consumption

Jitter



1kHZ
10kHZ
100kHZ
1MHz
4MHz
Output jitter by VCO
VCO phase noise
10^{-10}
10^{-11}
10^{-12}
10^{-13}
10^{-14}
10^{-15}
-140
-135
-130
-125
-120
-115
-110
-105
-100
-95
-90

To be discussed

- Bandwidth tuning
- Frequency ranges
- Oscillator type (FOM? Rad-hard?)
- Power consumption