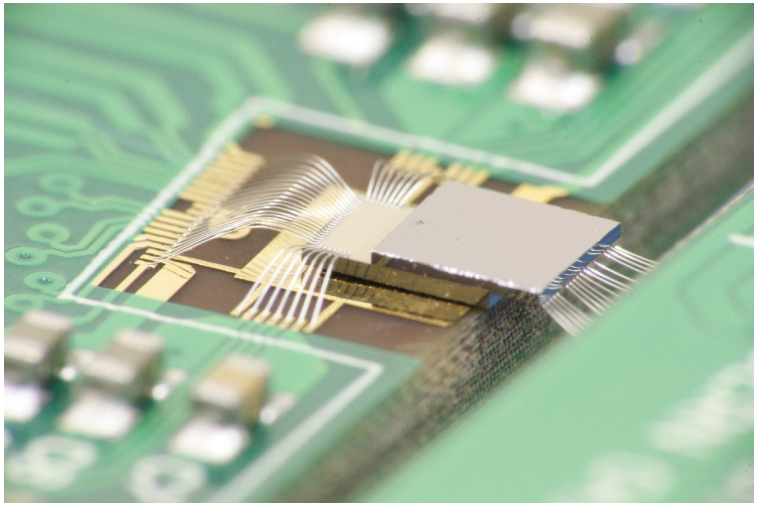
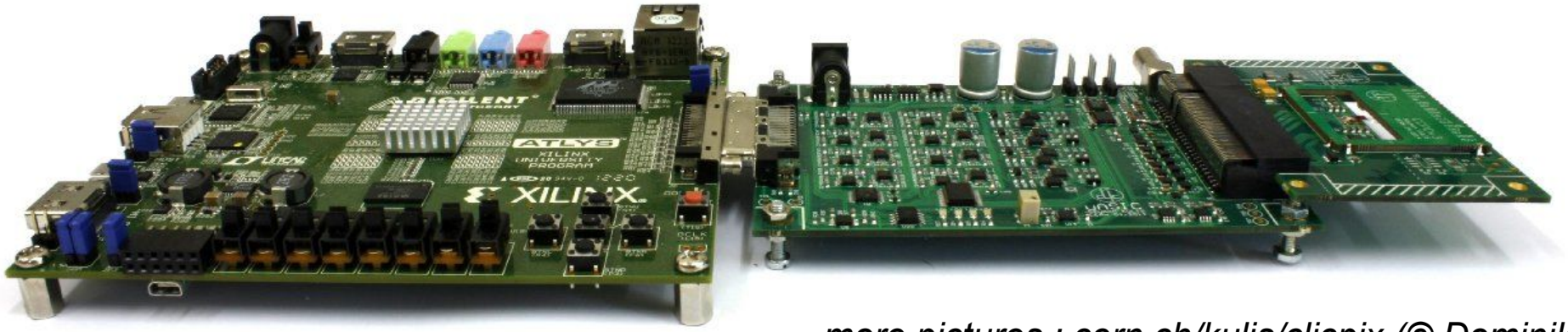
Basic CCPDV3 characterization



Agenda:
- Readout status
- Power consumption
- Pulse shape

Disclaimer: work in progress



more pictures : cern.ch/kulis/clicpix (© Dominik)

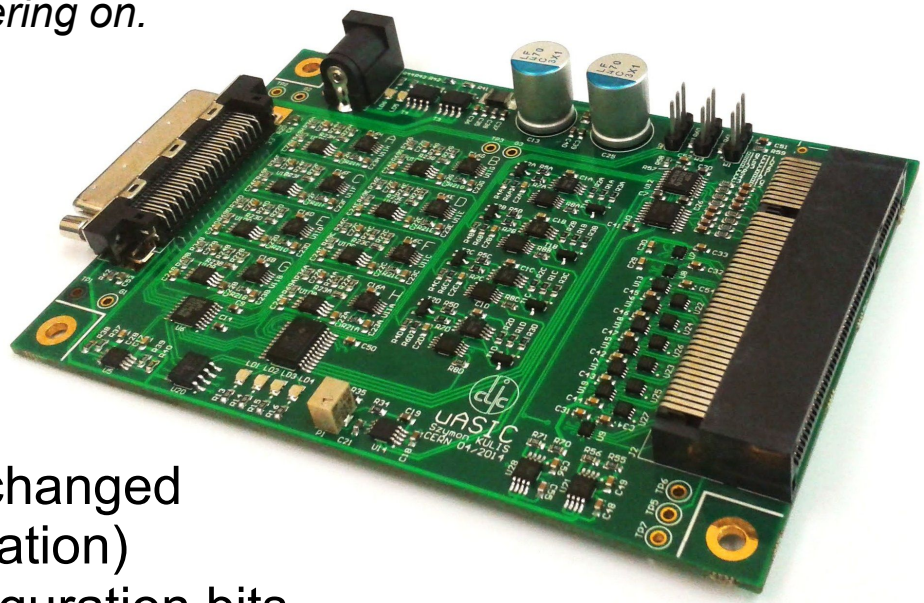
Readout status

Hardware status:

- minor bugs on interface board (were fixed using wires)
- test pulse signal missing on CCPDv3 board

  (signal is provided from external pulse generator)
- reset problem. After power cycling the FPGA board, supply voltage can be set to 4 V (destroying the chip).

  This behavior is caused by "feature" of one IC described in errata. To fix that for good, redesign is needed. Work around: let capacitors to discharge (>10s) before powering on.



Software:

- functional version exists

Chip interface:

- major configuration register can be changed (DAC values, analog output configuration)
- no knowledge about rest of the configuration bits

“Nominal” conditions

Power supply voltages:

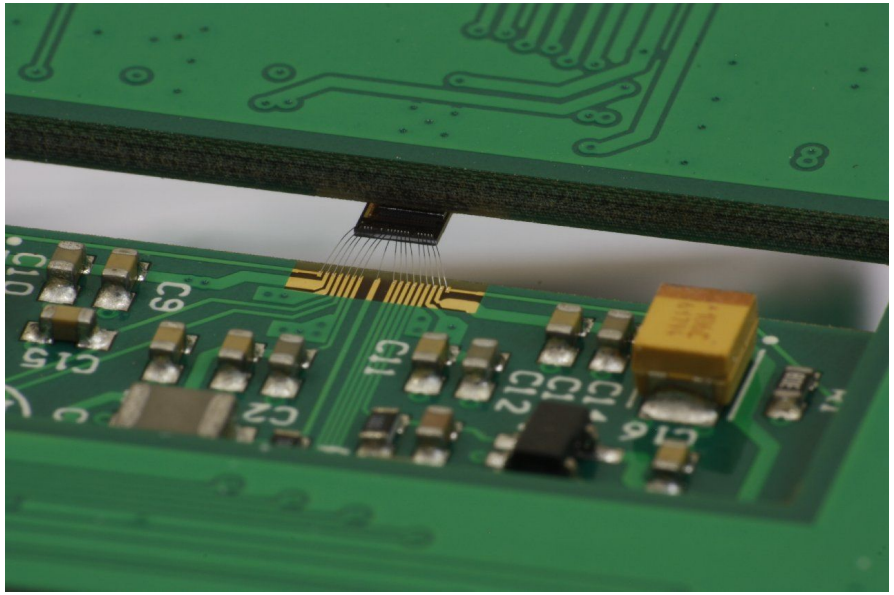
- VDDA 1.8 V (~3mA)
- VSSA 1.5 V (~43mA)
- VDD 1.8V (~0mA)

External voltages:

- VCAS 1.0 V
- TP 1.0 V
- BL 0.5V

DACs (used in CLIC part):

- BLres 1
- VNfb 1
- VNclic 63
- VNload 10
- VNfoll 10
  (is there a voltage follower after the preamp in CLIC part?)



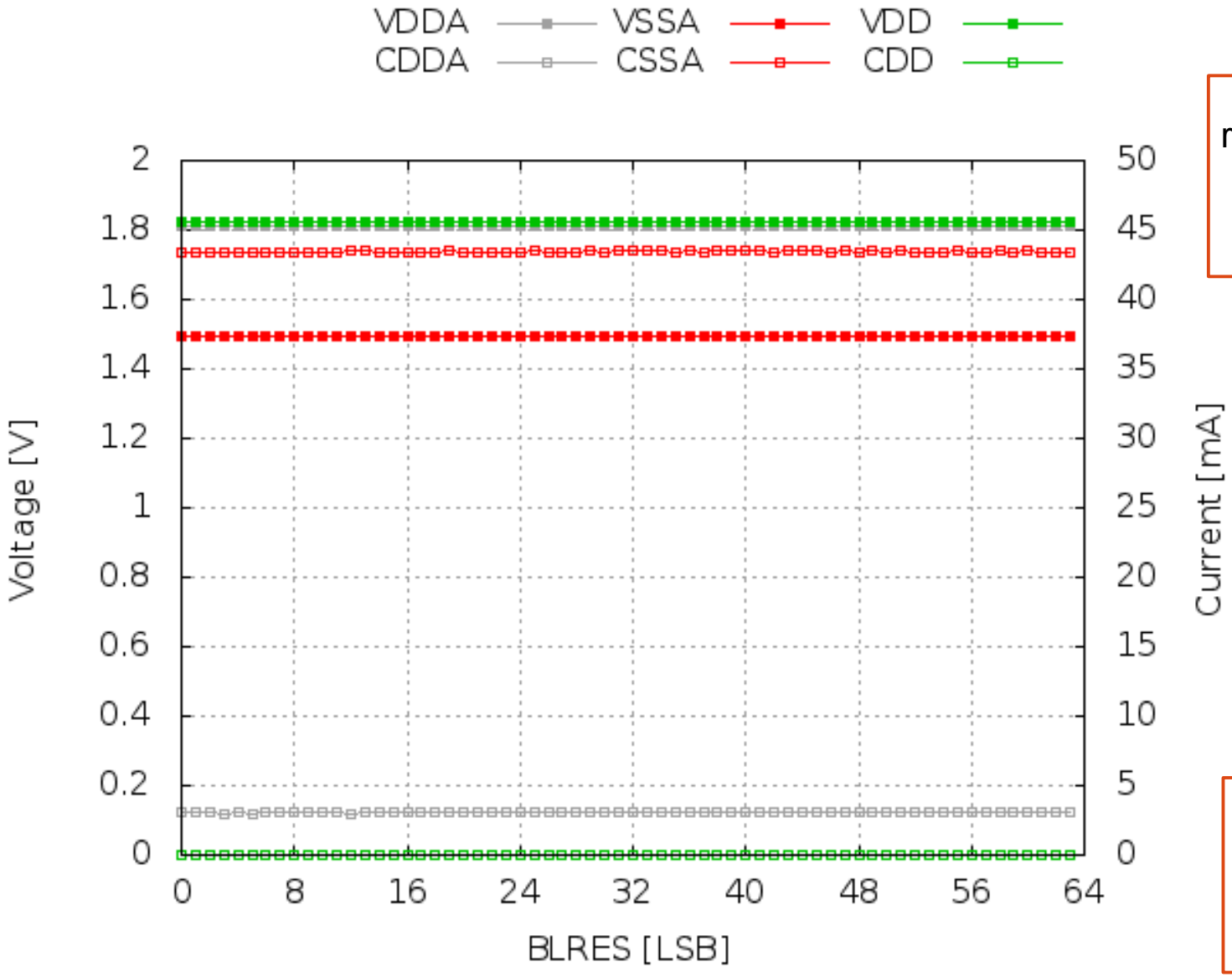
Remarks

- All measurement shown in flowing slides were obtained for chip board ID **001ec08a147f** (CCPDv3 only, no CLICpix)
- Test pulses frequency: **1 kHz**
- High Voltage: **-50 V**
- Why test pulse amplitude is expressed in V not in fC or electrons? The value of injection capacitance has not been extracted from the layout. Conversion factor taken from CCPM measurements is around 3.2 ke/V +/- 20 % ;)

CCPDv3 – DAC scans

- Chip doesn't have an analog output from DACs (like chips from Medipix family) → the only available observable is supply current

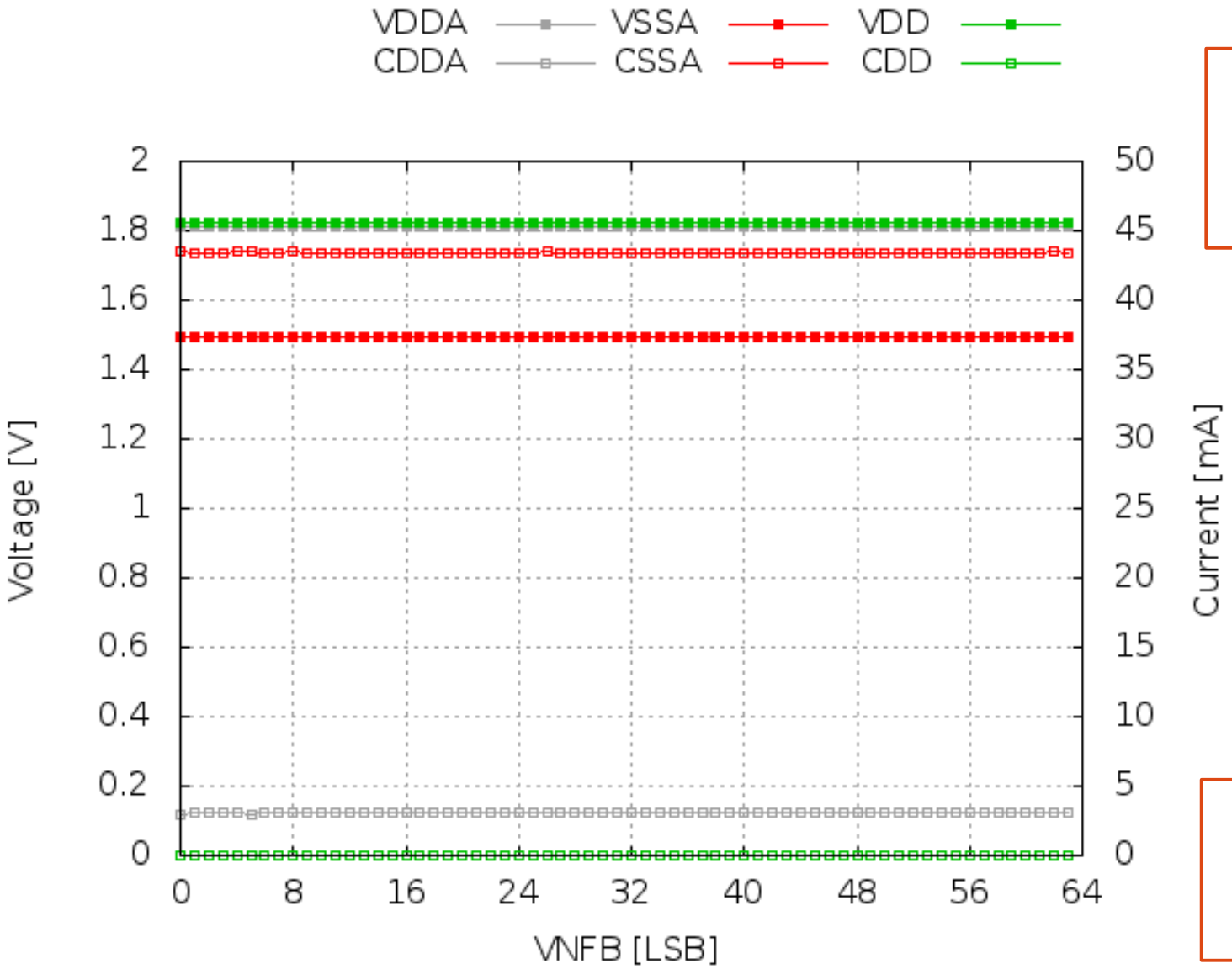
CCPDv3 – BLres



BIres controls resistance of coupling resistance between 1st and 2nd stage (to be confirmed)

BIres doesn't influence supply current (as expected)

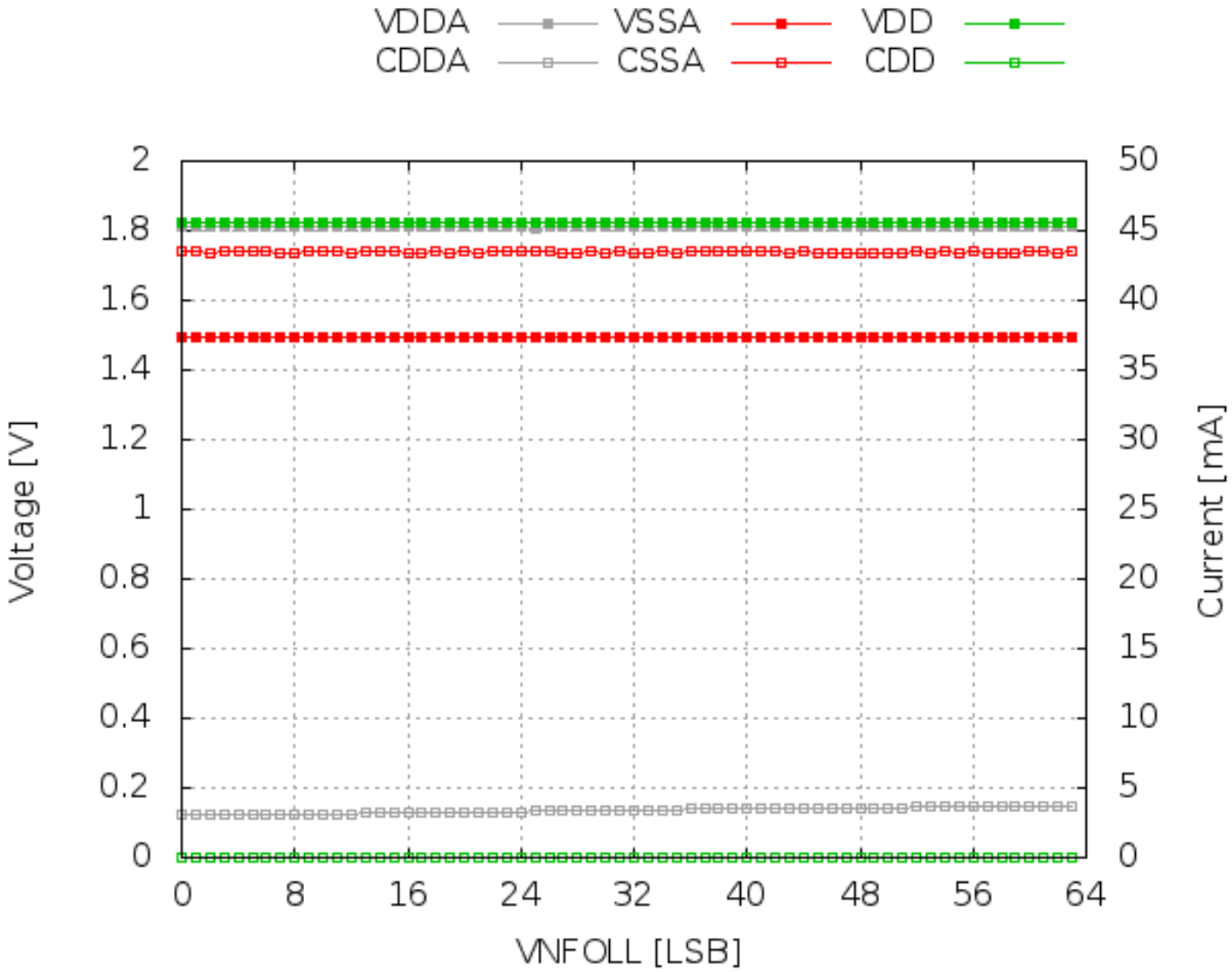
CCPDv3 – VNfb



VNfb controls resistance of substrate bias resistance (to be confirmed)

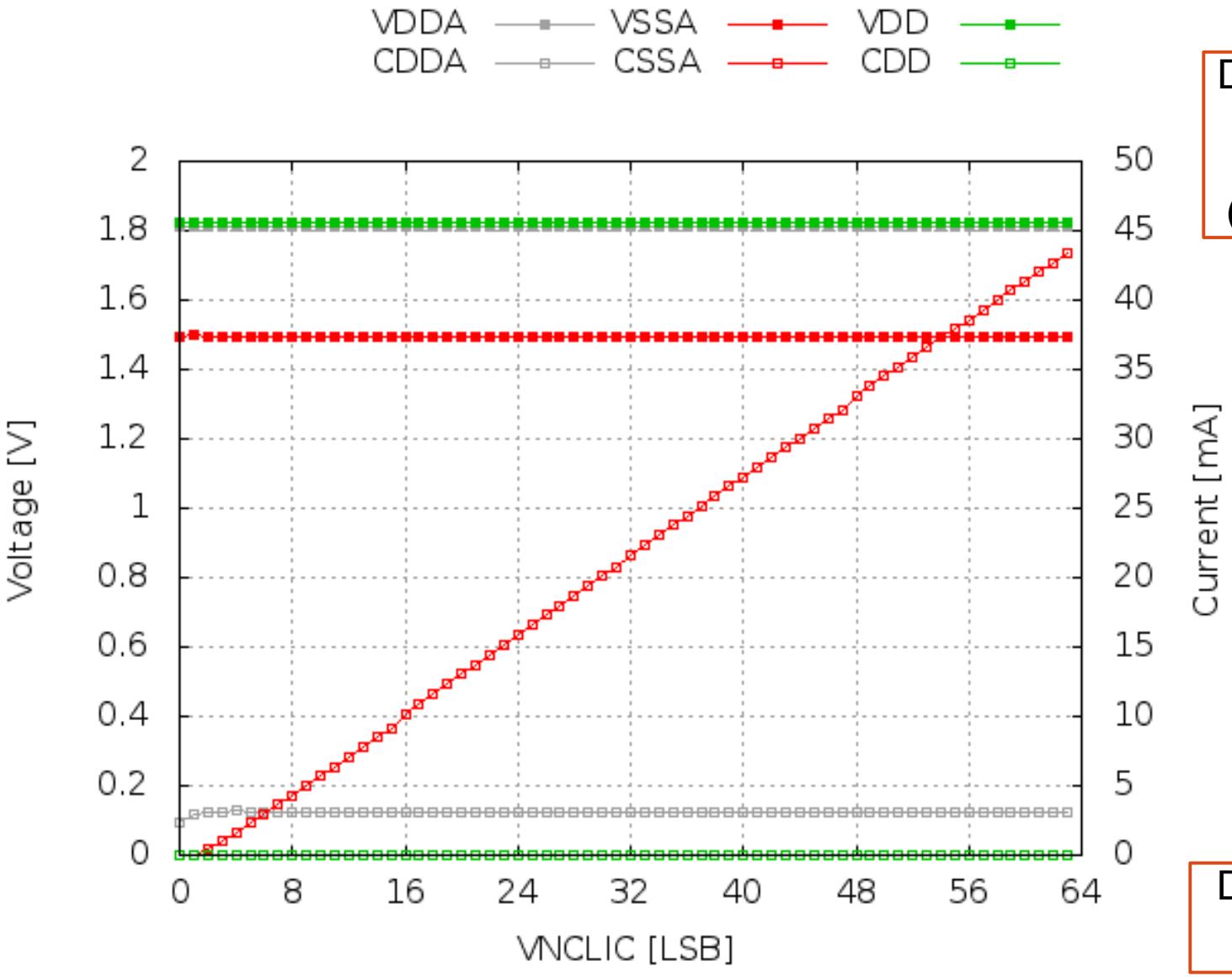
VNfb doesn't influence supply current (as expected)

CCPDv3 – VNfoll



VNfoll controls current of the voltage follower stage after the preamplifier (to be confirmed)

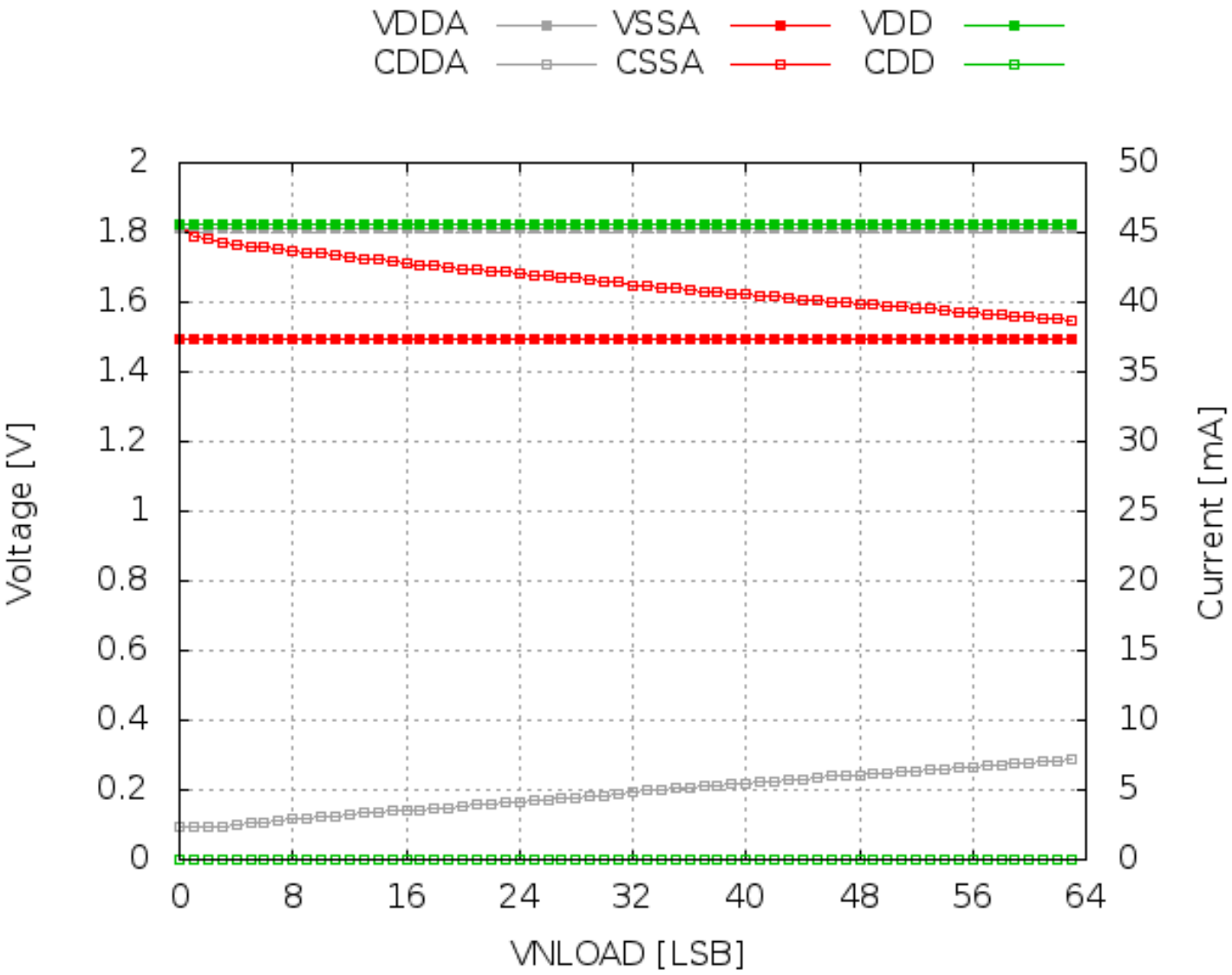
CCPDv3 – VNclic



DAC controls bias current of the preamplifier (to be confirmed)

DAC is quite linear, INL < 1 LSB

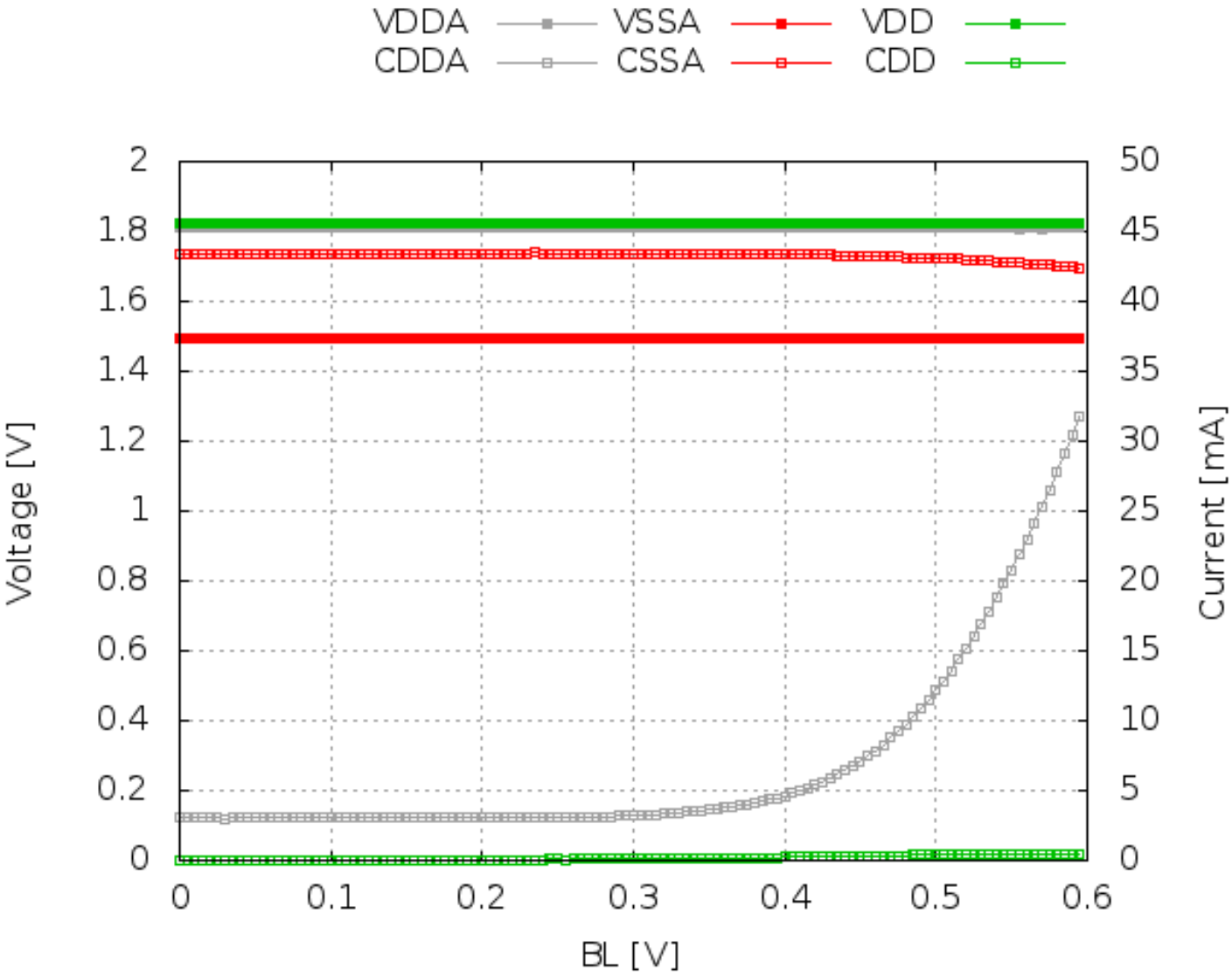
CCPDv3 – VNload



VNload controls current of the cascode stage in preamplifier (to be confirmed)

DAC is quite linear

CCPDv3 – BL



BL controls operating point of the second stage amplifier (to be confirmed)

BL is delivered as an external voltage (not internal DAC)

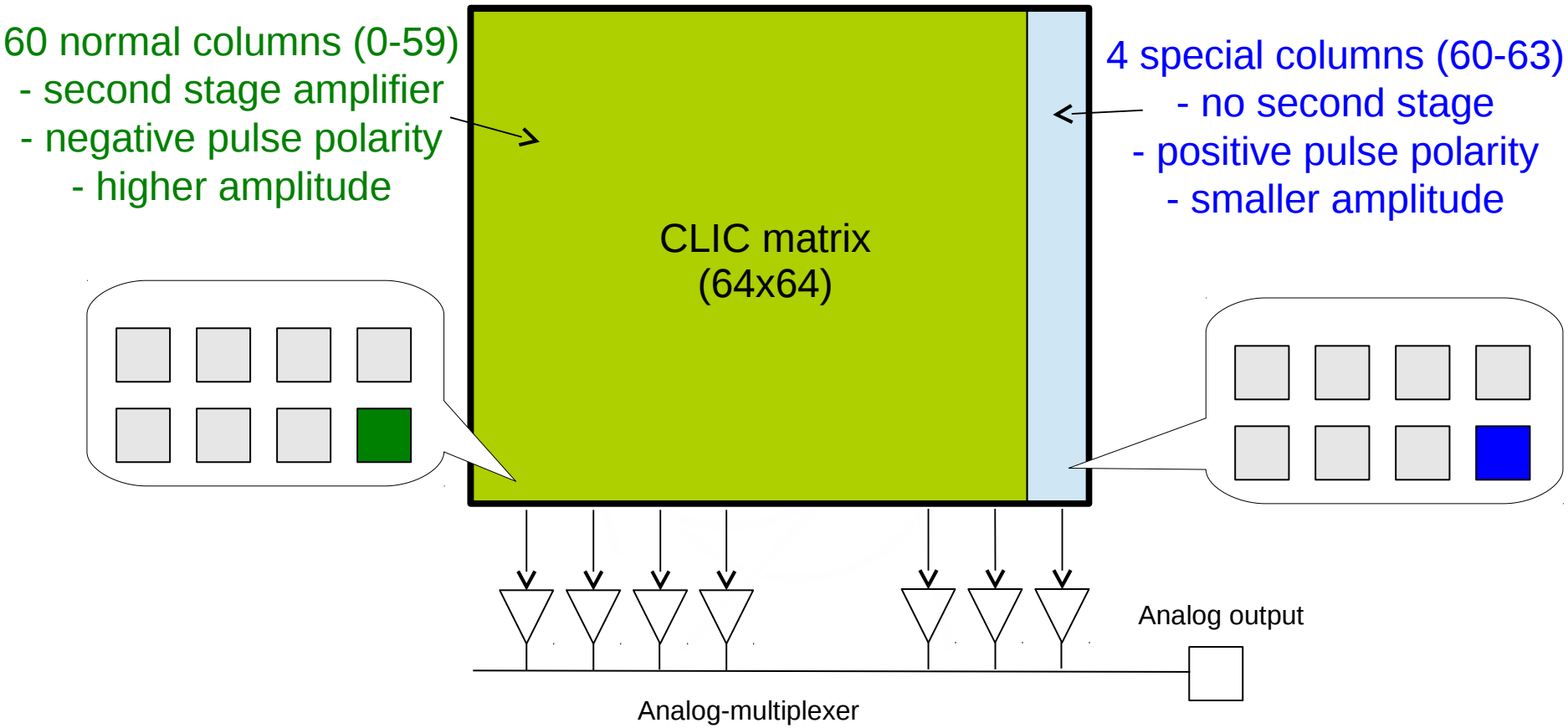
Characteristic looks fairly typical

DAC Scans - conclusions

- DAC scan exercise shows that we are able to control DACs
- Qualitative result: curves are reasonable
- Quantitative result: INL is <1 LSB for VNclic DAC

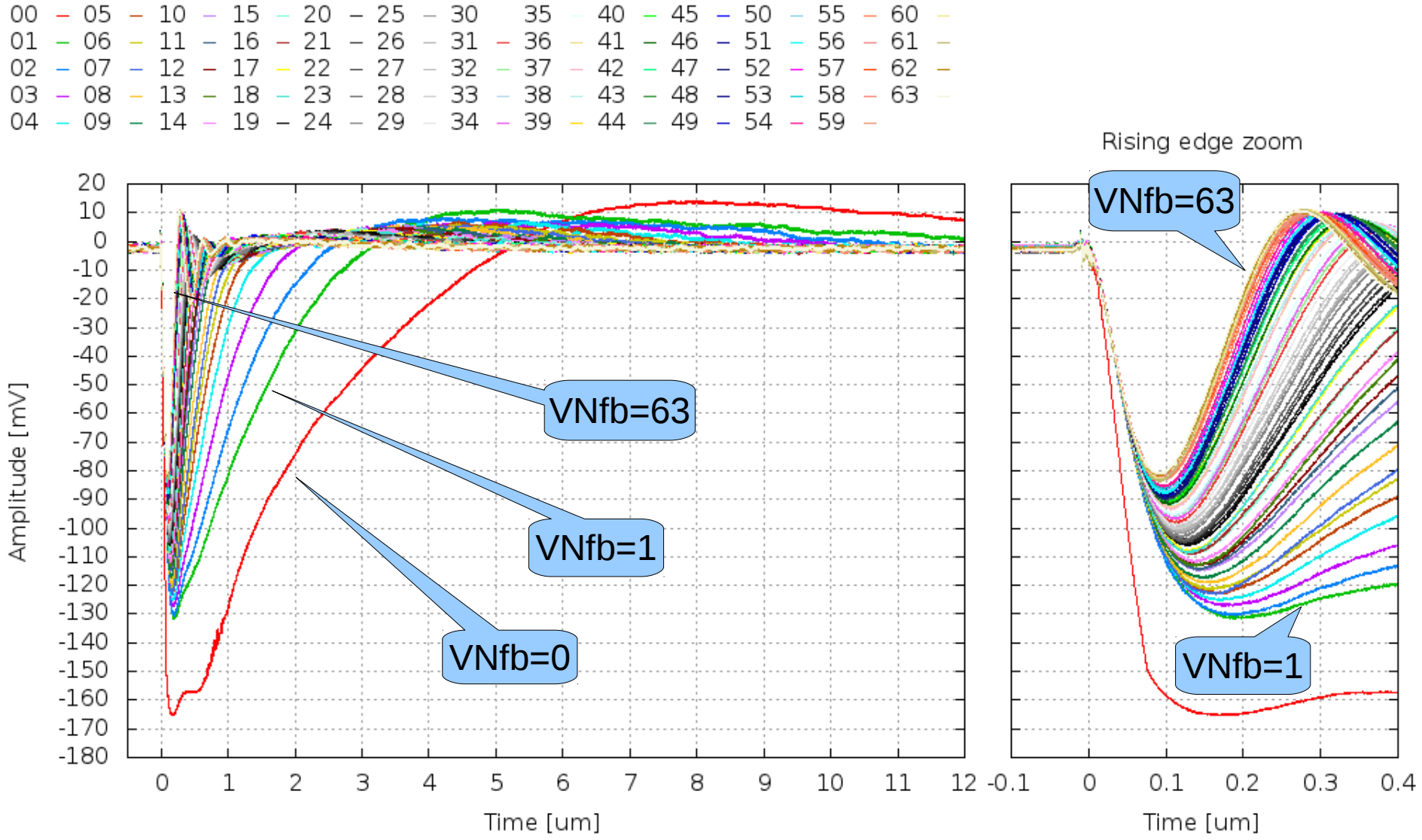
- Are the absolute current consumption values reasonable?

Monitoring amplifier output

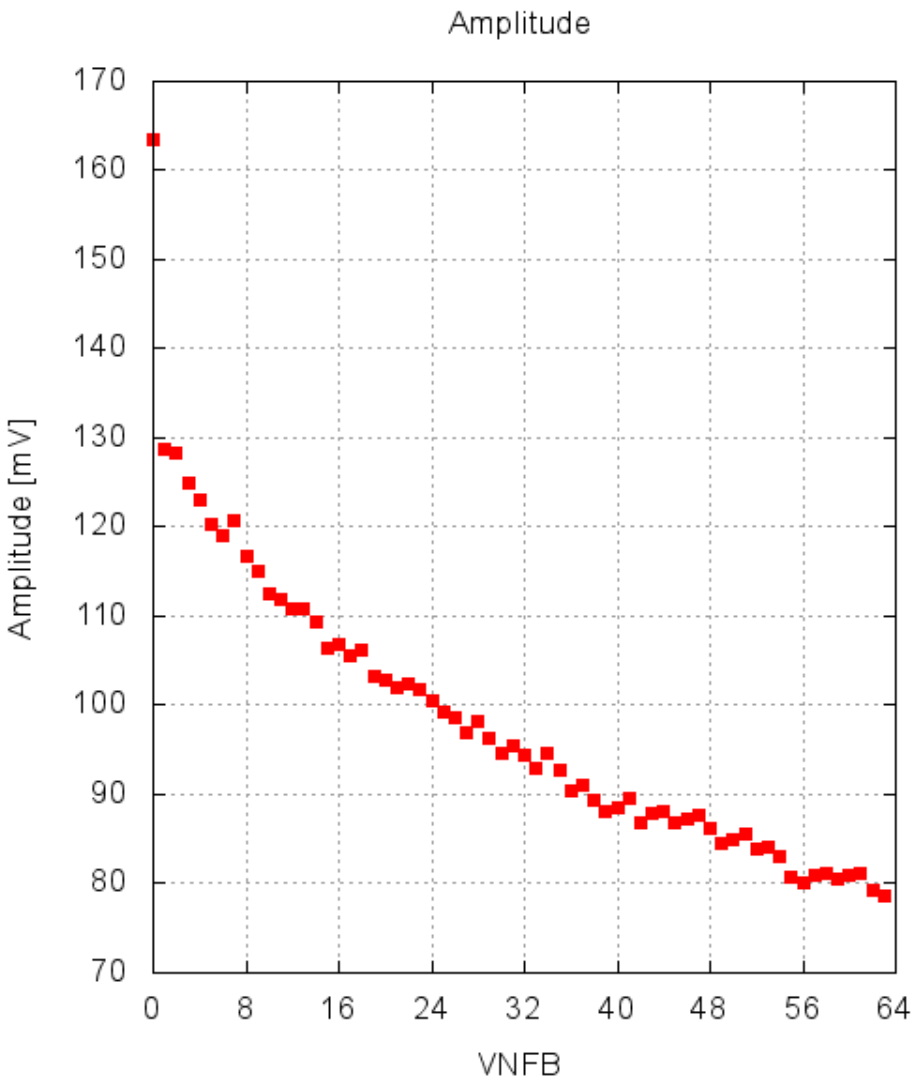


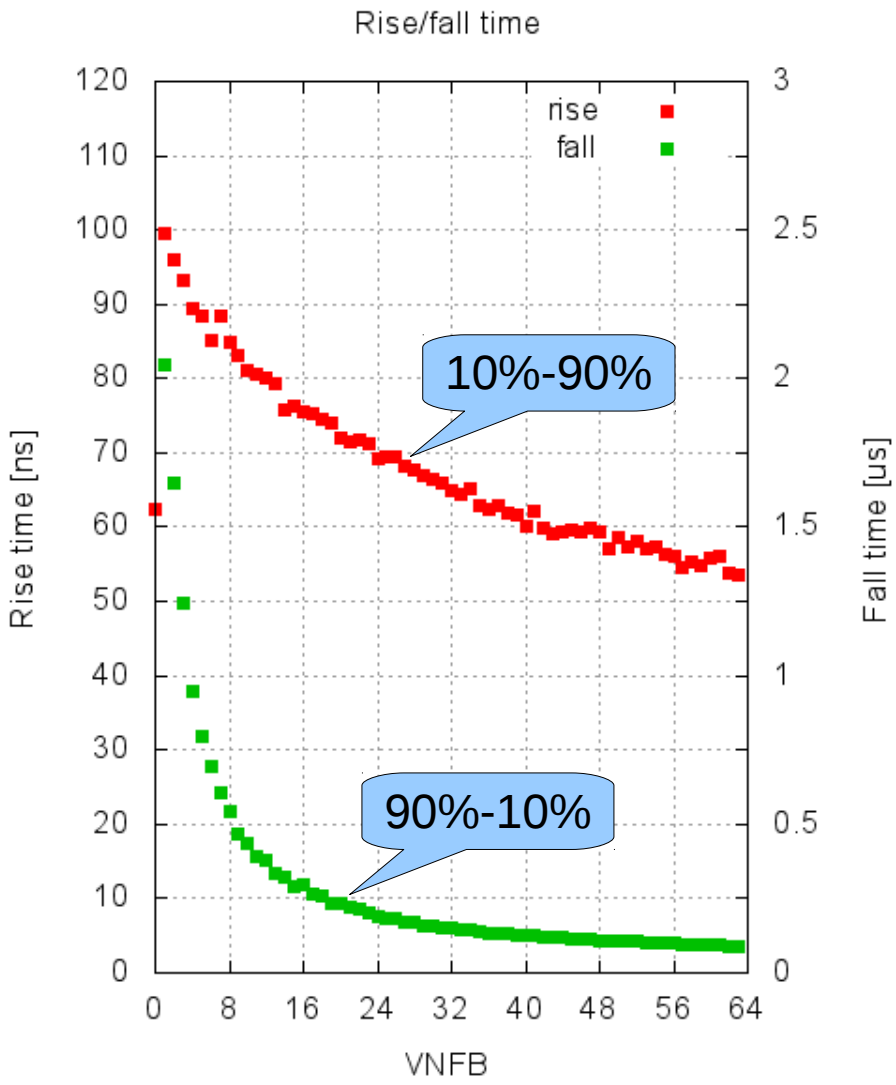
- We can monitor 15 normal pixels: (3,63), (7,63), (11,63) … (59,63) and one special pixel (63,63).
- Analog multiplexer is controled by configuration register (16 bits out of 336).
- Analog output is buffered on CCPD board and sent to fast sampling osciloscope.

Standard pixel response (35,63) | Waveforms

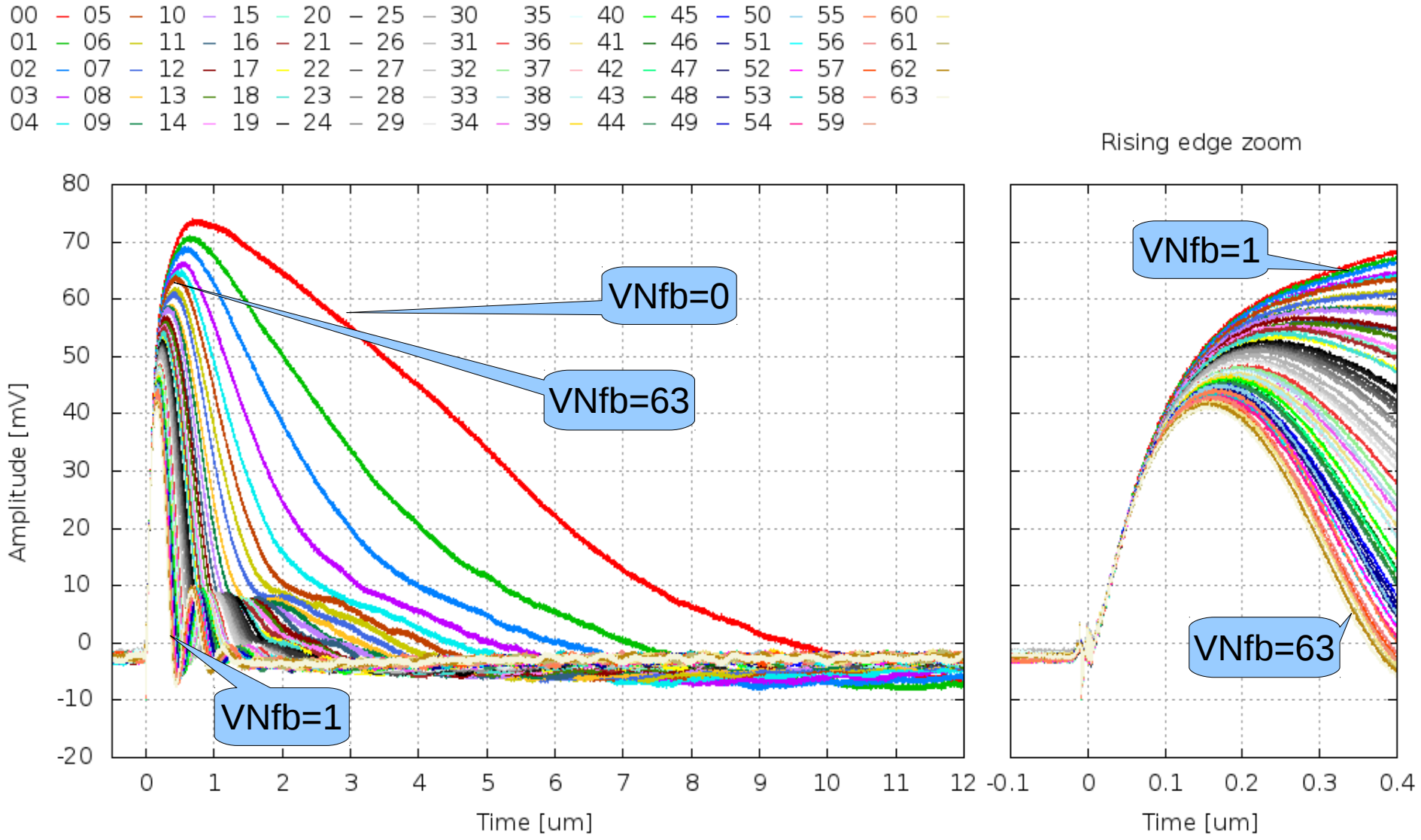


Standard pixel response (35,63) | Measurements

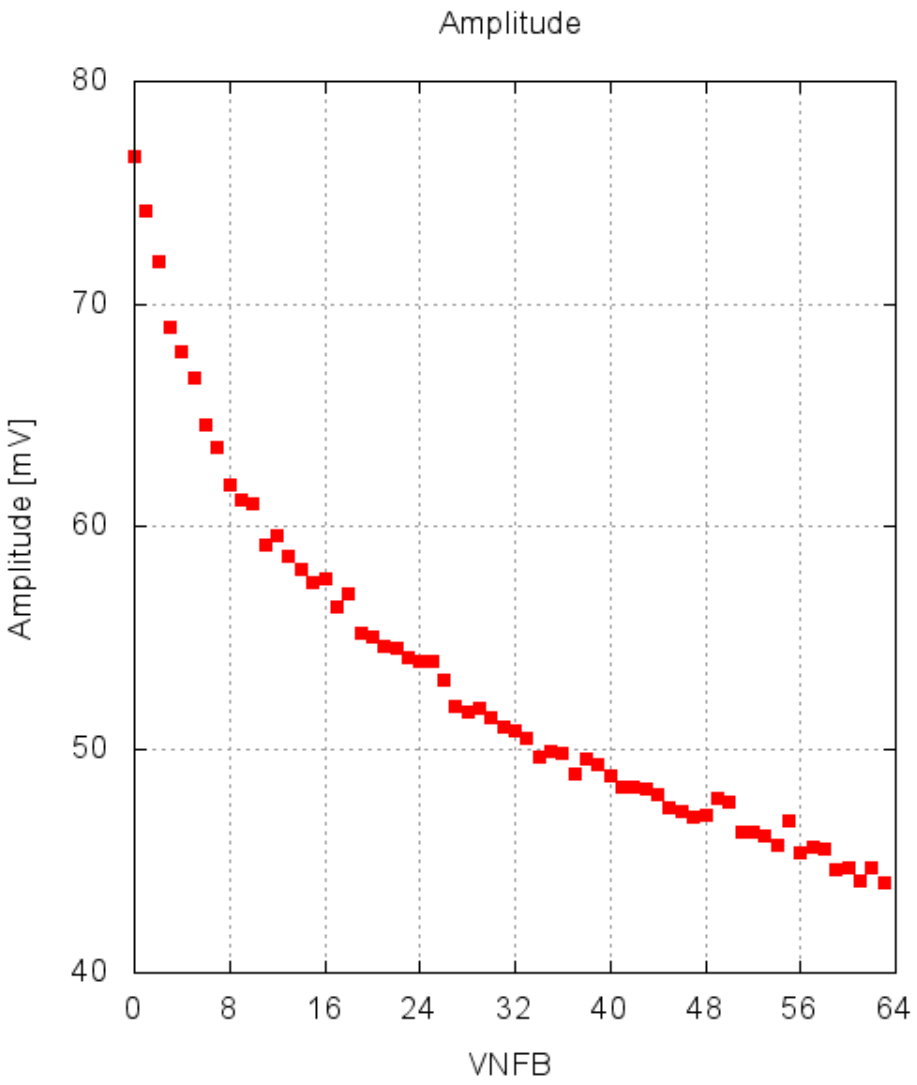


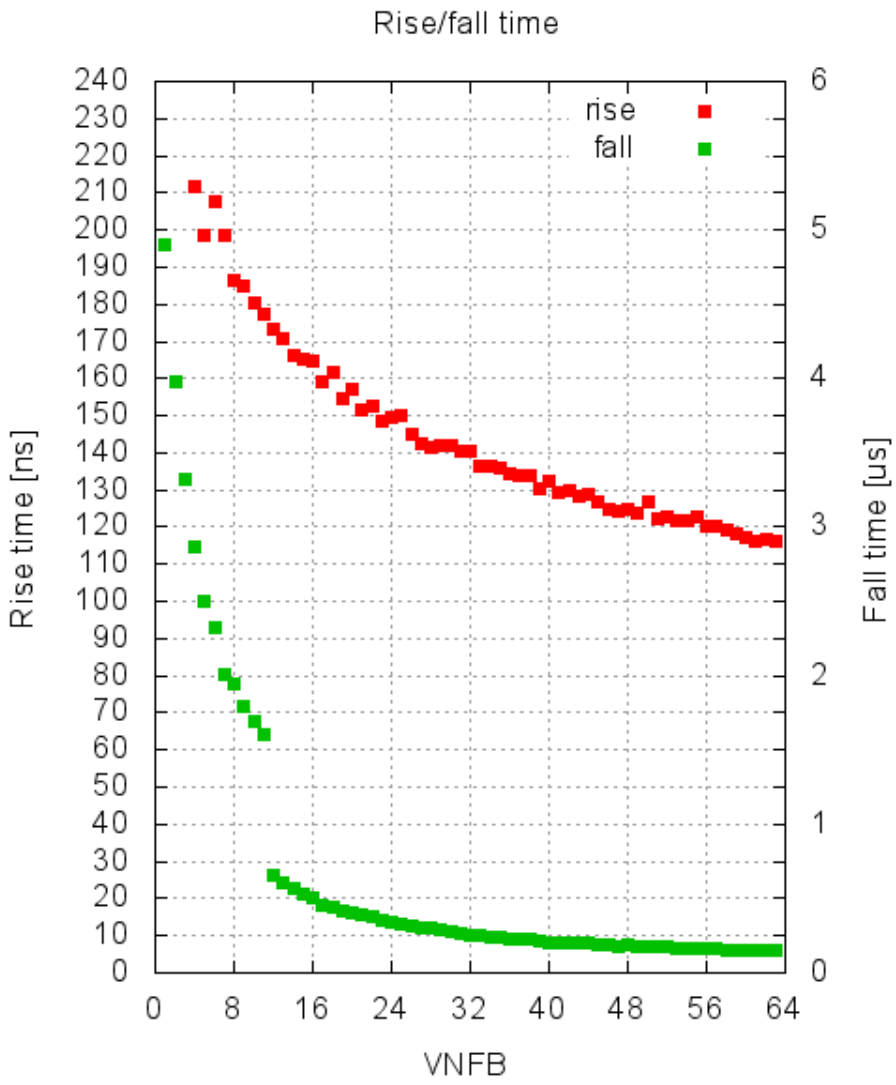


Special pixel response (63,63) | Waveforms



Special pixel response (63,63) | Measurements



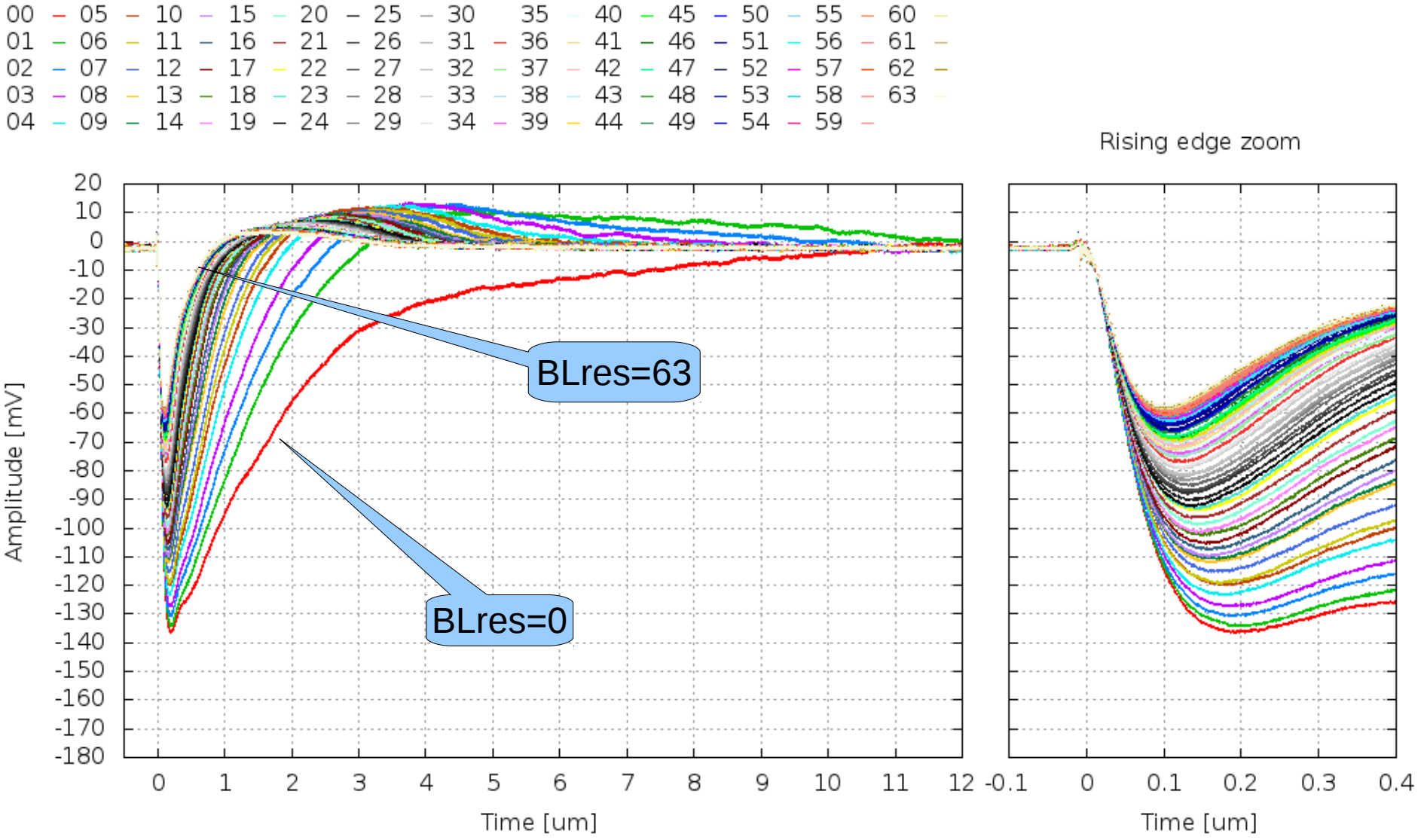


Pixel responses

- Special pixel has smaller gain than standard pixel
  (as expected)
- Standard pixel has larger undershoot (to be expected)
  → most likely due to additional zero in the transfer function
- Standard pixel returns to zero faster
  → most likely due to additional zero in the transfer function

  So … lets try to vary BLres

Special pixel response (35,63) | Waveforms

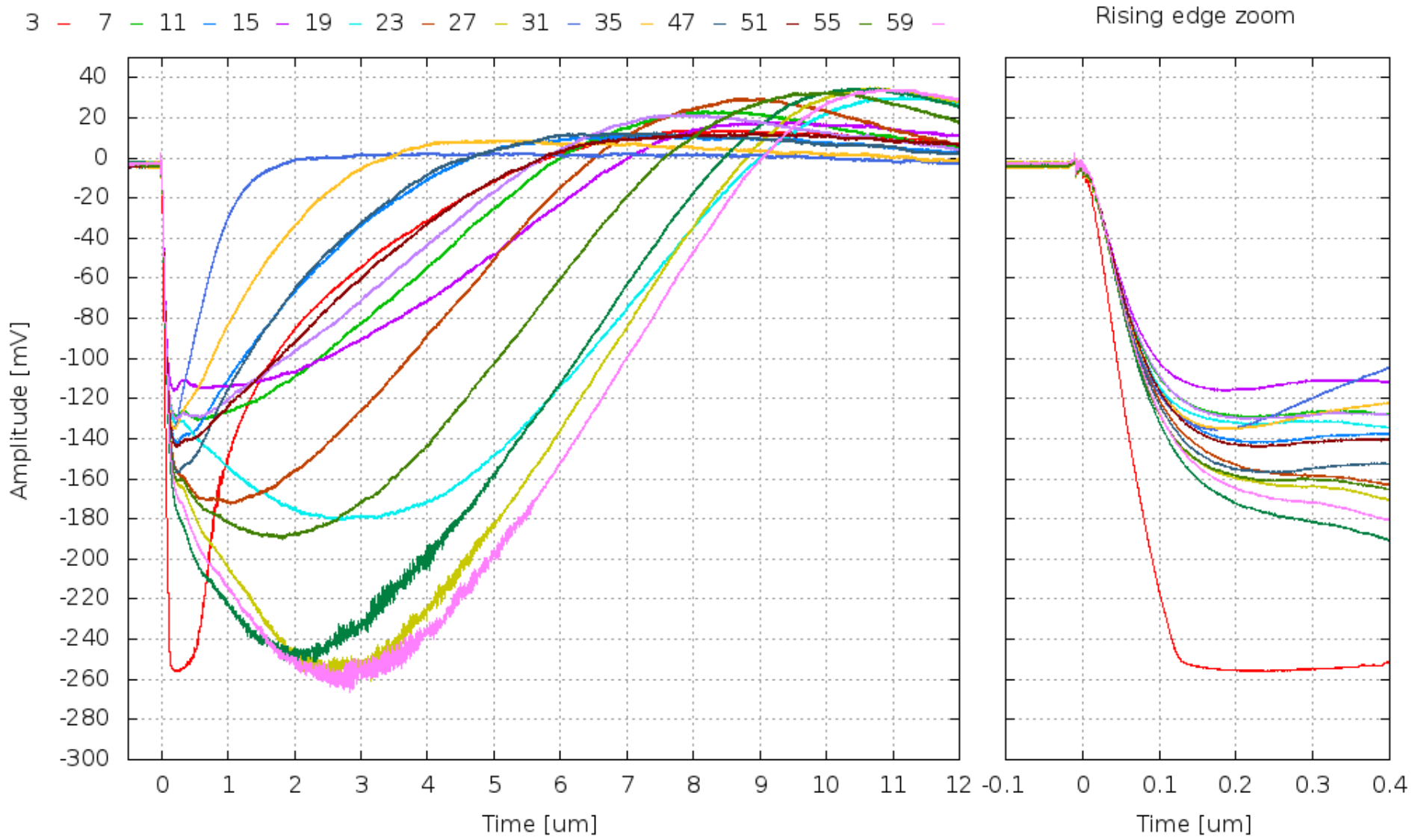


Pixel responses

- Impact of BLres is very similar to Vnfb (as expected)
  (it changes position of the zero in the transfer function,
  smaller value of DAC → smaller current → higher resistance → lower cutoff frequency → longer pulse)
- It has also quite significant impact on pulse amplitude
- Remark : small BLres → higher bandwidth → higher noise (possibly smaller SNR, too be verified)

So far so good, two types of pixels look fine, impact of DAC settings on pulse shape can be explained.

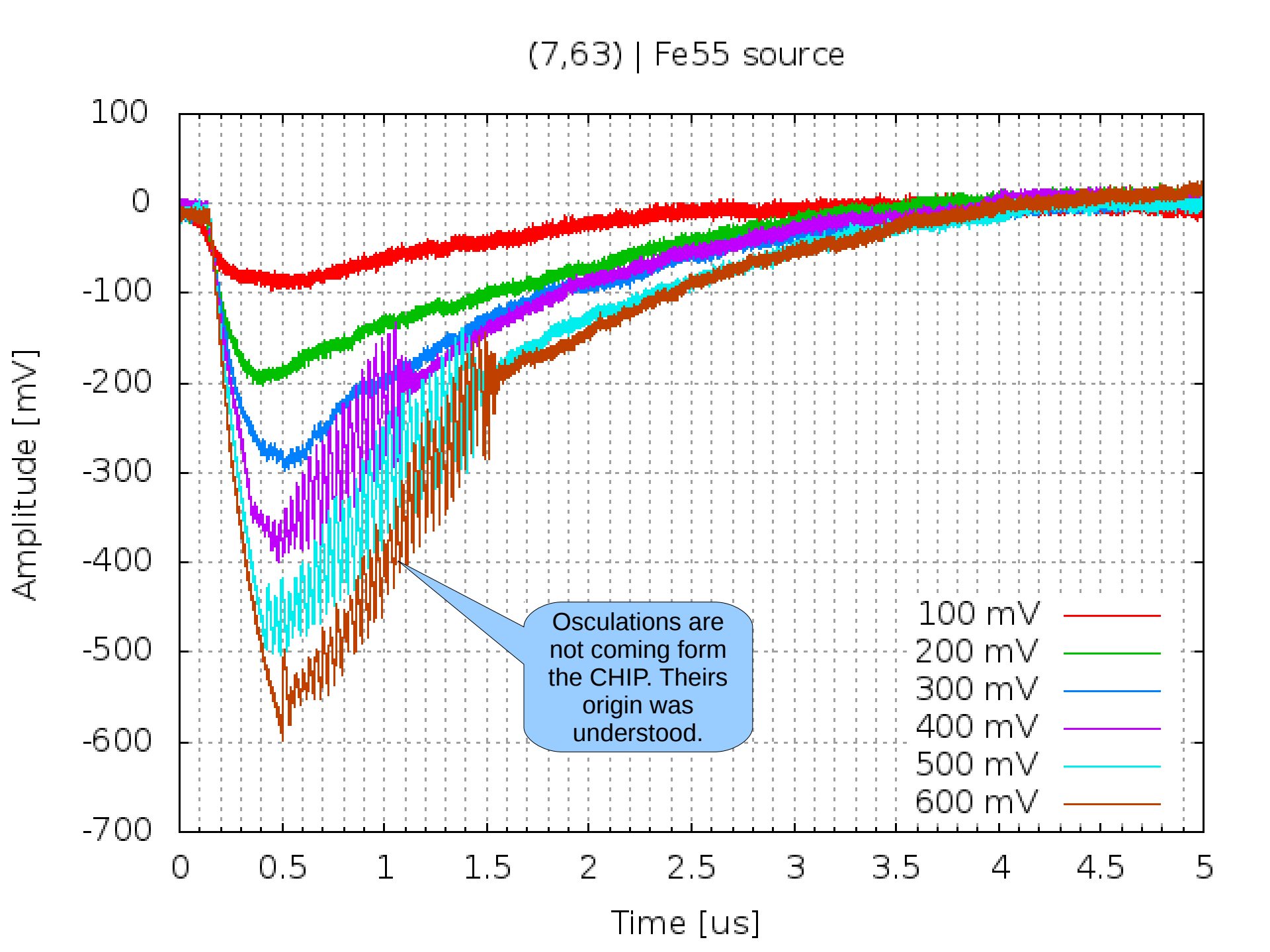
Pixel responses | various pixels from row 63

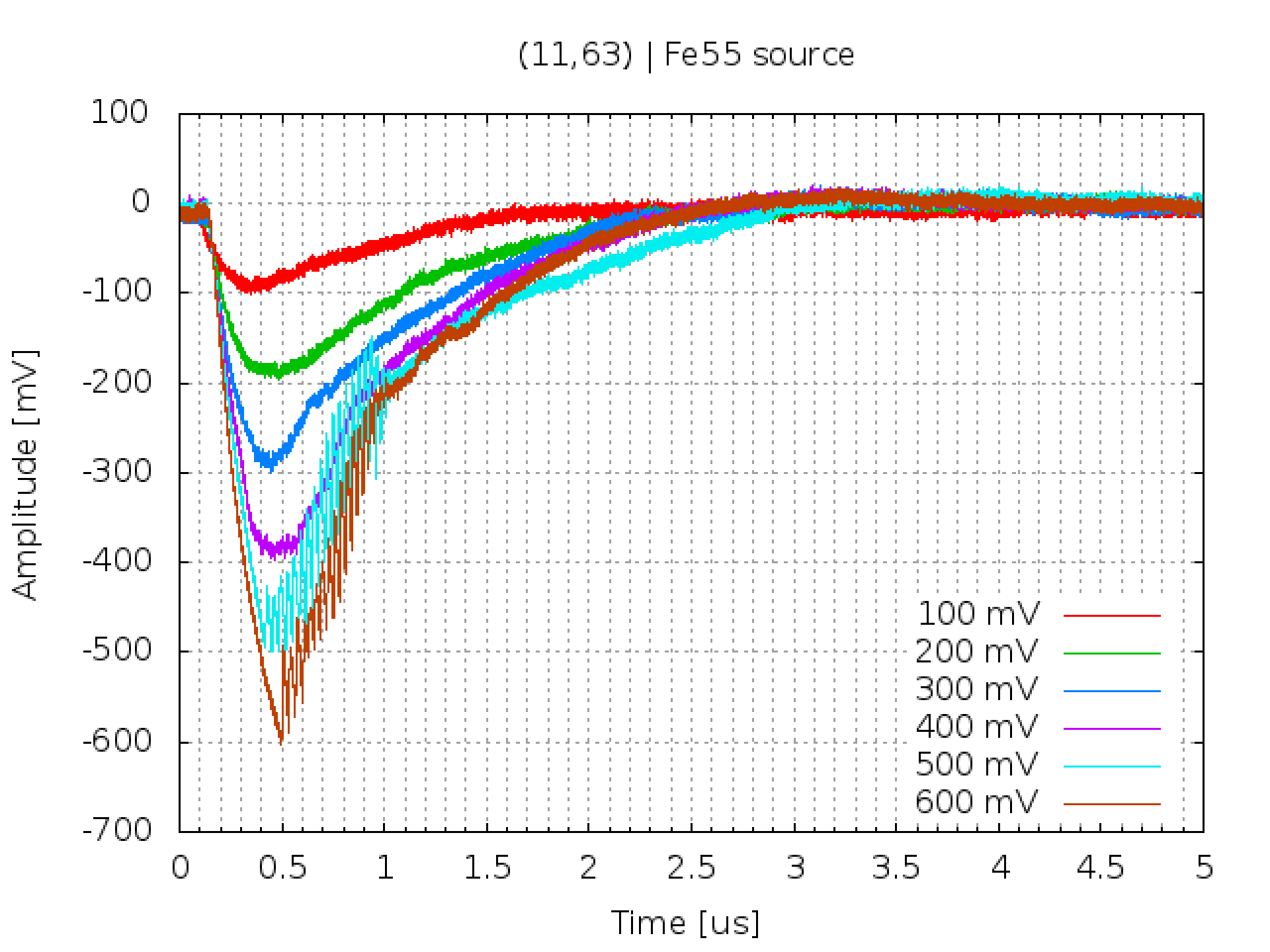


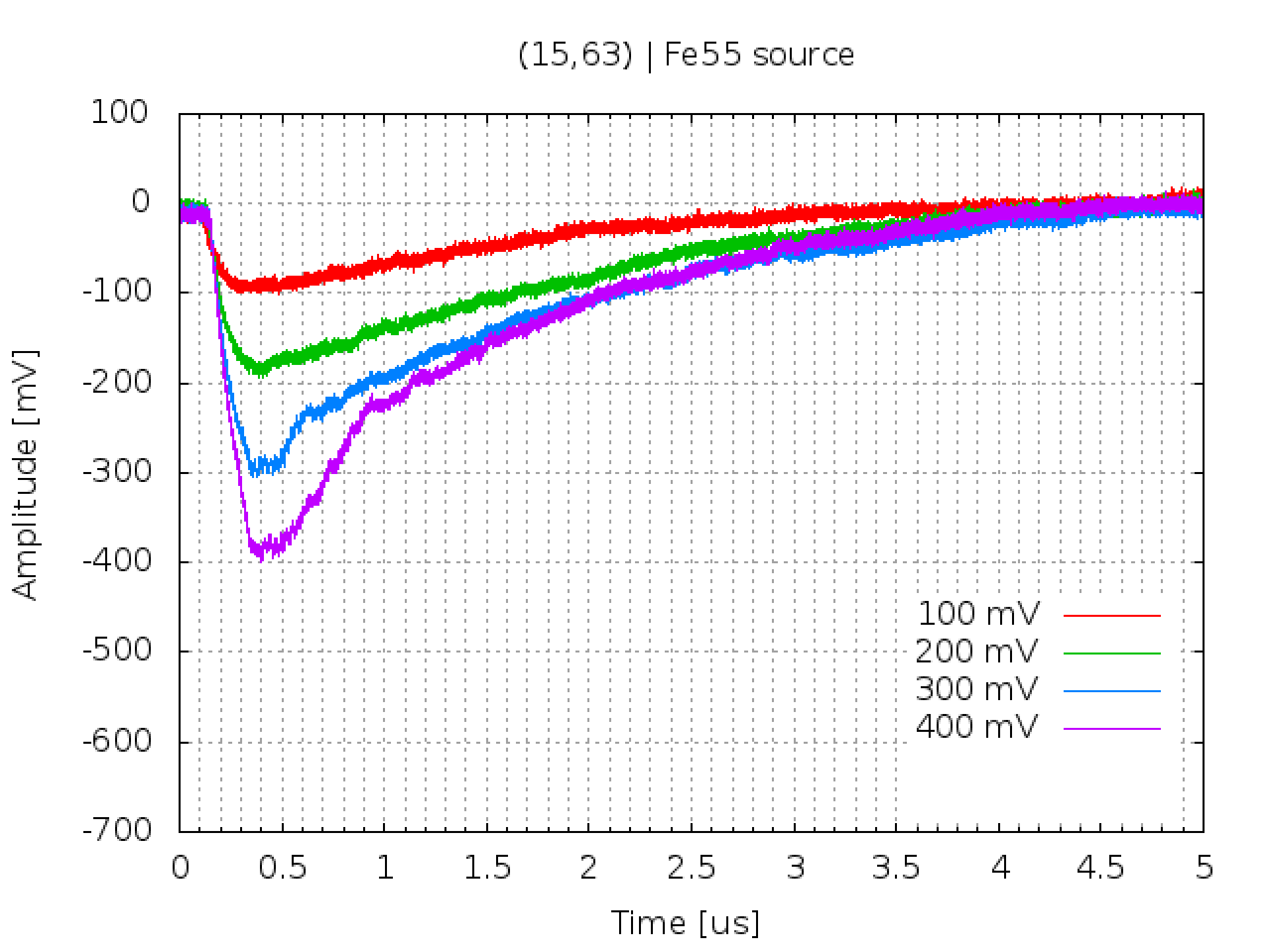
Pixel responses

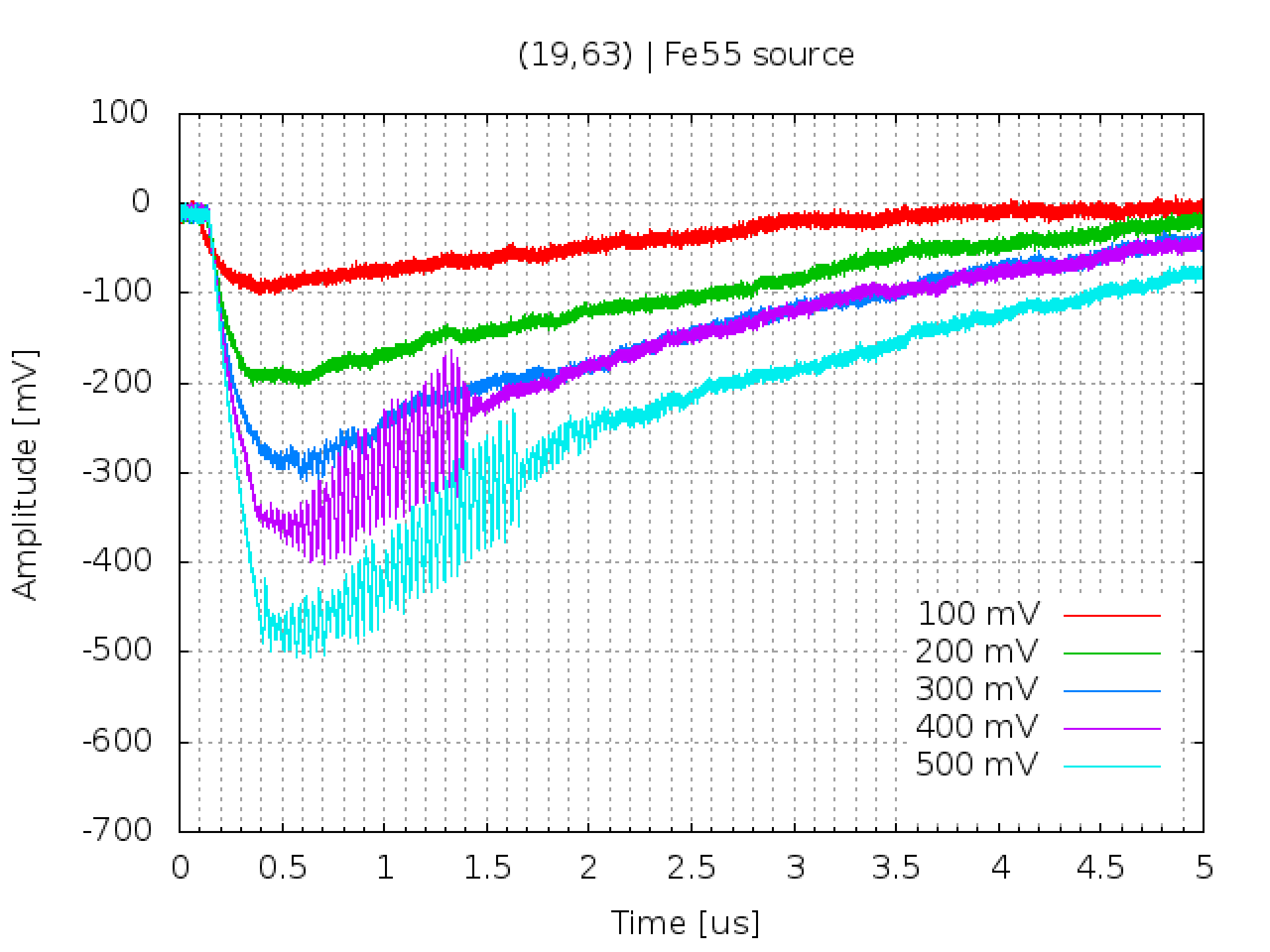
- Only 3-4 channels (out of 15) look reasonable
- Enormous gain variation (120 mV – 260 mV)
  remark: can be caused be a mismatch of injection capacitance
- Enormous shape variation
  probably can not be explained easily by (few %) mismatch in transistors / passives dimensions → MC simulation would be needed to confirm that.

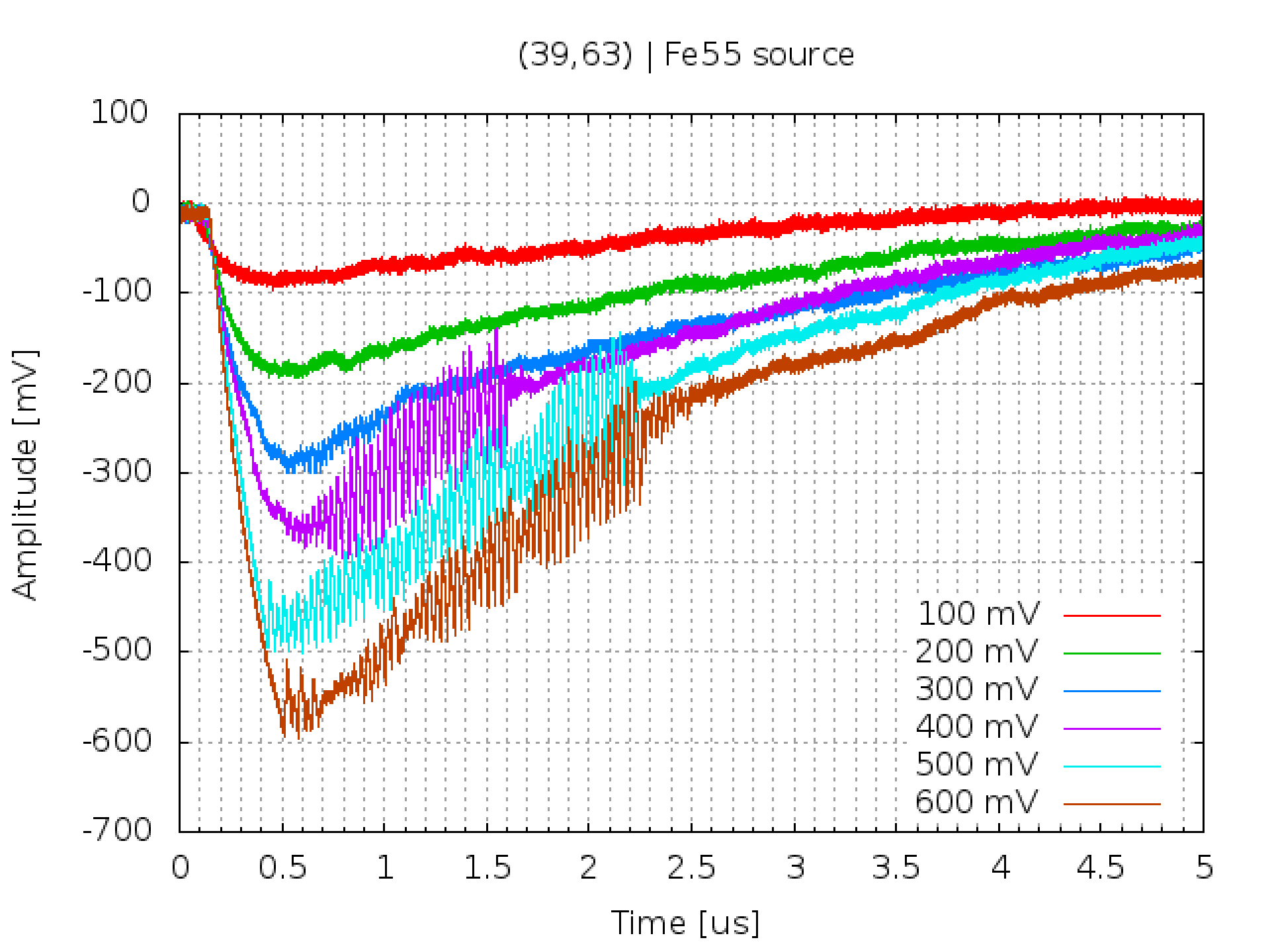
  Slew rate of the preamplifier is similar for all channels (besides channel 3), which suggests that preamplifier for various pixels behave in similar way.
- Is this effect real? Will we see it also with particles?
  On next slides you can see pixel responses with various amplitudes obtained with Fe55 source (curve selection was done based on output amplitude, as the input charge for individual events is not known)

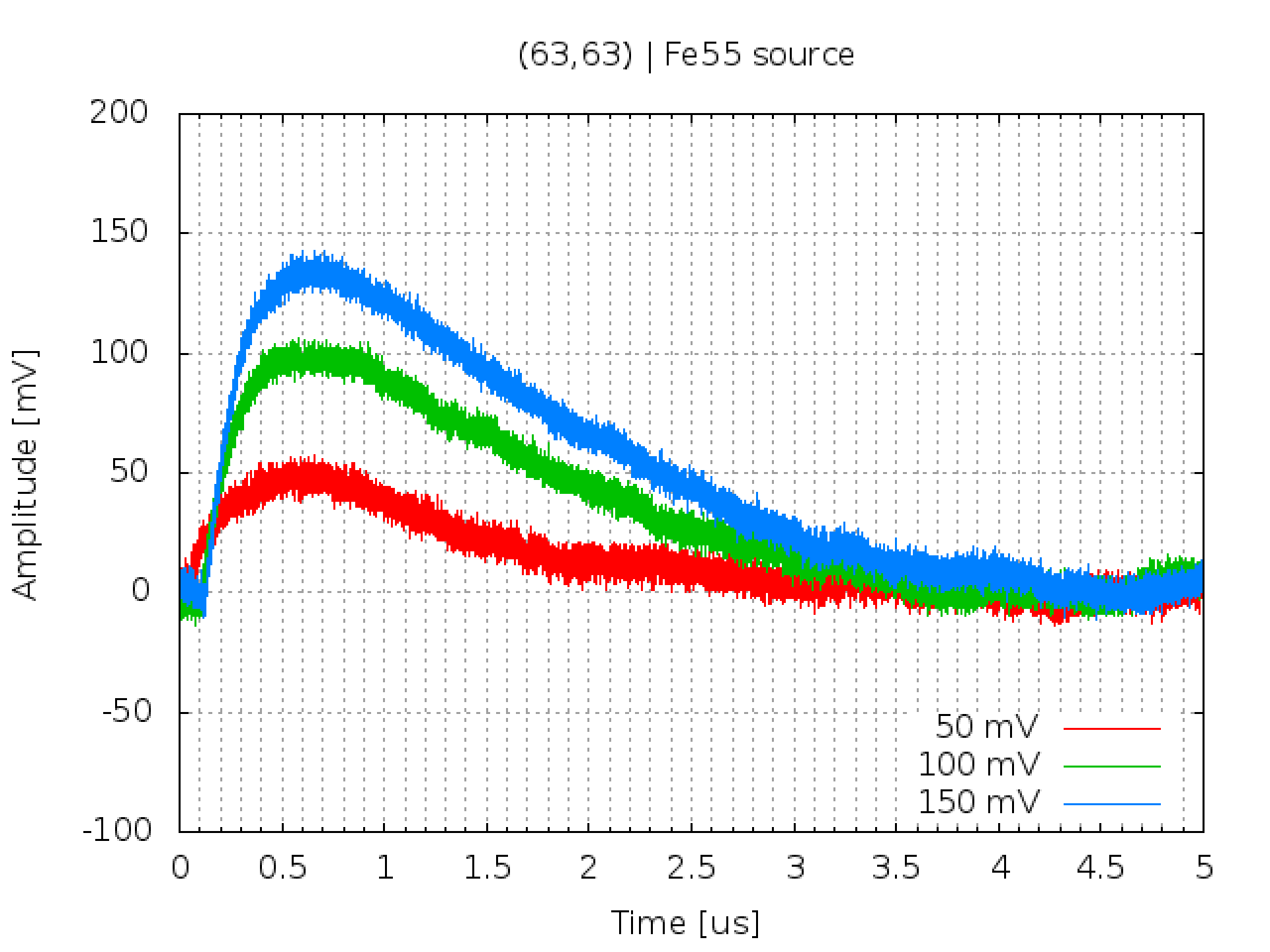

(7,63) | Fe55 source
Amplitude [mV]
Time [us]
100
0
-100
-200
-300
-400
-500
-600
-700
0
0.5
1
1.5
2
2.5
3
3.5
4
4.5
5
100 mV
200 mV
300 mV
400 mV
500 mV
600 mV
Osculations are not coming form the CHIP. Theirs origin was understood.


(11,63) | Fe55 source
100
0
-100
-200
-300
-400
-500
-600
-700
Amplitude [mV]
0
0.5
1
1.5
2
2.5
3
3.5
4
4.5
5
Time [us]
100 mV
200 mV
300 mV
400 mV
500 mV
600 mV


(15,63) | Fe55 source
100
0
-100
-200
-300
-400
-500
-600
-700
Amplitude [mV]
0
0.5
1
1.5
2
2.5
3
3.5
4
4.5
5
Time [us]
100 mV
200 mV
300 mV
400 mV


(19,63) | Fe55 source
Amplitude [mV]
Time [us]
100
0
-100
-200
-300
-400
-500
-600
-700
0
0.5
1
1.5
2
2.5
3
3.5
4
4.5
5
100 mV
200 mV
300 mV
400 mV
500 mV


(39,63) | Fe55 source
Amplitude [mV]
Time [us]
100
0
-100
-200
-300
-400
-500
-600
-700
0
0.5
1
1.5
2
2.5
3
3.5
4
4.5
5
100 mV
200 mV
300 mV
400 mV
500 mV
600 mV

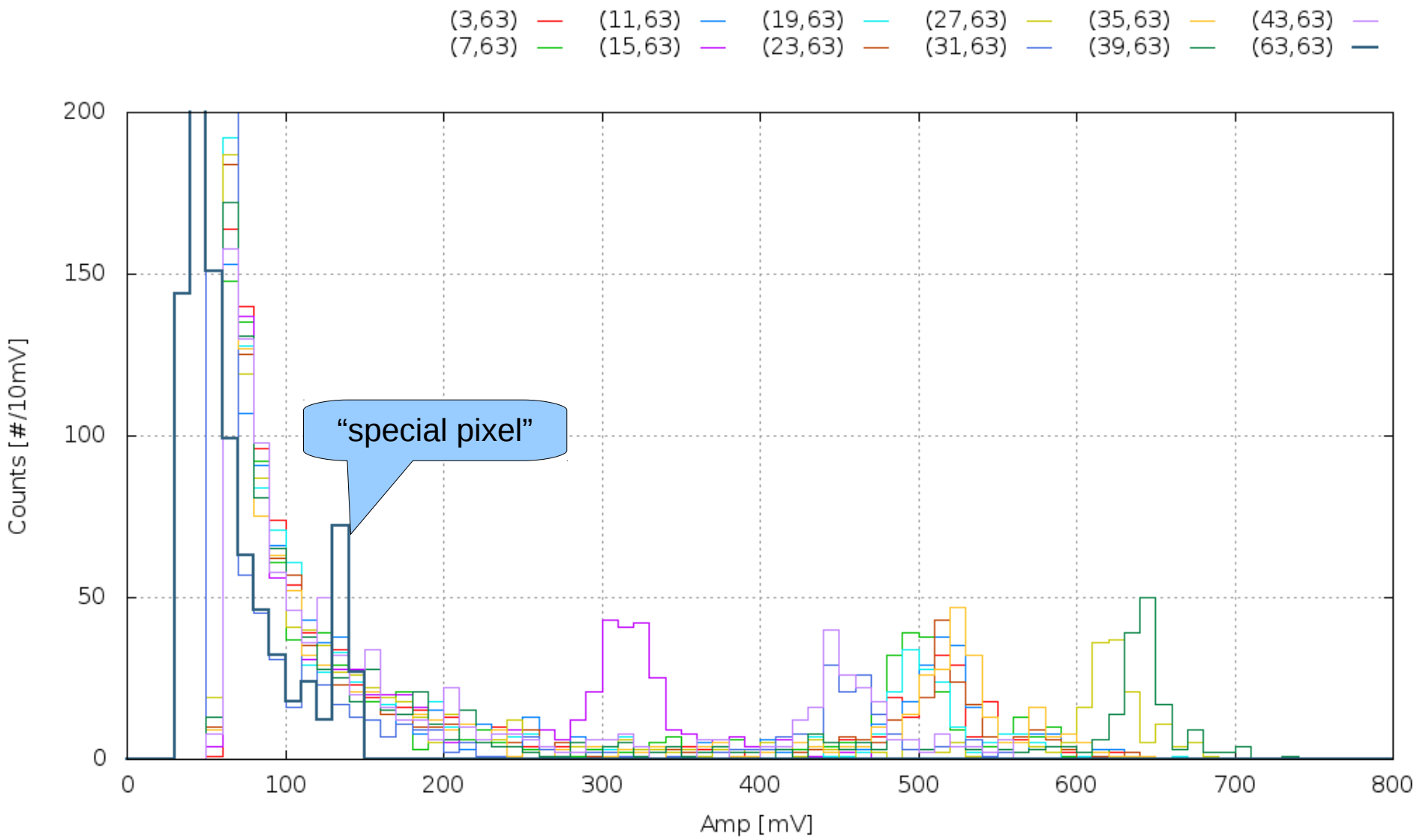

(63,63) | Fe55 source
Amplitude [mV]
Time [us]
200
150
100
50
0
-50
-100
0
0.5
1
1.5
2
2.5
3
3.5
4
4.5
5
50 mV
100 mV
150 mV

Pixel responses

- Shape variation is smaller than for the measurement with test pulse. However, fall time (return to baseline) still varies significantly (more than factor of 3 between pixels).

- Let try to make histogram of the amplitudes (minimum value) for 1000 collected events

Fe55 spectrum for various pixels

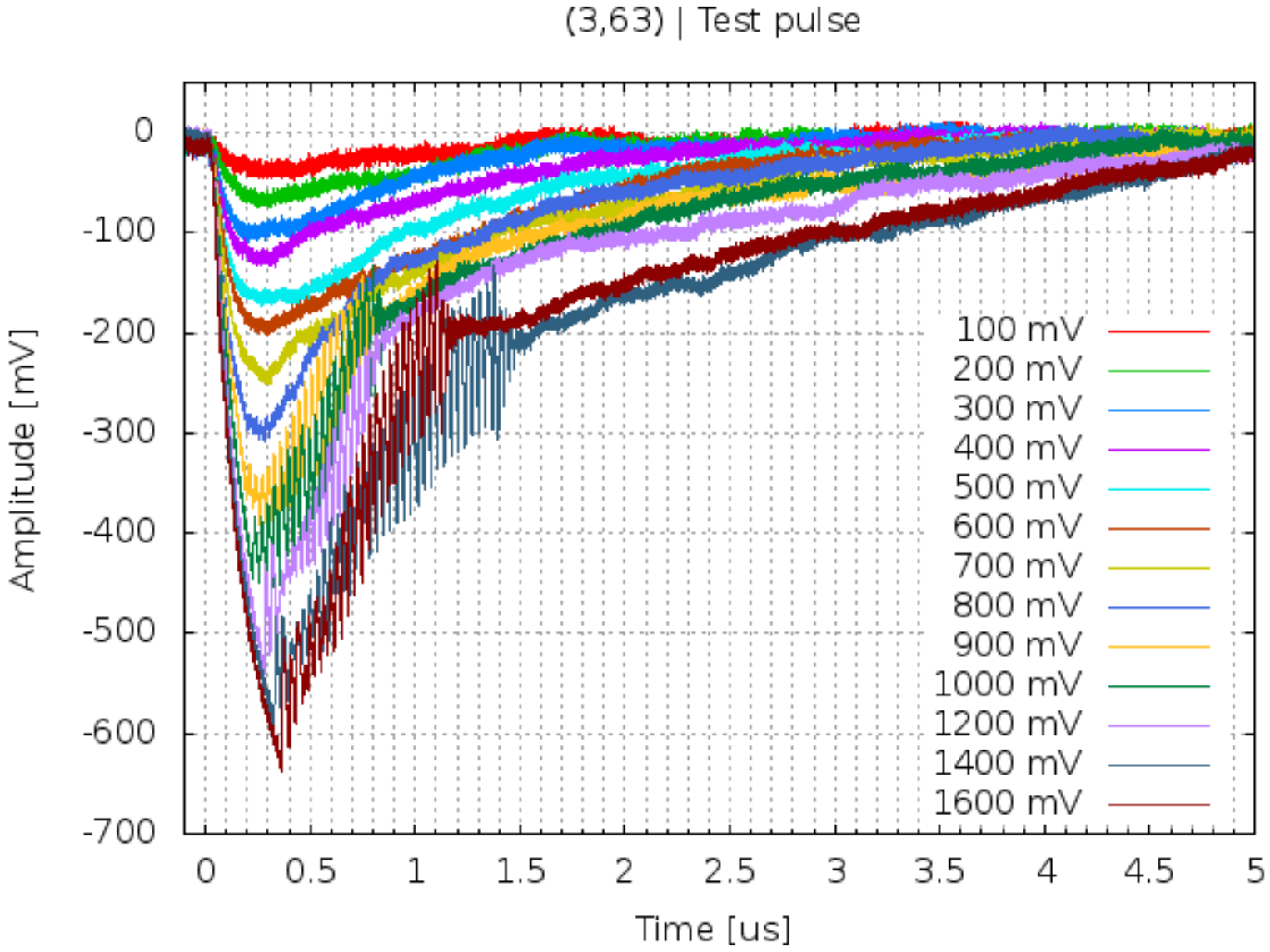


Summary

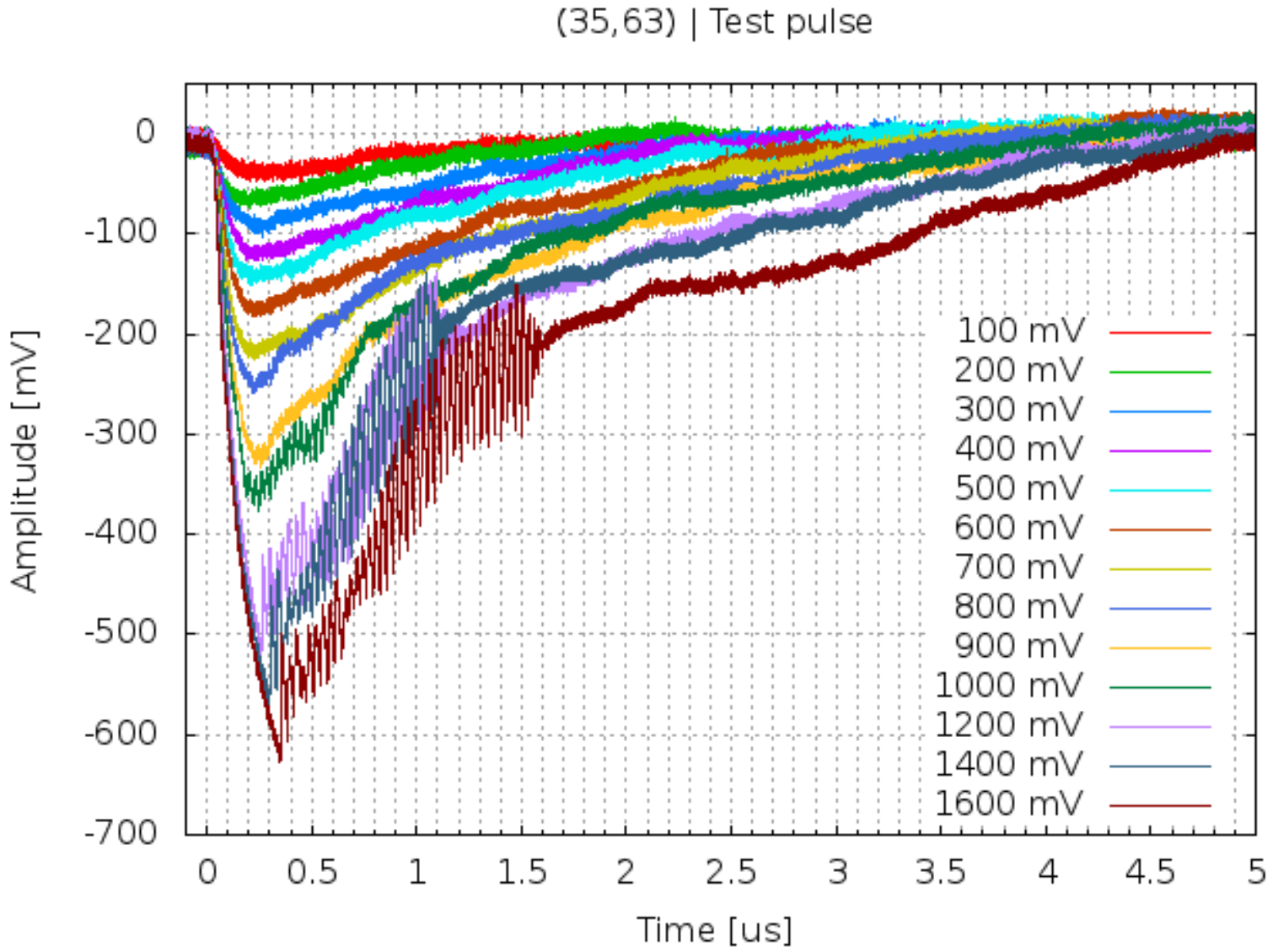
- Setup is ready for more systematic studies
- CCPDv3 :
  - is definitely able to detect Fe55 with good SNR
  - Rather big gain variation (more than factor of 2)
  - Significant shape (mainly falling edge time) variation
- Issues:
  - how to measure uniformity of the whole matrix?
    (can we do anything without CLICpix?)
  - what kind of source can we use for calibration?
- Remark: time needed to capture 1000 event for one pixels in the setup exceeds 4 hours (limitation comes from activity of the source and the pixel size → not much we can do to improve that).

BACKUP SLIDES

Pixel response (3,63) | Test pulse amp scan



Pixel response (35,63) | Test pulse amp scan



Pixel response (63,63) | Test pulse amp scan