Electronics front-end systems for High Energy Physics

Jorgen Christiansen - CERN

Outline

- Historical evolvement
- Amplifying detector signals
- Connecting to detectors
- Readout architectures
  - Analog/digital
  - Data buffering
  - Triggered
  - Zero-suppression and data compression
  - Synchronous/asynchronous readout
- Detector types and particularities of their electronics
- Control and Readout links
- Radiation effects
- Powering and cooling
- Some LHC examples
- Outlook for the future

Sources of information

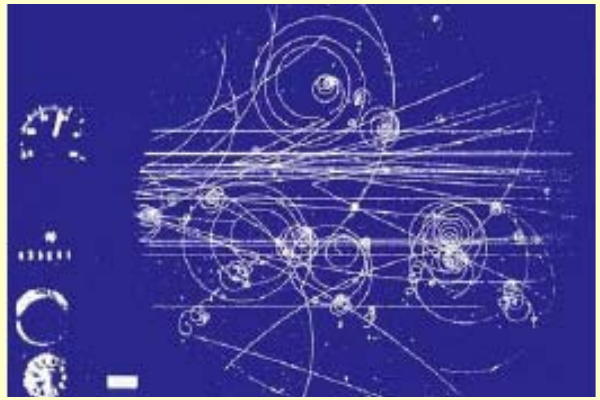
- Previous summer student lectures by C. la Taille: http://indico.cern.ch/conferenceDisplay.py?confId=a062747
  - Has more emphasis on the critical analog part
- CERN technical training ELEC 2005: http://humanresources.web.cern.ch/humanresources/external/training/tech/special/ELEC2005.asp
  - Analog, digital, VLSI, power, EMC, tracking, Calorimeter, etc.
- LEB/LECC/TWEPP workshops from last 10 years: http://lhc-electronics-workshop.web.cern.ch/LHC-electronics-workshop/
  - Lots of presentations and papers available here covering LHC electronics and other
- Common ATLAS CMS electronics workshop 2007: http://indico.cern.ch/conferenceTimeTable.py?confId=10010
- Web pages from the four LHC experiments
- Diverse information on the web (finding it thanks to Google)
- Many of my CERN, LHCb and other HEP colleagues

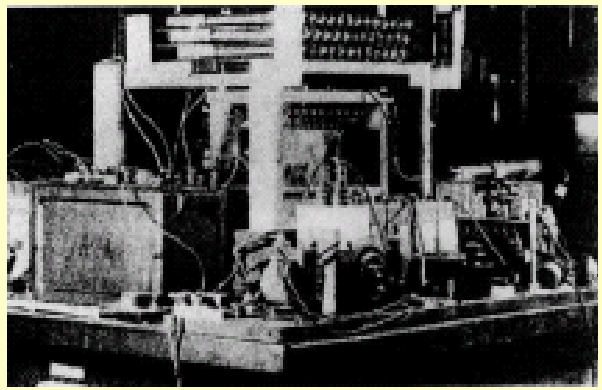
- No names given, none forgotten

I have borrowed/stolen left and right so nearly nothing of what is shown actually comes from me.
(hope nobody will sue me)

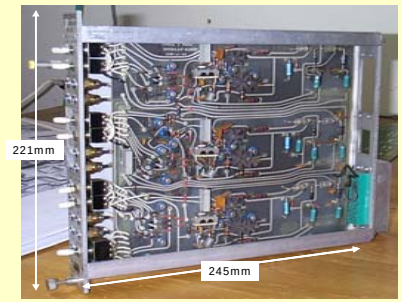
Historical evolvement

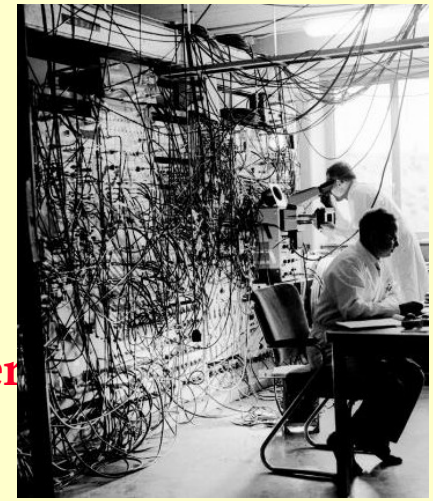
- Electronics has been the enabling technology that has allowed the development of modern HEP detectors.
- First particle detectors relied on direct eye observation (and films)
  - Phosphorus screen, cloud chamber, Bubble chamber, Spark chamber
- The use of electronics has allowed the development of a large multitude of detector types
  - Scintillators with PM or APD's, gas detectors, liquid detectors (liquid Argon), solid state (silicon), ,

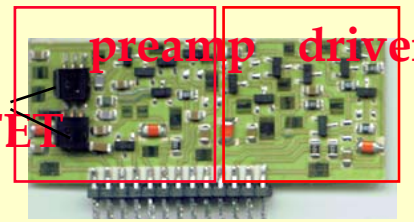


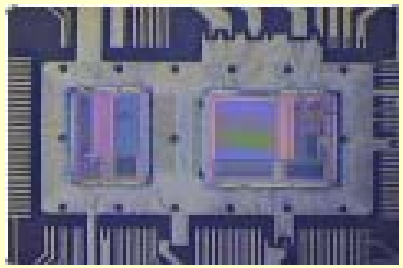


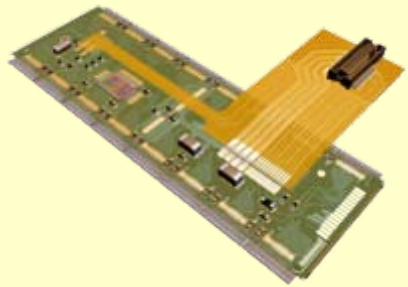
- Use of basic amplifiers with analog oscilloscope displays
- Use of modular electronics with digital computer interfaces
- Use of discrete front-end electronics within detector
- Use of highly integrated custom front-end electronics with digital signal processing and massive high speed connections to large computer farms (also electronics)

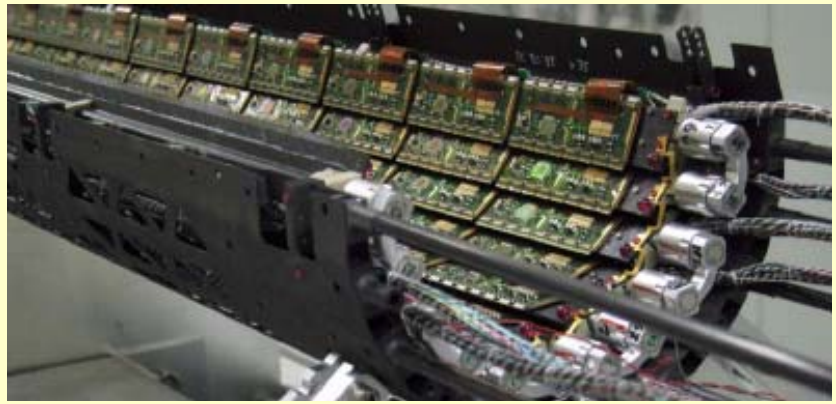






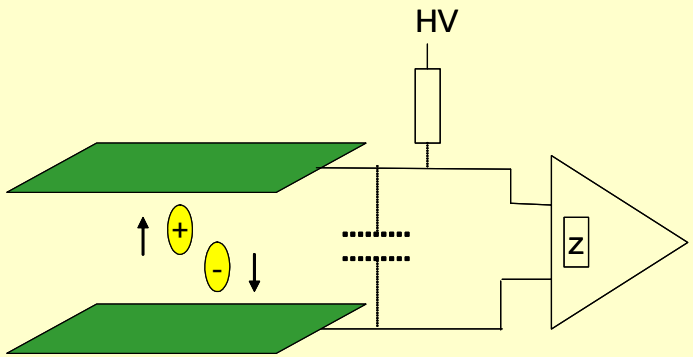


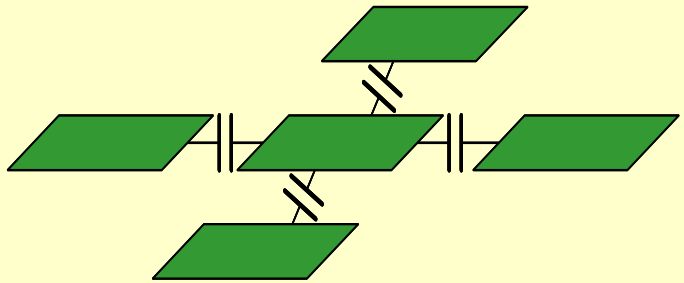




Signals from detectors

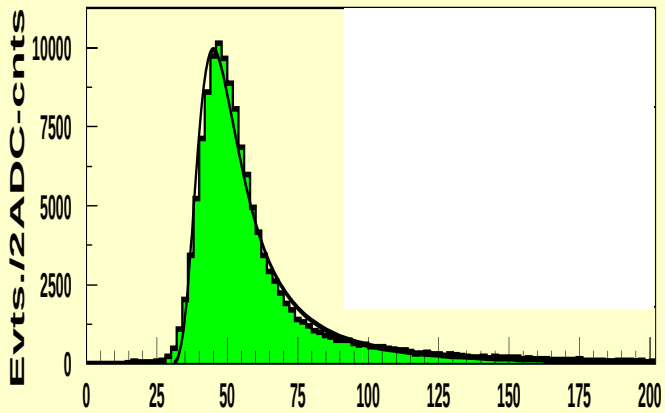
- Detector generates basic signal (charge) from ionization in gas, liquid or solid state (or photo electrons) with detector "gain" in some cases (gas, PM)
- The detector can from an electronics point of view be considered as a simple capacitor (with some possible leakage and a simple HV biasing circuit).
  - Induced signal modeled as current source
- The signal shape (charge collection) depends on the details of the detector
  - Normally relatively fast rising edge
  - May possible have a slow tail (ion tail in gas detectors)
- Typical signal is a few femto coulombs (e.g. 22ke=4fC in 300um silicon detector)
- In an open detector with 10pf capacitance this gives a voltage buildup of only few hundred uV
- There are in most cases also significant capacitive coupling to neighbor detector channels

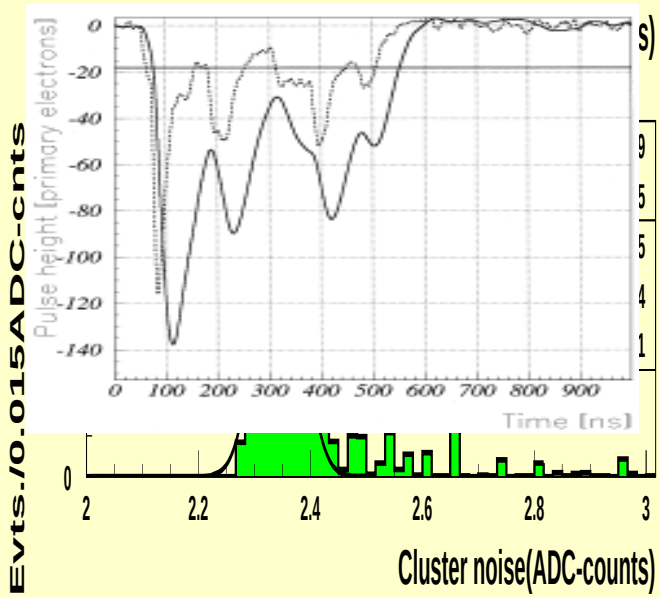


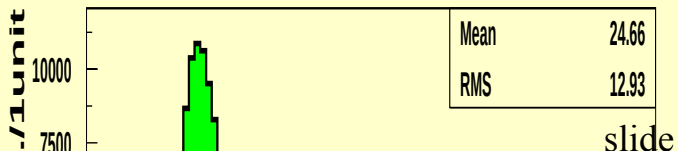


Detector signal

- Traversing particles may deposit randomly different signals in tracking detectors
  - Landau distribution for silicon detectors with a given "minimum" MIP (minimum ionizing particle: ~20ke in 300um silicon
- Signal may consist of multiple sub-pulses for one particle
  - Drift tubes with clusters originating from individual primary ionizations in gas
  - One would like to detect first cluster or "merge" all into one signal with "constant" shape
- Measurement of energy (calorimeters)
  - Measurements over large linear range with high resolution

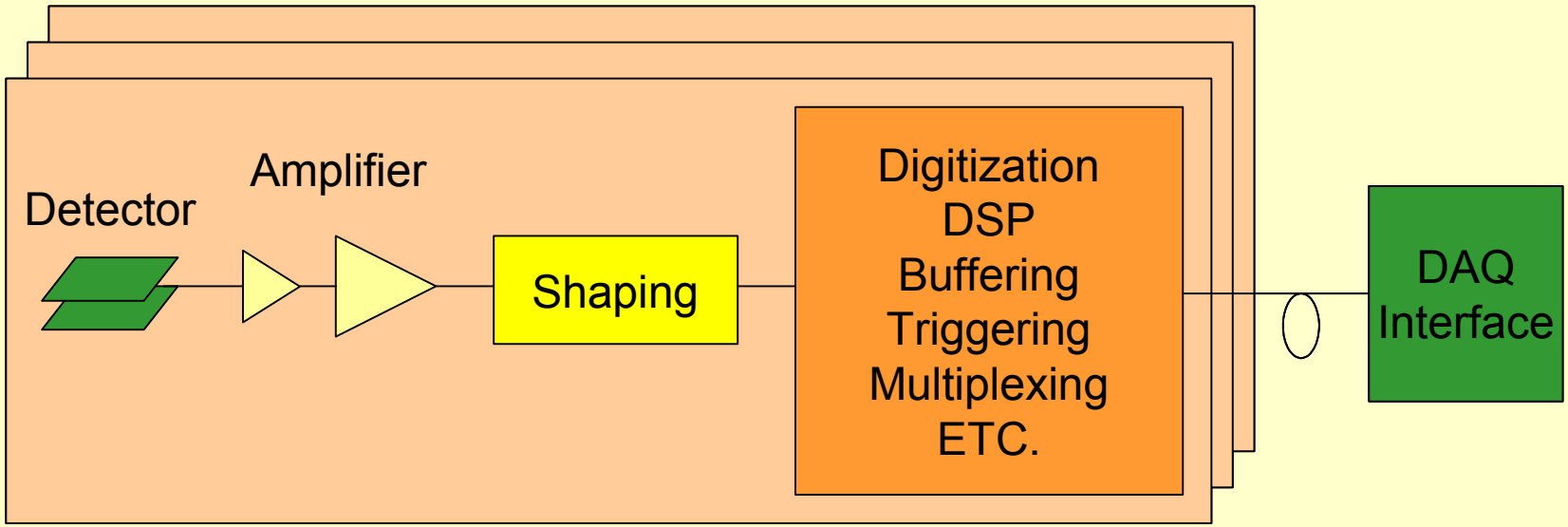






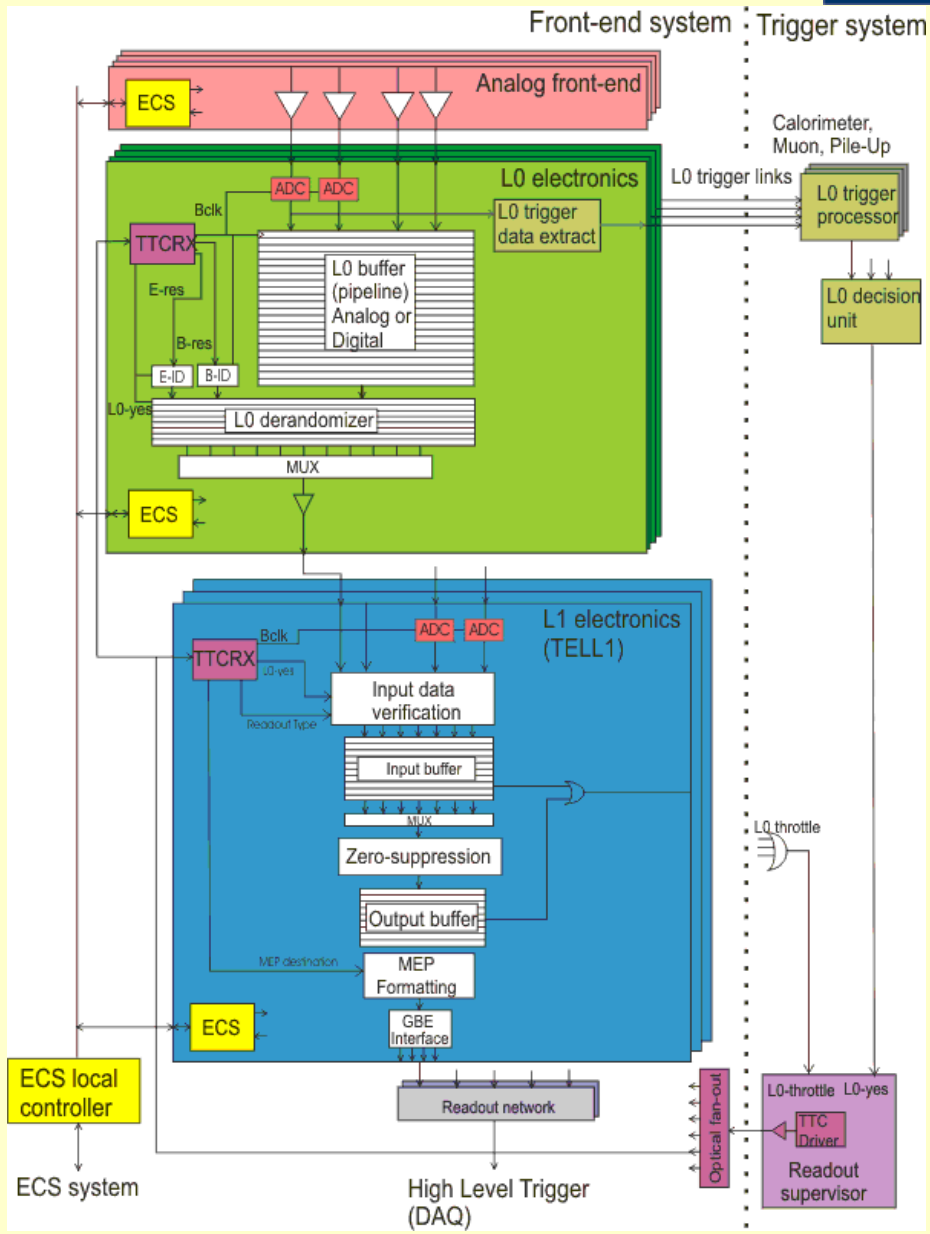
Basic Front-end

- Pre-amplifier interfacing to detector
- Additional gain stages if needed.
- Shaping – filtering
- Further treatment



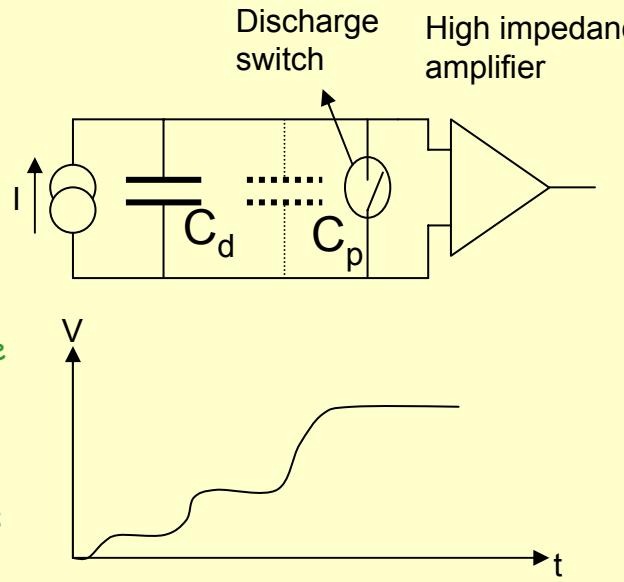
Typical LHC front-end

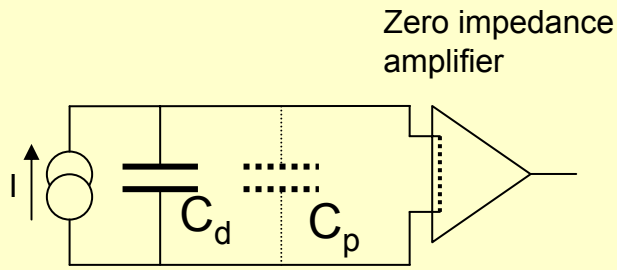
- 40MHz sampling rate
- Triggered at few kHz - 1MHz rate
- Constant latency buffer of a few us (few hundred samples at 40MHz)
- On-detector:
  - Analog front-end
  - Extraction of data for trigger
  - Latency buffer
  - Readout via optical links (many)
  - Timing and trigger control
  - Controls and monitor interface
  - Difficulties: radiation, space, cooling, access, magnetic fields
- Off-detector:
  - Trigger systems
  - DAQ interface
  - Global readout and trigger control
- Digitization: **on-detector** or off-detector



Amplifying signals

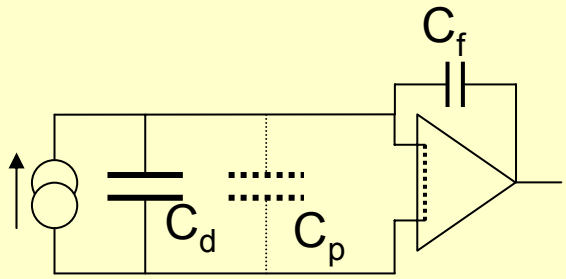
- Detector signal must be amplified to allow further processing and readout
  - Optimal interface to detector
  - Minimize noise
  - Minimal coupling to neighboring channels - crosstalk
  - Sufficient gain and linearity
  - Sufficiently fast according to the particle rate in a given experiment (pile-up, spill-over)
  - Drive next stages of analog processing
  - Allow extraction of important parameters: amplitude and/or time
- With a high impedance amplifier the voltage will build up until detector capacitance discharged
  - Some external circuit must discharge (switch)
  - Gain depends on detector capacitance and parasitic capacitances: V= Q/(Cd + Cp), gain = $1/C_{tot}$ (amplifier capacitance included in Cp)
  - Voltage buildup will give large crosstalk on neighboring channels
- "Medium impedance" amplifier will still have low gain with dependency on parasitic's and crosstalk to neighbor cells
- With a low impedance amplifier the detector capacitor is continuously discharged and the amplifier must extract/amplify the discharge current.
  - We must find a "short circuiting" amplifier that still gives some output with a good gain in respect to discharged current
  - No dependence on detector and parasitic capacitances !
  - No crosstalk to neighboring channels



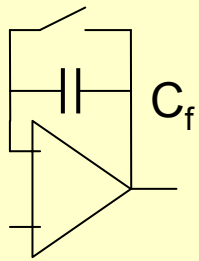


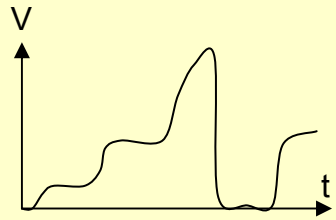
Charge integrator

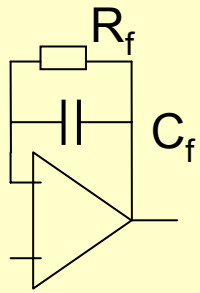
- Charge integrator used to integrate collected charged on virtually "short-circuited" detector capacitance: $V_{out} = -1/C_f \int I_{in}(t)\, dt$, Gain = $-1/C_f$
- Gain of this only depends on charge integration capacitor C_f and not on capacitance of detector
  - Makes gain independent of detector and parasitic capacitor variations
  - Detector capacitance though have direct effects in practice on noise of circuit and the effective speed
- Output voltage continuously integrates detector current which implies forever increasing output voltage with multiple hits (same problem as we had before but now on feedback capacitor and not on detector)
  - Switch to discharge integration capacitor
    - An appropriate moment for this needed (low rate detectors)
    - Double integrator with one integrating when the other is being reset
  - Continuous discharge via resistor (integrator baseline restoration)
    - Must be adapted to hit rate (occupancy in time)
    - Frequency response of this can be compensated for in following filtering with what is called "Pole – zero cancellation"
- Large majority of pre-amplifiers for HEP made like this.

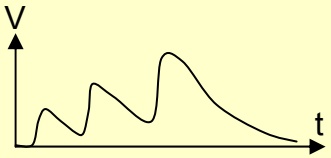


Ideal operational amplifier



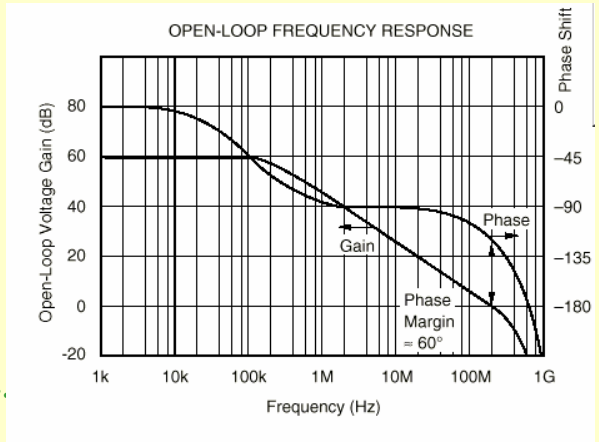


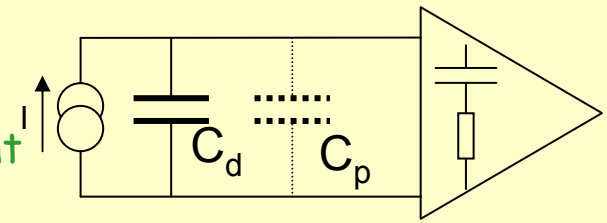




Non ideal charge integrator

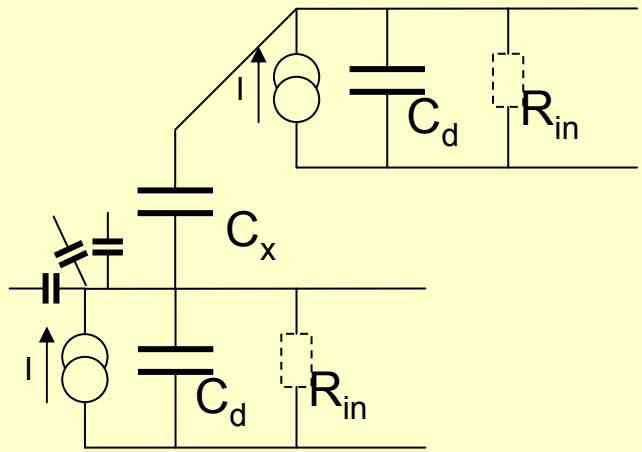
- Assume simple amplifier with G_0 low frequency gain and dominating pole at ω_0
  $G(\omega) = G0/(1+j\ \omega/\omega_0)$
- Small loss in gain: C_d/G_0C_f (normally insignificant)
- Finite rise time because of gain reduction at high frequencies: $Tau=C_d/C_f * 1/G_0\omega_0$
  - Rise time slower with larger detector capacitance
  - Rise time slower with smaller gain-bandwidth product
  - Faster with large C_f (but smaller gain)
- Input impedance
  - Ideally: 0 ohm, Detector instantaneous discharged
  - Real: $Zin = 1/j\omega G_0C_f + 1/G_0\omega_0C_f$
    Capacitive term: $G0 * Cf >> Cd$,
    Resistive term that together with detector capacitance (incl. parasitic and amplifier capacitances) determines effective time constant of input circuit.
    - Example: Cd=10pf, Cf=0.1 pf (preamp gain 100), $G_0\omega_0 = 10^9$ rad/s
      $Tau_{in} = Cd/Cf * 1/ G_0\omega_0 = 10^{-7}s$=100ns





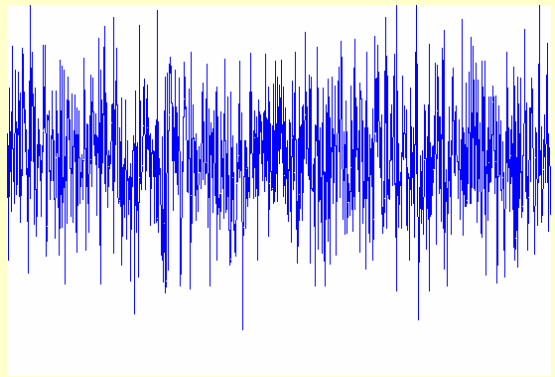
Minimizing crosstalk

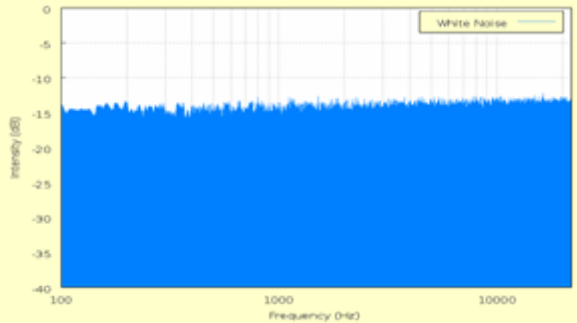
- Crosstalk effects increasingly important as channel densities in modern detectors constantly increasing.
  - In fine grain pixel detectors capacitance to neighbor pixels gives a significant contribution
- Effective input time constant has effects for crosstalk as deposited detector charge not instantaneously discharged to ground.
- Coupling capacitance differentiates voltage seen on detector terminal until charge integrator has managed to remove this
  - Detectors with slow intrinsic charge collection (compared to effective speed of charge integrator) will have limited cross talk to neighbors
  - Detectors faster that input time constant will transfer charge proportional to capacitive charge division Cx/Ctot

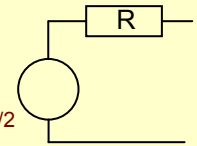


Intrinsic electronics noise

- Noise of random nature
  - Characterized in terms of noise power within a given frequency band
  - When adding noise sources of random nature they must always in added in square (assuming they are fully uncorrelated)
    $v_{tot}^2 = v_1^2 + v_2^2 + v_3^2 +$
- Thermal noise from conductors/resistance
  - Random thermal excited vibrations of charge carriers in conductor
  - White noise spectrum (proportional to frequency band)
  - Noise power $\langle v^2 \rangle = 4KTR\Delta f$
    - K Boltzmann constant: 1.383 10^{-23} VC/K
    - 100ohm, 100MHz bandwidth: 12.8 uV_{rms}
    - 1Mohm, 100MHz bandwidth 1.28mV res (larger than most detector signals)
- Shot noise
  - Carrier transportation across semiconductor junctions (diodes and bipolar transistors). Proportional to current
  - White noise
  - Noise power: $\langle i^2 \rangle = 2eI\Delta f$
- 1/F noise (Flicker noise)
  - Constant noise power in each decade 1-10, 10-100, 100-1000, ,
  - Noise power: $\langle v^2 \rangle = A/f^{\alpha} * \Delta f$
  - Present in MOS devices

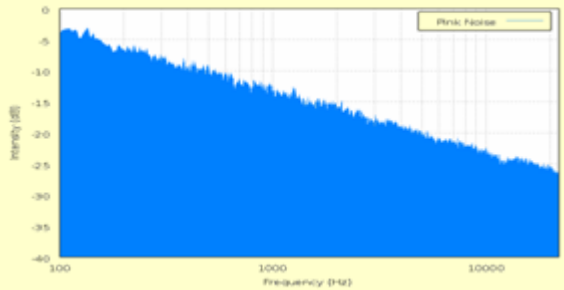






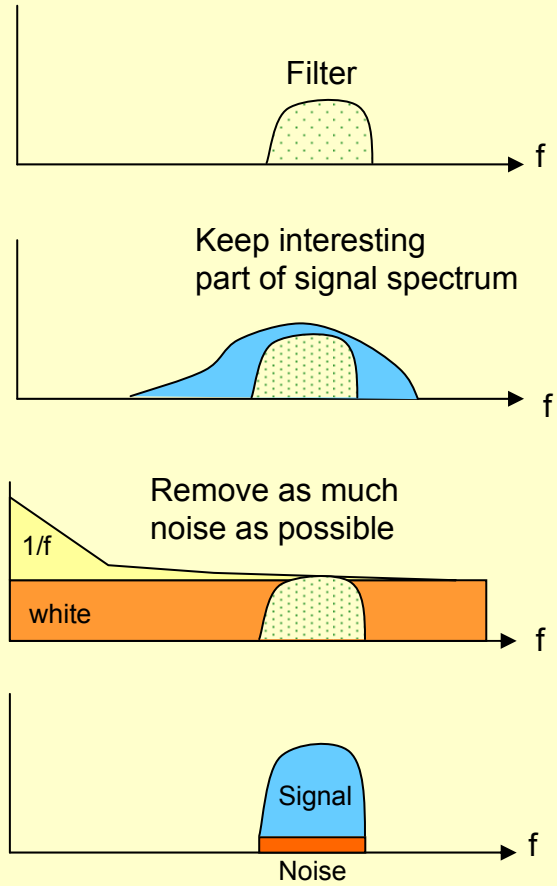
Available noise power

$E = (4KTR\Delta f)^{1/2}$



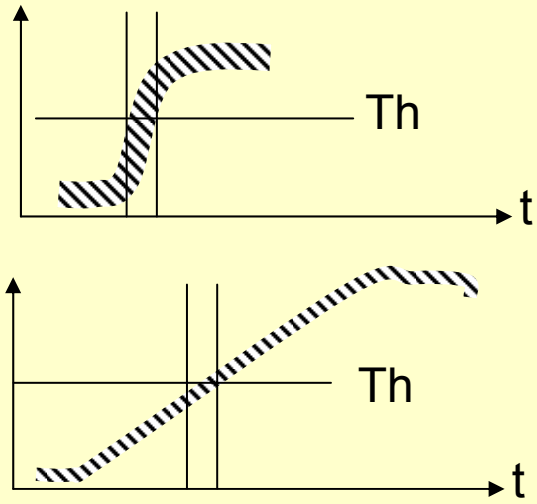
Signal & Noise filtering

- The total noise will depend on the effective bandwidth of the circuit
  - Shaping/filtering
- Minimize bandwidth to what is really needed
  - Worth to sacrifice a part of the signal to decrease noise
  - What counts is Signal/Noise Ratio (SNR)
- Determined by bandwidth of interest in detector signal
  - Speed of detector itself
  - Time separation of hits from consecutive collisions
  - Need for time information (e.g. drift time)



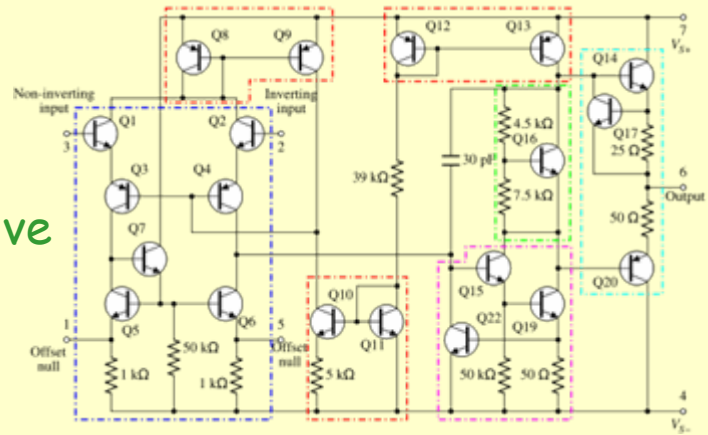
Simple question, but complicated optimization

- Needs good time precision ~100ps (e.g. TOF)
  - Do I need a ~10GHz bandwidth ?
    - Obviously not but what is best choice ?
- Lower bandwidth in front-end amplifier gives lower noise but slower signal gives bad time resolution
  - Lower slew-rate of signal makes the discrimination more sensitive to noise
- High bandwidth gives fast signal to discriminator but also more noise in signal
- As usual, best choice is a non obvious compromise taking into account many factors
  - Detector signal itself and its bandwidth
    - One obviously needs to use a detector with an intrinsic fast response
  - Noise and speed characteristics of technology used to make analog front-end: Bipolar or MOS or GaAs
  - Allowed power consumption (often constrained)
  - Amplitude dependency must also be compensated for (see late)



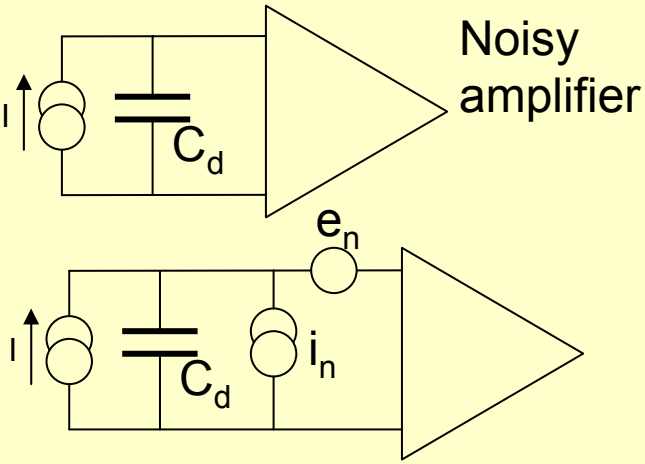
Calculating noise of circuit

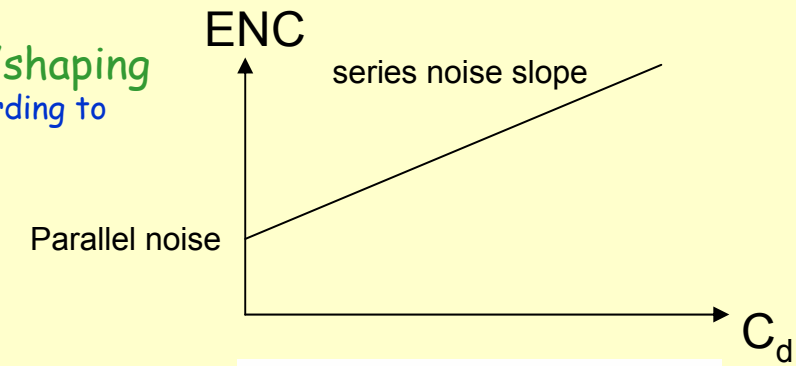
- Many circuit elements in modern analog front-ends
  - Capacitors and inductors noise free (except from parasitic resistance)
  - Resistors and active elements (bipolar/MOS) are the intrinsic noise sources
  - The first stage amplification dominant from point of view of noise sources. Following shaping determining for effective bandwidth
- How to **estimate** noise level of circuit
  - Hand calculations of input stage with basic noise figures for resistors and active elements.
  - Noise simulations in Spice simulator based on noise models from technology supplier
- Measurements on final circuit

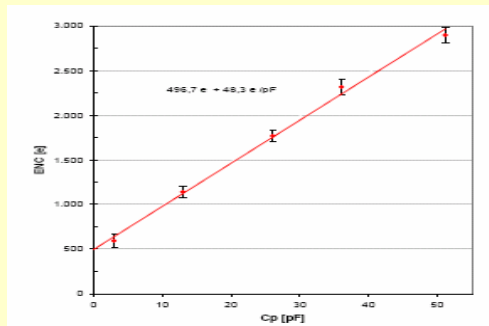


How to quantify total noise

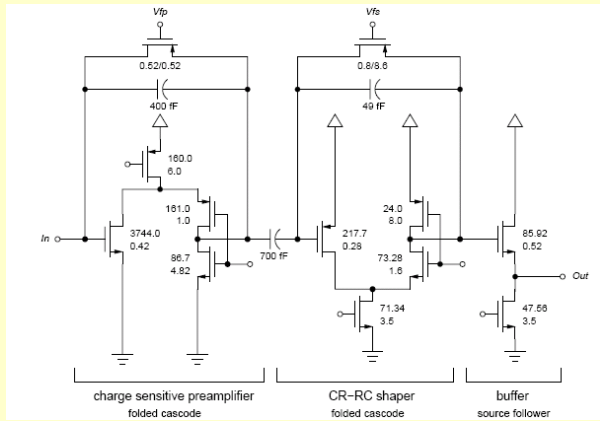
- Total contribution of all the different noise sources within the analog circuit can be referred to the input as two input noise sources
  - e_n : Series noise
    (total noise if amplifier input shorted to ground)
    Dominating at high frequency
  - i_n : Parallel noise
    (total noise if amplifier input left open)
    Dominating at low frequency
- Total effective noise depends on
  - The bandwidth of the following filtering/shaping
    - An optimized shaping/filtering can be made according to detector capacitance
  - The basic coupling to the detector
  - Detector capacitance
    - zero capacitance: only parallel noise
    - Series noise increases with detector capacitance
  - High voltage biasing network (resistor)
- Extracting the Equivalent Noise Charge (ENC) for a given detector capacitance
  - In practice Equivalent Noise Charge
    $ENC = ENC_0 + ENC_{slope} * C_d$

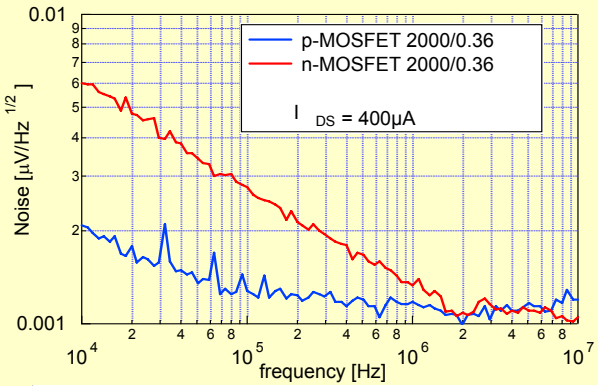


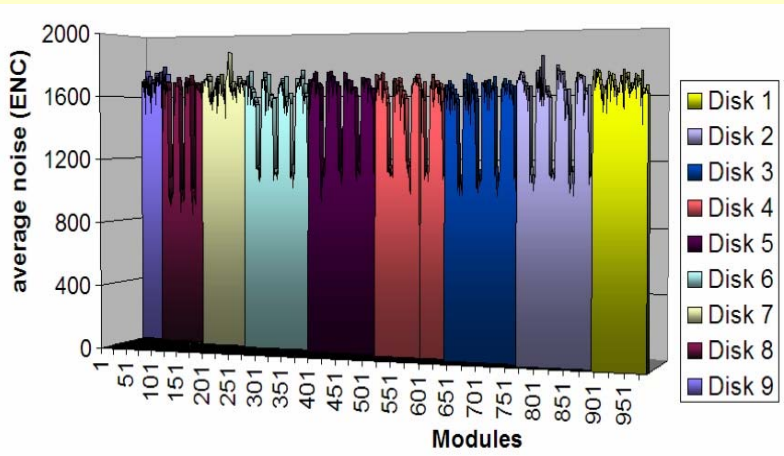


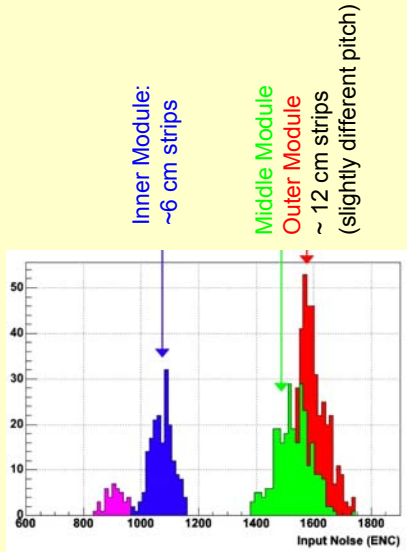


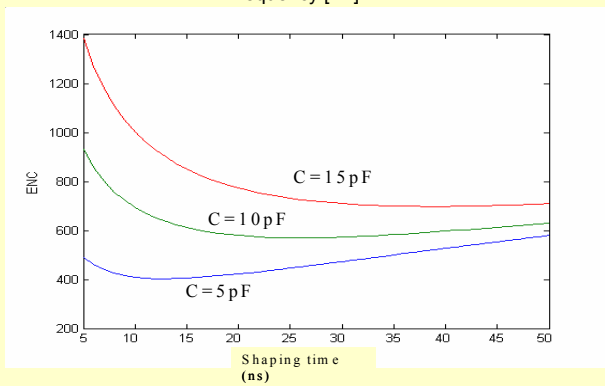
- For CMOS preamplifier
  - Large MOS input transistor: W/L and Large biasing current: I_{DS} (Limited by acceptable power)
  - MOS gate is a significant capacitive load: $C_{ox}WL$.
    Minimized noise when: $C_{gate} \approx C_{det}/3$
  - PMOS has less 1/f noise so normally favored as input transistor
  - A given detector capacitance has an optimum shaping time for minimal noise







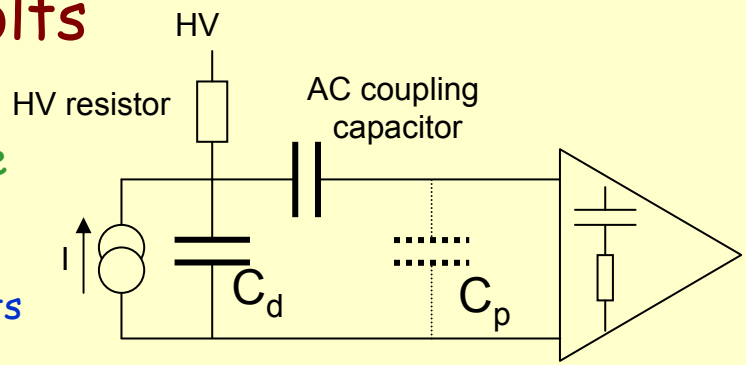


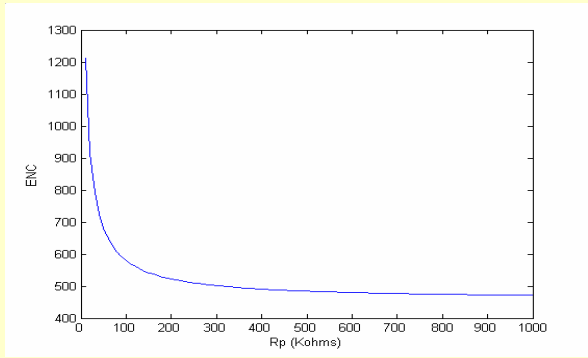


ENC dependence to the shaping time

HV and AC coupling

- In practice the detector must be connected to a High Voltage (HV) biasing source (few hundred volts to several kV)
  - Resistive connection to HV with some local filtering
    - Resistor must be small enough to supply required leakage + particle induced currents with small voltage drop
    - Resistor should be made as large as possible to reduce noise
- AC coupling may be needed because of the HV biasing of the detector
  - Must stand high voltage (reliability)
  - Capacitance chosen sufficiently high that it does not have major impact on signal to preamplifier.

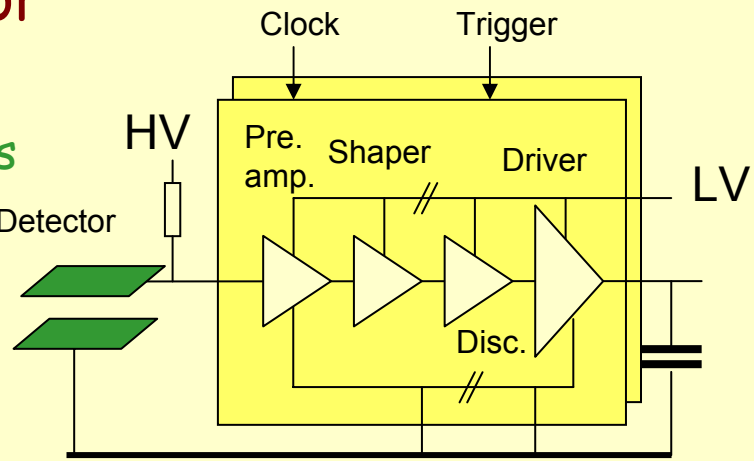


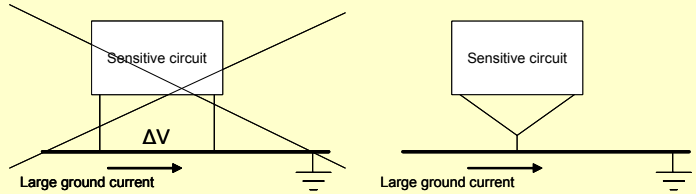


ENC dependence to the parallel resistance at the input

System noise

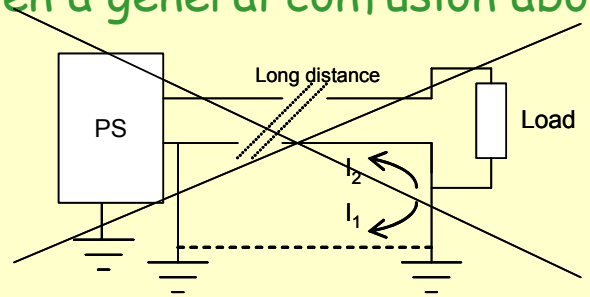
- Critical coupling between detector and its electronics
  - Typical problem of coupling from outputs of FE chips to the very sensitive inputs
    - Oscillators are not so difficult to make !.
    - Prevent output ground currents to be injected into input ground
    - Use differential signals (no ground/power current changes)
  - "Religious question": One common ground or separate analog/digital grounds
    - For sure do not feed power/ground to noisy digital logic via sensitive analog front-end. Coupling via common impedance.



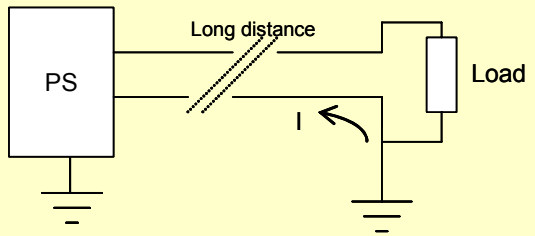


System noise

- Power supply noise
  - Power supply noise rejection for analog front-end
    - Analog FE can be very sensitive to any power supply noise
    - Separation of analog and digital power domains
    - Good local decoupling required
  - HV connects directly to detector and local HV filtering and shielding is critical
  - Differential mode and common mode components
    - Common mode component often badly defined/specified/understood/etc
  - Use of floating power supplies to prevent forcing high return currents into global grounding of experiment and its electronics
  - Often a general confusion about power return and ground



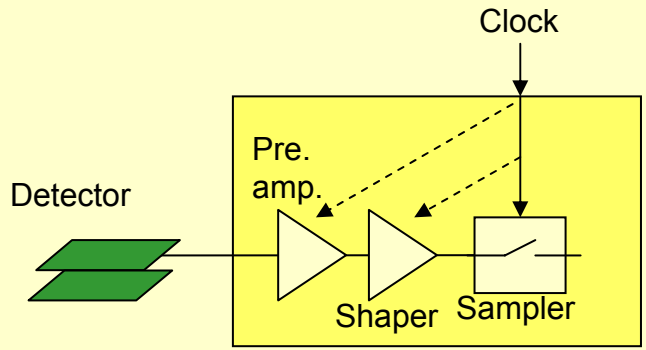
Generation of return currents in grounding network

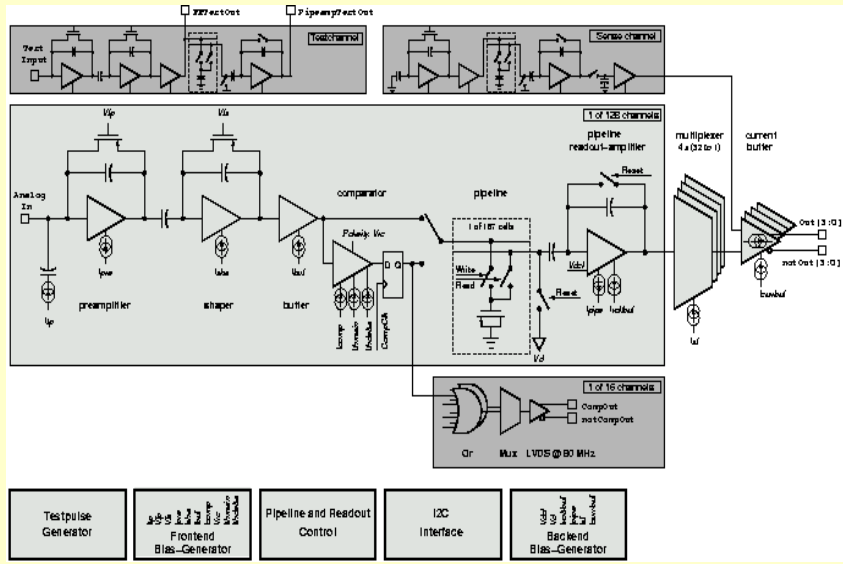


No return currents in grounding network

System noise

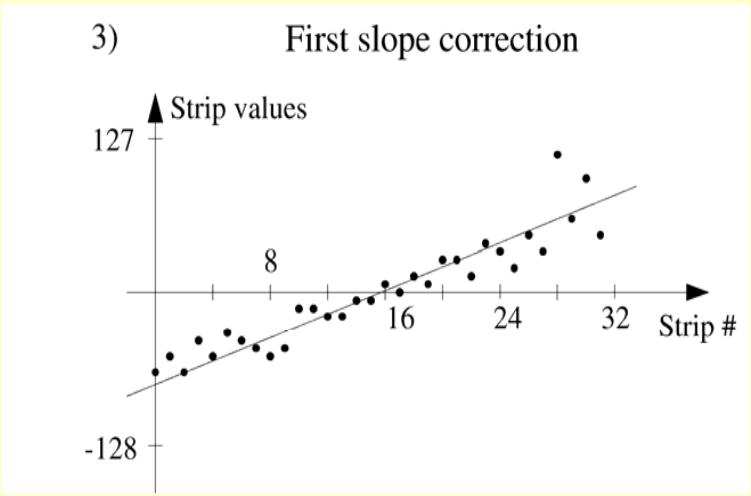
- Crosstalk from other sources
  - Neighbor channels
    - Minimized with charge integration readout
    - Can in some cases be compensated for if amplitude information for all channels available.
      In many cases impossible to distinguish from charge sharing from hit between neighboring channels
      (actually gives information on location of hit)
  - Regular sources: Clocking
    - Synchronous noise – constant pedestal (OK)
    - Even OK for binary detectors as threshold just needs to be adapted
  - Non regular "internal" sources: Trigger, Readout, etc.
    - Non constant pedestal
      E.g. dependency of previous trigger/readout (NOT OK)
    - Can be common across a group of channels (common mode) so it can be calculated on a event by event basis. Simple digital processing if all channels readout with amplitude information.
      Does not work for binary !.
    - Some readout chips (e.g. LHCb BEETLE tracker chip) even have a dummy reference channel used to subtract common mode from all channels on same chip.
  - External sources (unpredictable)
    but may again be corrected for as common mode across group of channels

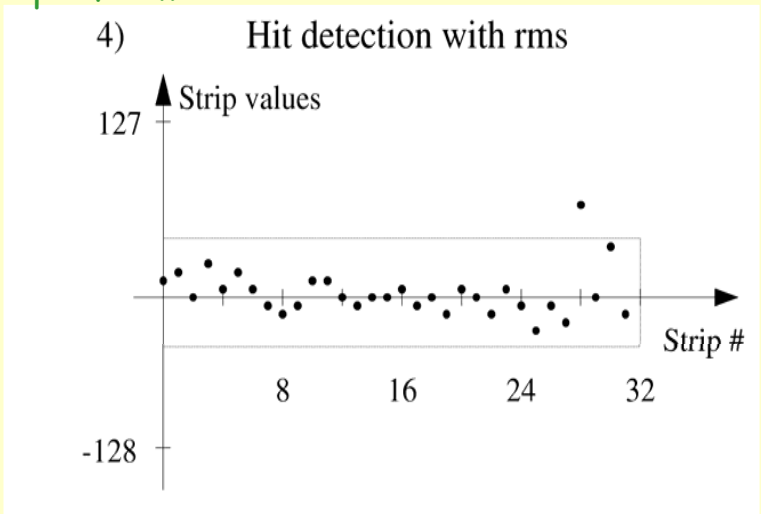




Common mode suppression

- Suppression of systematic noise sources from a non perfect system
- Fixed pedestal or dynamic pedestal follower per channel
- Systematic effect across channels in same event
  - Typically per front-end chip or front-end module
- The "shape" of the systematic effect must be known in advance
  - Proportional to detector capacitance (if varying across channels)
  - Proportional to distance to a given noise source (beam for a vertex detector)
- Channels with active hits must somehow be exclude from the calculation of the common mode
  - Iterative processing with simple thresholding
- This only works if one has access to full analog information from all channels in same event
  - Must be done before zero-suppression is performed

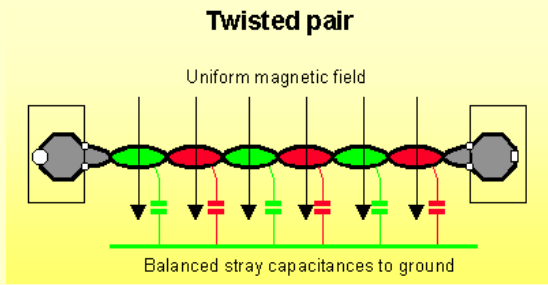


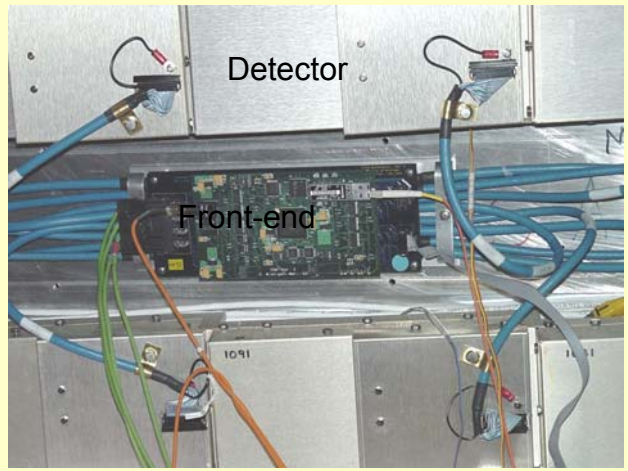


And then do it again with detected hits removed from common mode calculation

EMC

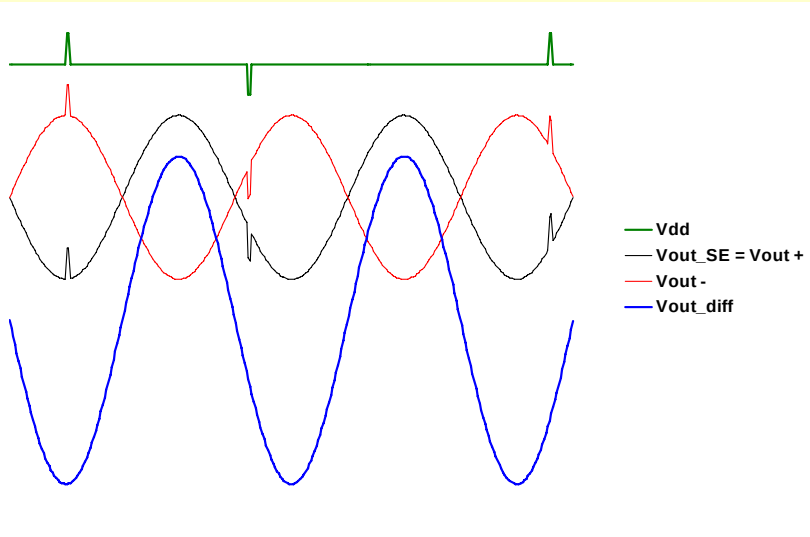
- Shielding - Grounding – EMC
  - This is a critical and far from easy aspect of large scale systems
  - Faraday cage shielding of whole detector and front-end electronics.
  - Use of differential and optical signals when ever possible
  - Twisted pairs when ever possible to minimize noise pickup and noise generation (also for power)
  - Grounding non trivial and there are different "religions"
    - No ground loops – tree structure (In practice impossible and badly made will be very problematic)
    - **Meshed with lost of non critical ground loops to neutralize noise effects from ground currents in sensitive circuits**

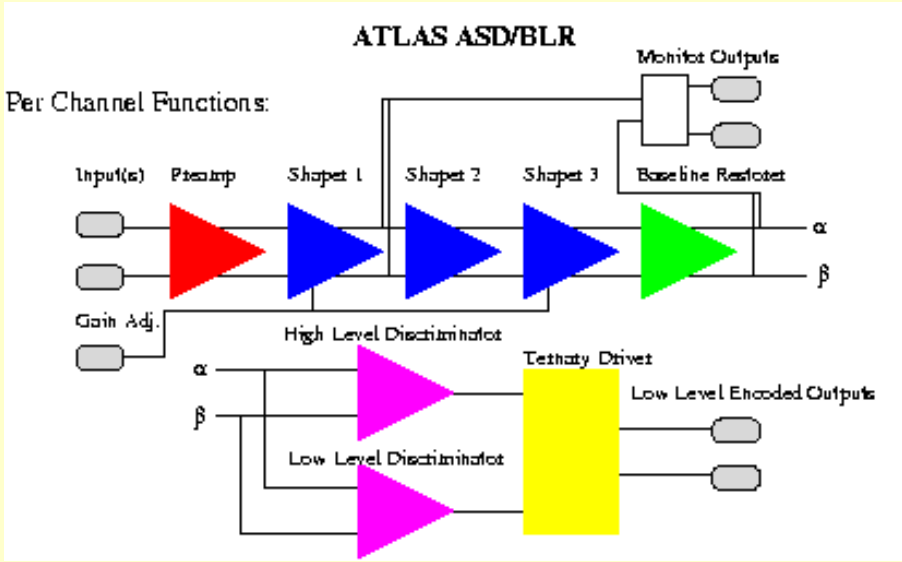




Differential architectures

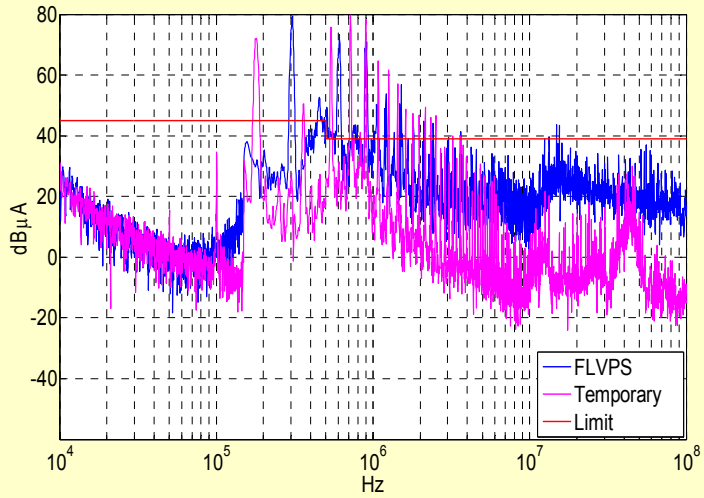
- Can reject many of these system noise components but will typically have slightly higher intrinsic electronics noise in pre-amplifier (e.g. $2^{\frac{1}{2}}$)
- Detectors them selves are though intrinsically single ended with detector ground being the reference terminal
  - Unused dummy differential input should see same impedance (e.g. detector capacitance) and same coupling as real detector input (e.g. HV biasing) to improve differential immunity, but this will increase serial noise from pre-amp

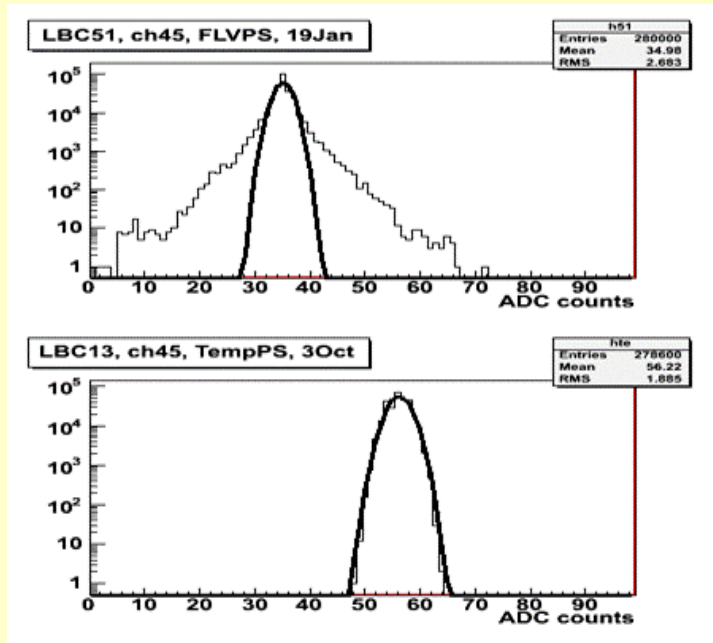




Power supply example

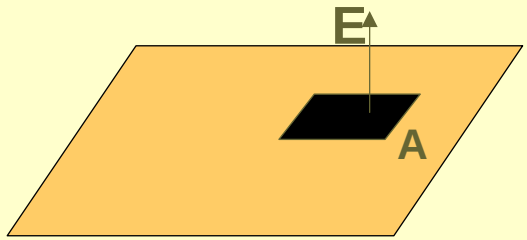
- Widening of pedestal distribution in final system with unfortunate PS in ATLAS tile cal
- Caused by HF common mode noise from power supply and front-end not sufficiently immune.
- Simple power supply filtering resolved the problem
  - But this only after a significant time needed to understand and correctly measure the cause.
  - Common mode noise measurements needs specific equipment
    - Common mode probes (pick up coils) and spectrum analyzer

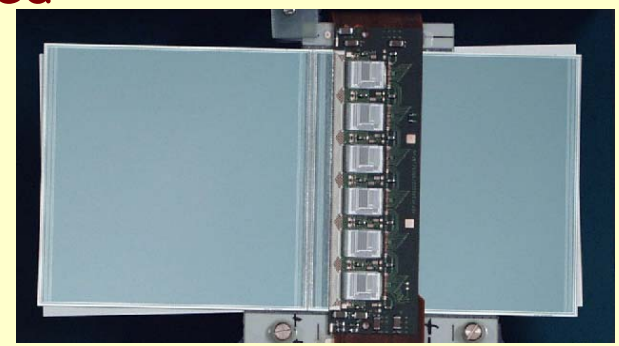




Detector shielding

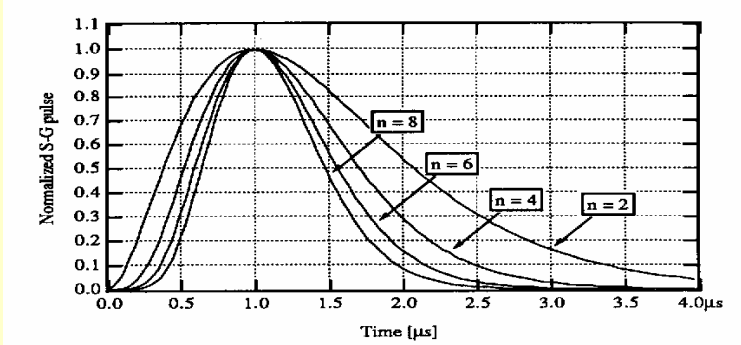
- Induced charge by an electric field E in an area A: $Q = \varepsilon E A$
  - E = 1 V/m
  - Silicon strip A = 100 x 0.1mm = 10 mm^2
    - Q = 0.09 fC or 560 e-
    - Signal: 20ke, noise: ~1000e
  - Wire chamber A = 3m x 4 cm = 1200 cm^2
    - Q = 1000 fC
    - Threshold for good timing and good detection efficiency: few fC
  - This obviously ignores frequency characteristics of the electrical field and the filtering/shaping used in the analog front-end
- Faraday cage shielding from the environment (or neighbors or even noisy parts of ones own sub-system) needed

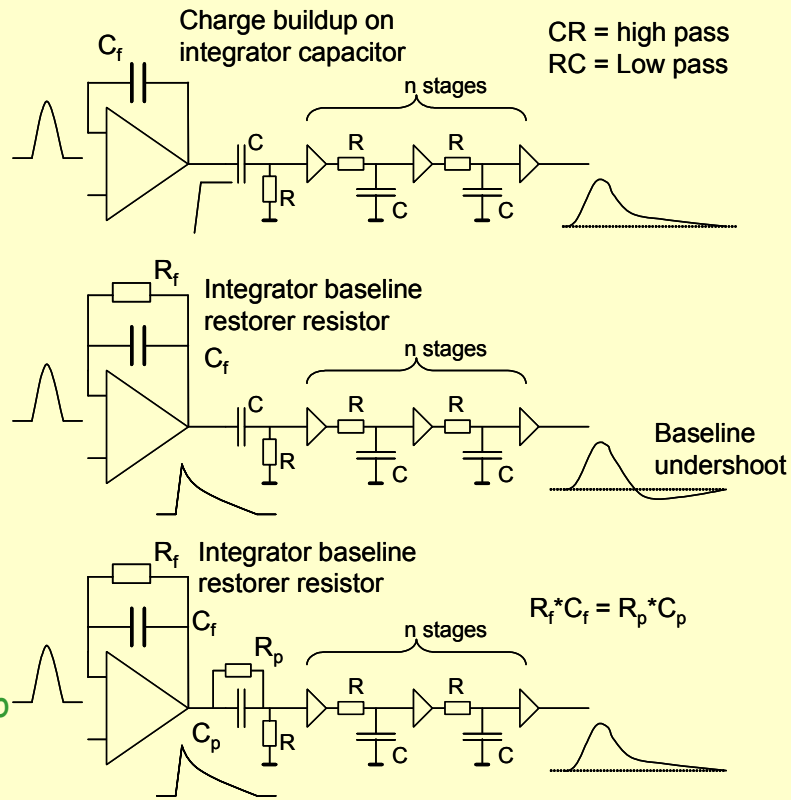




Shaping/filtering

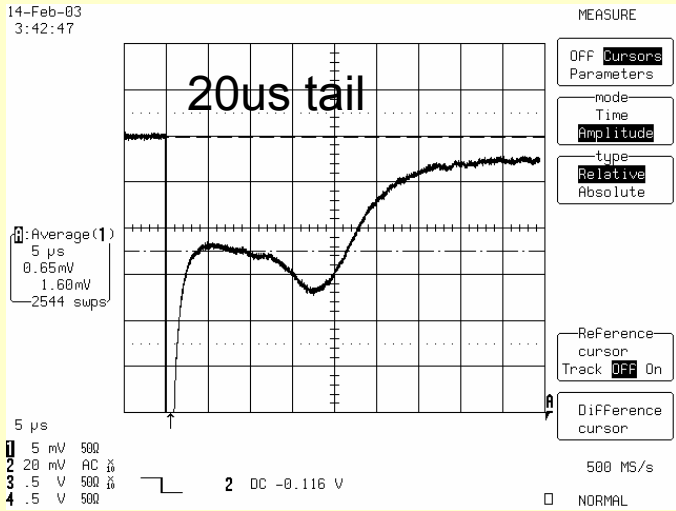
- Compromise between
  - Noise minimization
  - Speed – pileup
  - Baseline restoration
  - Particularities: Ion tail cancellation, etc.
- Typical use of CR-RC^n shaping
  - High pass followed by a series of low pass filters
    - Higher n gives quicker baseline restoration for same peaking time
  - Pole-zero cancellation of discharging resistor in integrator
  - Vital to minimize noise from pre-amplifier.
  - Noise contribution from shaping itself normally insignificant.
- Increasing use of digital filtering but analog shaping must assure that expensive ADC used efficient.
  - Minimize pileup to prevent using significant dynamic range of ADC for this
  - Assure that no frequency components above $f_{sample}/2$
  - For binary readout the analog shaping before discrimination must obviously be quite efficient to allow high counting rates

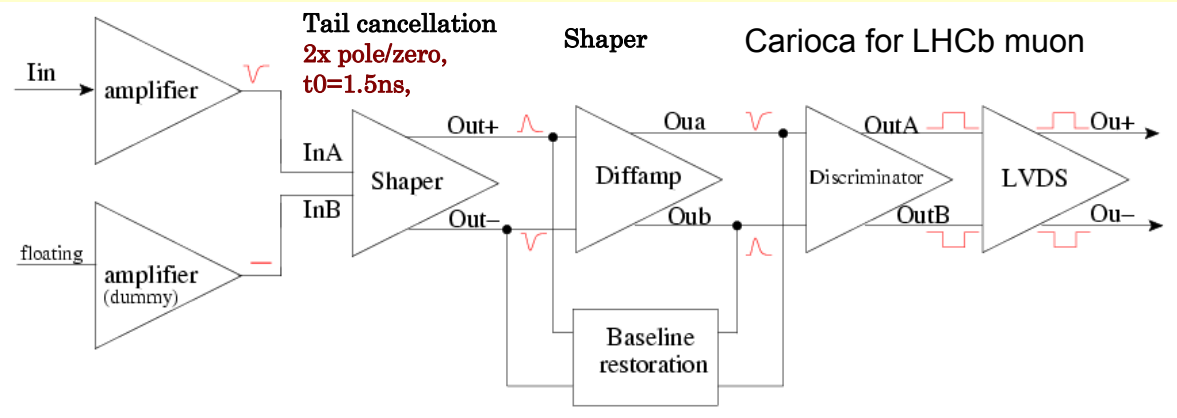


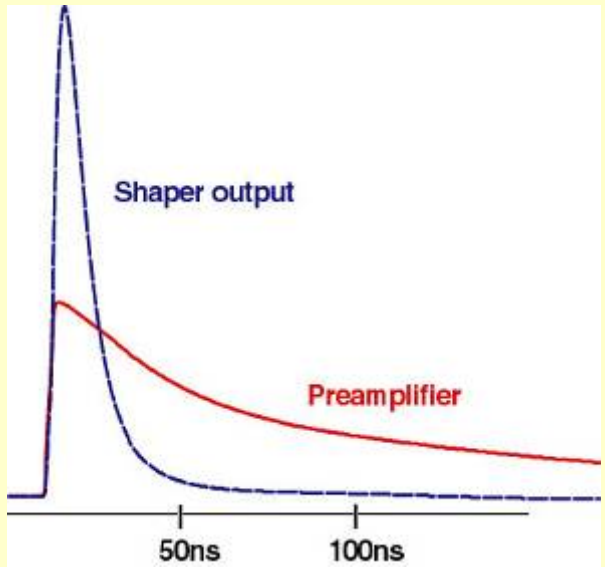


Tail cancellation

- Ion-tail for gas detectors
  - Slow drift of ion "tail" as getting away from high electrical field region (us)
  - For high rate applications this must be filtered to limit pile-up
  - Ion tail can approximatively be cancelled by a linear filter with different time constants
  - For detectors with continuous digitization this can be done very efficiently by digital filters (e.g. ALICE TPC see later)
  - Non linear baseline restorer often needed in addition for binary detectors as they are very sensitive to any baseline shifts (e.g. muon detectors based on drift tubes or wire chambers)

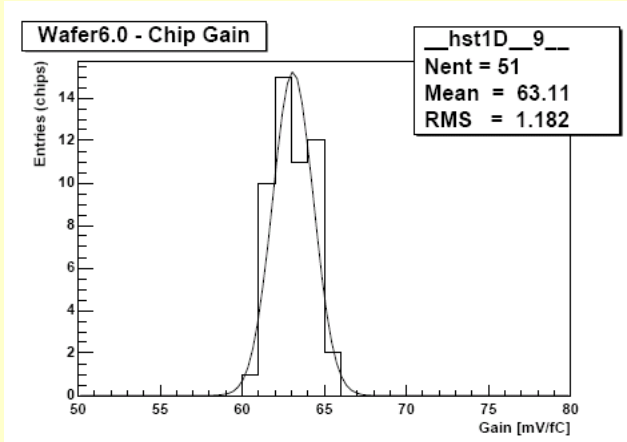


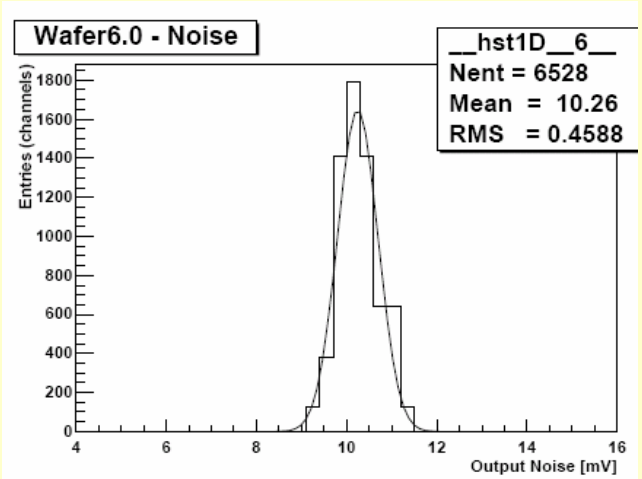




Parameter variations

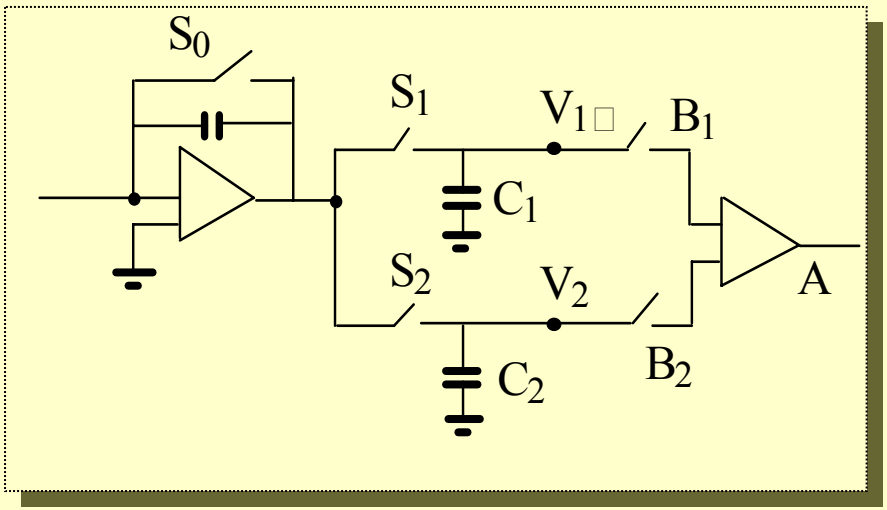
- IC technologies can have significant parameter variations of capacitances, resistors and gm of MOS transistors
  - Chip to chip on same wafer
  - Wafer to wafer in same lot
  - Lot to lot variations
  - Also significant temperature dependence (especially MOS gm)
- Within the IC the relative differences can be made quite small (matching)
  - Special layout tricks to get this: Orientation, same "environment", centroid layout.
  - ADC's heavily relying on this
- For analog circuits this will give variations from chip to chip of gain, shaping, etc.
  - Total gain depends on many different components and parameters: Monte Carlo simulations of total effects of this
  - For detectors making precise amplitude measurements (calorimeters) built in calibration systems required that must be run at regular intervals.
- For digital circuits this is not critical (except defining maximum working frequency)





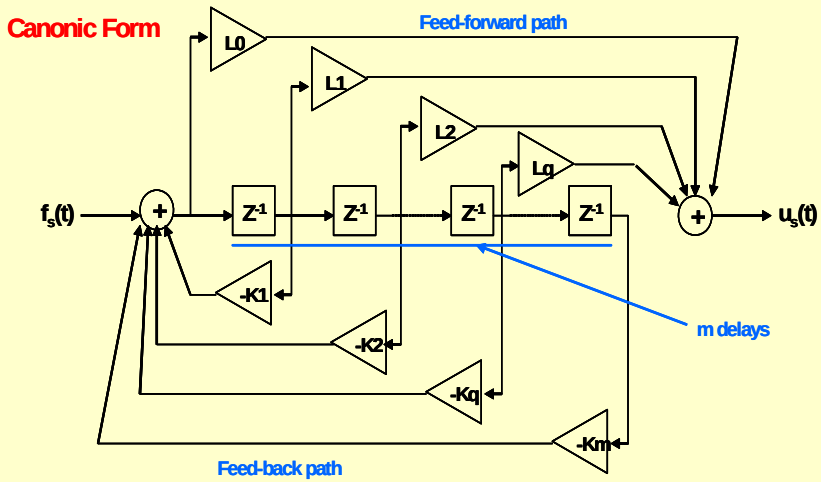
Switched capacitor filters

- Alternative to analog filters
  - Based on capacitors, switches and summations
  - Works with analog sampled data (not digitized)
  - Filter characteristics based on circuit topology and matching of capacitors (normally very good within same chip)
  - In combination with double correlated sampling many imperfections and common mode effects in circuits can be compensated for
  - CMOS is the perfect technology for this as it has good analog switches and high input impedance amplifiers
  - Normally used for limited frequency filters: up to few MHZ



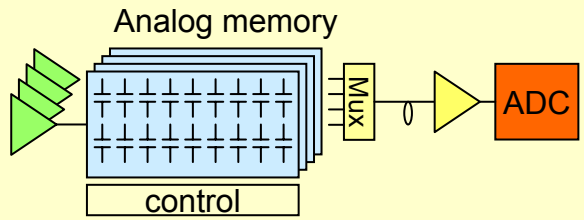
Digital Signal Processing DSP

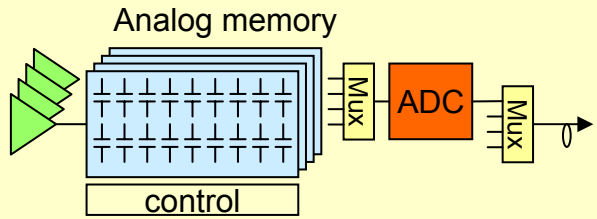
- Similar to switched capacitor and using same basic algorithms for their design and optimization
  - For continuously sampled analog data
  - For nonlinear processing this does not apply
- Needs: delays (clocked registers), additions, multiplications
- Needs **ADC**
- No additional noise
  - But may have rounding effects depending on effective bit width used in processing (integer versus float)
- Filters can be made highly programmable and can therefore be much better optimized for final needs.
- Availability of filtering types that are not possible with normal analog filters
- Welcome to a world with its own language: Z transform, FIR, IIR, Canonic, recursive, feed forward/backward, FFT, butterfly, etc.

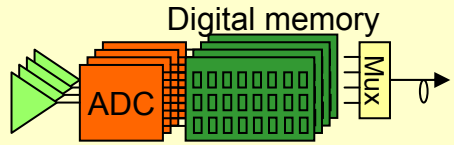


Analog/Digital/binary

- After proper amplification and shaping the signals must at some point be converted into the digital domain to allow final readout to DAQ system
- Analog readout
  - Analog buffering with digitization done after buffer or after analog transmission off detector (at DAQ interface)
- Analog buffer with digital readout
- Digital readout
  - Information digitized after shaping and all further processing done digital
- Binary: discriminator right after shaping
  - Binary tracking
  - Drift time measurement with following TDC

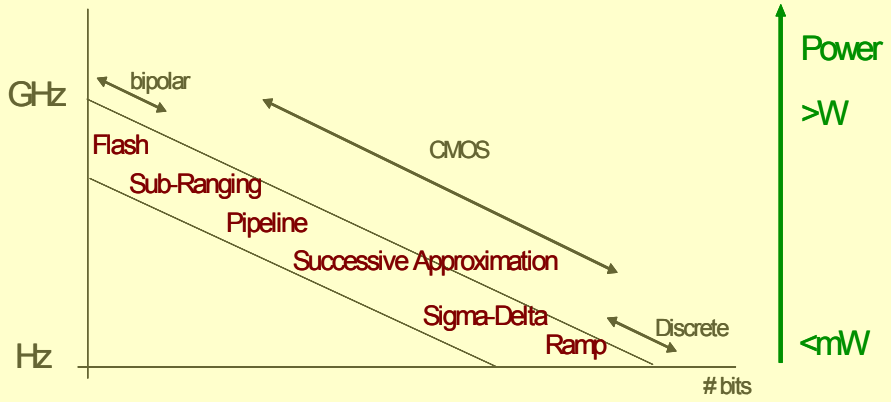


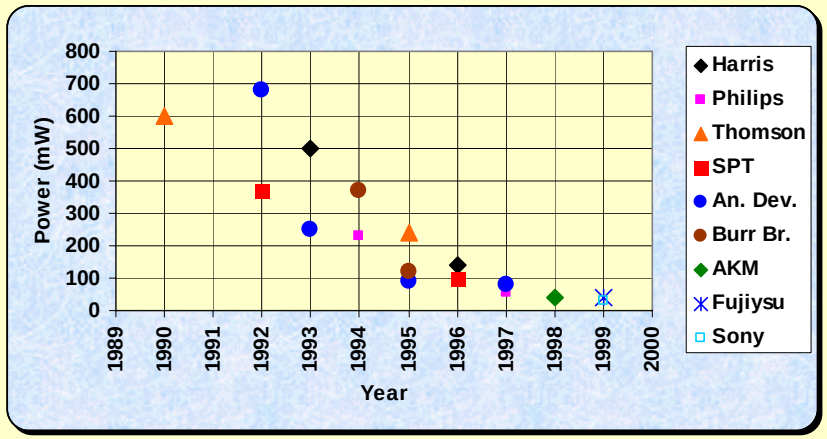




Analog to digital conversion

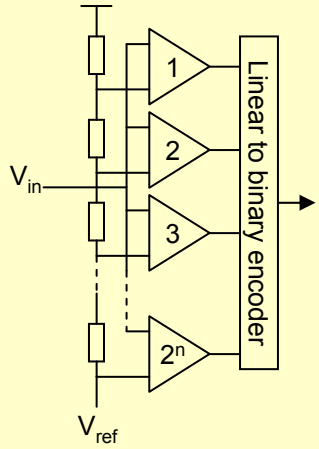
- There is clearly a tendency to go digital as early as possible
  - This is extensively done in consumer goods (but they only have one channel)
- The "cost" of the ADC determines which architecture is chosen
  - Strongly depends on speed and resolution
- Cost is here
  - **Power consumption**
  - Silicon area
  - Availability of radiation hard ADC
- Input frequencies must be limited to max Fs/2.
  - Otherwise this will fold in as additional noise.
- High resolution ADC also needs low jitter clock to maintain effective resolution

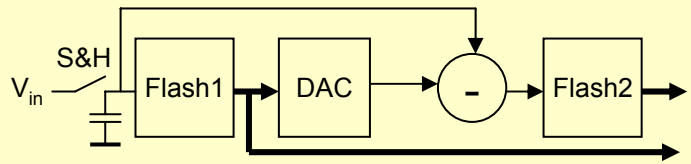




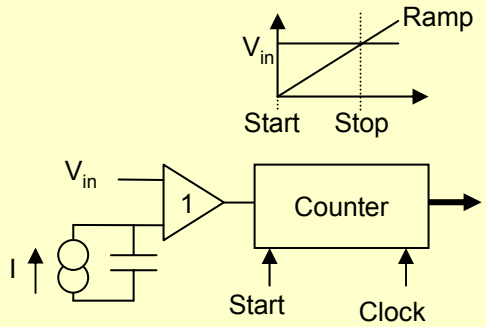
ADC architectures

- Flash
  - A discriminator for each of the 2^n codes
  - New sample every clock cycle
  - Fast, large, lots of power, limited to ~8 bits
  - Can be split into two sub-ranging Flash $2x2^{n/2}$ discriminators: e.g. 16 instead of 256 plus DAC
    - Needs sample and hold during the two stage conversion process



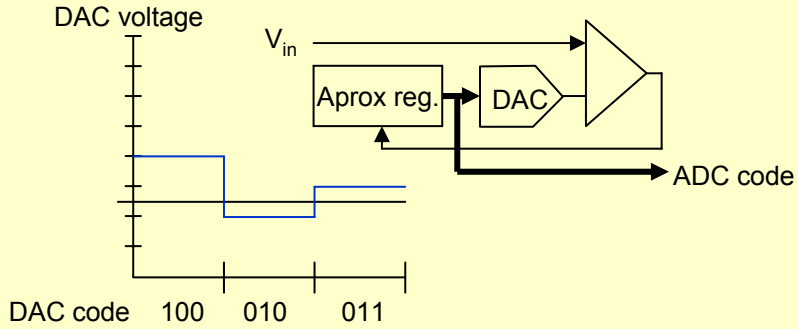


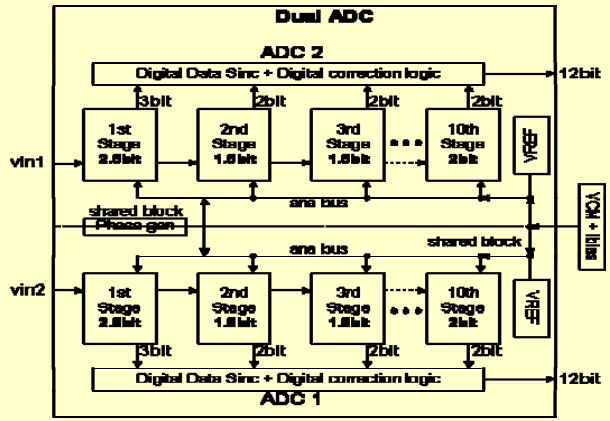
- Ramp
  - Linear analog ramp and count clock cycles
  - Takes 2^n clock cycles
  - Slow, small, low power, can be made with large resolution

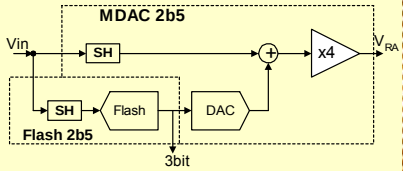


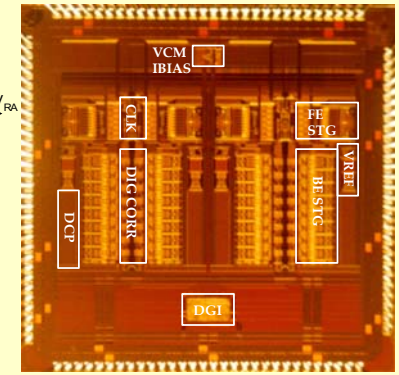
ADC architectures

- Successive approximation
  - Binary search via a DAC and single discriminator
  - Takes n clock cycles
  - Relatively slow, small, low power, medium to large resolution
- **Pipelined**
  - Determines "one bit" per clock cycle per stage
    - Extreme type of sub ranging flask
  - n stages
  - In principle 1 bit per stage but to handle imperfections each stage normally made with ~2bits and n*2bits mapped into n bits via digital mapping function that "auto corrects" imperfections
  - Makes a conversion each clock cycle
  - Has a latency of n clock cycles
    - Not a problem in our applications except for very fast triggering
  - Now dominating ADC architecture in modern CMOS technologies and impressive improvements in the last 10 years: speed, bits, power, size



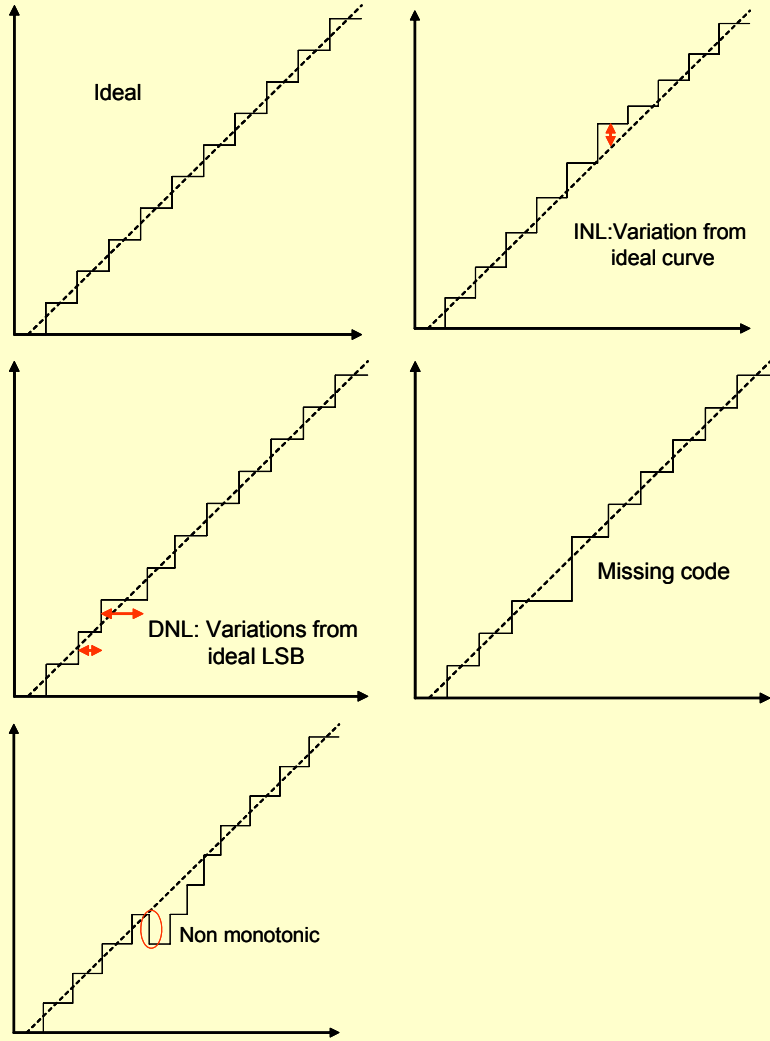




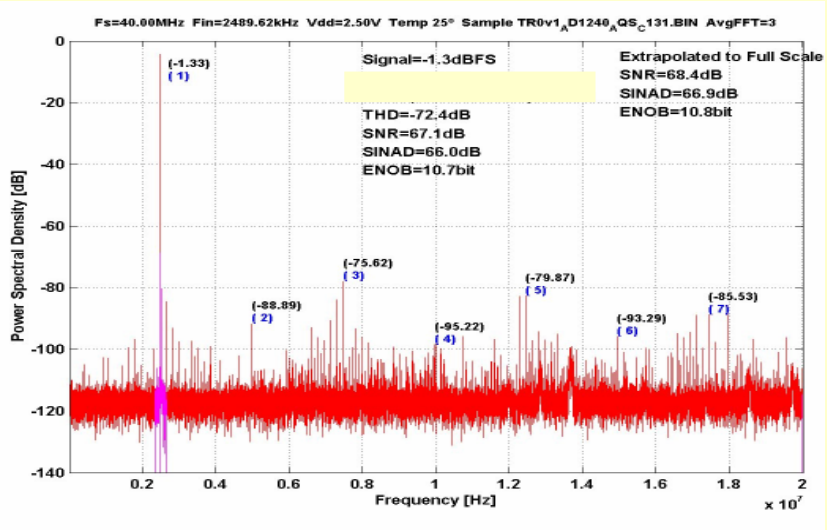


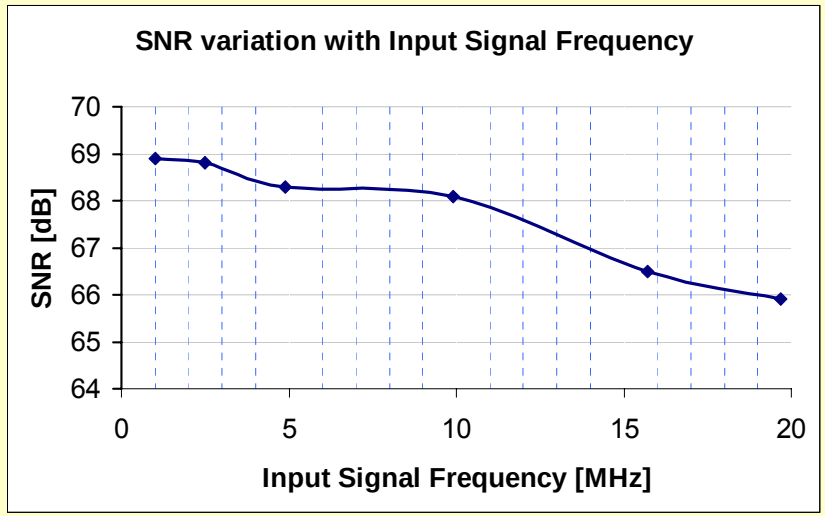
ADC imperfections

- Quantization (static)
  - Bin size: Least significant bit (LSB) $=V_{max}/2^n$
  - Quantization error: RMS error/resolution: $LSB/\sqrt{12}$
- Integral non linearity (INL): Deviation from ideal conversion curve (static)
  - Max: Maximum deviation from ideal
  - RMS: Root mean square of deviations from ideal curve
- Differential non linearity (DNL): Deviation of quantization steps (static)
  - Min: Minimum value of quantization step
  - Max: Maximum value of quantization step
  - RMS: Root mean square of deviations from ideal quantization step
- Missing codes (static)
  - Some binary codes never present in digitized output
- Monotonic (static)
  - Non monotonic conversion can be quite unfortunate in some applications.
    A given output code can correspond to several input values.



- Effective number of bits (dynamic)
  - Signal to noise ratio for ideal ADC (SNR): 6n + 1.8dB
  - Effective bits for a given input signal: (Measured SNR -1.8dB)/6
  - Typical input: Full range sinus at 1/10 – 1/20 of the sampling frequency
    - To assure that first level harmonics visible in the FFT spectrum
  - Effective number of bits will depend on reference signal frequency used.
    - Large variations on this between different implementations !
- Clock jitter affects dynamic performance
  - 1 ps jitter on 100Msamples/s ADC can result (depends on effective input bandwidth) in same error as basic quantization error of 11 bit ADC
  - Must be carefully looked at for high resolution calorimeter applications
    - Particles them selves also have jitter related to global system clock

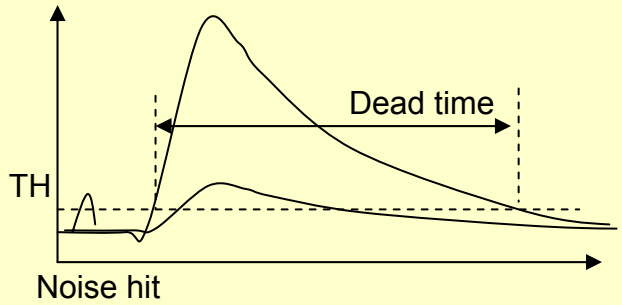


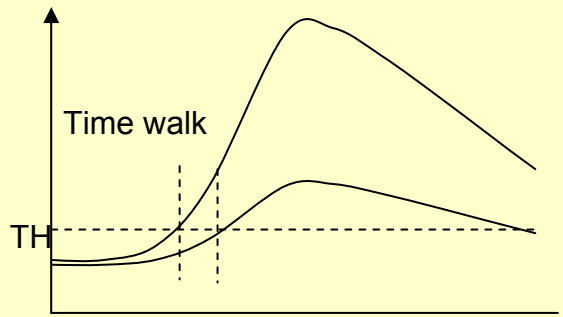


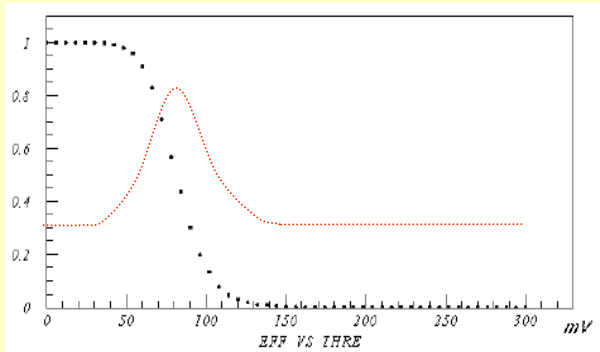
12 bit, 40Msamples used in CMS Ecal. Designed by Chipidea, IP provider

Binary systems

- Thresholding (1bit ADC)
  - Binary trackers (strips or pixels)
  - Trackers with drift time measurement (drift tubes)
  - Time of flight detectors
  - Threshold put as low as possible, without excessive noise hits, as hit signals in HEP detectors have quite large amplitude variation (compromise between hit detection efficiency and noise rates)
- Only small pedestal variations allowed
  - No dynamic range (head room) for pedestal and baseline variations
  - Requires careful analog shaping and baseline restoring
  - Good immunity to external interferences.
- Time walk
  - Threshold crossing time depends on amplitude of signal (next slide)
- Pulse width
  - Dead time limits effective hit rate that can be supported
- S curve noise extraction
  - For a large set of thresholds measure fraction of samples at 1
  - Width of transition window is a measure of noise levels. Noise histogram can be directly derived from this.

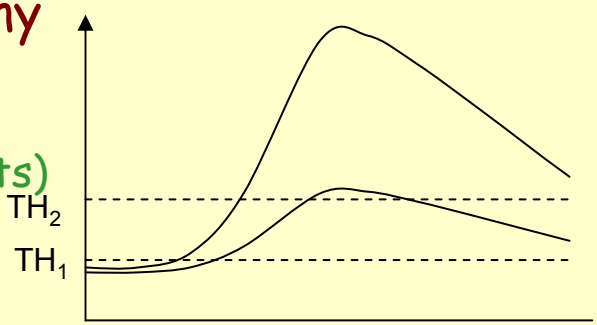




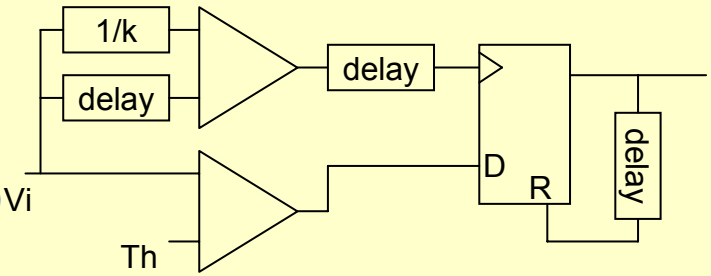


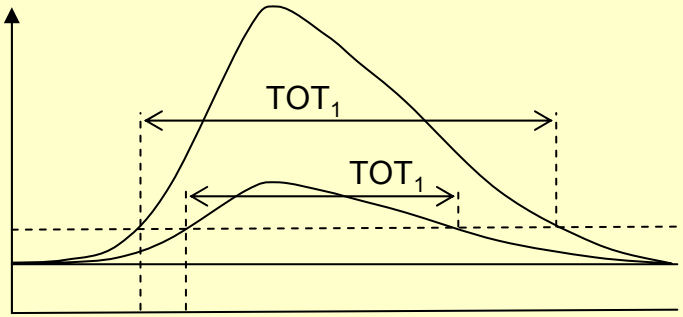
Time measurements

- Time measurements are important in many HEP applications
  - Identification of bunch crossing (LHC: 25ns)
  - Distinguishing among individual collisions (events) in continuous beam like experiments (or very short bunch interval like CLIC: ~250ps)
  - Drift time
    - Position in drift tubes (binary detectors with limited time resolution: ~1ns)
    - Time projection chamber (both good time and amplitude)
    - Time Of Flight (TOF) detectors (very high time resolution: 10-100ps)
- Time walk: Time dependency on amplitude
  - Low threshold (noise and pedestal limited)
  - Constant fraction discrimination
    - Works quite well but needs good analog delays (cable delay) which is not easy to integrate on chip.
  - Amplitude compensation (done in DAQ CPU's)
    - Separate measurement of amplitude (expensive)
    - Time measurements with two thresholds: 2 TDC channels
    - Time over threshold (TOT): 1 TDC channel measuring both leading edge and pulse width
- Time Over Threshold (TOT) can even be used as a poor mans ADC
  - E.g. ATLAS Pixel



Constant fraction discriminator

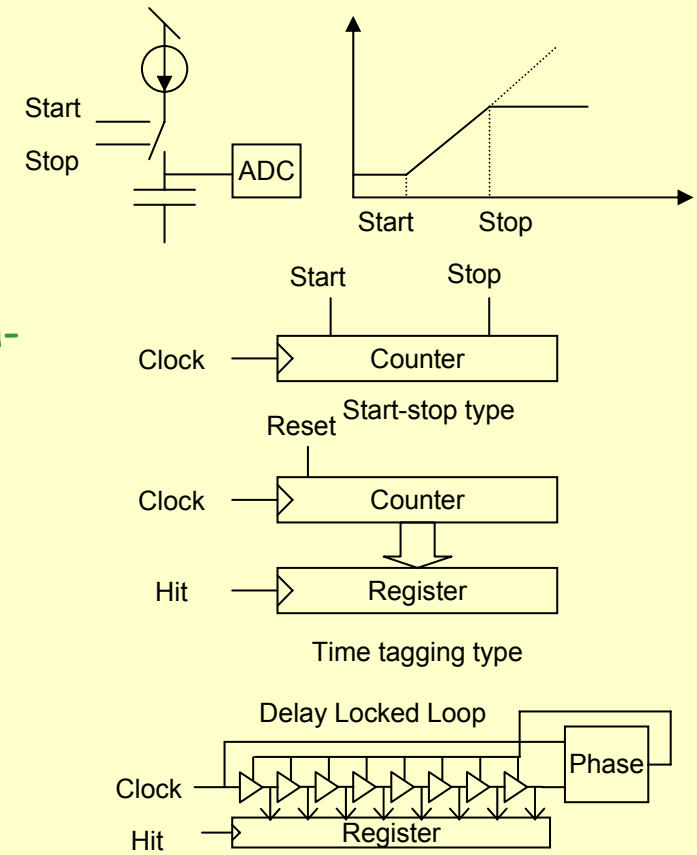




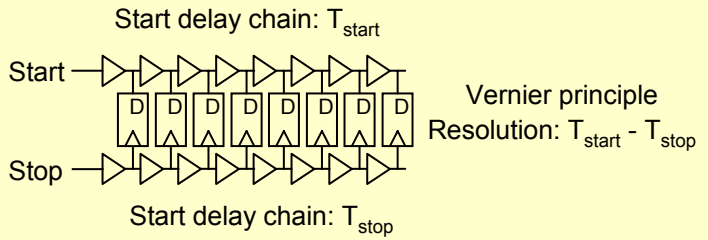
$T=T_r - f(TOT)$

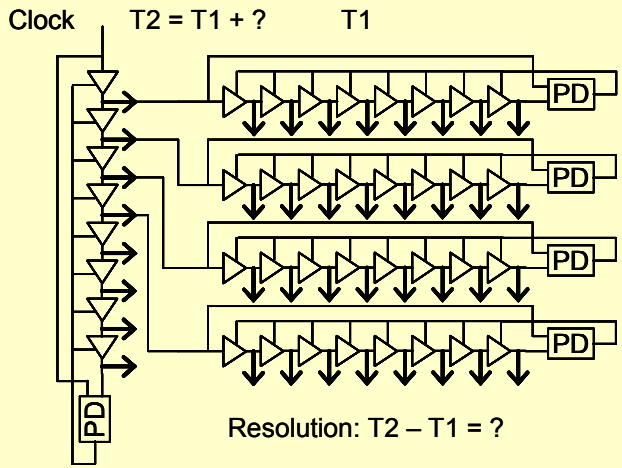
Time to digital conversion

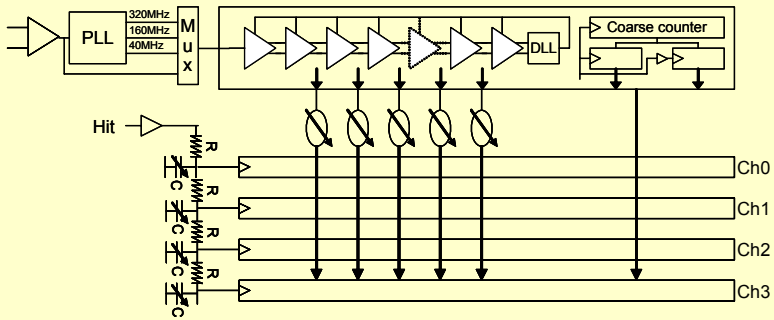
- Charge integration (start – stop)
  - Limited dynamic range
  - High resolution: ~1-100 ps
  - Sensitive analog circuit needing ADC for final conversion.
  - Sensitive to temperature, etc. so often needs in-system calibration
  - Can be combined with time counter for large dynamic range
- Counter
  - Large dynamic range
  - Good and cheap time references available as crystal oscillators
  - Synchronous to system clock so good for time tagging
  - Limited resolution: ~1ns
- Counter plus delay locked delay elements
  - Delay elements time locked to master counter clock
  - Resolution: 25 – 100ps



- Use of delay difference between delay elements in start and stop delay chains
  - Very good resolution can be obtained but in practice limited by matching of elements and time jitter in the long delay chains
  - Very long delay chains needed for each channel
  - Limited dynamic range
  - Delay element not locked to a time reference (CMOS has large variations with process, temperature and supply voltage)
- Array of delay locked loops
  - One common time reference for multiple channels
  - Locked to a time reference
- 2.nd interpolation delay chain in Channel
  - Allows a flexible architecture where channel count per chip depends on time resolution needed.

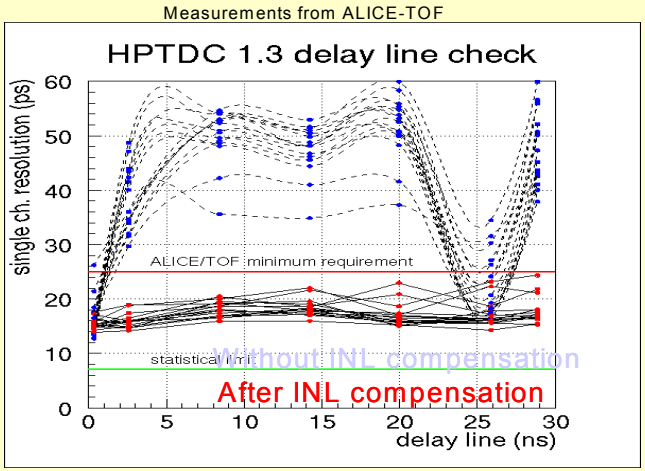


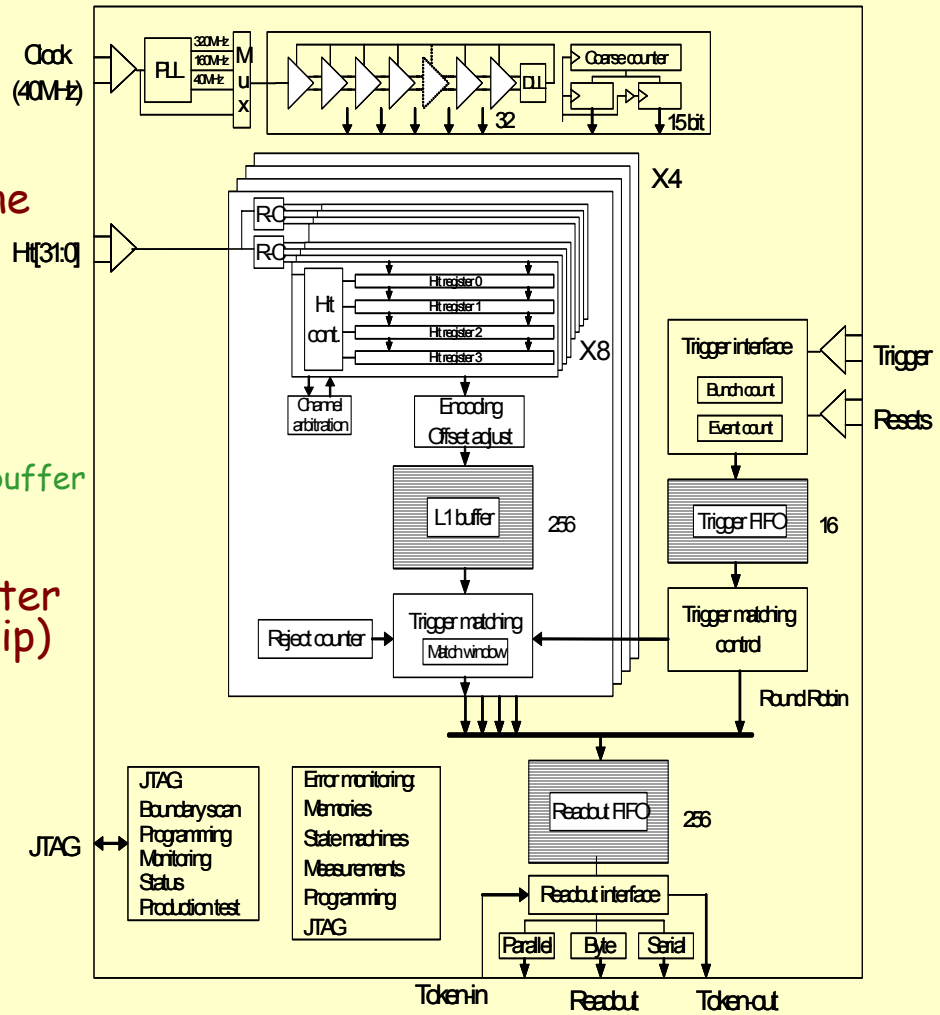




TDC example: HPTDC

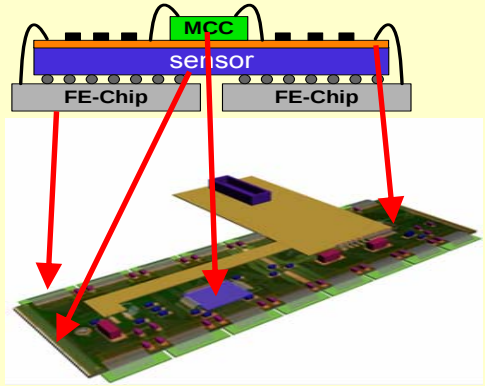
- PLL for clock frequency multiplication
- Counter for course time
- Delay locked loop for 1/32 interpolation within clock cycle
- 2nd order $\frac{1}{4}$ interpolation with RC delay line
- 32 channels with 100ps binning
- 8 channels with 25ps binning
- Data driven (not clocked pipeline buffer) architecture allows its use in a large multitude of applications
  - Exercise for you: How to make constant latency buffer in a TDC not using a pipeline.
- INL imperfections can be corrected with lookup table, as fixed pattern across master clock period (synchronous crosstalk on chip)

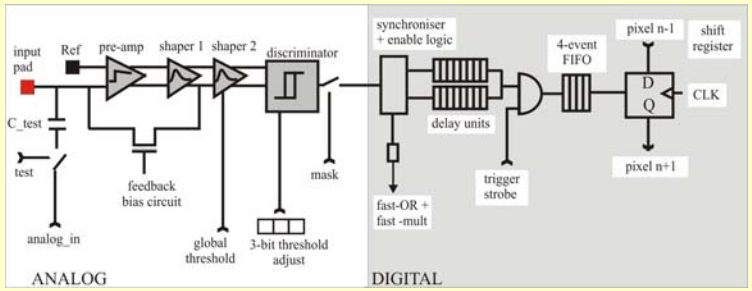


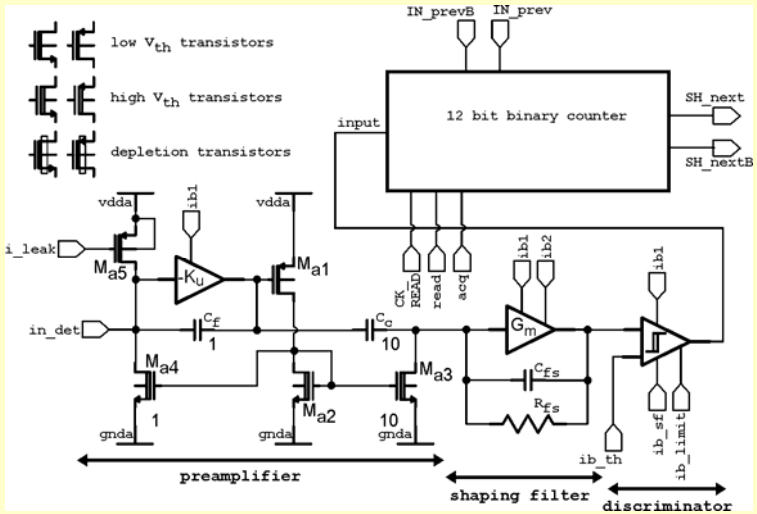


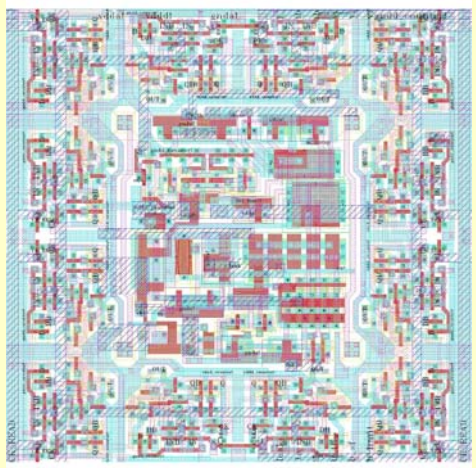
Pixel detectors

- Very tight coupling between electronics and detector.
  - Detector - electronics connection critical (bump bonding)
- Very limited area available for channel electronics
  - Pre-amp, shaper, discriminator, (buffer)
  - Use of modern high density IC technologies
  - Different basic electronics architectures to fit within limited area
- Significant sharing of deposited charge between neighbor cells in detector.
- Low detector capacitance (but significant capacitance to neighbors)
- Used for tracking in the highest particle rate parts of the detectors (close to interaction point) so detector and electronics must stand very high radiation levels (100Mrad).



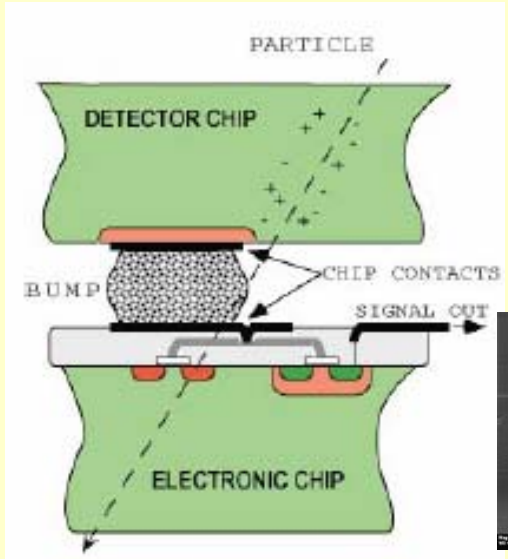


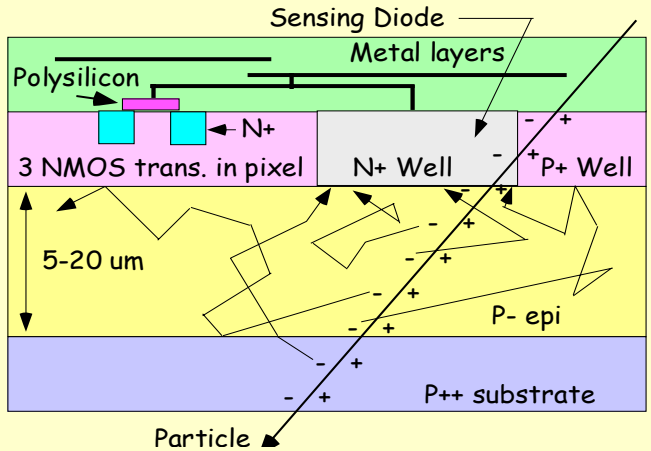




Pixels

- Separate detector with bump bonding
  - Bump bonding pitch and yield critical
  - Not compatible with standard bump bonding used to connect chips to IC packages.
- Same silicon substrate as electronics (dream/nightmare ?)
  - Use of silicon substrate below electronics as detector: Monolithic Active Pixel Sensor (MAPS)
  - No dead spots allowed in HEP (not like a CMOS camera sensor that can allocate part for electronics and other part for photon detector within pixel !.
  - Silicon substrate used for electronics chips in most cases far from ideal as silicon detector
  - Connection to the detector in the substrate and get sufficient charge collection (and speed) efficiency





Silicon strips

- Front-end chips with ~128 channels wire bonded to silicon strip detectors via pitch adaptors.
  - Wire bonding close to reach its limits with the use of ~4 layers of bond wires
- Typical front-end hybrid with single silicon strip detector and 4-8 chips. Basic building block to make whole detector
  - End caps though have many different configurations for "optimal" coverage
- Binary, Digital or Analog architecture that's the question
  - Readout of amplitude information allows strip interpolation and common mode correction
  - 4(1) – 8 bits resolution sufficient
- SNR 10 – 30 as strips have relatively high capacitance ~10pf and signal ~20ke.

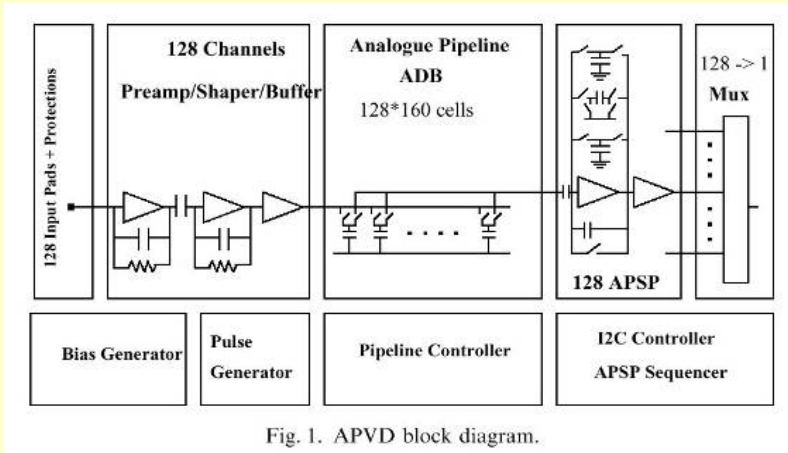
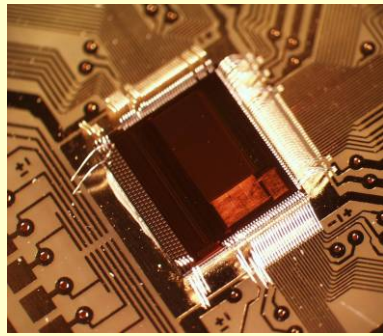
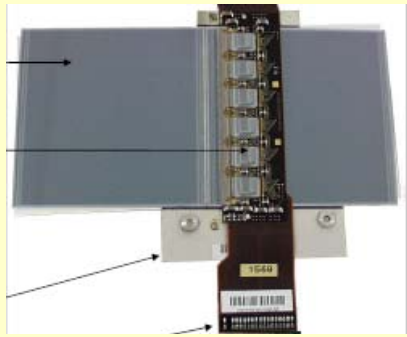
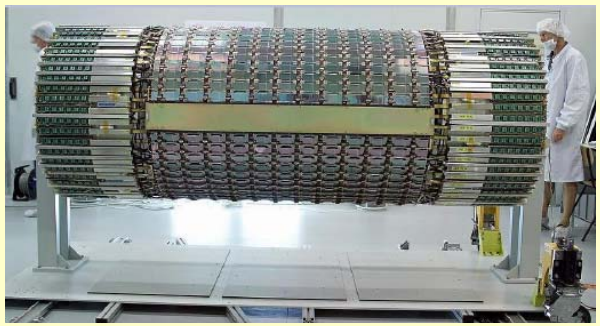


Fig. 1. APVD block diagram.

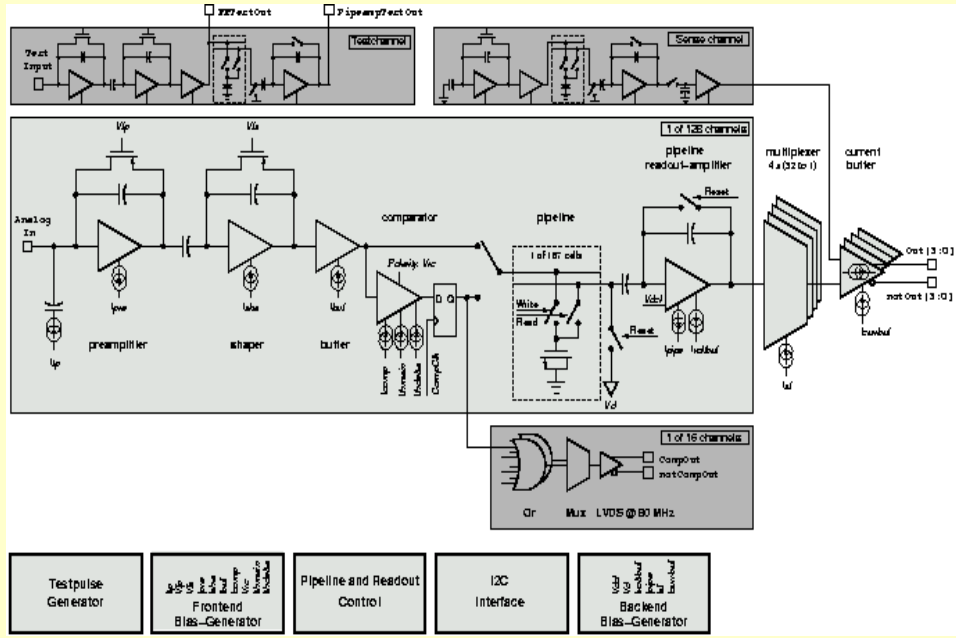


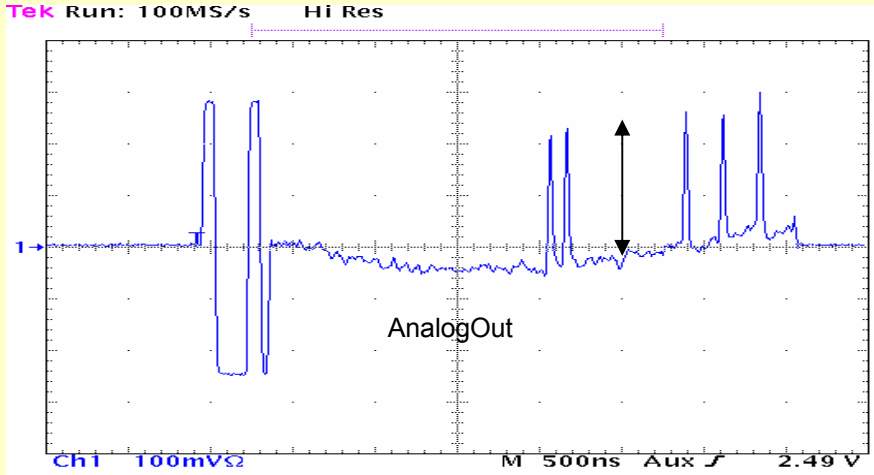


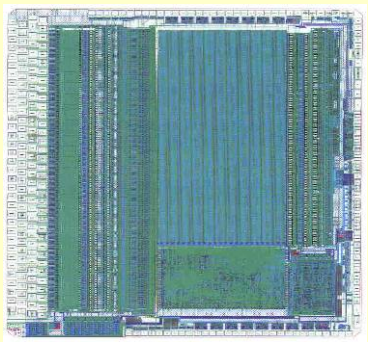


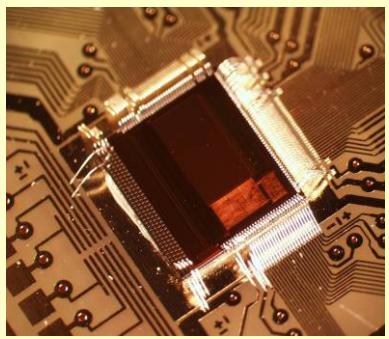
BEETLE

- Front-end chip of LHCb Vertex, trigger tracker, silicon tracker and pileup detectors.
  - 128 channels
  - Low noise preamp
  - Shaper with programmable shaping time
  - Analog memory for L0 latency and L0 derandomizer,
  - Analog readout at 1 MHz event rate over four analog differential links.
  - Discriminators for pileup (or of 4 ch.)
  - Radiation hard 0.25 um CMOS.
  - Triple redundant logic (SEU)
- Performance
  - Fully functional up to 100MHz
  - Excellent noise characteristics
    - ~540 e^- + 50e^-/pf
  - Temperature, voltage, and trigger tests performed
  - Extensive detector tests made
  - Radiation hard to above 10Mrad



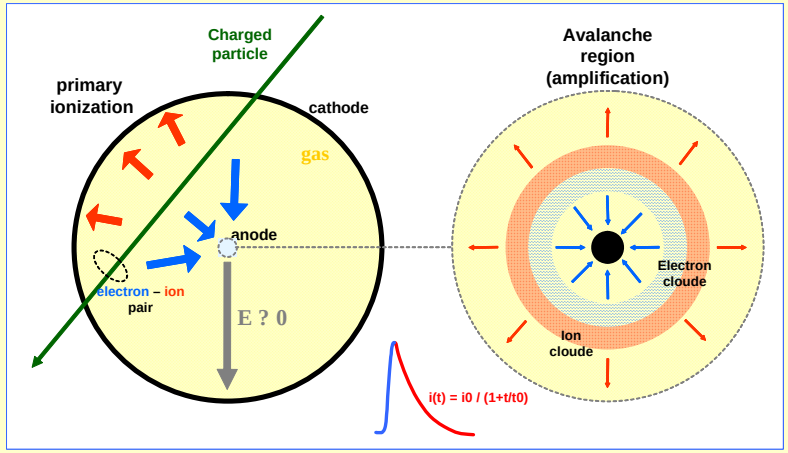


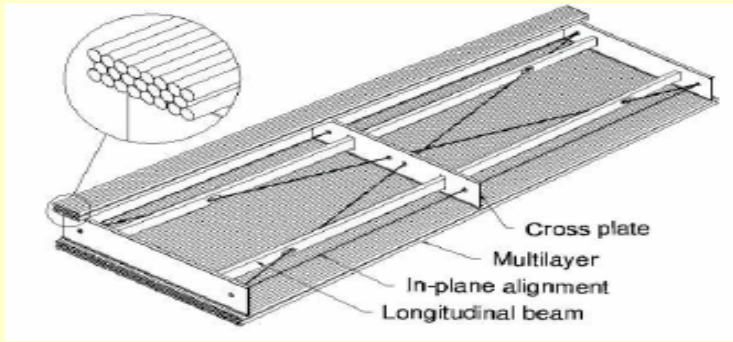


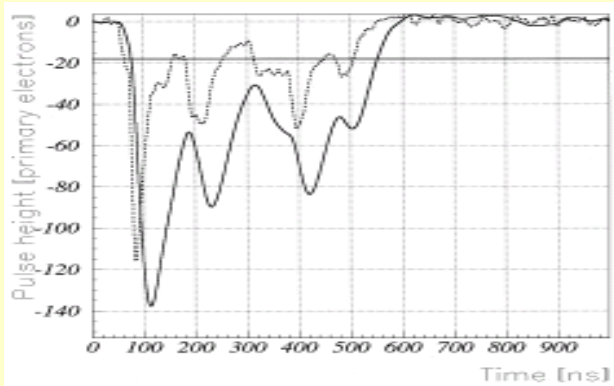


Drift tubes

- Used for tracking where hit rates are limited (but can be several MHz)
- Limited integration of electronics needed as channel density given by size of tubes (0.5 – 5 cm)
- ASDBLR and TDC with data buffering
- As drift tubes can be relatively long (several meters) the preamplifier must terminate the signal propagation with the characteristic impedance of the "coax" tube.
  - Otherwise multiple reflections will occur
  - Far end of tube should also be terminated but resistive termination will give some noise increase (signal reflections can though be a worse problem)
- Ion tail to be removed in dedicated filtering
- Signal consists of multiple clusters from primary ionizations
- Maximum drift time can be longer that maximum spacing between triggers
  - Requires special logic to allow detected hits to be assigned to multiple events for readout

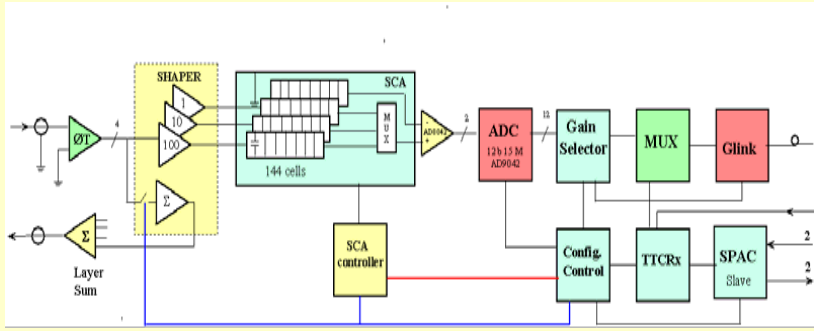


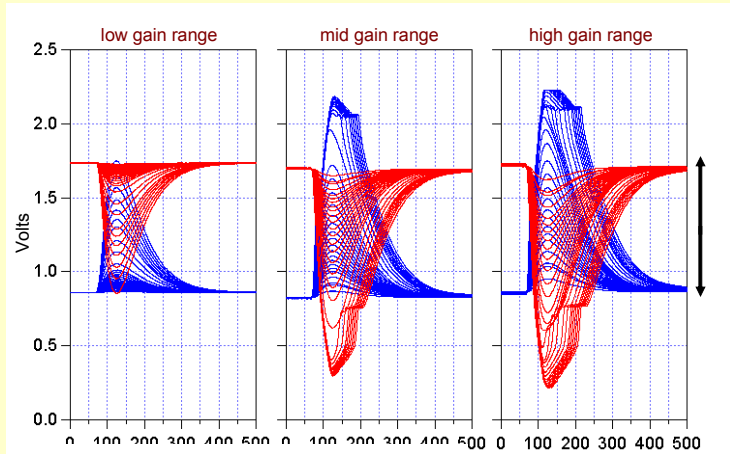


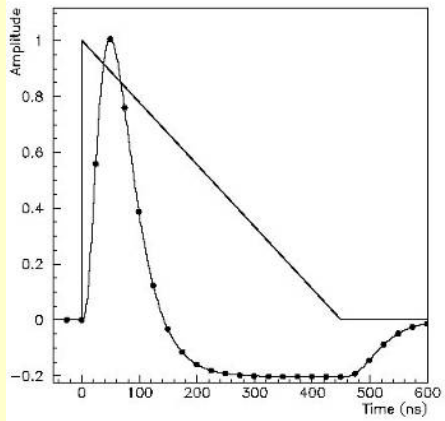


Calorimeters

- Large dynamic range 12 – 16 bit
- Two common schemes to obtain required resolution and dynamic range
  - Multi gain architectures with ~3 signal paths. E.g. relative gains of 1, 4, 32. Use of single or multiple ADC's per channel
  - Non linear ADC with 10-12 bit resolution but covering 16 bit dynamic range
    - Has been tried on multiple occasions but turns out to be difficult to make in practice (calibration, assure constant nonlinear shape, etc.)
- Analog shaping typically done such that multiple samples per pulse are available
  - Lower bandwidth -> Lower noise in analog front-end
  - Digital filtering can remove pileup signals
  - Decreased quantization noise when multiple samples with real signal content are available
  - 4 – 8 samples per event including pre-samples to measure well baseline levels or pileup from previous signals.
- Zero-suppression with simple thresholding normally not applicable as this will give reduced energy resolution (halo of small signals around cell with major signal).
  - Zero-suppression with neighbor information
  - Data compression instead of zero-suppression
- Limited integration needed as Calorimeter cells normally several centimeters wide
  - Exception for new class of tracking calorimeters under development for ILC, CLIC, etc.

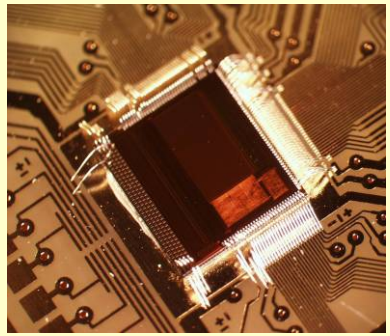


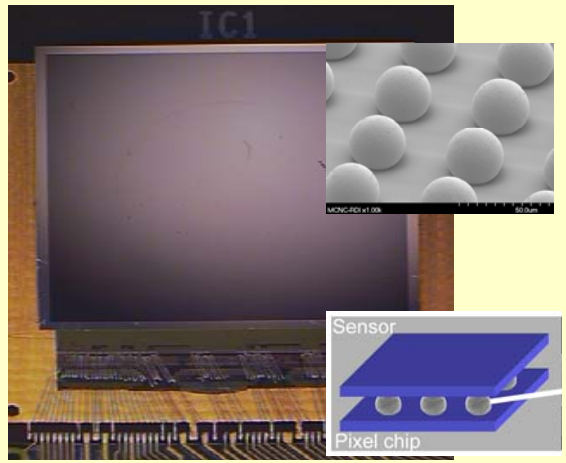


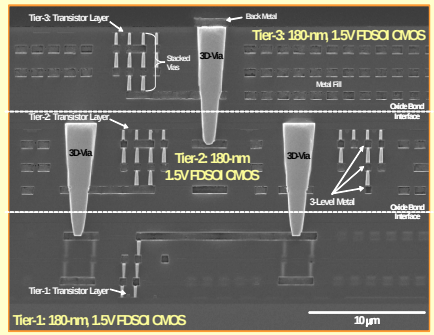


Connection to detector

- Discrete (Detector itself may be made from PCB)
  - Calorimeters, drift tubes, wire chambers, etc.
- Wire bond (silicon strips)
  - Use of multi level wire bonding have reached its limits
- Bump bonding (pixels)
  - Pixel chip and pixel detector bump bonded to each other
  - Fine pitch bump bonding not really yet standard industrial process so yield problems and delays are often encountered
- MAPS
  - Use electronics chip substrate as detector
  - Substrate may not be perfect for detector purposes. (leakage, charge collection, etc.)
  - Biasing and connection to detector part not obvious
- 3D: Our dream for the future
  - Multi level electronics and dedicated detector substrate in a chip stack
  - In R&D phase in several labs and companies
  - Will it offer sufficient yield and low cost for it to become available to us and others (consumer applications will determine its future or it may stay too expensive for us)
- Electronics is getting more and more integrated with detector itself (may even be on same silicon substrate)





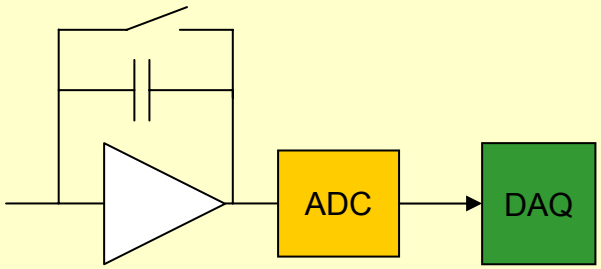


Readout architectures

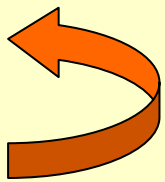
- After basic analog amplification and shaping the architecture of the remaining front-end readout systems depends on many factors
  - Number of channels and channel density
  - Collision rate and channel occupancies
  - Triggering: levels, latencies, rates
  - Available technology and cost
  - What you do in custom made electronics and what you do in CPU farm based DAQ system
  - Radiation levels
  - Power consumption and related cooling
  - Location of digitization
  - Given detector technology
- All sub-detectors in an experiment MUST comply to one common basic architecture and some key parameters
  - There are lots of different good ideas of what is the best architecture and what suits my "private" sub-detector best.
  - Simplicity for large complicated systems for sure makes the difference between a good working experiment and a nightmare
  - A globally defined architecture can be implemented in many different ways

Single integrator

- Simple (only one sample per channel)
- Slow rate (and high precision) experiments
- Long dead time
- Nuclear physics
- Not appropriate for HEP

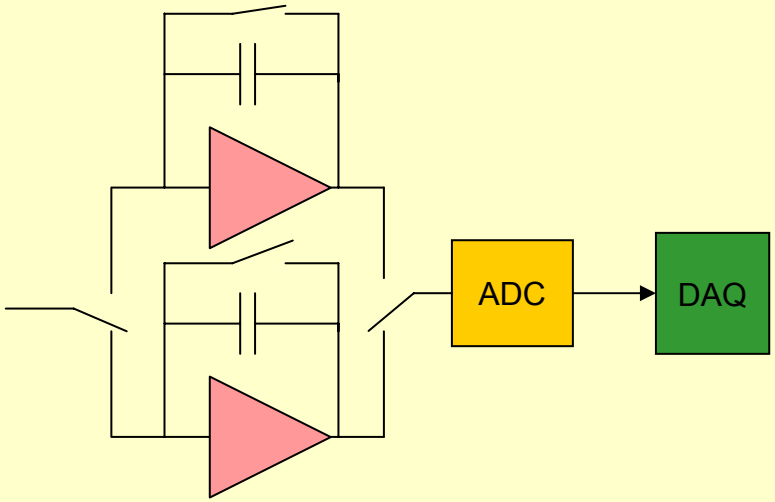


1. Reset charge integrator
2. Collect charge from event
3. Convert with ADC
4. Send data to DAQ



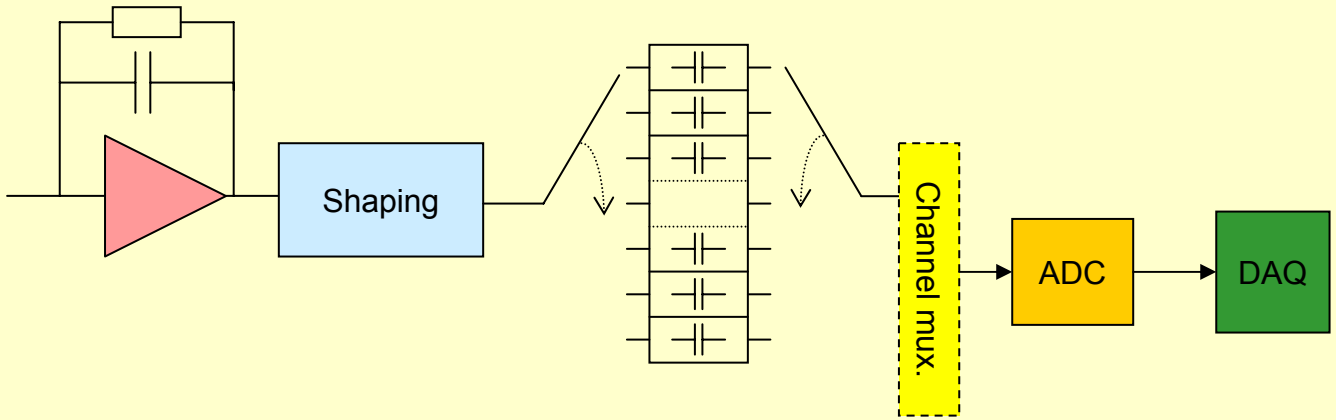
Double buffered

- Use a second integrator while the first is readout and reset
- Decreases dead time significantly
- Still for low rates



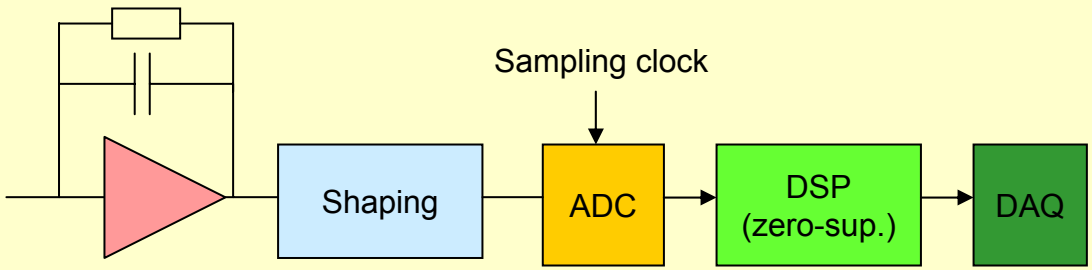
Multiple event buffers

- Good for experiments with short spills and large spacing between spills.
- Fill up event buffers during spill (high rate).
- Readout between spills (low rate).
- ADC can possibly be shared across channels
- Buffering can also be done digital



Constantly sampled

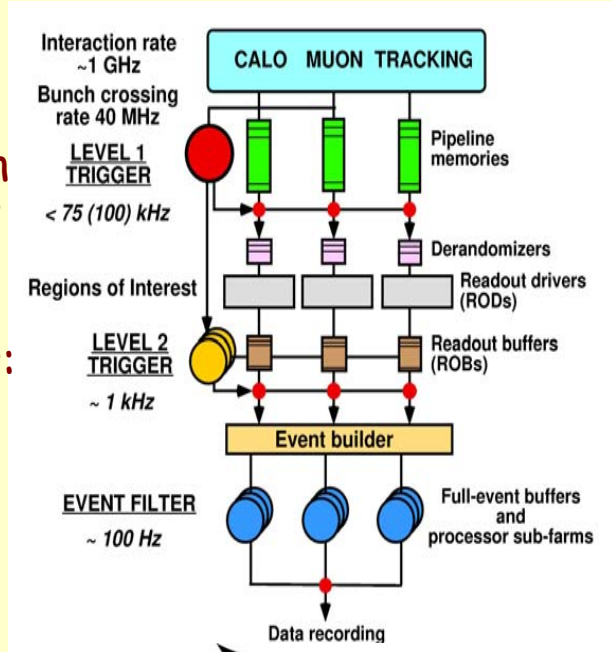
- Needed for high rate experiments with signal pileup
- Shapers and not switched integrators
- Allows digital signal processing in its traditional form (constantly sampled data stream)
- Output rate may be far to high for what following DAQ system can handle

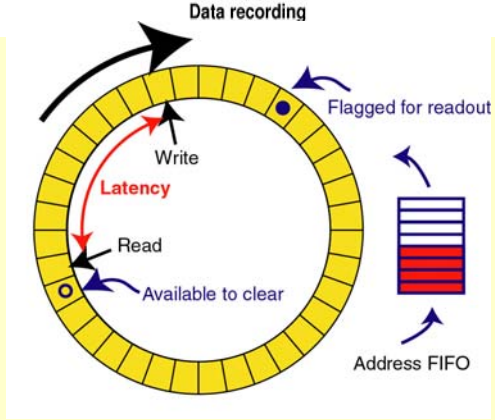


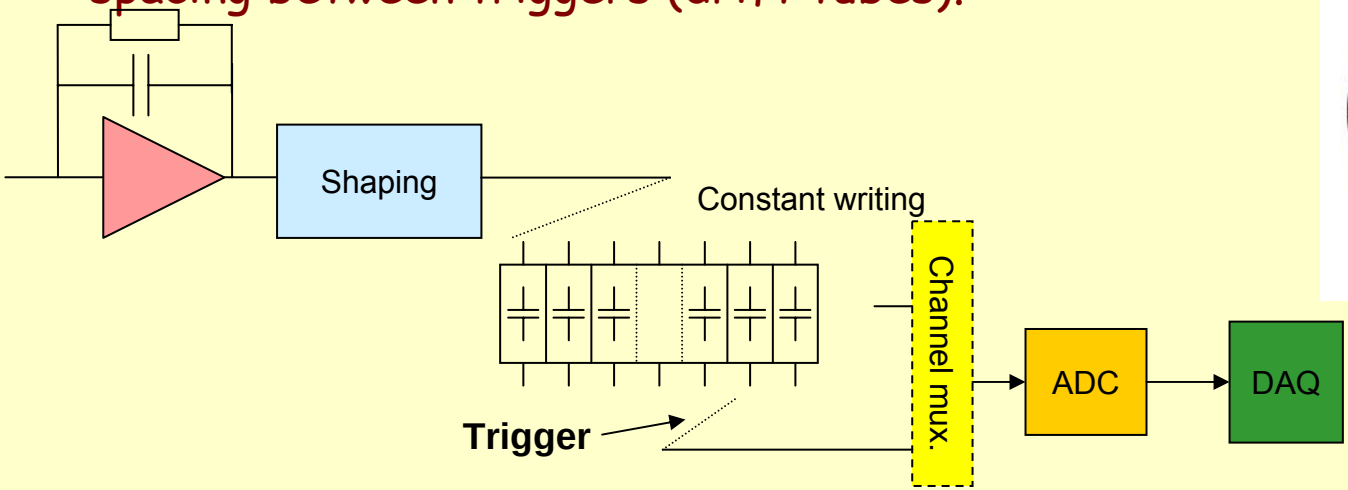
- With local zero-suppression (DSP) this may be an option for future high rate experiments

Triggered

- Separate trigger system quickly determines events of interest and informs front-end about this
- Trigger processing requires some data transmission and processing time to make decision so front-ends must buffer data during this latency
- For constant high rate experiments a "pipeline" buffer is needed in all front-end detector channels: analog or digital
  1. Real clocked pipeline (high power, large area, bad for analog)
  2. Circular buffer
  3. Time tagged (zero suppressed latency buffer based on time information)
- Specific complications for detectors where more data samples must be extracted than minimum spacing between triggers (drift tubes).

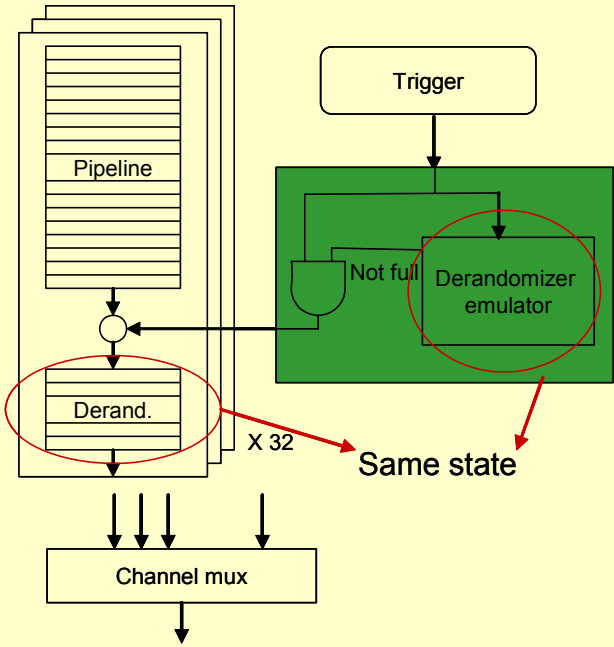




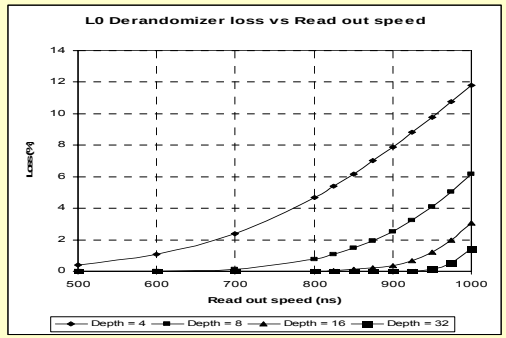


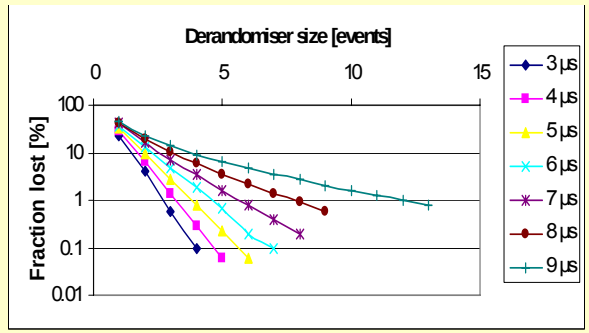
Trigger rate control

- Trigger rate determined by physics parameters used in trigger system: 1 kHz – 1MHz
  - The lower rate after the trigger allows sharing resources across channels (e.g. ADC and readout links)
- Triggers will be of random nature so a burst of triggers can occur within a short time window so some kind of rate control/spacing is needed
  - Minimum spacing between trigger accepts
  - Maximum number of triggers within a give time window
- Derandomizer buffers needed in front-ends to handle this
  - Size and readout speed of this determines effective trigger rate
  - A centralized control mechanism needed to prevent any derandomizer to overflow as the system may otherwise get desynchronized.



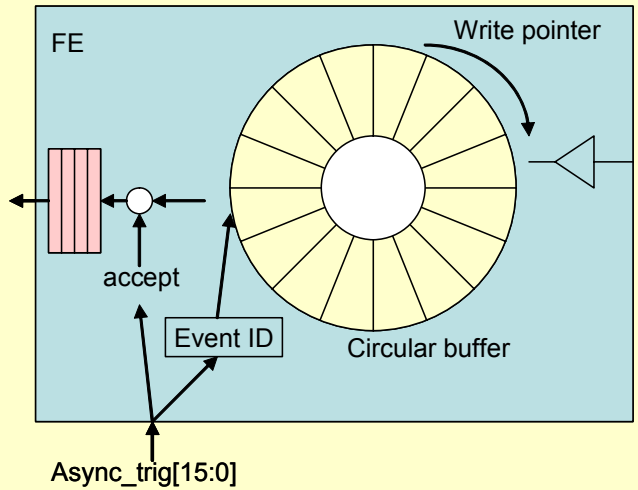
Rule example (LHCb) : 1MHz
Depth: 16 events
Max readout time: 900ns

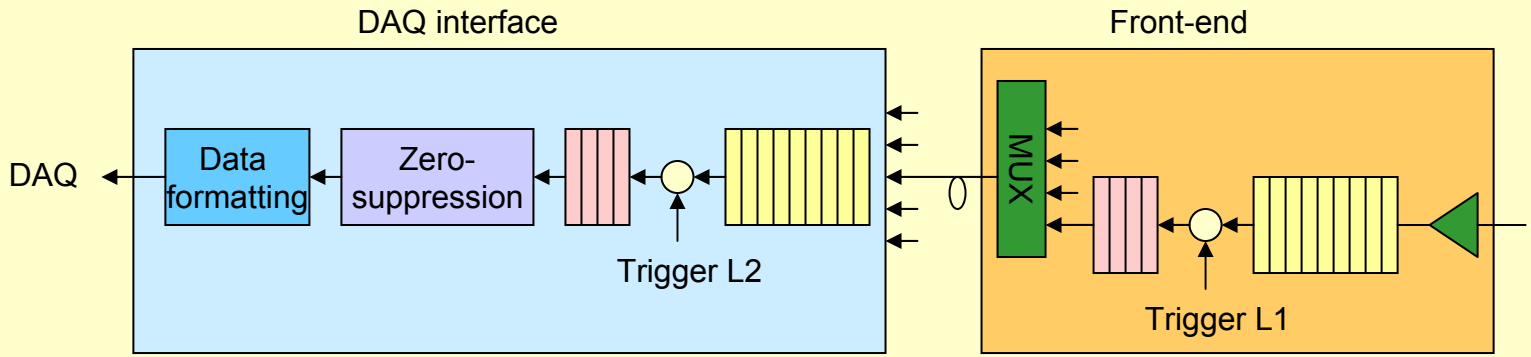




Multilevel triggering

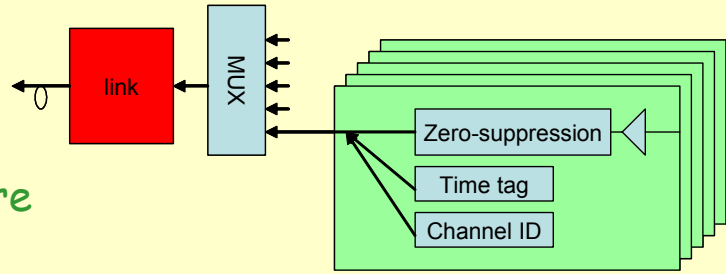
- First level triggering.
  - Hardwired trigger system to make trigger decision with short latency.
  - Constant latency buffers in the front-ends
- Second level triggering in DAQ interface
  - Processor based (standard CPU's or dedicated custom/DSP/FPGA processing)
  - FIFO buffers with each event getting accept/reject in sequential order
  - Circular buffer using event ID to extracted accepted events
    - Non accepted events stays and gets overwritten by new events
- High level triggering in the DAQ systems made with farms of CPU's: hundreds – thousands. (separate lectures on this)

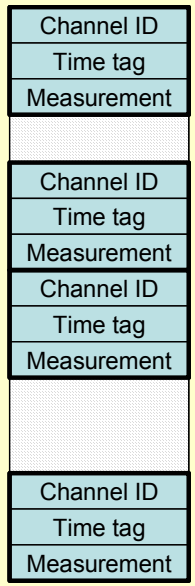




Local zero-suppression

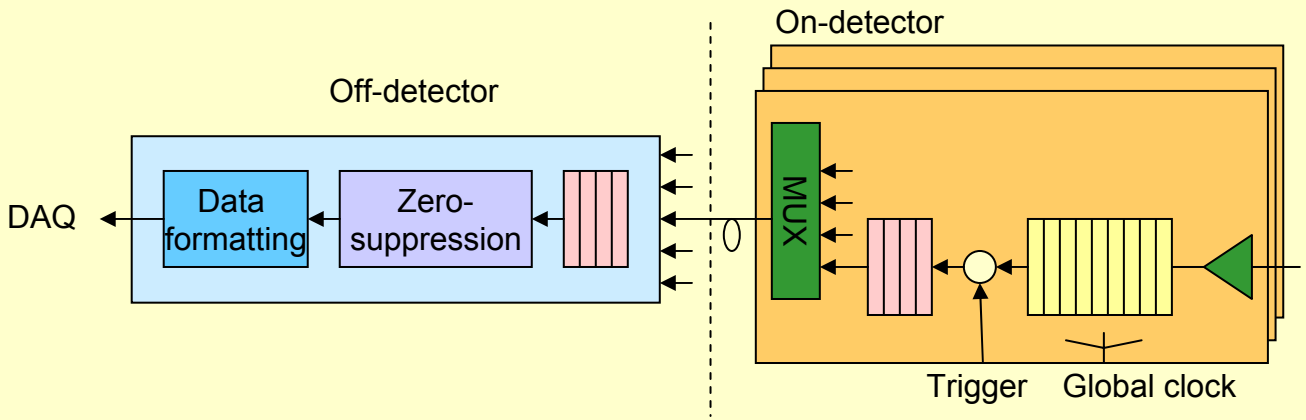
- Why spend bandwidth sending data that is zero for the majority of the time ?
- Perform zero-suppression on detector and only send data with real content
  - We do not want to loose information of interest so this must be done with great care taking into account pedestals, baseline variations, common mode, noise, etc.
  - Use of digital signal processing
  - Not worth it for occupancies above ~10%
- Alternative: data compression
  - Huffman encoding and alike
- Gives some system problems that makes it non trivial
  - Data rates fluctuates all the time and we have to fit this into links with a given bandwidth
  - Not any more event synchronous
  - Complicated buffer handling (overflows)
  - Before an experiment is built and running it is very difficult to give reliable estimates of data rates needed (background, new physics, etc.)





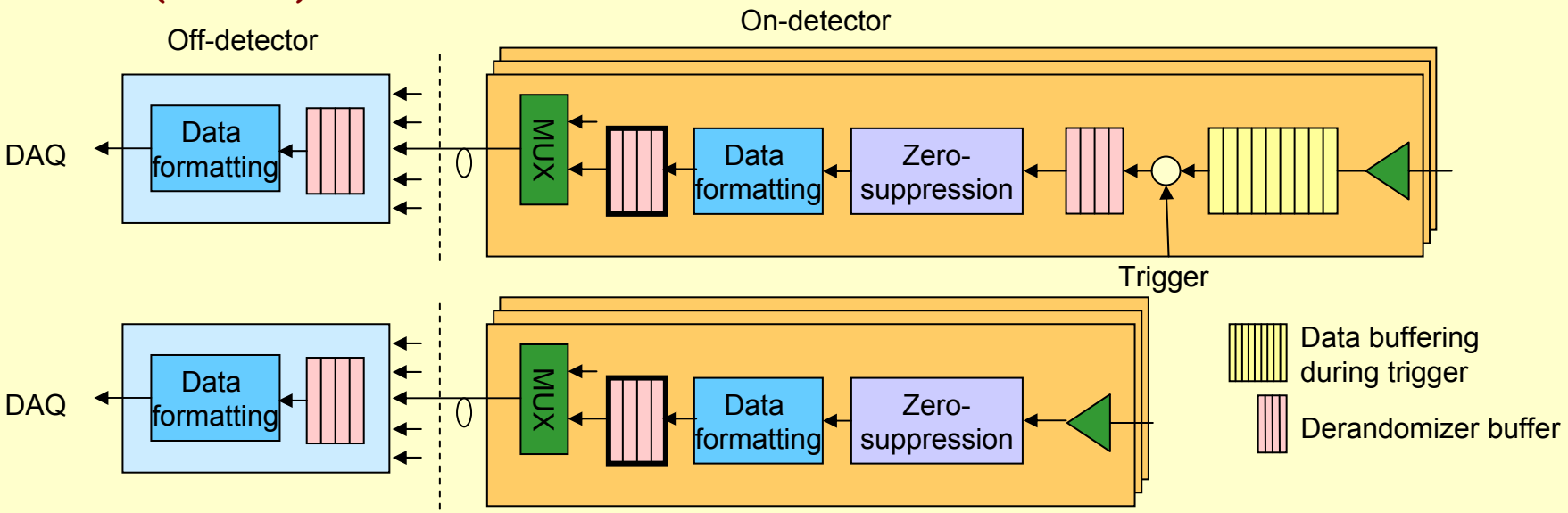
Synchronous readout

- All channels are doing the same "thing" at the same time
- Synchronous to a global clock (bunch crossing clock)
- Data bandwidth is "constant" (depends on trigger rate only)
- Data from all channels readout which allows DAQ system to perform common mode compensation and alike
- Buffers (de-randomizers) in the front-ends runs synchronous and can be prevented to overflow with a single central control
- Lots of bandwidth wasted for zero's
  - Price of links determine if one can afford this
- No problems if occupancy of detectors higher than expected
  - But there are other problems related to this: spill over, saturation of detector, etc.



Asynchronous readout

- Only readout of non zero data
- Lower average bandwidth needed for readout links
  - Especially interesting for low occupancy detectors
- Each channel "lives a life of its own" with unpredictable buffer occupancies
- It is unknown if collected event actually contains all hits (unless running at very low trigger rate)
  - Or having a complicated scheme to keep track of what has been lost when a local data buffer has overflowed.
  - Detectors themselves do not have 100% detection efficiency either.
- Requires sufficiently large local buffers to assure that data is not lost too often
  - Channel occupancies can be quite non uniform across a detector with same front-end electronics
  - Efficient for detectors with low occupancies
- (may still use a global synchronous clock but is not synchronous at the event level)
- DAQ systems runs with zero-suppressed data but has very large buffers, lower rates and much more intelligence to handle this
- Async. readout of detectors in LHC: ATLAS and CMS muon drift tube detectors, ATLAS and CMS pixel detectors, ATLAS SCT, several ALICE detectors as relatively low trigger rate (few kHz).



Analog buffers

- Extensively used when ADC not available with sufficient speed and resolution or consuming too much power
- Large array of storage capacitors with read and write switches (controlled digitally)
- For good homogeneity of memory
  - Voltage mode
  - Charge mode with Charge integrator for reading
- Examples:
  - Industrial: Sampling oscilloscopes
  - HEP: CMS tracker, ATLAS calorimeter, LHCb trackers, etc.

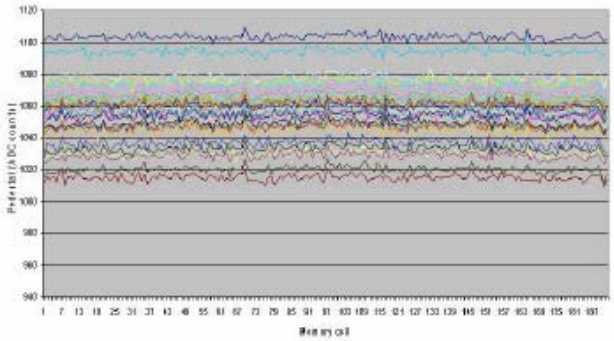


Fig. 9 Pedestals for each memory cell in the analog memory. All 32 channels plotted for each of the 192 columns. This plot is of a packaged PACE3 device. 1 ADC count = 0.435mV.

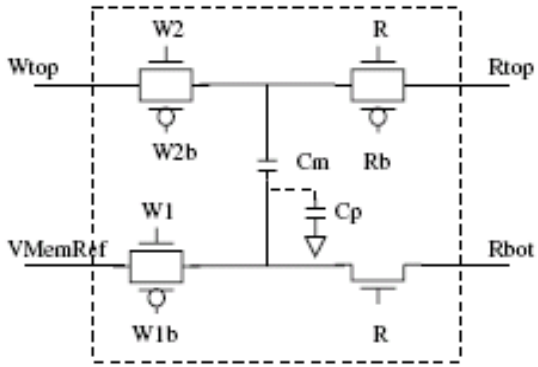
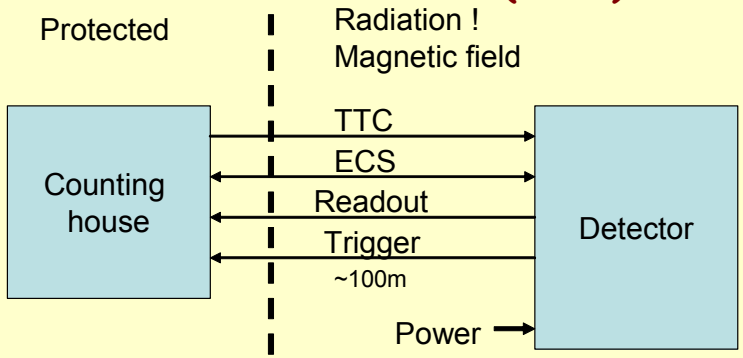


Fig. 5 The analog memory cell of PACE3

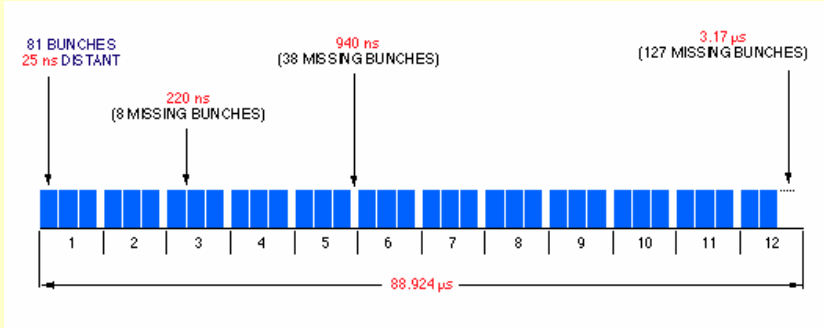
Connections to detector

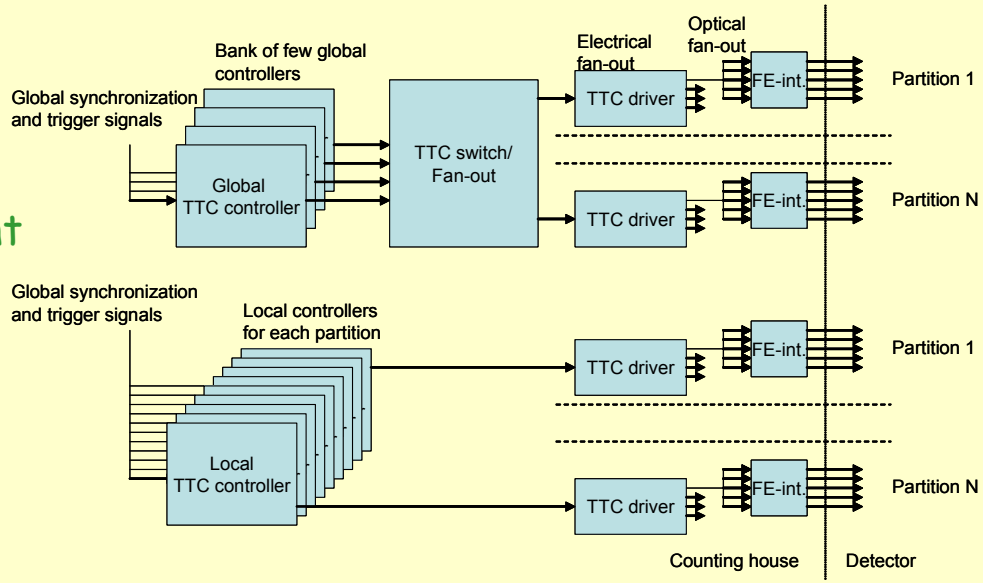
- Timing Trigger Control (TTC) of front-end
  - Synchronize all detector channels to particle collisions and between channels to correlate hits from same event (not mixing events)
  - Trigger decisions to all pipeline buffers.
  - Speed and time precision determined by accelerator and specific requirements of detector (e.g. high resolution calorimeters)
- Control and monitoring: ECS=Experiment Control System or DCS= Detector Control System, Slow control
  - Read and write control and monitoring front-end registers
- Readout
  - Sending collected information from detector to DAQ interface
- Trigger
  - Sending high speed low latency information to trigger system (similar to readout links)
- Power
  - Obviously a very different connection type (see later)
- On-detector side may have significant radiation levels that prevent existing commercial solutions to be used (LHC).



Timing & sync control

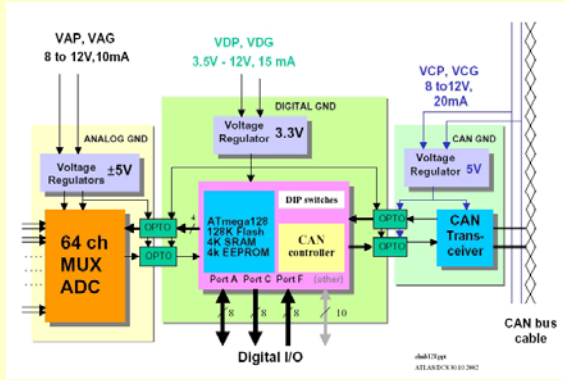
- Sampling clock with low jitter
- Synch reset
- Synchronization with machine bunch structure
- Calibration
- Trigger (with event type)
- Time align all the different sub-detectors and channels
  - Programmable delays
- Fan-out – unidirectional
  - Global fan-out to whole experiment or
  - Sub-detector fan-out
- Must be reliable as system otherwise may get de-synchronized which may take quite some time to correct





Control and monitoring

- Access to setup registers (must have read-back)
- Access to local monitoring functions
  - Temperatures, power supply levels, errors, etc.
- Bidirectional with addressing capability (module, chip, register)
- Speed not critical and does not need to be synchronous
  - Low speed serial bus: I^2C, JTAG, SPI
- Must be reasonably reliable (read-back to check correct download and re-write when needed)



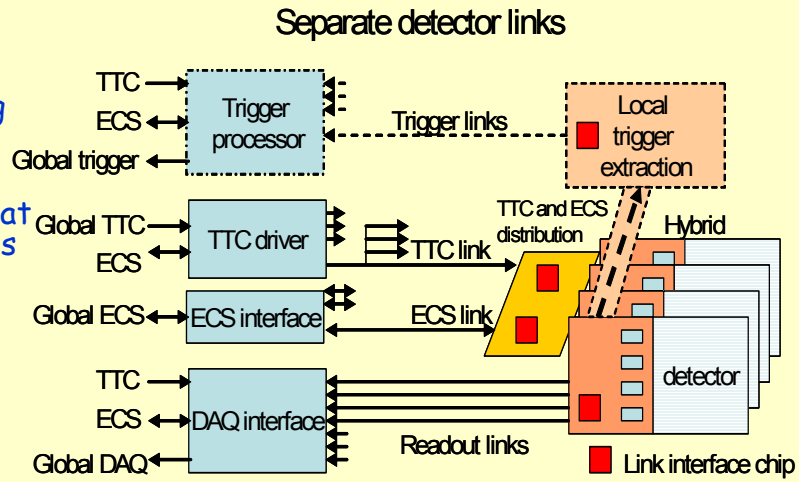
Example: ELMB

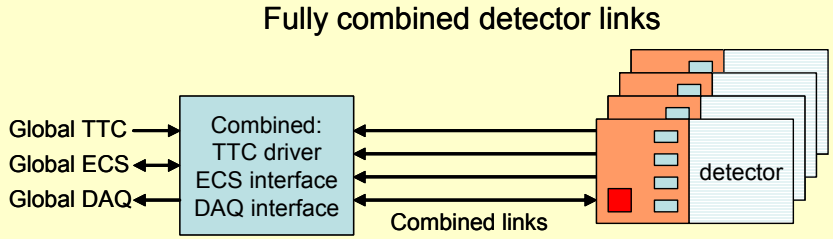
Readout

- Large amount of data to bring out of detector
  - Large quantity: ~100k in large experiment
  - High speed: Gbits/s
- Point to point unidirectional
- Transmitter side has specific constraints
  - Radiation
  - Magnetic fields
  - Power/cooling
  - Minimum size and mass
  - Must collect data from one or several front-end chips
- Receiver side can be commercially available module/components (use of standard link protocols when ever possible)

Separate or shared links

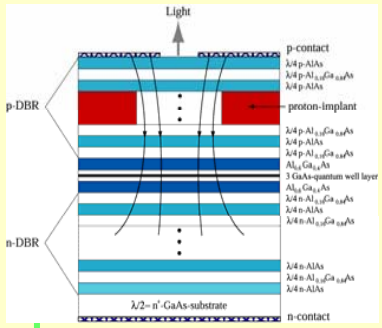
- There has been a tendency to keep the 3 (4) link types separate
  - Minimize interference
    - E.g. do not interrupt readout data flow when reading some monitoring information
    - Requirements for the three quite different
    - If the TTC or DAQ link does not work then one can at least diagnose problem via control and monitoring bus (but this part of the detector does still not work)
  - Three different cultures
    - Timing: hardware guys
    - Readout: DAQ guys
    - Control and monitoring: Slow control guys.
- Merged/shared
  - Modern optical links have so large bandwidth that a simple non interfering bandwidth sharing scheme can be used
  - Bus structures on its way out of computing (switched)
  - Each link only connects to small part of detector so failing link only implies loss of small detector part
  - Minimizes the number of interfaces to develop on front-end side and in counting house side

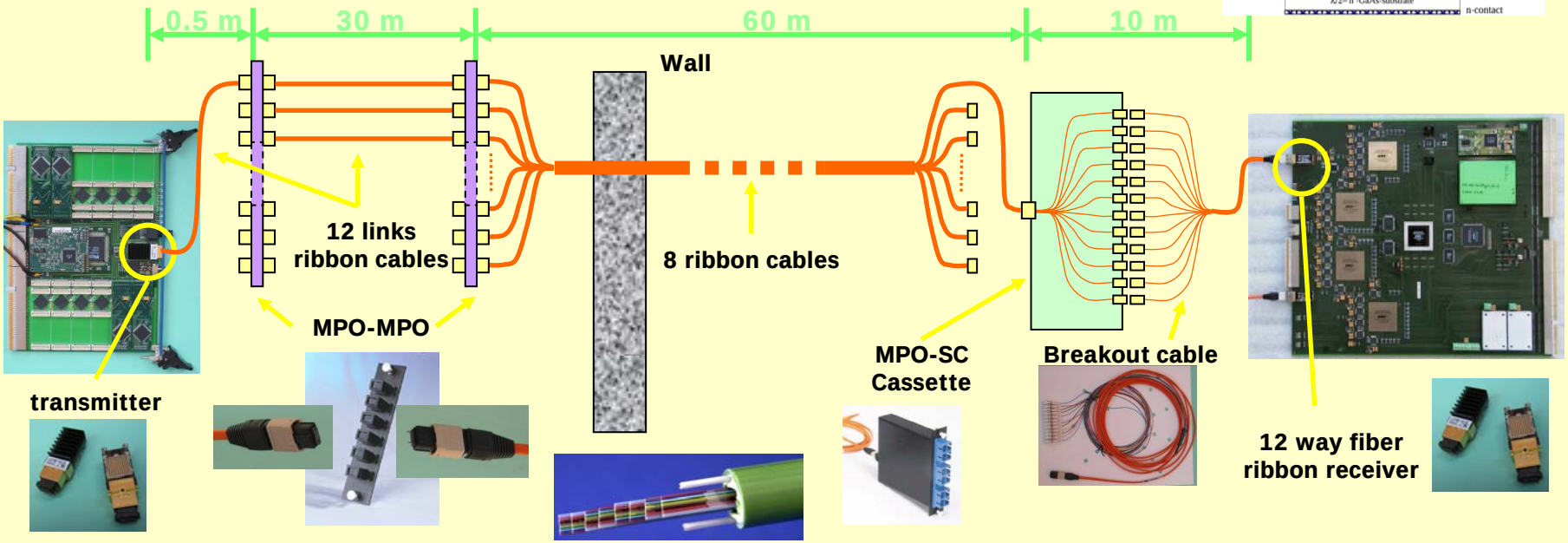




Optical links

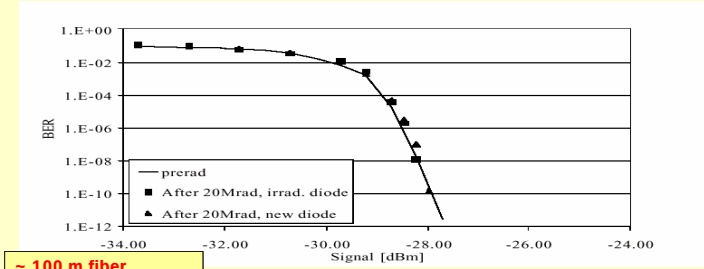
- High speeds
- Covers relatively easy distances needed for experiments: ~100m
- Galvanic isolation and no EMC/coupling problems
- High density cabling
- High density transmitters and receivers (e.g. 12 channels in snap12 module)
- Radiation effects on fibre, Laser and PIN
  - Appropriate components have been identified (e.g. VCSELS)
- Critical packaging (optical alignment) and fragile

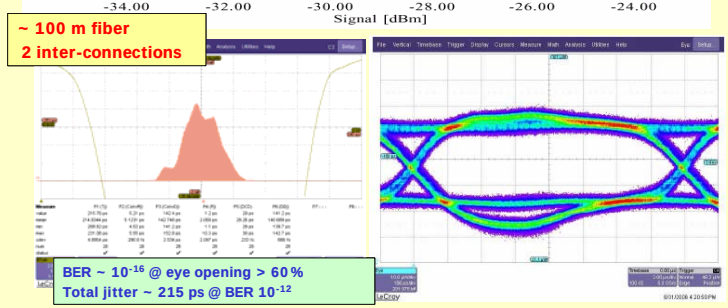


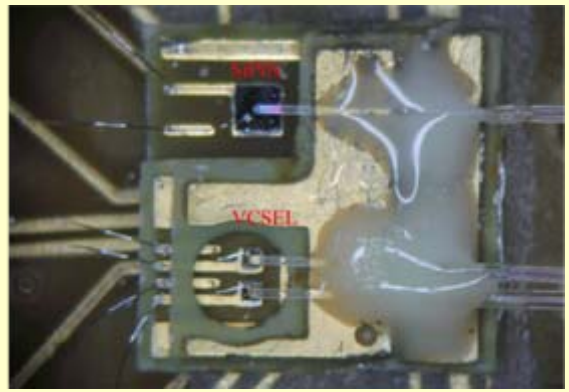


Digital optical links

- High speed: 1Ghz - 10GHz – 40GHz
- Extensively used in telecommunications (expensive) and in computing ("cheap")
- Encoding
  - Inclusion of clock for receiver PLL's
  - DC balanced
  - Special synchronization characters
  - Error detection and or correction
- Reliability and error rates strongly depending on received optical power and timing jitter
- Multiple (16) serializers and deserializers directly available in modern high end FPGA's.

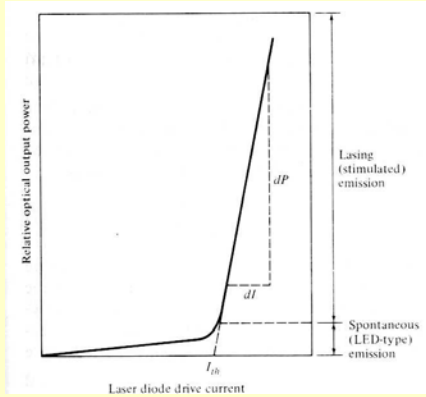


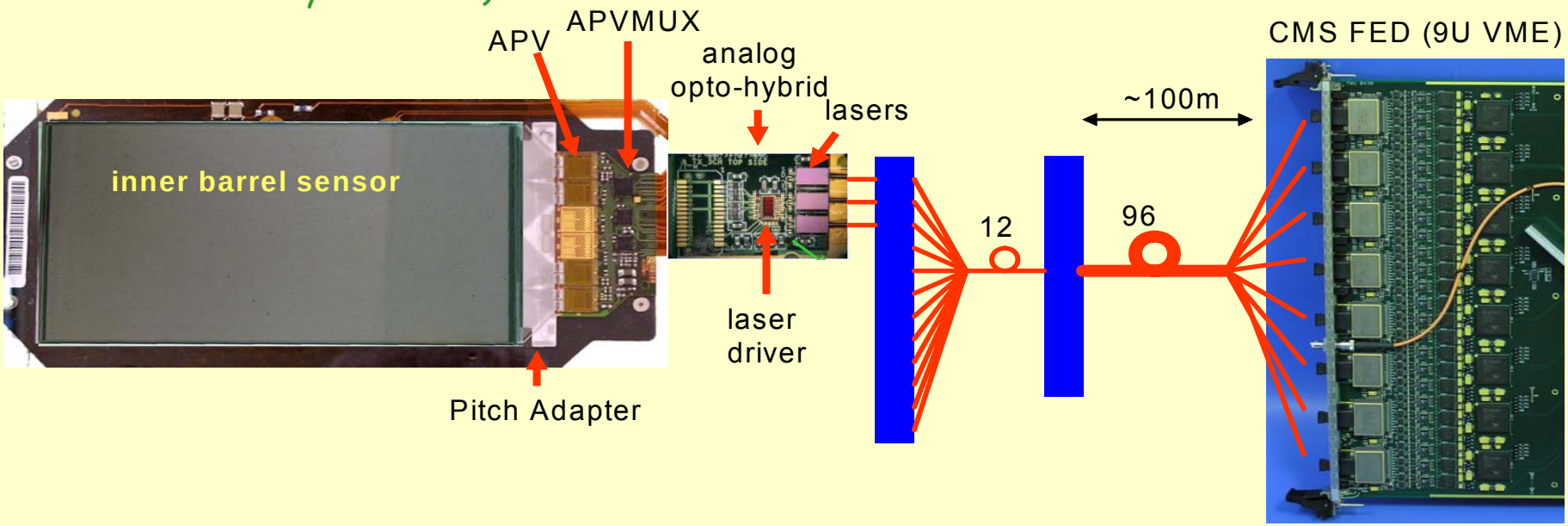




Analog optical links

- Lasers above DC biasing point behaves relatively nice and linear
  - Use for analog link
- Used in large quantity for CMS silicon tracker with analog readout
  - 50 k links
  - ~8 bits dynamic range x 40 Msamples/s = 320 Mbits/s
- Not mainstream technology so the design and use of such a link is non trivial (in house development)
  - Prevents the need for radiation hard ADC's in the front-end electronics (Low power ADC's with small area and low power are today available)





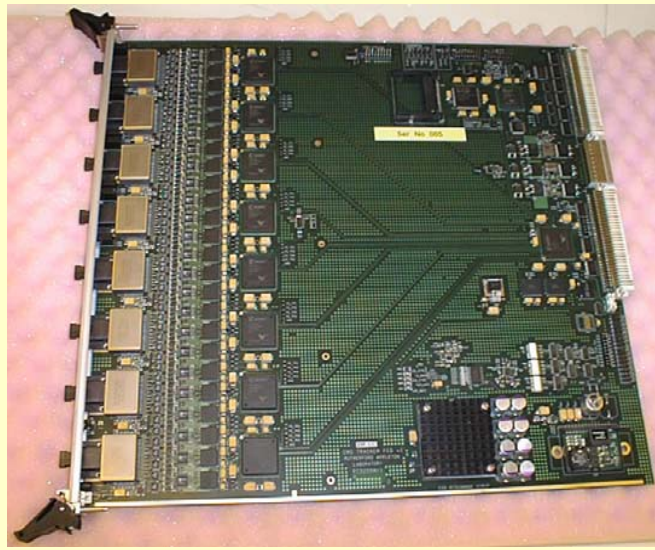
DAQ interfaces

- Front-end data reception
  - Receive optical links from multiple front-ends: 24 - 96
  - Located outside radiation
- Event checking
  - Verify that data received is correct
  - Verify correct synchronization of front-ends
- Extended digital signal processing to extract information of interest and minimize data volume
- Event merging/building
  - Build consistent data structures from the individual data sources so it can be efficiently sent to DAQ CPU farm and processed efficiently without wasting time reformatting data on CPU.
  - Requires significant data buffering
- High level of programmability needed
- Send data to CPU farm at a rate that can be correctly handled by farm
  - 1 Gbits/s Ethernet (next is 10Gbits/s)
  - In house link with PCI interface: S-link

Requires a lot of fast digital processing and data buffering: **FPGA's**, DSP's, embedded CPU

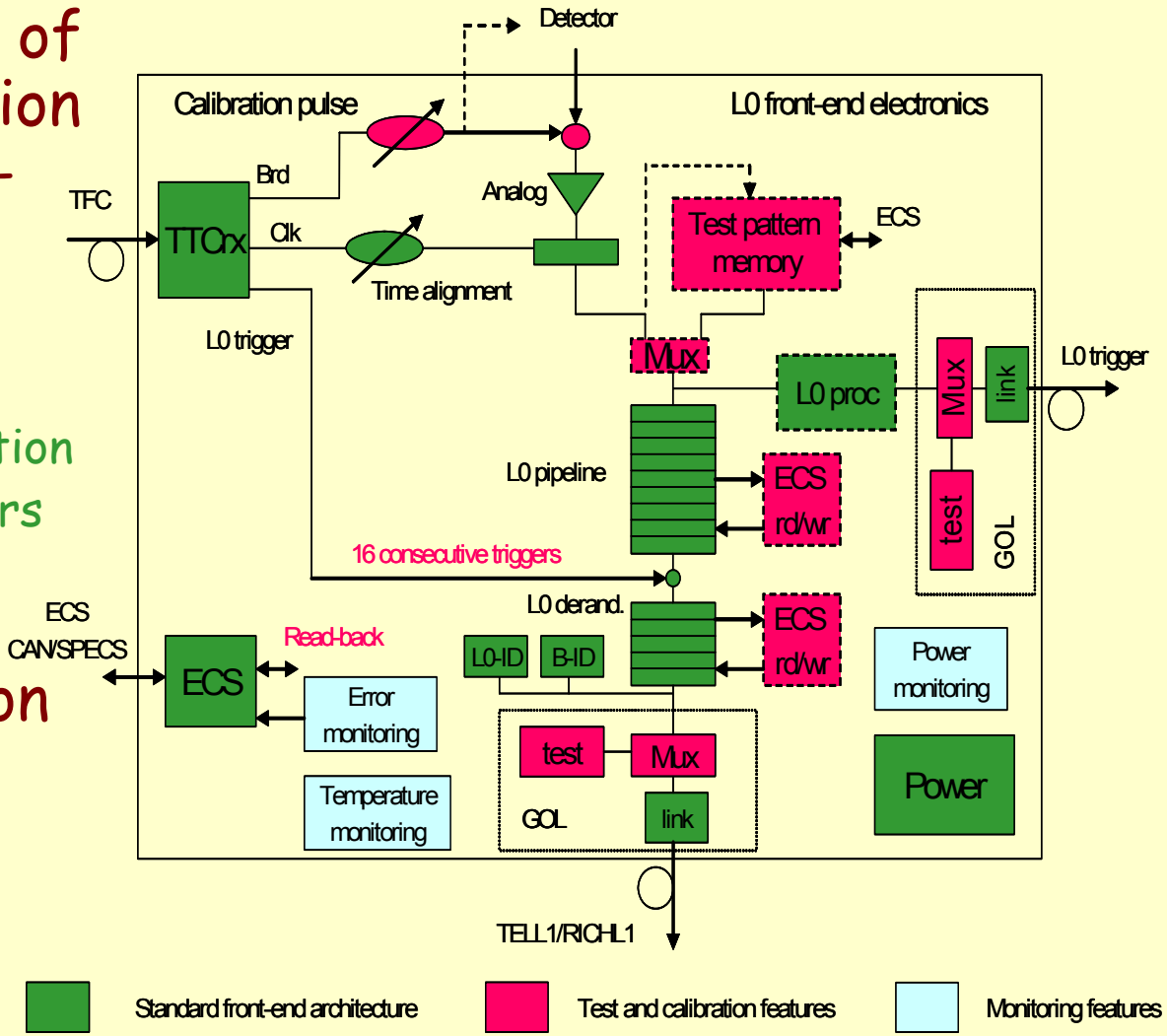
Use of ASIC's not justified

Complicated modules that are only half made when the hardware is there: FPGA firmware (from HDL), DSP code, on-board CPU software, etc.



Calibration and test

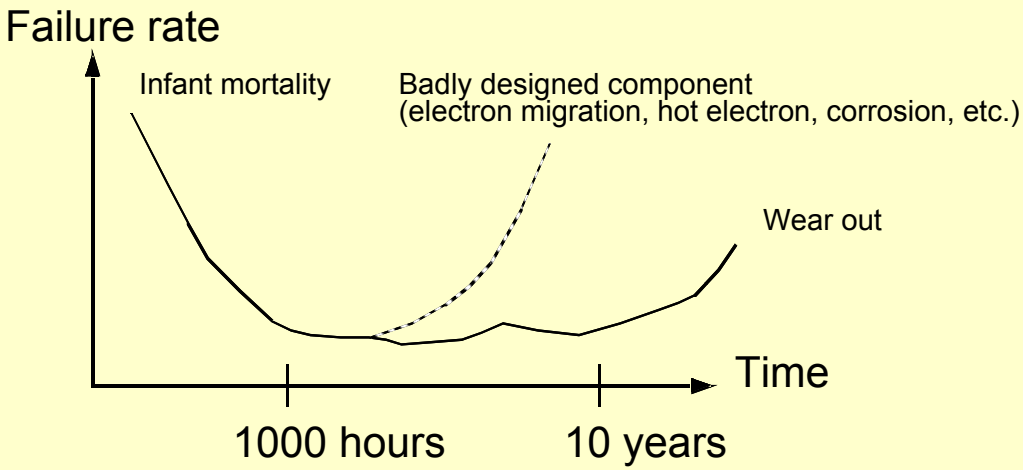
- Front-end systems needs extended set of testing and calibration features to allow in-situ verification of modules and all the interconnections
  - Calibration pulse injection
  - Test pattern generators
  - Read/write access to embedded buffers
- Amplitude calibration
- Time alignment
- Local monitoring
- Etc.



Reliability

- Front-end electronics are in many cases enclosed in locations where it is very difficult to replace or repair it.
- Harsh environment (radiation ,magnetic fields, cooling, etc.)
- Huge systems (so there will always be something not working)
  - Detector layout has in most cases been made such that a failing module in a detection layer does not significantly deteriorate physics performance
  - Calorimeter is only single layer !
- Electronics will not work for ever
- Most failures occur in the beginning of its lifetime (infant mortalities)
- Infant mortalities can be sorted out by burn-in
  - Run electronics at increased temperature (or even better with temperature cycling) for 24hours or more
- All electronics located within detector with difficult access must pass serious reliability qualification.
- In some cases special redundancy must be implemented

Example of BGA failure



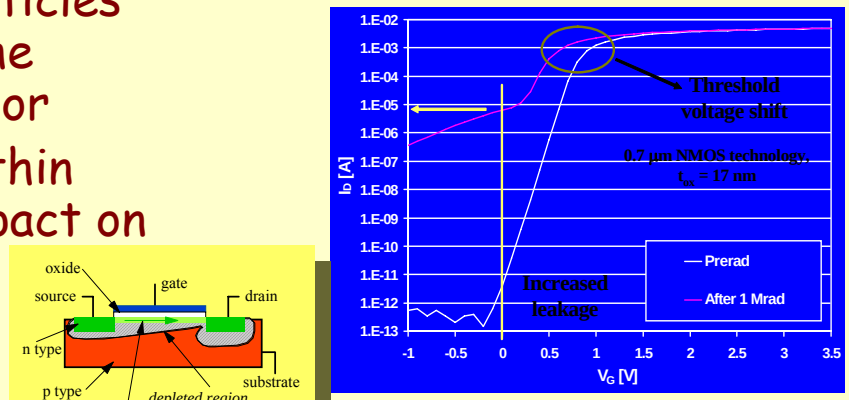
Failing parts within first 1000 hours: ~0.1%

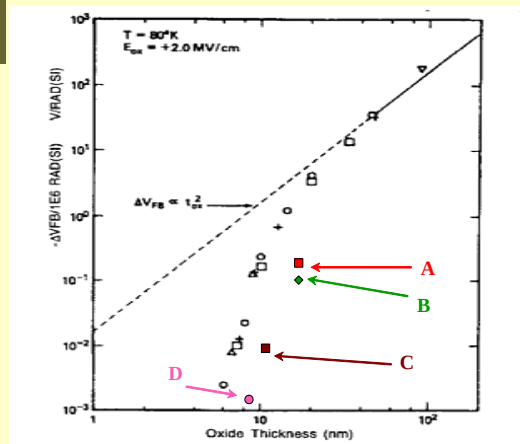
Radiation effects

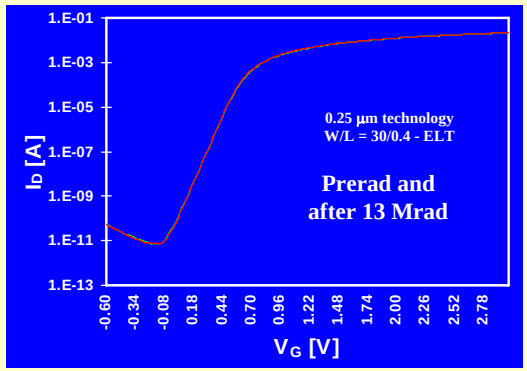
- In modern experiments large amounts of electronics are located inside the detector where there may be a high level of radiation
  - This is the case for 3 of the 4 LHC experiments (10 years running)
    - Pixel detectors: 10 -100 Mrad
    - Trackers: ~10Mrad
    - Calorimeters: 0.1 – 1Mrad
    - Muon detectors: ~10krad
    - Cavern: 1 – 10krad
- Normal commercial electronics will not survive within this environment
  - One of the reasons why all the on-detector electronics in the LHC experiment are custom made
- Special technologies and dedicated design approaches are needed to make electronics last in this unfriendly environment
- Radiation effects on electronics can be divided into three major effects
  - Total dose
  - Displacement damage
  - Single event upsets

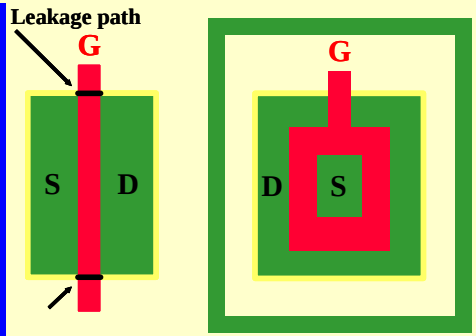
Total dose

- Generated charges from traversing particles gets trapped within the insulators of the active devices and changes their behavior
- For CMOS devices this happens in the thin gate oxide layer which have a major impact on the function of the MOS transistor
  - Threshold shifts
  - Leakage current
- In deep submicron technologies (<0.25um) the trapped charges are removed by tunneling currents through the very thin gate oxide
  - Only limited threshold shifts
- The leakage currents caused by end effects of the linear transistor (NMOS) can be cured by using enclosed transistors
  - For CMOS technologies below the 130nm generation the use of enclosed NMOS devices does not seem necessary. But other effects may show up
- No major effect on high speed bipolar technologies



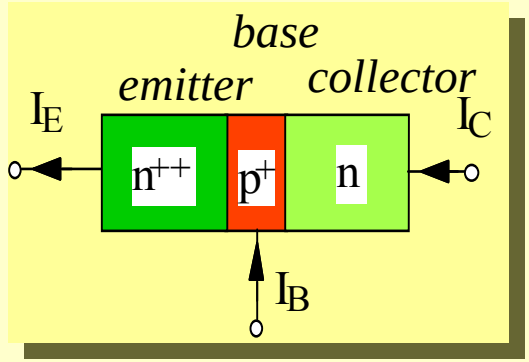


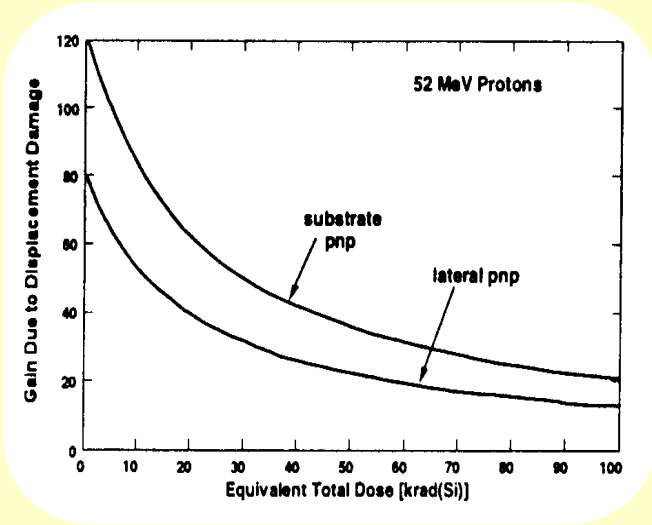




Displacement damage

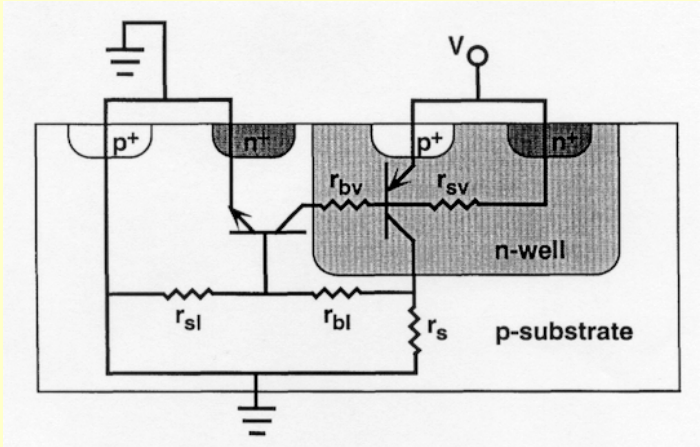
- Traversing hadrons provokes displacements of atoms in the silicon lattice.
- Bipolar devices relies extensively on effects in the silicon lattice.
  - Traps (band gap energy levels)
  - Increased carrier recombination in base
- Results in decreased gain of bipolar devices with a dependency on the dose rate.
- No significant effect on MOS devices
- Also seriously affects Lasers and PIN diodes used for optical links.





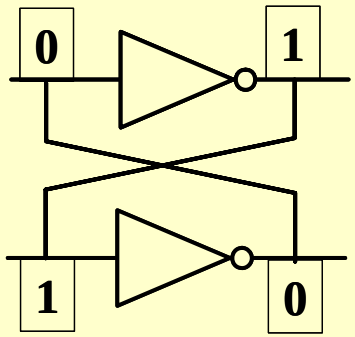
Single event latch-up

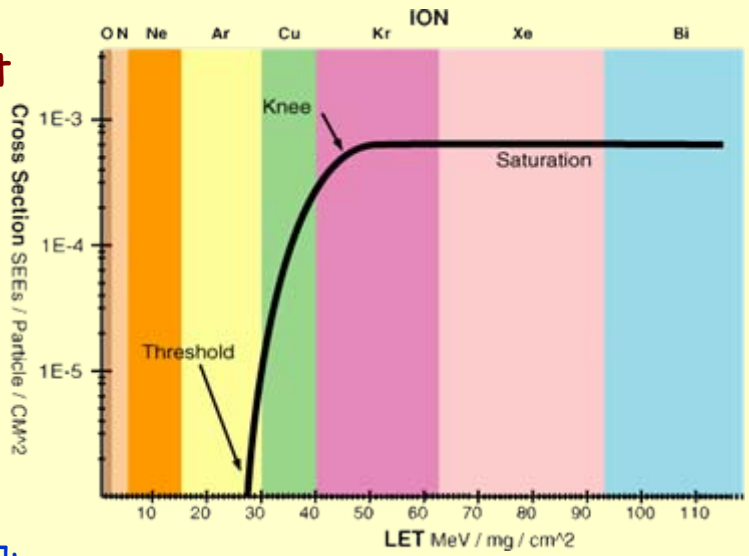
- Deposited charge from traversing particles provokes a power supply short circuit via an intrinsic parasitic device in CMOS technologies
  - Equal to SMOKE
- Traversing hadrons can only deposit sufficient charge if they make nuclear interaction with silicon
  - Heavily ionizing particles can generate the SEL directly (ions from an accelerator)
- The latchup circuit can by the IC technology be made such that it does not trigger (epi).
- For modern technologies, with low power supply voltage, the latch-up can in general not be generated



Single event upsets

- Deposition of sufficient charge can make a memory cell or a flip-flop change value
- As for SEL, sufficient charge can only be deposited via a nuclear interaction for traversing hadrons
- The sensitivity to this is expressed as an efficient cross section for this to occur
- This problem can be resolved at the circuit level or at the logic level
- Make memory element so large and slow that deposited charge not enough to flip bit
- Triple redundant (for registers)
- Hamming coding (for memories)
  - Single error correction, Double error detection
  - Example Hamming codes: 5 bit additional for 8 bit data
    - ham[0] = d[1] $ d[2] $ d[3] $ d[4];
      ham[1] = d[1] $ d[5] $ d[6] $ d[7];
      ham[2] = d[2] $ d[3] $ d[5] $ d[6] $ d[8];
      ham[3] = d[2] $ d[4] $ d[5] $ d[7] $ d[8] ;
      ham[4] = d[1] $ d[3] $ d[4] $ d[6] $ d[7] $ d[8];
      $ = XOR
  - Overhead decreasing for larger words
    32bits only needs 7hamming bits





Use of COTS in radiation

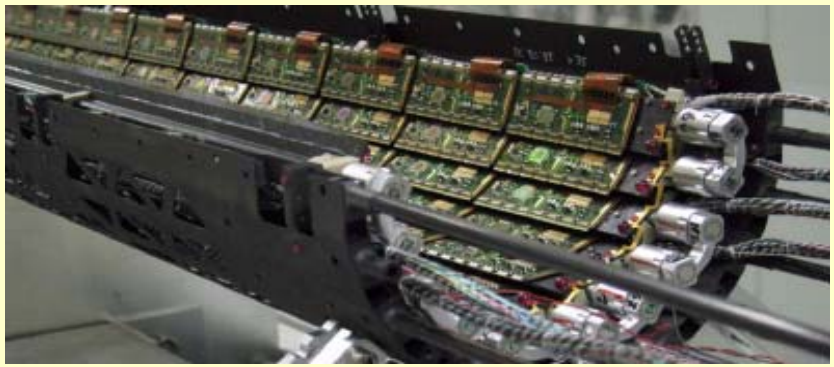
- The use of Commercial Of The Shelf (COTS) components in a radiation environment is a particular tricky point
- Extensive radiation tests required to characterize sensitivity to total dose, displacement damage, SEL, SEU
  - This is a significant amount of work
- It is difficult to get a guarantee that purchased components come from the same fab. with exactly the same technology as those circuits that have been radiation tested
  - Multiple fabs with slightly different details
  - Continuous fab and technology improvements
  - External 2nd. sourcing
- The fact that one chip from a family of chips have had no radiation problems is no guaranteed that the others will not
- Special radiation (space, military) qualified components are very expensive.

Use of FPGA's in radiation

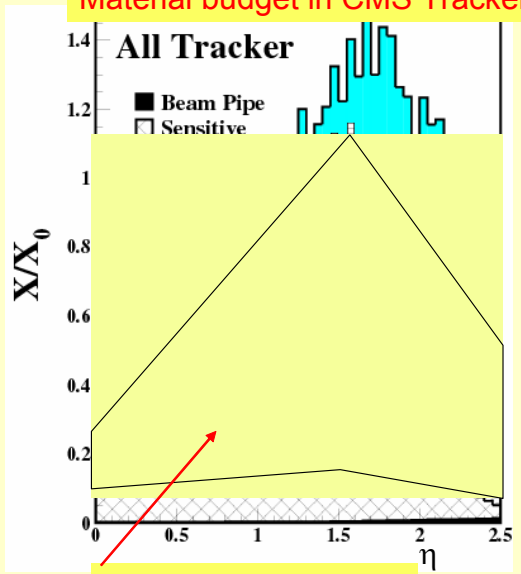
- For digital functions we would often like to use FPGA's in radiation environments.
  - Impressive performance that continuously improve
  - Reprogram functions as needed
- Modern FPGA's (in 130nm and below) can stand significant total dose and normally does not have SEL problems
- Main problem is SEU
  - Ahhhh but I have now just learned to solve this with triple redundancy (TR). Yes but this does unfortunately not work for the most common FPGA's based on SRAM configuration.
    - SEU in my registers can be resolved with TR
    - A SEU in the configuration SRAMS may change my logic or even make short circuits. I as a FPGA user can NOT change this
    - Can be used in non "mission" critical parts where it can be accepted to reprogram FPGA's when they have been seen to malfunction (if not too often)
  - Antifuse FPGA's can effectively use TR (but my FPGA can not be reprogrammed)
  - FLASH memories have been seen to be quite resistant to radiation effects so FLASH based FPGA's are also an alternative

Powering

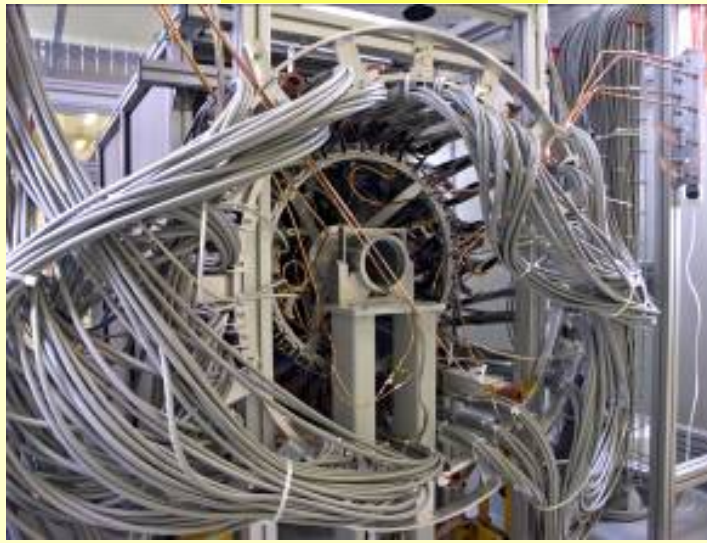
- Delivering power to the front-end electronics highly embedded in the detectors has been seen to be a major challenge (underestimated).
- The related cooling and power cabling infrastructure is a serious problem of the inner trackers as any additional material seriously degrades the physics performance of the whole experiment.
- A large majority of the material in these detectors in LHC relates to the electronics, cooling and power and not to the silicon detector them selves (which was the initial belief)
- How to improve
  1. Lower power consumption
  2. Improve power distribution



Material budget in CMS Tracker

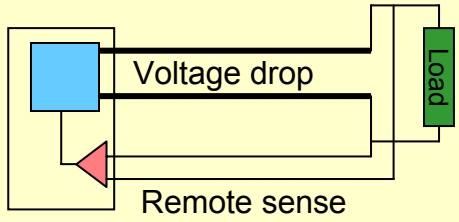


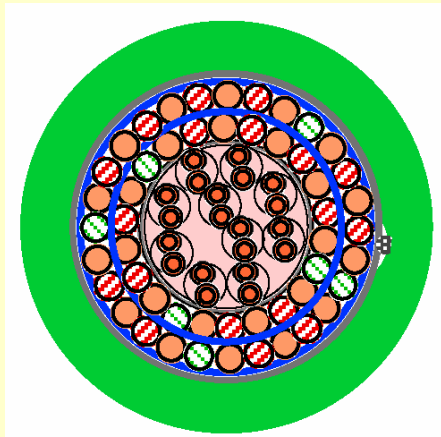
All electronics related

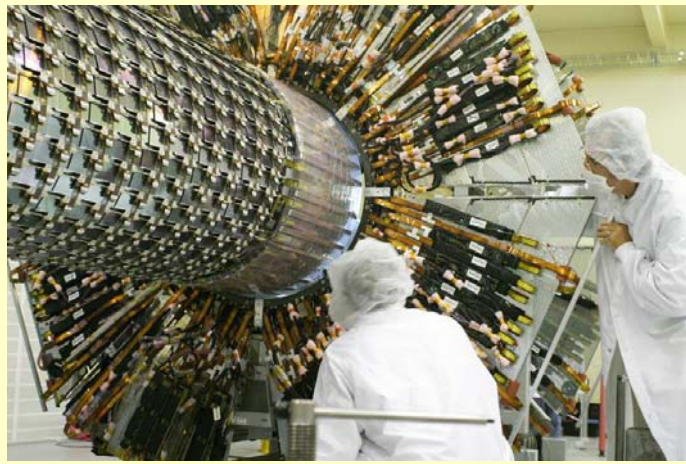


The problem as is

- Total power: ~500kw (to be supplied and cooled)
  - Trackers: ~ 60 kW
  - Calorimeters: ~ 300 kW
  - Muon: ~ 200 kW
  - Must for large scale detectors be delivered over 50m – 100m distance
- Direct supply of LV power from ~50m away
  - Big fat copper cables needed
    - Use aluminum cables for last 5-10m to reduce material budget
  - Power supply quality at end will not be good with varying power consumption (just simple resistive losses)
    - If power consumption constant then this could be OK
  - Use remote sense to compensate
    - This will have limited reaction speed
    - May even become unstable for certain load configurations
  - Power loss in cables will be significant for the voltages (2.5v) and currents needed: ~50% loss in cables (that needs to be cooled)
- Use of local linear regulators
  - Improves power quality at end load.
  - Adds additional power loss: 1 – 2 v head room needed for regulator
  - Increases power losses and total efficiency now only: ~25% (more cooling needed)







Use of DC-DC converters

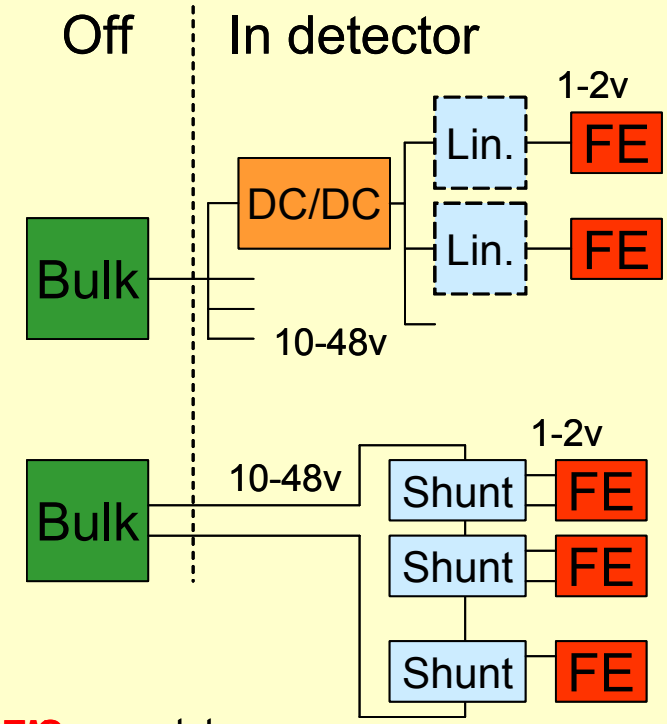
- For high power consumers (e.g. calorimeter) the use of local DC-DC converters are inevitable.
- These must work in radiation and high magnetic fields
  - This is not exactly what switched mode DC-DC converters like
  - Magnetic coils and transformers saturated
  - Power devices do not at all like radiation: SEU - > single event burnout -> smoke -> disaster
- DC-DC converters for moderate radiation and moderate magnetic fields have been developed and used
  - Some worries about the actual reliability of these for long term

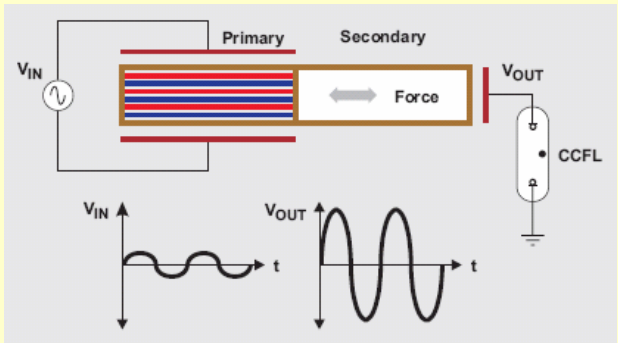
Future power problems

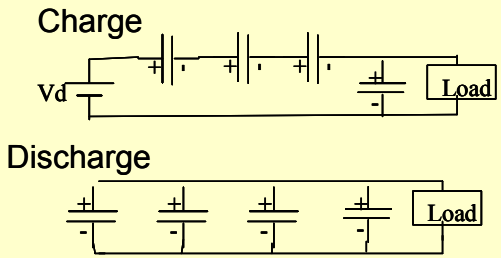
- For future front-end electronics based on new deep sub-micro technologies the power per function is clearly decreasing
  - Not always the case for the analog part
  - We will put in more channels and more functions
  - Uses lower power supply voltage (e.g. 1.2 v instead of 2.5v)
- If we in the end need the same power the required current will become ~2 times larger which implies that our cable losses will get ~2 times worse.
- So thicker cables and more cooling needed: DOES NOT LOOK LIKE A GOOD IDEA

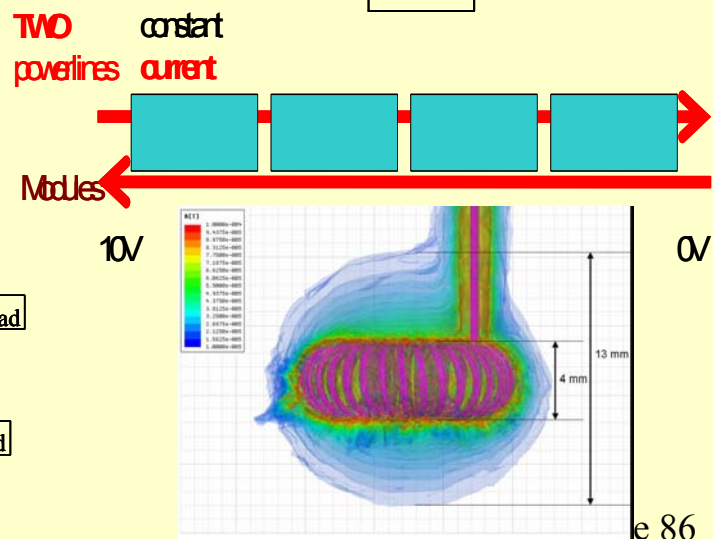
What is the solution ?

- Consume less power (but not so easy)
- Use of local DC-DC converters at the loads
  - Radiation, magnetic fields
  - Switched capacitor converters
    - Unconventional, limited voltage ratio
  - Use of air core inductor converter
    - Efficiency ?, EMC noise ?
  - Use of ceramic transformers ?
    - Not a well known and mature technology
- Serial powering
  - Grounding, failure modes ?, noise coupling ?







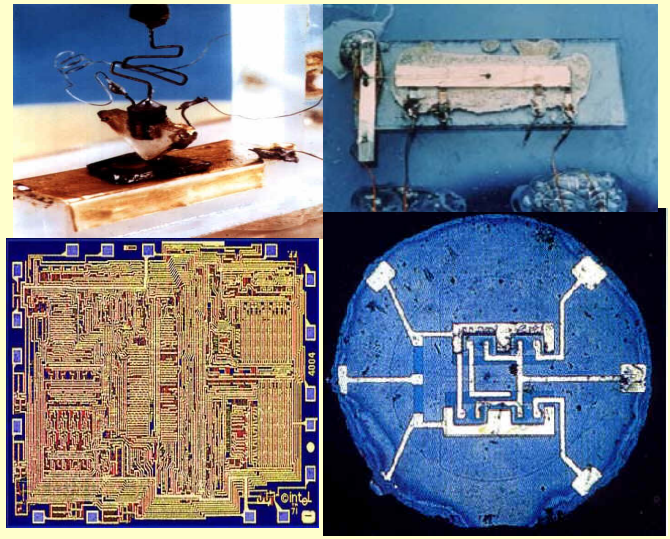


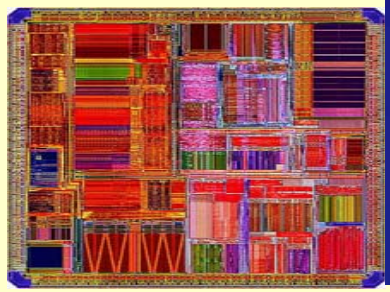
Low power

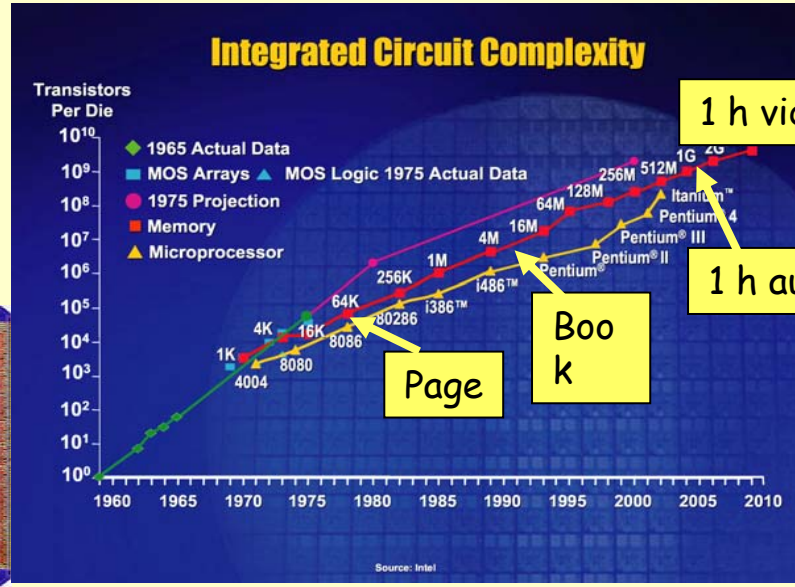
- Very low power designs are key for future tracker detectors
  - Willing to sacrifice other performance figures: resolution, etc.
- The largest part of the power is normally burned in the pre-amplifier where large transistors with a significant biasing current is used to get the lowest noise.
- What gives the least material tracker: ?
  - Thin silicon where the pre-amplifiers must be very low noise and therefore consumes quite some power
  - Thick silicon with lower power pre-amplifier
- Use of SiGe bipolar technology (very fast but expensive)
- Use of pulsed power in experiments with a spill structure (not LHC but ILC and CLIC)
  - All the analog biasing circuits must then be quick to stabilize
  - Large current variations in cables, connectors and bond wires that will then tend to move/oscillate when in a strong magnetic field and may then break (this problem has been seen in the past)
  - Thermal effects as not running with constant power.

IC technologies

- The fast development of IC technologies is what has enabled current detectors with their electronics to be built
- It has been our luck that the 0.25um CMOS technology can be used in very high radiation environments (with appropriate special design techniques).
  - The following 0.18um and 0.13um is even better
  - Next generation technologies could be different as they use other gate and wire insulators.
- Next generation technologies are much more complicated and very expensive (~1M$ for masks) so we may have to rethink how our community makes chips for HEP.
- The close integration of integrated circuits and detectors are critical: Combined electronics and detectors and 3D packaging will pose new challenges.



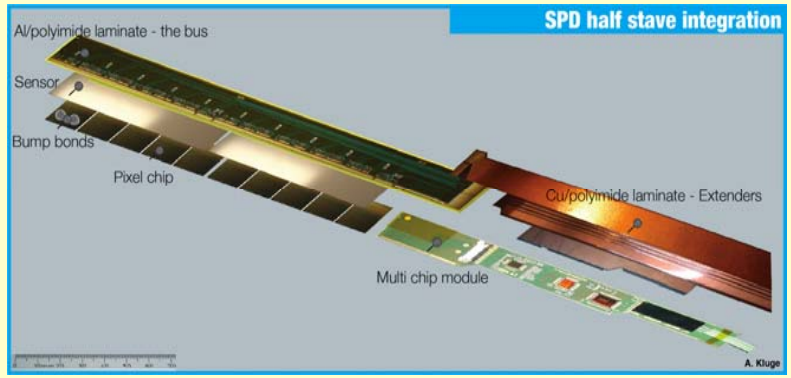


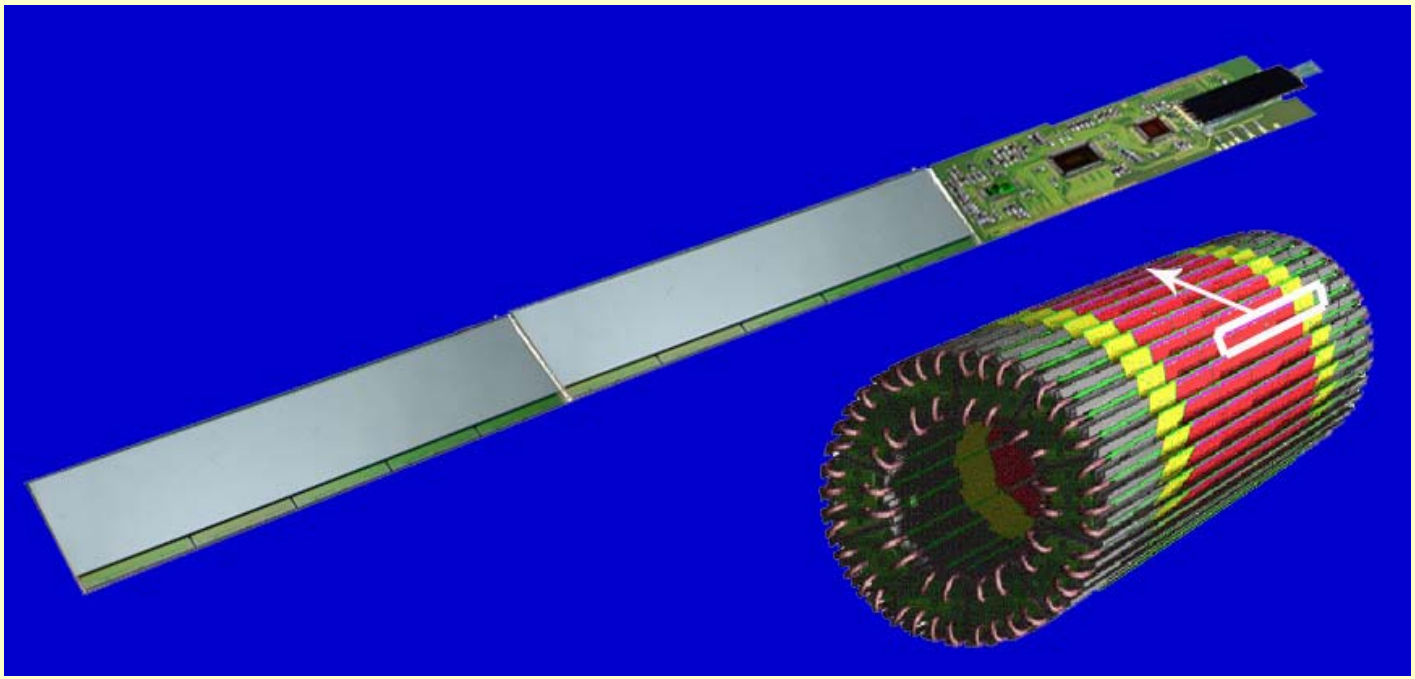


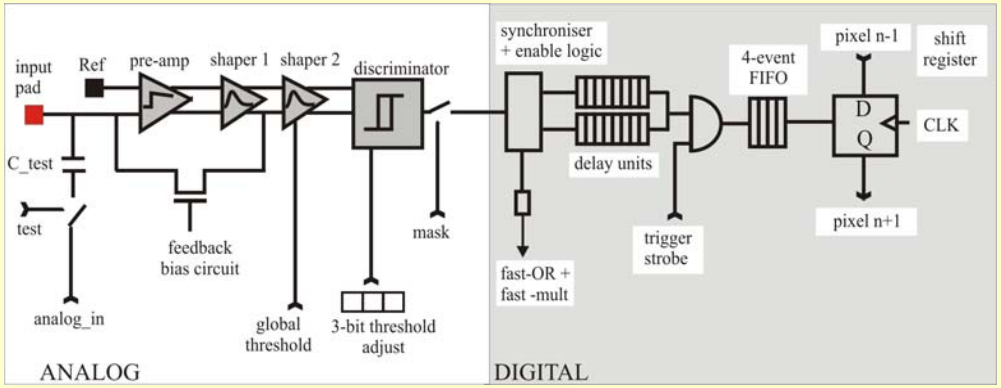
Specific examples

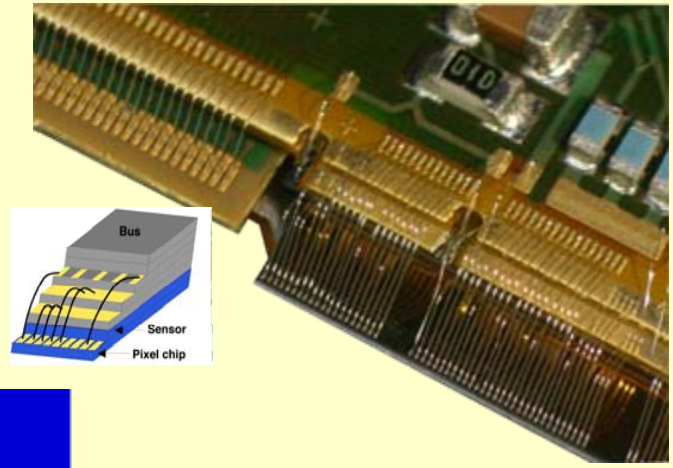
ALICE pixel

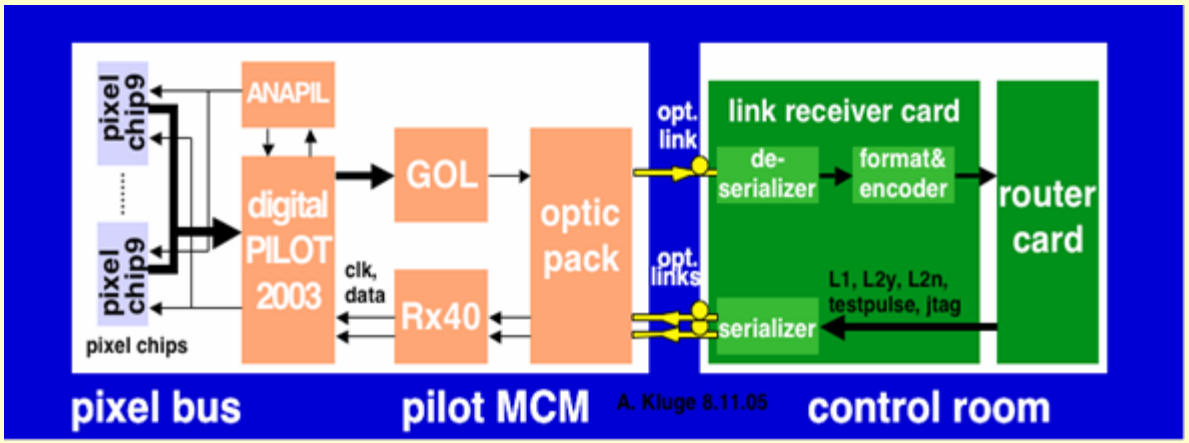
- 10M channels, 1200 pixel chips
- 120 detector modules
- Readout time: 256 μs
- Radiation: 250 krad
- Material: 1% X_0 per layer
- Power: 1kW

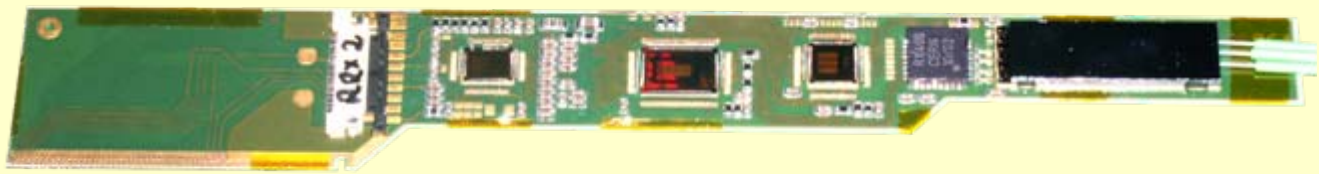





input pad
Ref
pre-amp
shaper 1
shaper 2
discriminator
C_test
test
feedback bias circuit
analog_in
global threshold
3-bit threshold adjust
mask
ANALOG
synchroniser + enable logic
delay units
4-event FIFO
pixel n-1
shift register
D
Q
CLK
pixel n+1
trigger strobe
fast-OR + fast -mult
DIGITAL

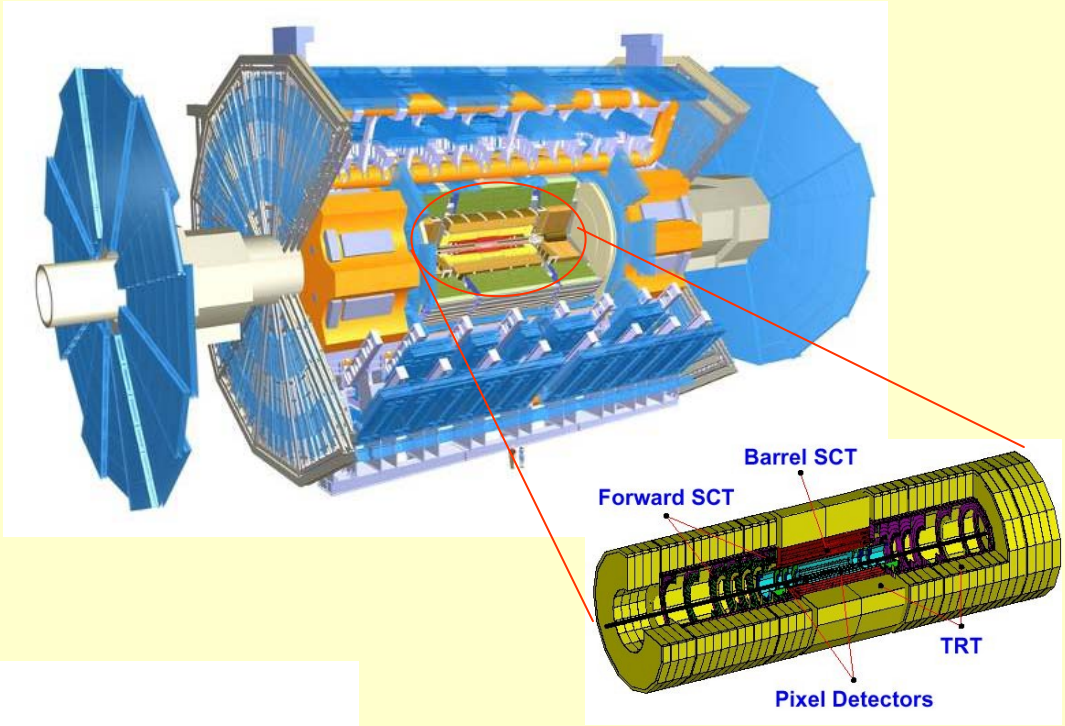

Bus
Sensor
Pixel chip

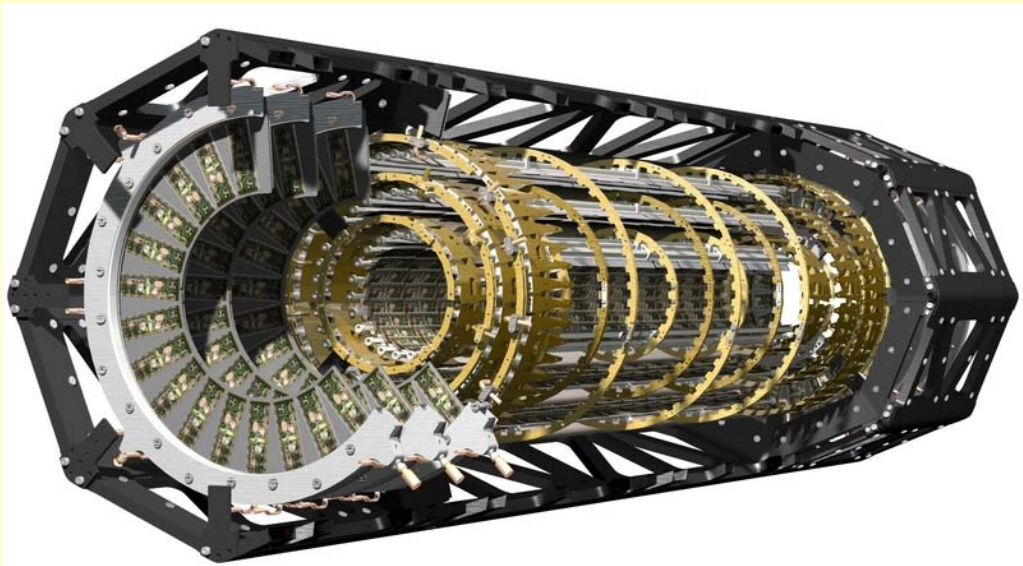

pixel chip9
pixel chip9
pixel chips
ANAPIL
digital PILOT 2003
GOL
Rx40
clk, data
optic pack
opt. link
opt. links
link receiver card
de-serializer
format& encoder
router card
L1, L2y, L2n, testpulse, jtag
serializer
pixel bus
pilot MCM
A. Kluge 8.11.05
control room

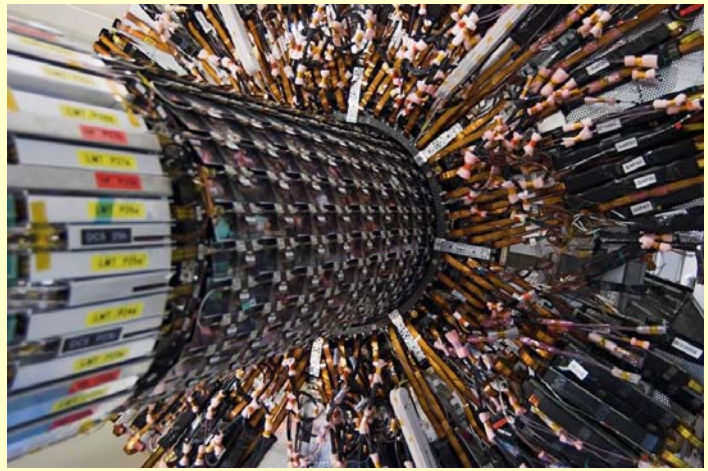


ATLAS tracker

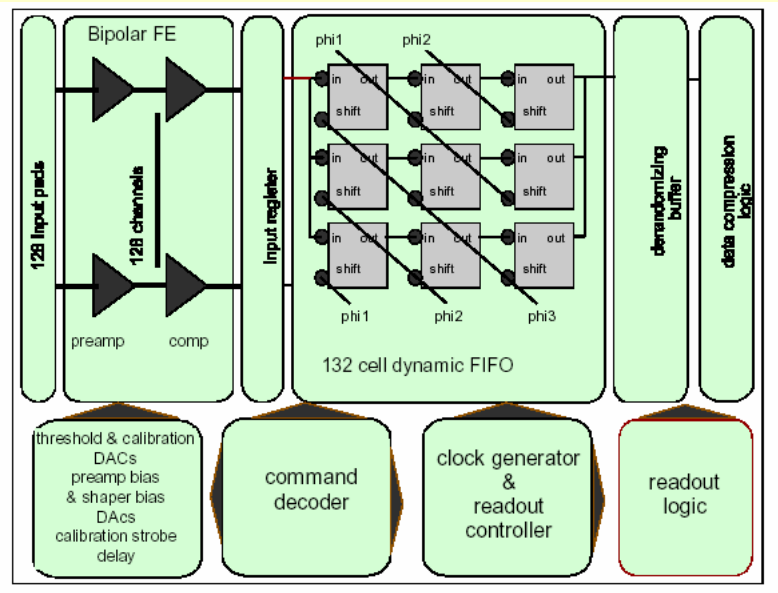
- Strips: 6M
  - Binary system
  - 128 channels per chip
  - pipeline
  - Threshold adjust per channels
- Pixels:80M
  - Storage of time stamps
  - TOT amplitude measurement

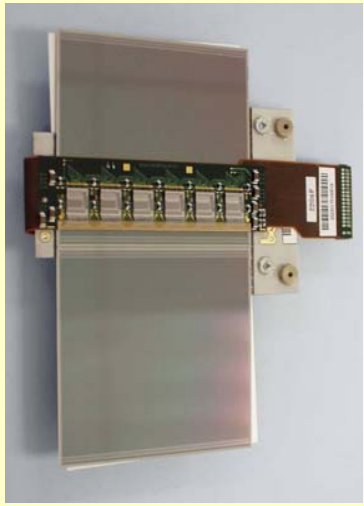


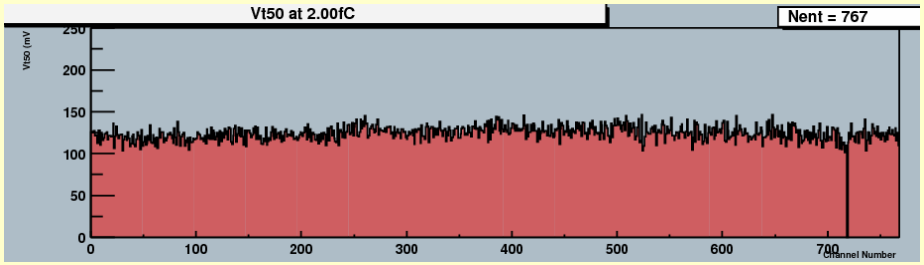




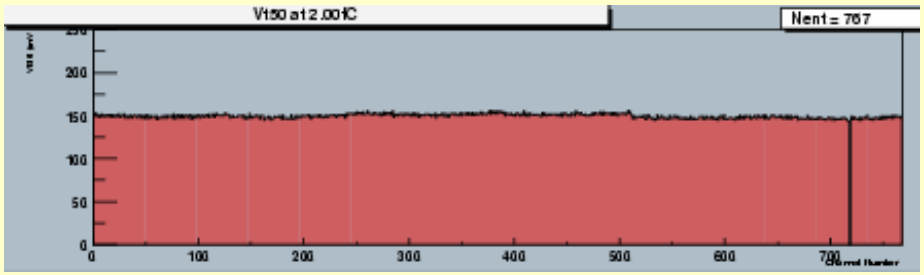
ATLAS silicon strip





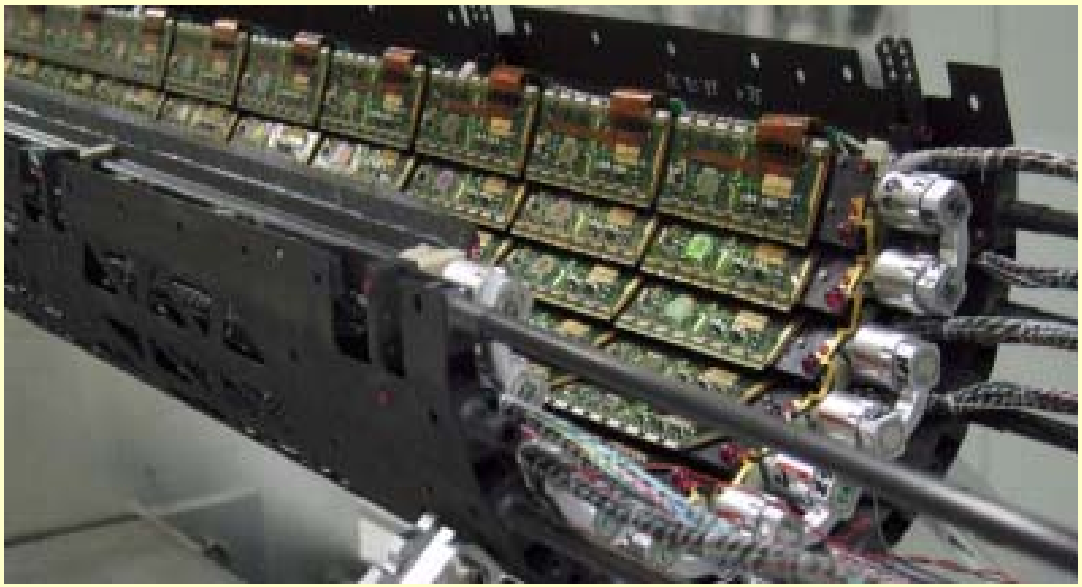


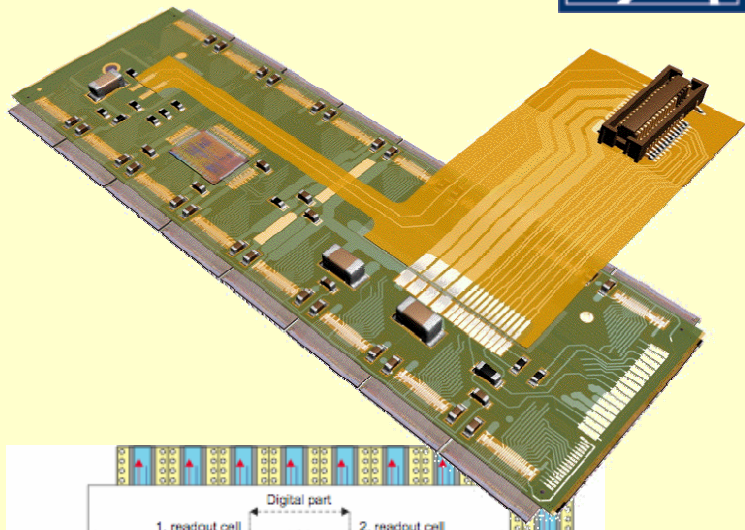
Before individual threshold adjust

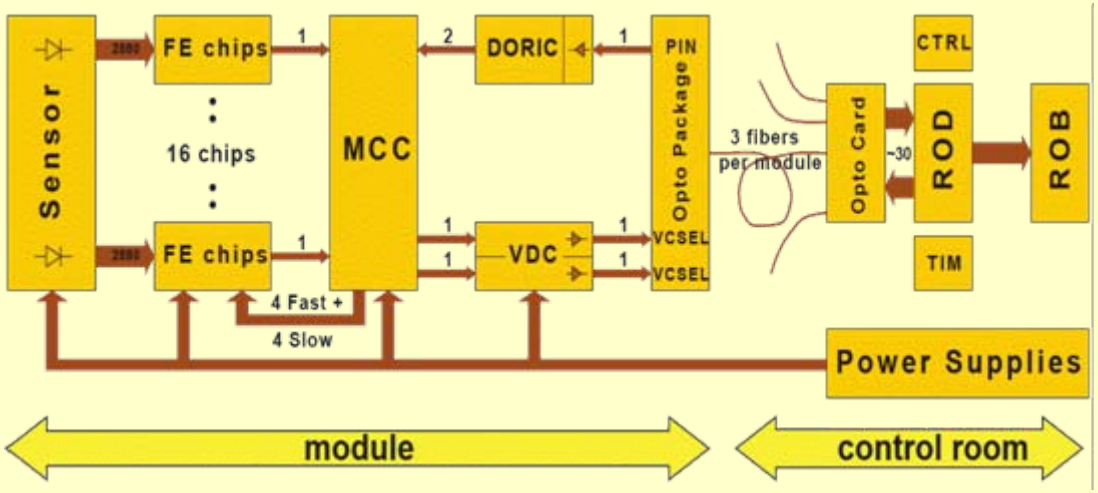


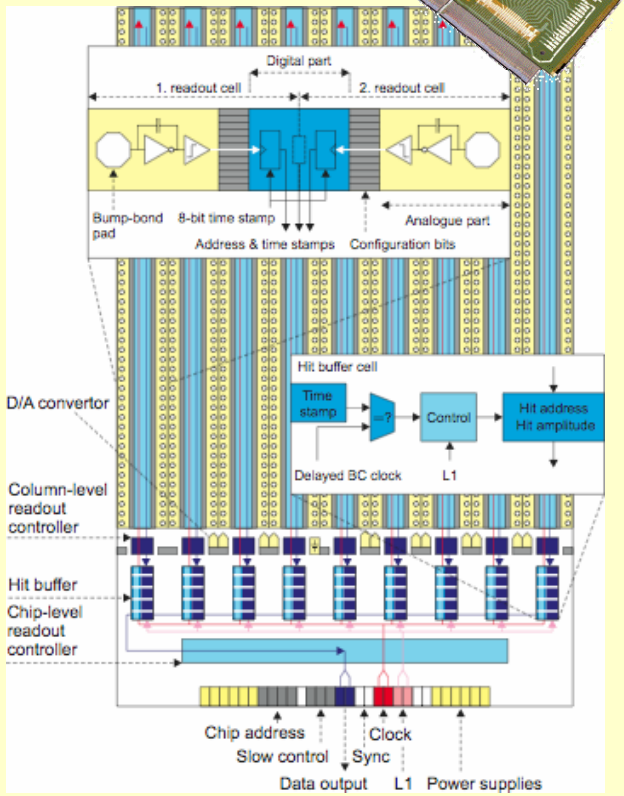
individual adjusted

ATLAS pixel



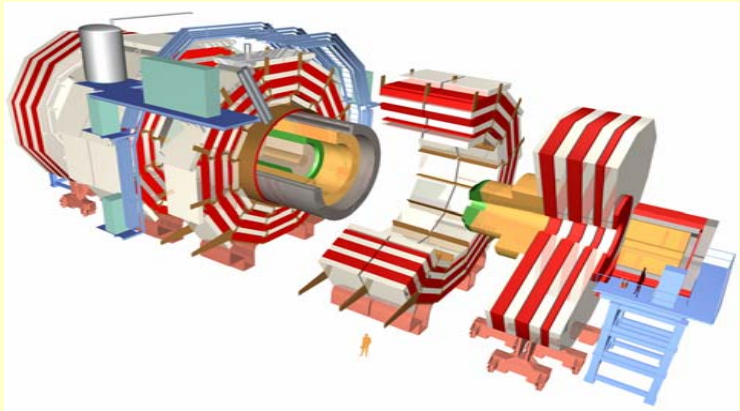


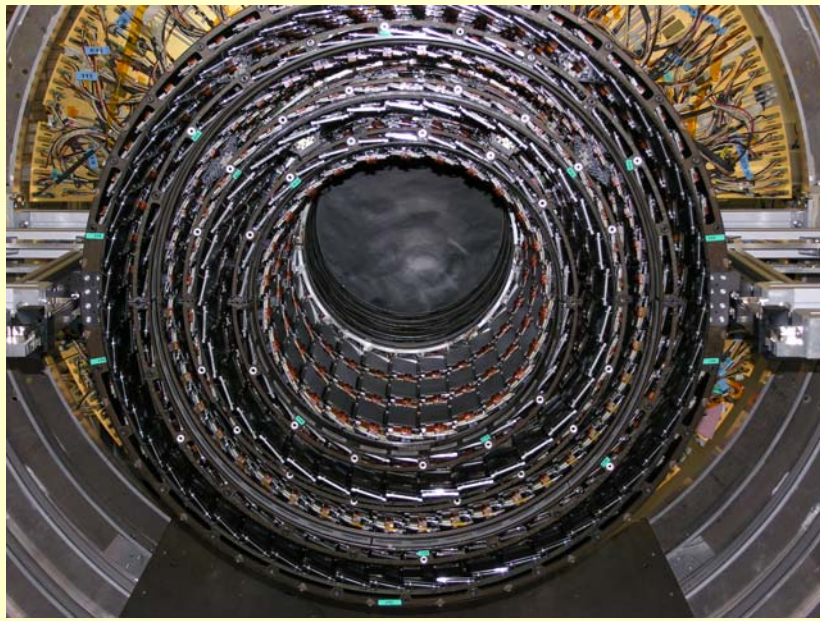

Sensor
FE chips
16 chips
FE chips
MCC
DORIC
PIN
Opto Package
3 fibers per module
Opto Card
CTRL
ROD
TIM
ROB
VDC
VCSEL
VCSEL
4 Fast +
4 Slow
Power Supplies
module
control room

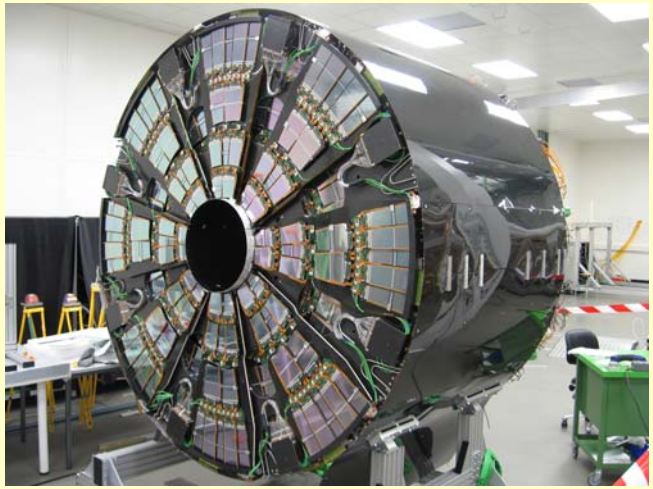

Digital part
1. readout cell
2. readout cell
Bump-bond pad
8-bit time stamp
Address & time stamps
Analogue part
Configuration bits
Hit buffer cell
Time stamp
Control
Hit address
Hit amplitude
Delayed BC clock
L1
D/A convertor
Column-level readout controller
Hit buffer
Chip-level readout controller
Chip address
Slow control
Clock
Sync
Data output
L1
Power supplies

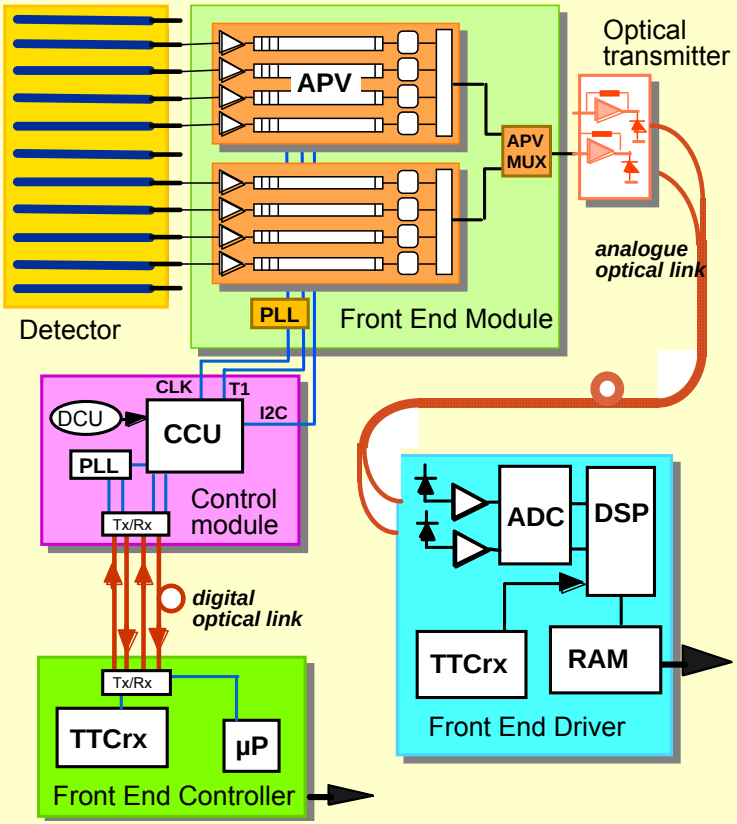
CMS tracker

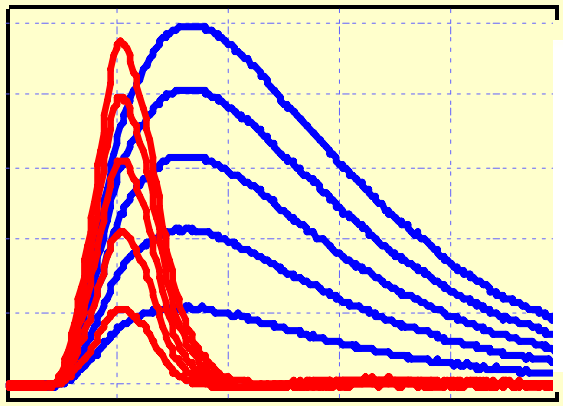
- 10M channels
- Relatively slow analog shaping: 50ns
- Analog pipeline
- Switched capacitor deconvolution after trigger acceptance
- Analog optical links
- Digitization at link receiver

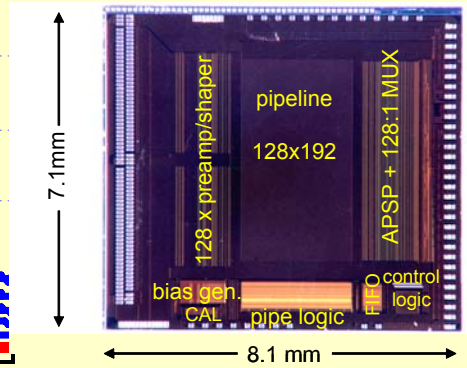


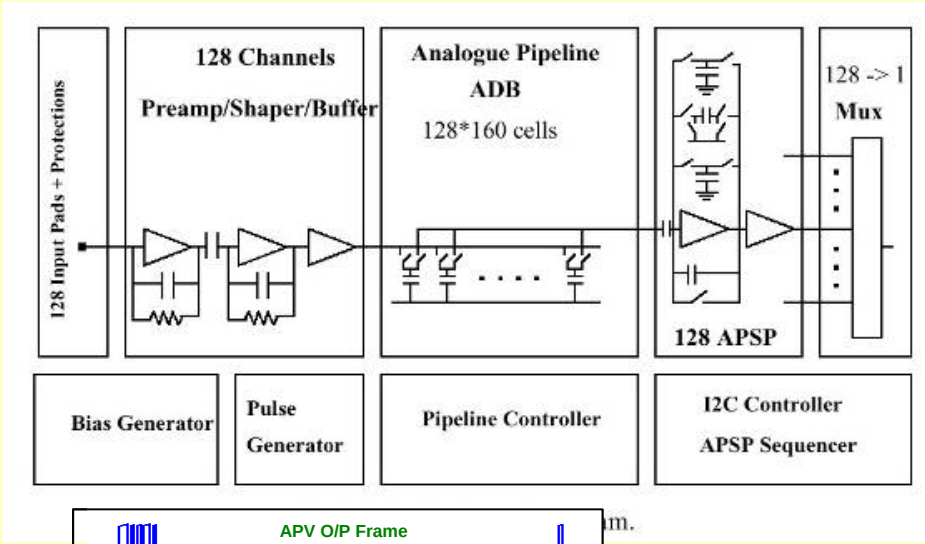


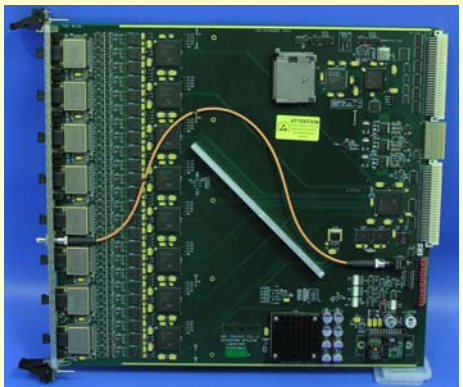


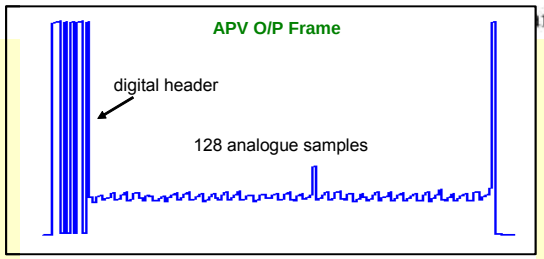

Optical transmitter
APV
APV MUX
analogue optical link
Detector
PLL
Front End Module
CLK
T1
I2C
DCU
CCU
PLL
Control module
Tx/Rx
digital optical link
ADC
DSP
TTCrx
RAM
Front End Driver
Tx/Rx
TTCrx
µP
Front End Controller



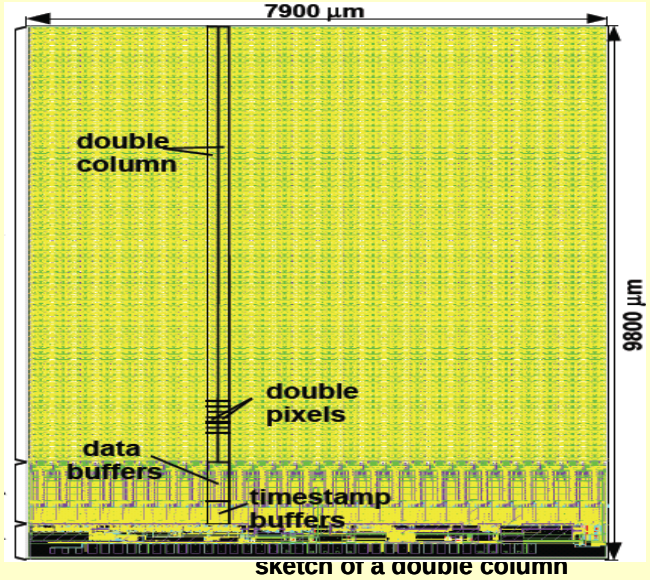

7.1mm
pipeline
128x192
128 x preamp/shaper
APSP + 128:1 MUX
bias gen.
CAL
pipe logic
FIFO
control logic
8.1 mm


128 Input Pads + Protections
128 Channels
Preamp/Shaper/Buffer
Analogue Pipeline
ADB
128*160 cells
128 APSP
128 -> 1
Mux
Bias Generator
Pulse Generator
Pipeline Controller
I2C Controller
APSP Sequencer

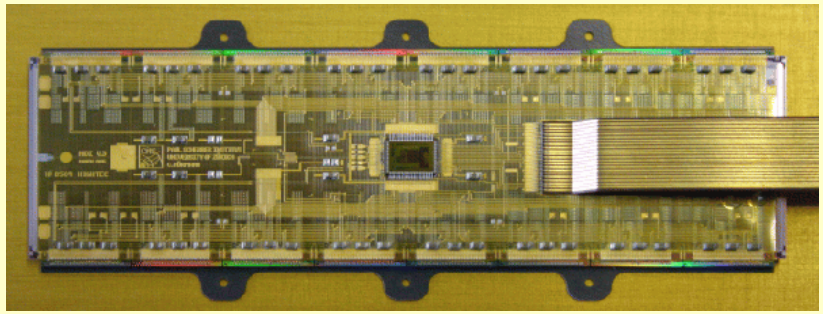


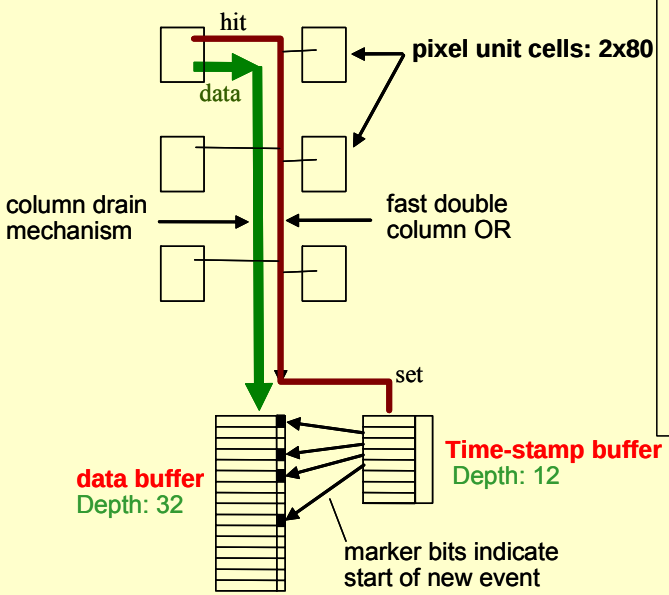

APV O/P Frame
digital header
128 analogue samples

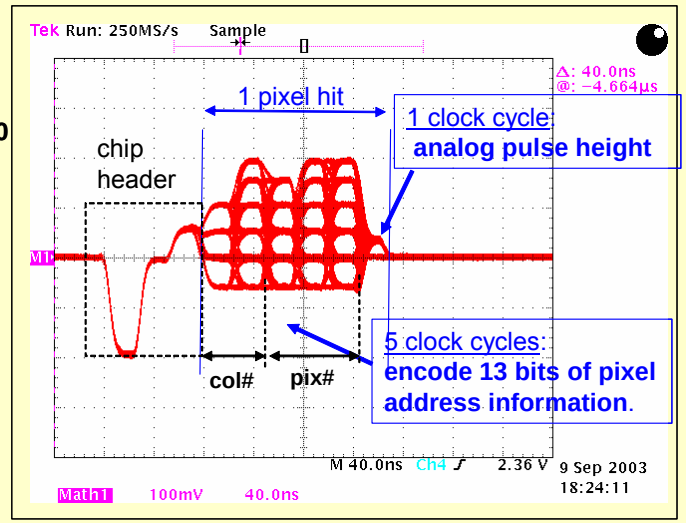
CMS pixel



sketch of a double column

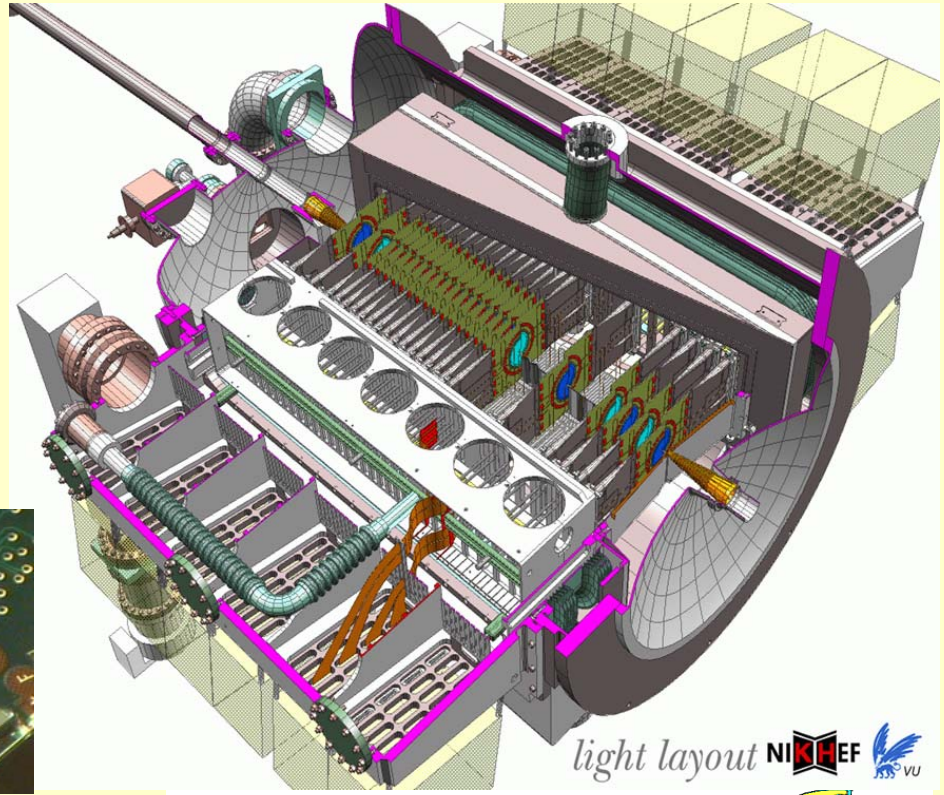


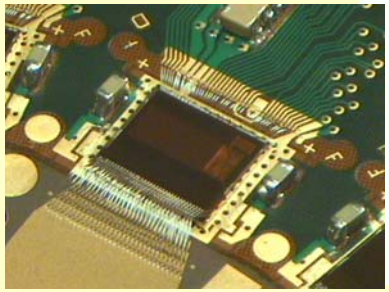


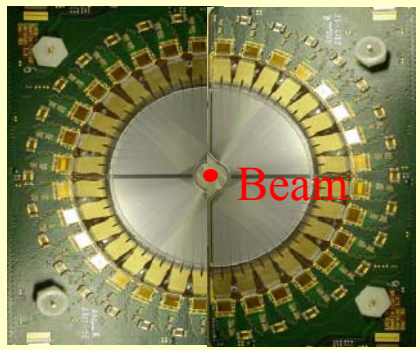


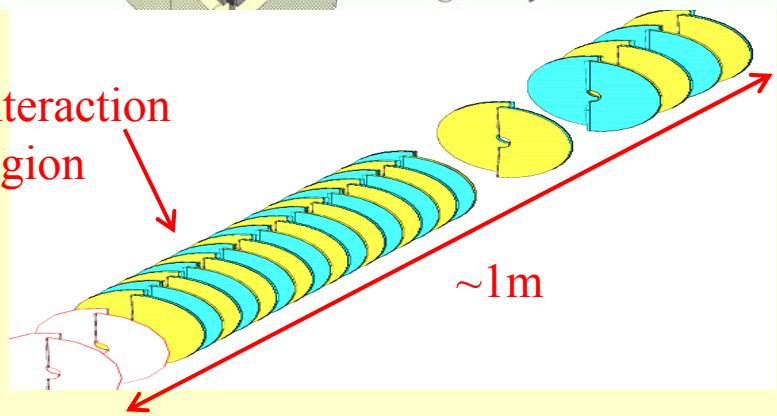
LHCb vertex

- 172k Channels
- Strips in R and φ projection (~10um vertex resolution)
- Located 1cm from beam
- Analog readout (via twisted pair cables over 60m)



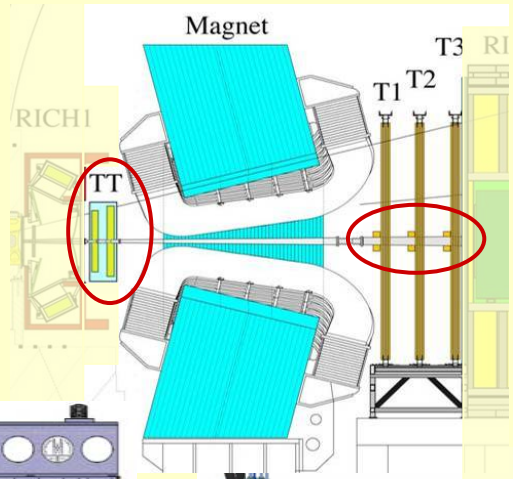


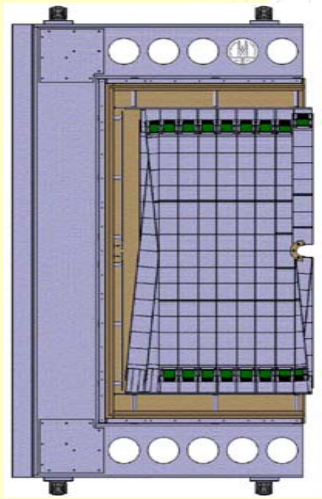


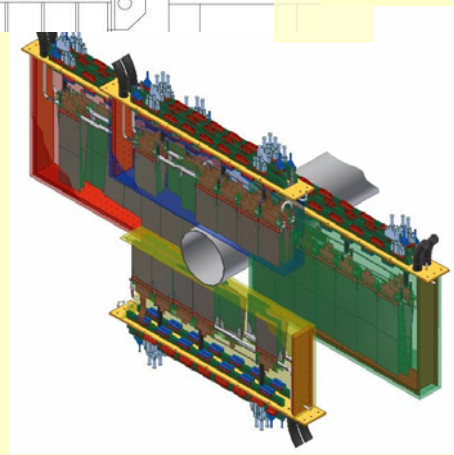


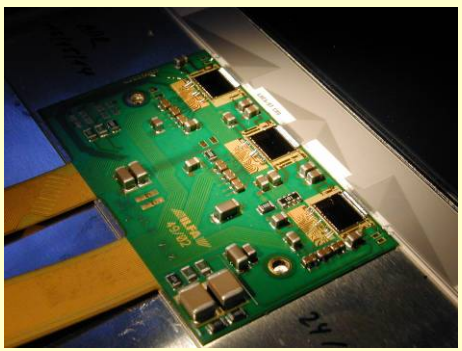
LHCb Silicon tracker

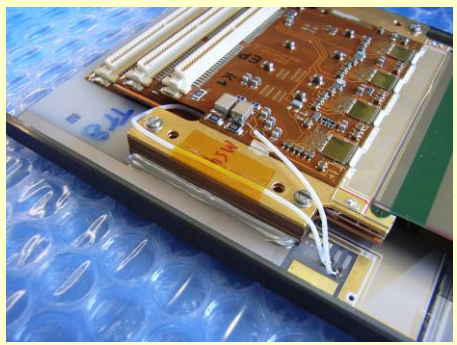
- 300k channels
- Silicon ladders of 2 – 4 silicon detectors chained to one electronics channel (relatively high capacitance)
- 600 Hybrids with 3 / 4 Beetle.
- Digitization on detector and digital optical links

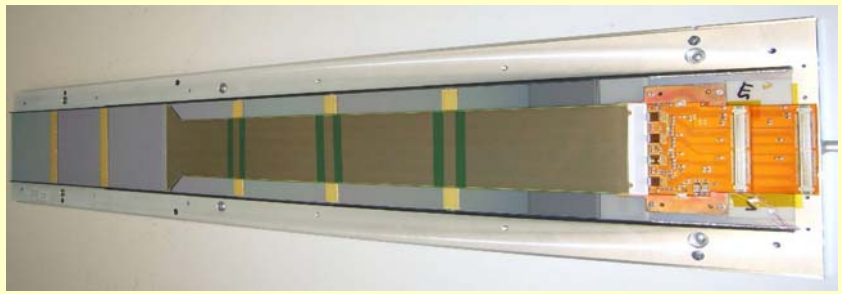






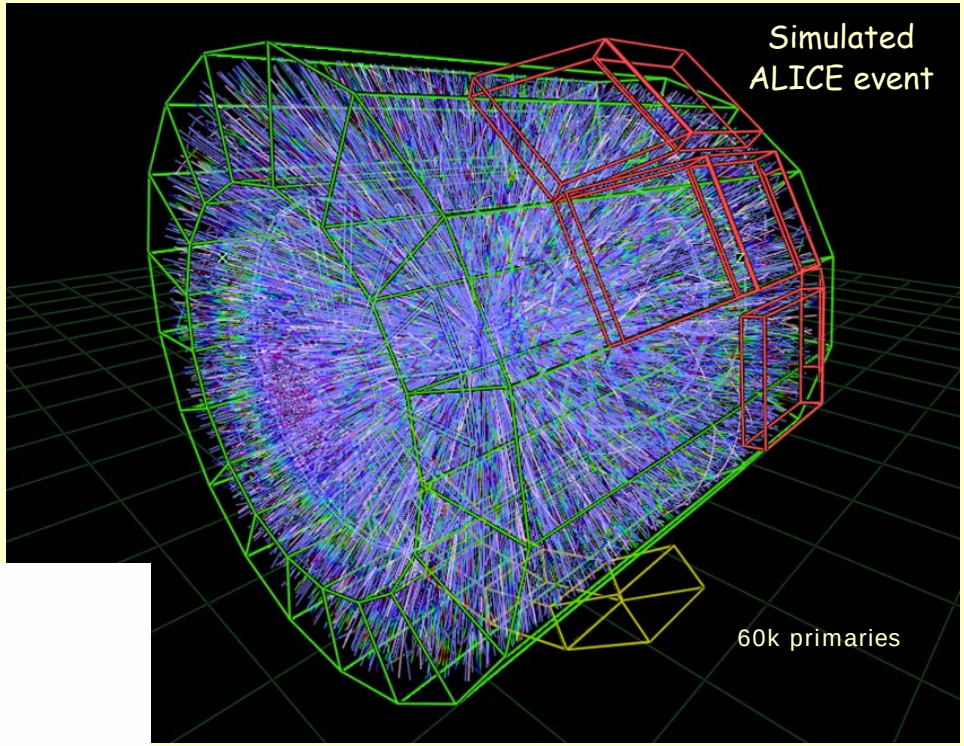


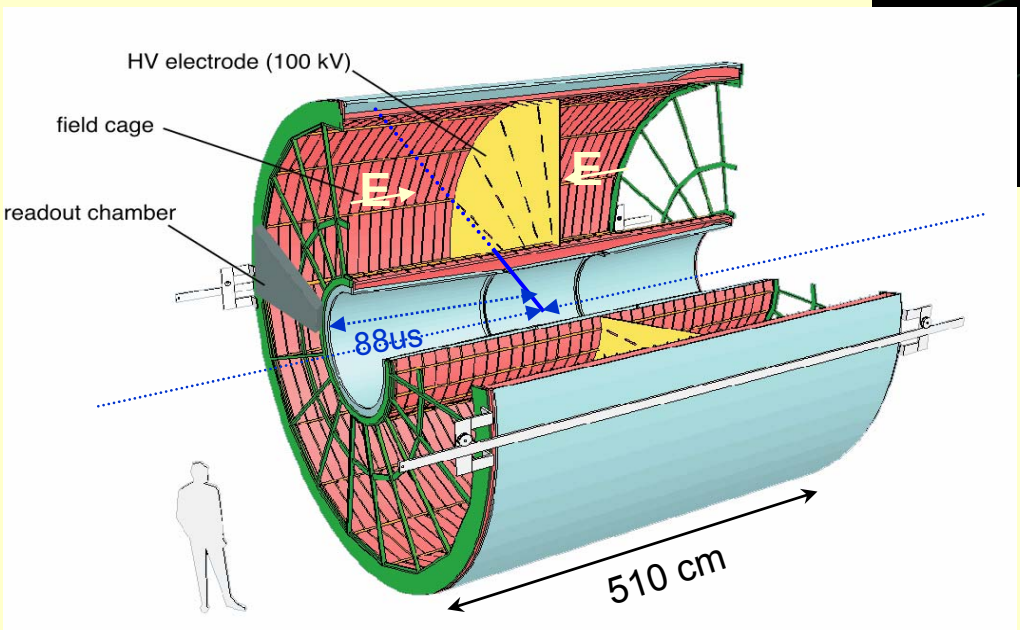


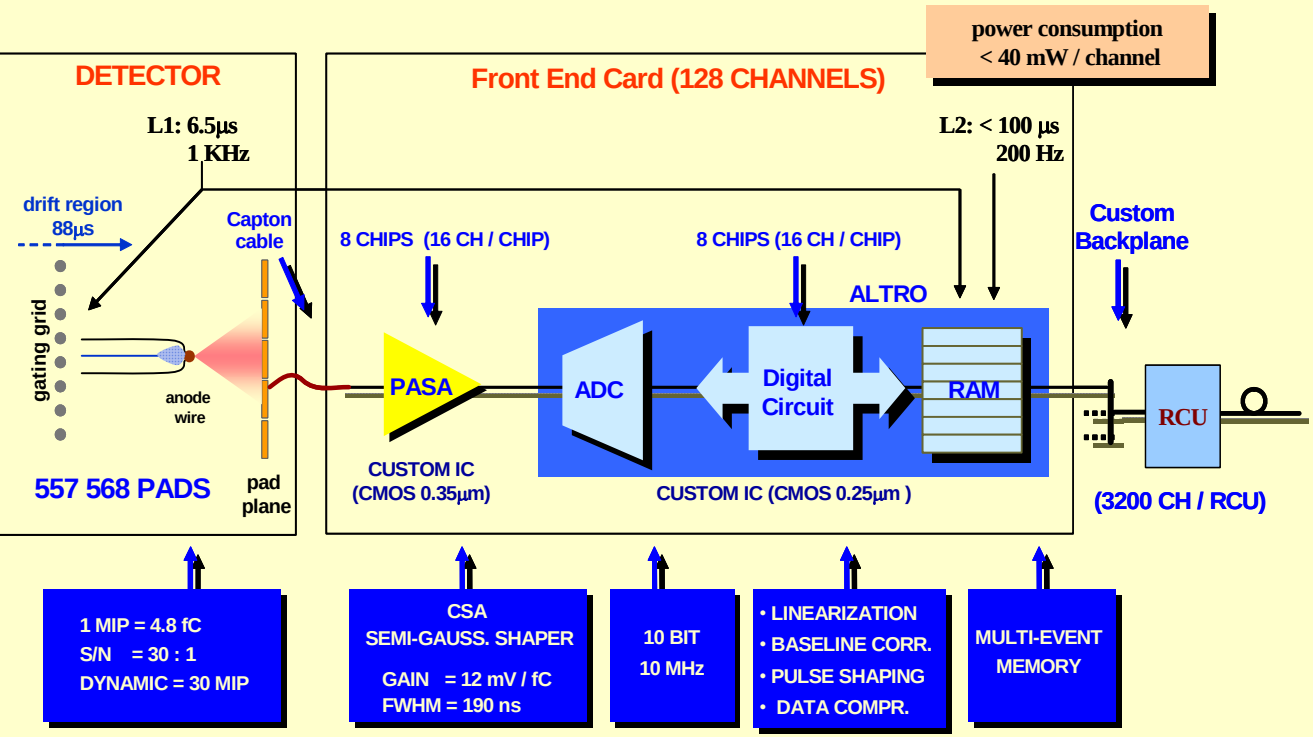


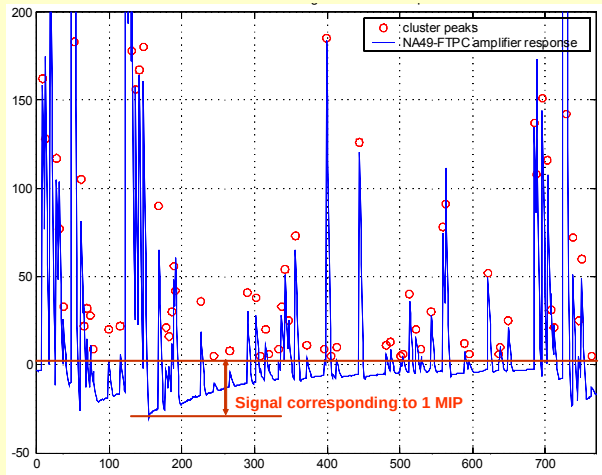
Alice TPC

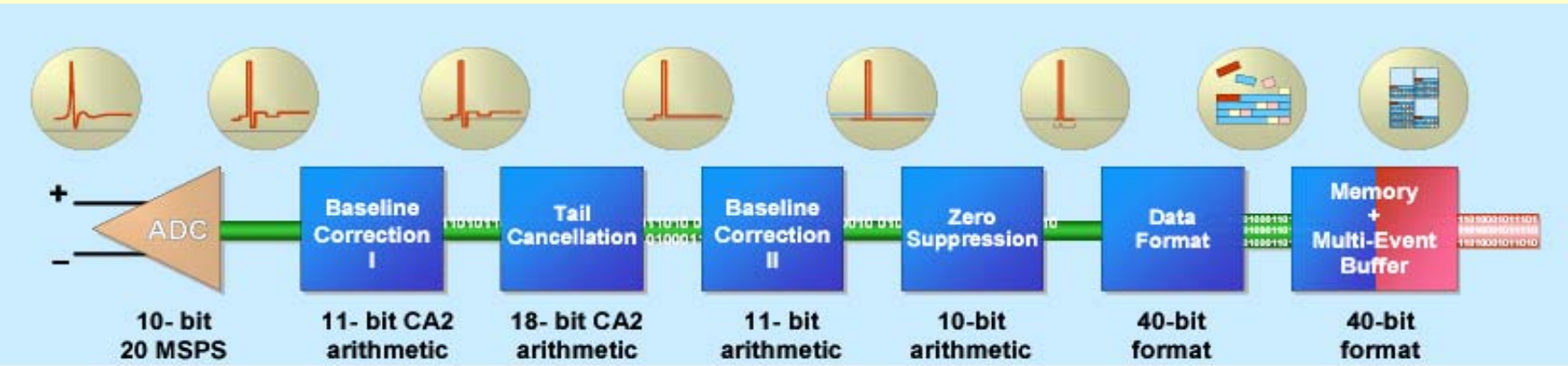
- Time projection chamber (long readout time)
- Main tracking/PID detector in ALICE
- Very high track density
- 558k pad channels
- Continuously sampled signal with on-detector DSP and zero-suppression





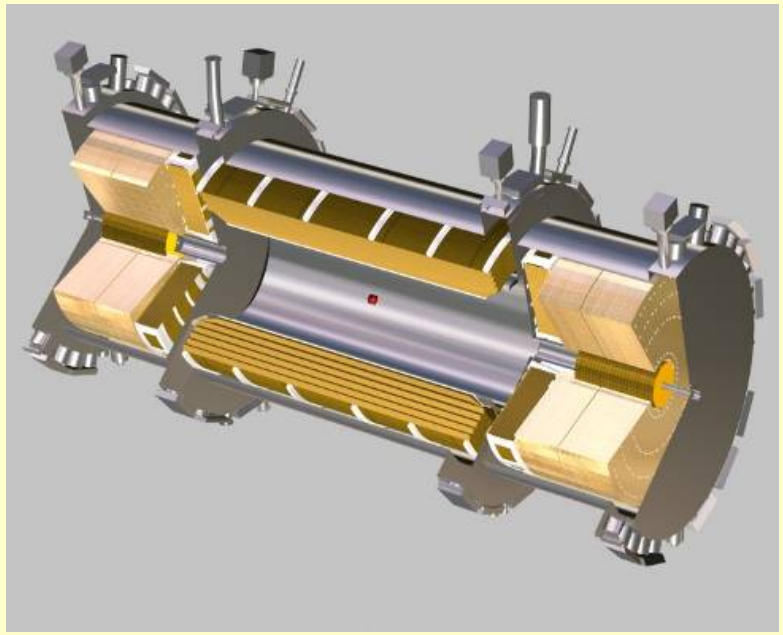

DETECTOR
Front End Card (128 CHANNELS)
power consumption
< 40 mW / channel
L1: 6.5µs
1 KHz
L2: < 100 µs
200 Hz
drift region
88µs
Capton
cable
8 CHIPS (16 CH / CHIP)
8 CHIPS (16 CH / CHIP)
ALTRO
Custom
Backplane
gating grid
anode
wire
PASA
ADC
Digital
Circuit
RAM
RCU
557 568 PADS
pad
plane
CUSTOM IC
(CMOS 0.35µm)
CUSTOM IC (CMOS 0.25µm)
(3200 CH / RCU)
1 MIP = 4.8 fC
S/N = 30 : 1
DYNAMIC = 30 MIP
CSA
SEMI-GAUSS. SHAPER
GAIN = 12 mV / fC
FWHM = 190 ns
10 BIT
10 MHz
• LINEARIZATION
• BASELINE CORR.
• PULSE SHAPING
• DATA COMPR.
MULTI-EVENT
MEMORY

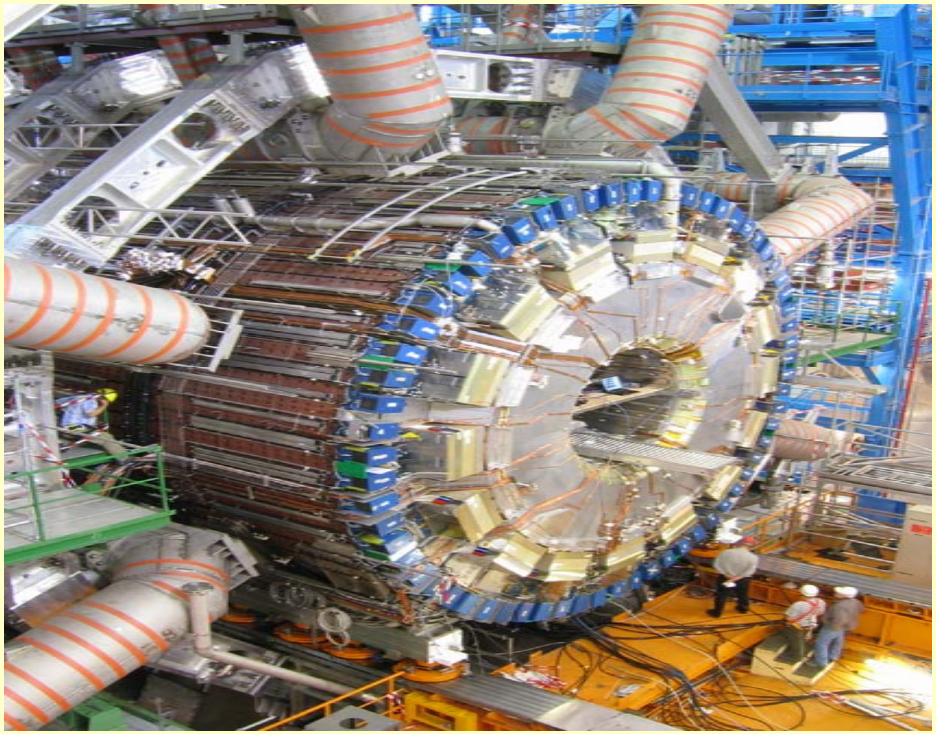

cluster peaks
NA49-FTPC amplifier response
Signal corresponding to 1 MIP
200
150
100
50
0
-50
0
100
200
300
400
500
600
700

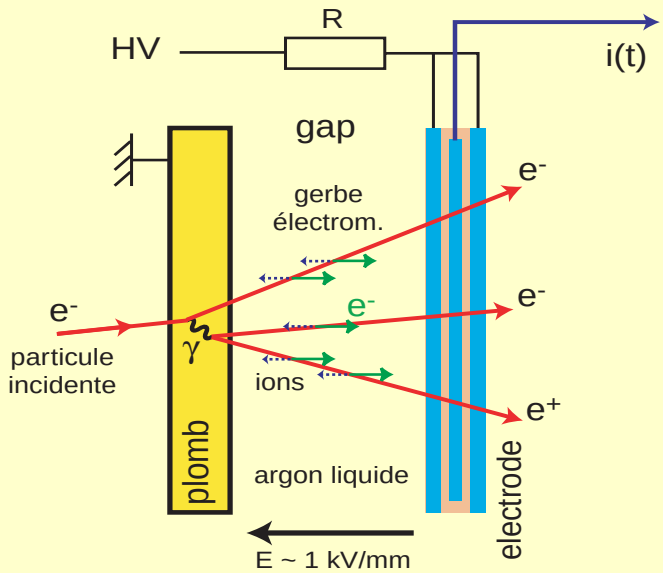

ADC
Baseline
Correction
I
Tail
Cancellation
Baseline
Correction
II
Zero
Suppression
Data
Format
Memory
+
Multi-Event
Buffer
10- bit
20 MSPS
11- bit CA2
arithmetic
18- bit CA2
arithmetic
11- bit
arithmetic
10-bit
arithmetic
40-bit
format
40-bit
format

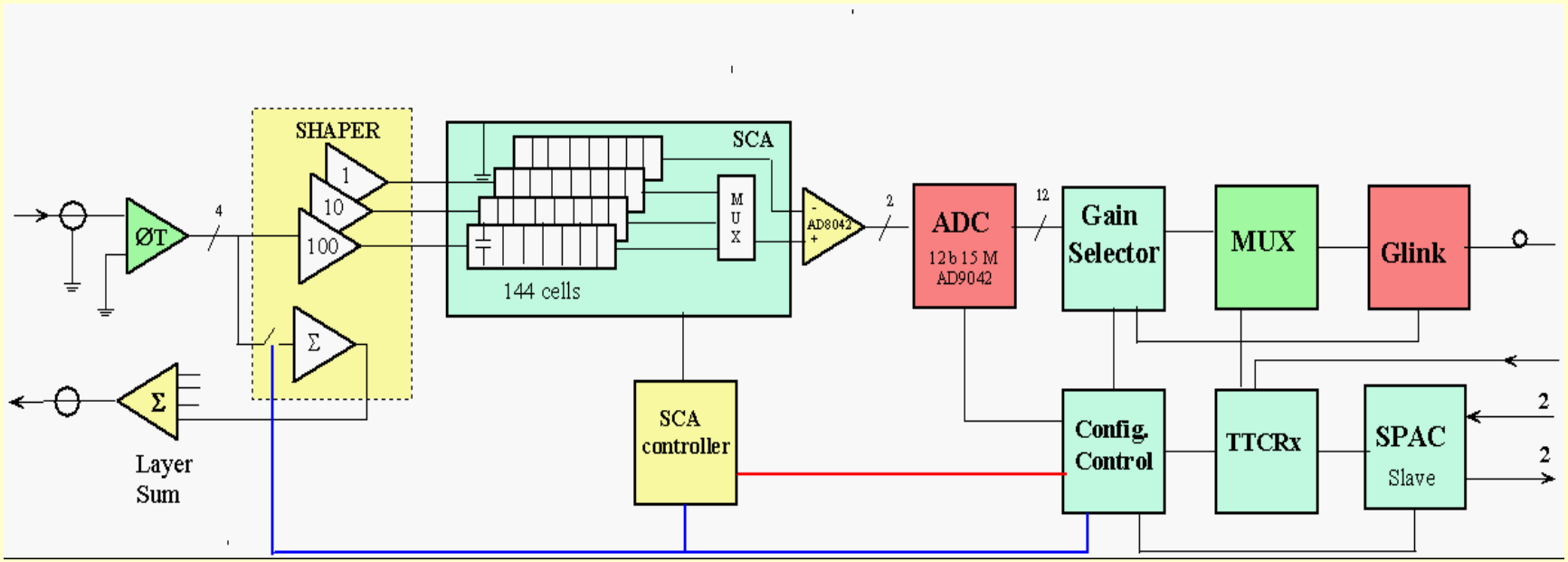
ATLAS Ecal

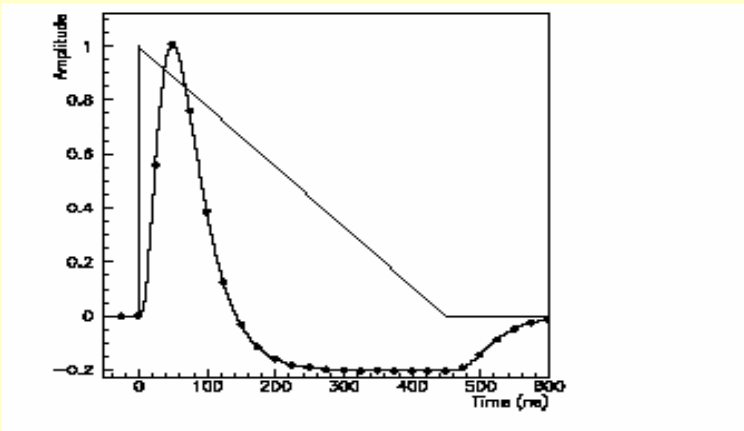
- 200k Channels
- 3 gain sub-channels
- Analog buffers
- 12 bit ADC

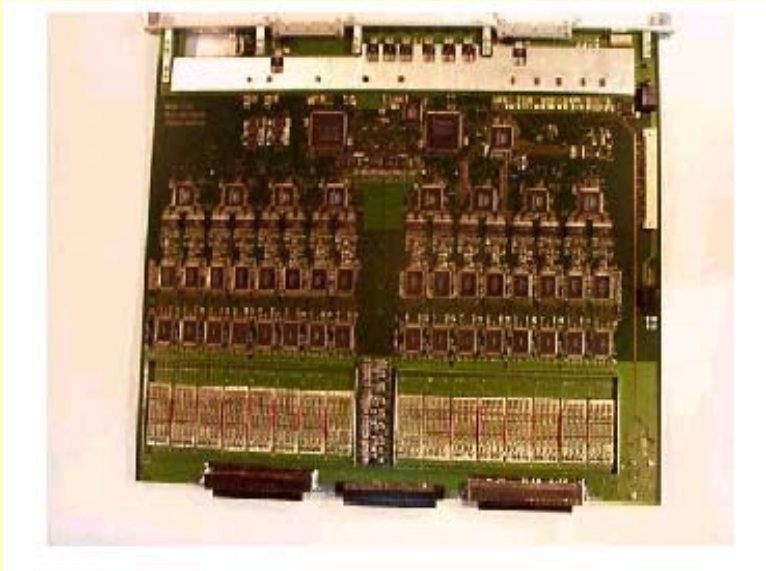






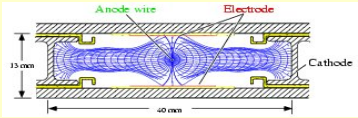

SHAPER
1
10
100
ØT
4
Σ
Σ
Layer
Sum
SCA
M
U
X
144 cells
AD8042
2
ADC
12b 15 M
AD9042
12
Gain
Selector
MUX
Glink
SCA
controller
Config.
Control
TTCRx
SPAC
Slave
2
2

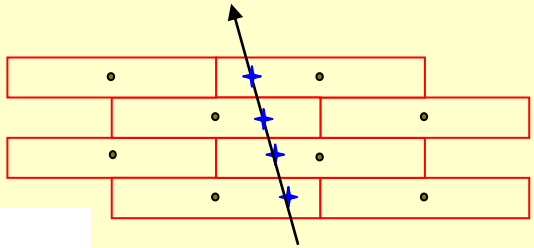

Amplitude
1
0.8
0.6
0.4
0.2
0
-0.2
0
100
200
300
400
500
600
Time (ns)

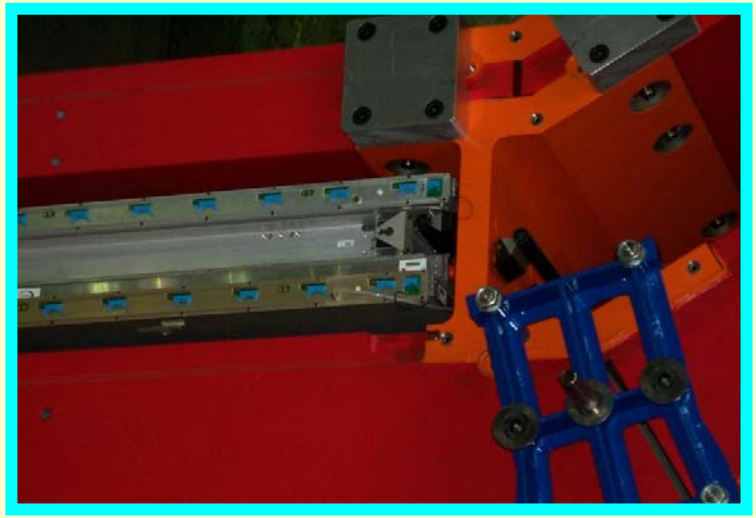


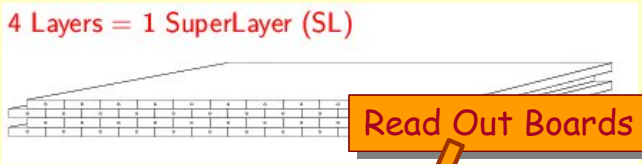
CMS muon

- 172k drift tubes
- 450ns drift time, Overlapping triggers
- ASDBLR and TDC



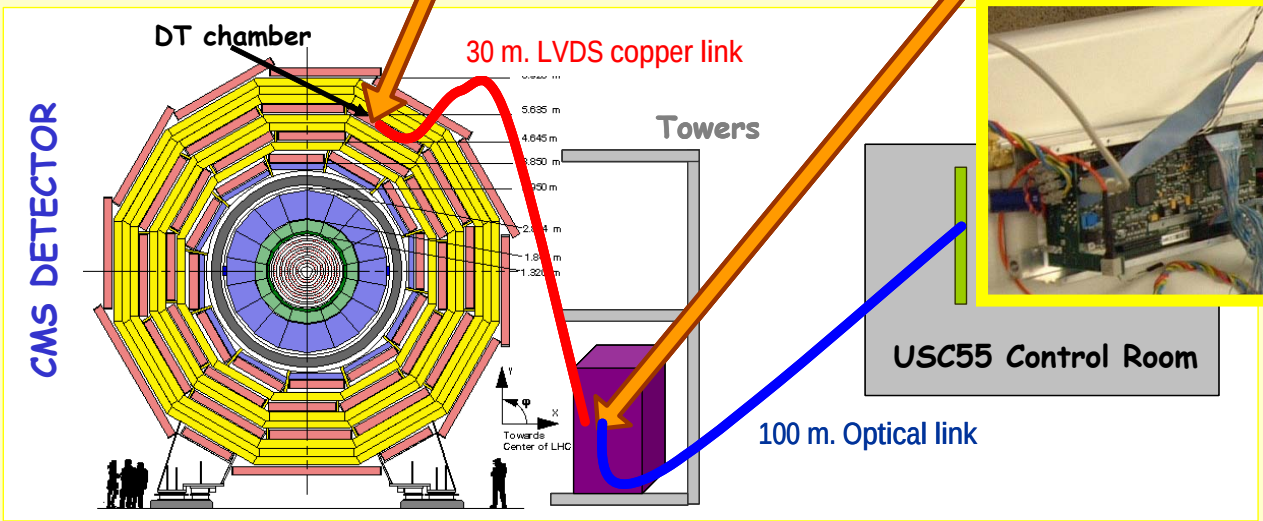


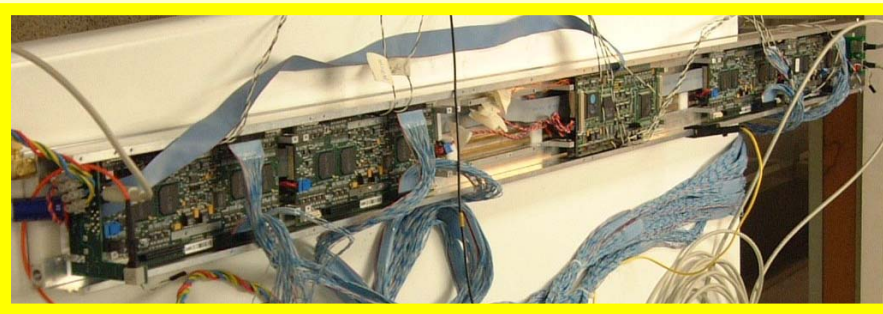


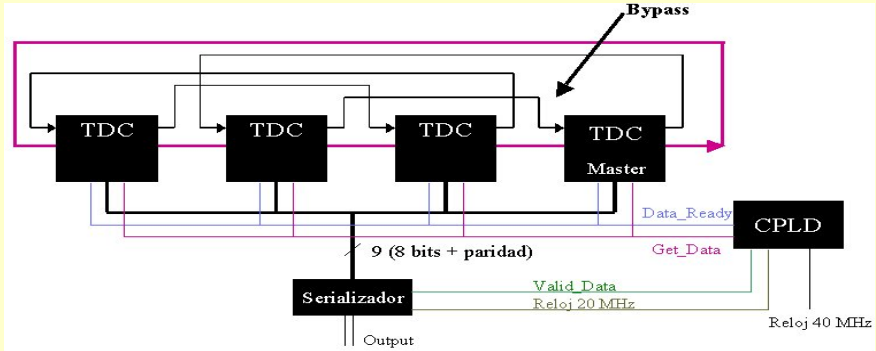


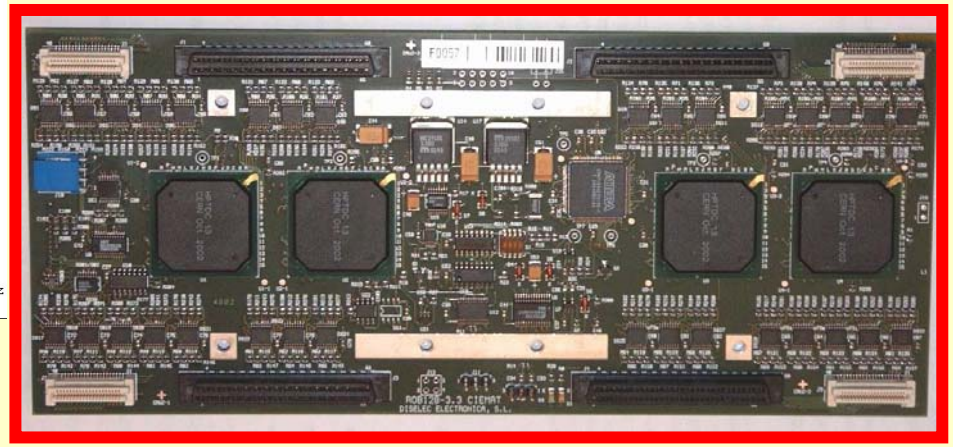
Read Out Boards (ROB)

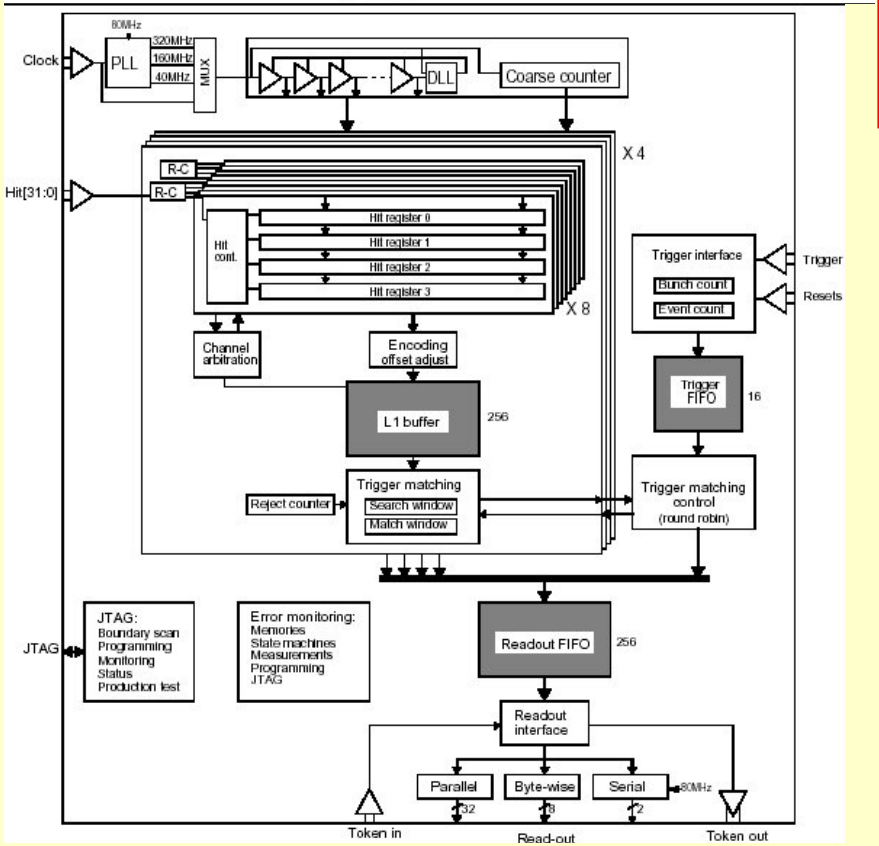
Read Out Server boards (ROS)

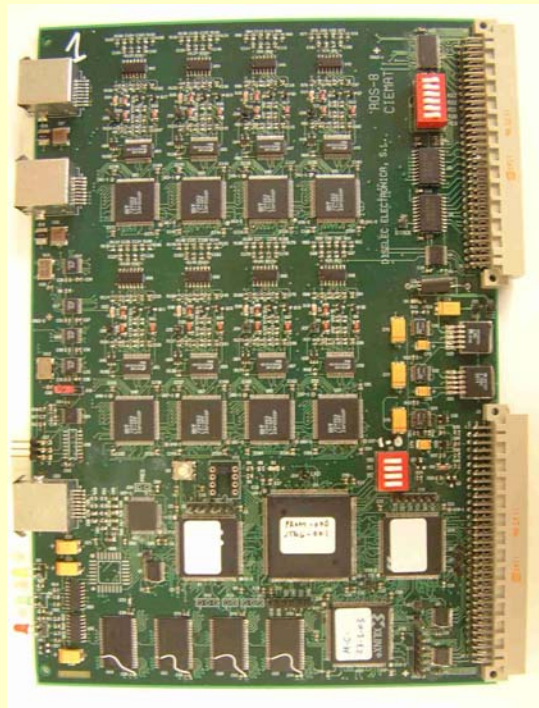





Bypass
TDC
TDC
TDC
TDC
Master
Data_Ready
CPLD
9 (8 bits + paridad)
Get_Data
Serializador
Valid_Data
Reloj 20 MHz
Reloj 40 MHz
Output

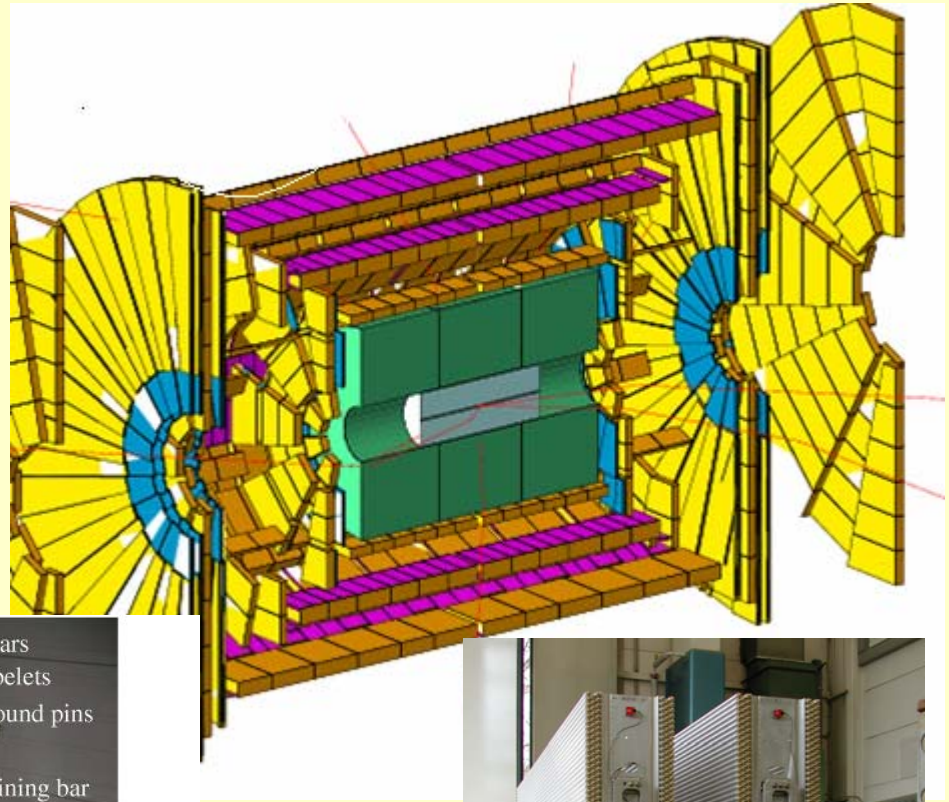


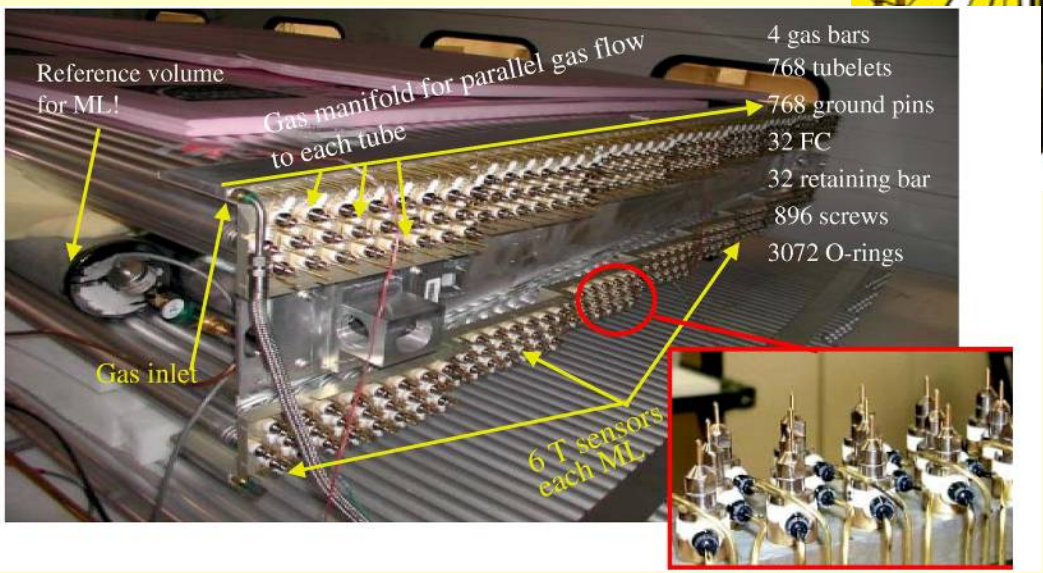

80MHz
Clock
PLL
320MHz
160MHz
40MHz
MUX
DLL
Coarse counter
X 4
Hit[31:0]
R-C
R-C
Hit cont.
Hit register 0
Hit register 1
Hit register 2
Hit register 3
X 8
Channel arbitration
Encoding offset adjust
L1 buffer
256
Trigger interface
Bunch count
Event count
Trigger
Resets
Trigger FIFO
16
Reject counter
Trigger matching
Search window
Match window
Trigger matching control (round robin)
JTAG
JTAG: Boundary scan Programming Monitoring Status Production test
Error monitoring: Memories State machines Measurements Programming JTAG
Readout FIFO
256
Readout interface
Parallel
Byte-wise
Serial
80MHz
32
8
2
Token in
Read-out
Token out

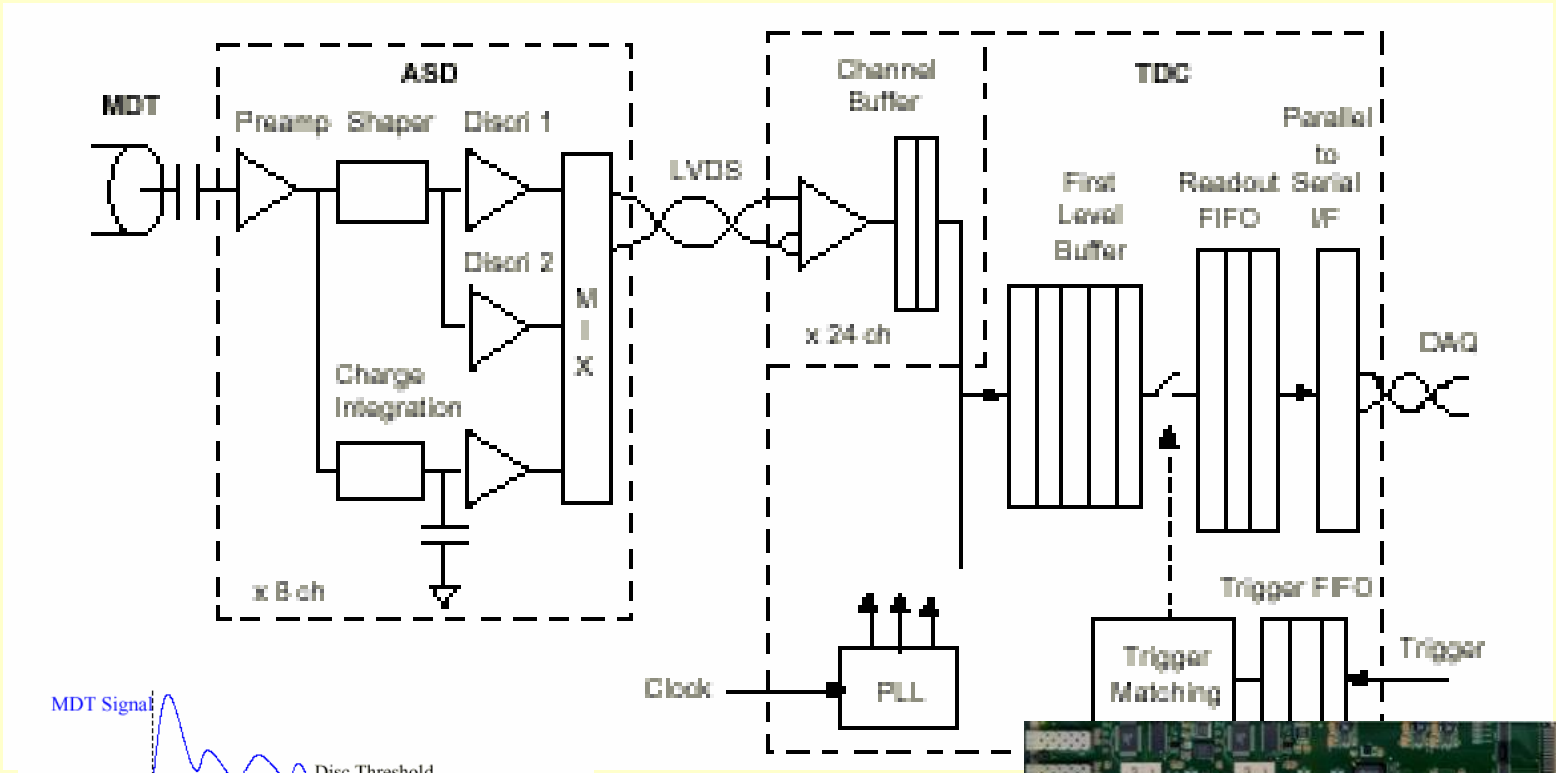


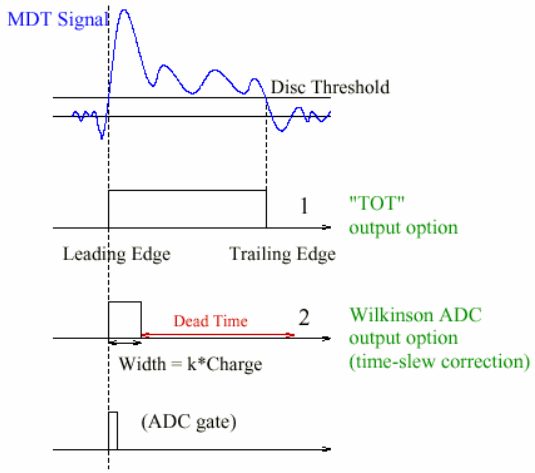
ATLAS MDT

- 370k Channels
- 3 m long drift tubes
- Covers 5500m^2
- 500ns drift time



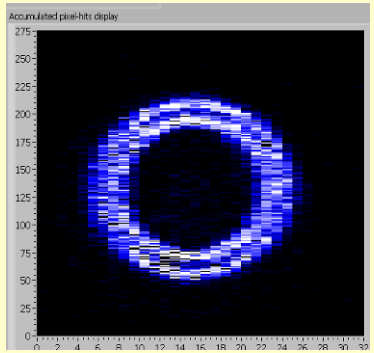


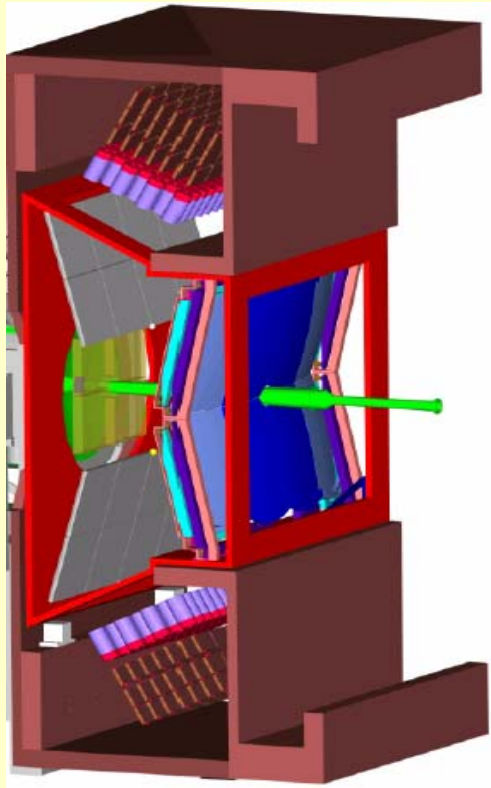

MDT
ASD
Preamp
Shaper
Discri 1
Discri 2
Charge Integration
M
I
X
x 8 ch
LVDS
Channel Buffer
x 24 ch
TDC
First Level Buffer
Readout FIFO
Parallel to Serial I/F
DAQ
Trigger FIFO
Trigger Matching
Trigger
Clock
PLL

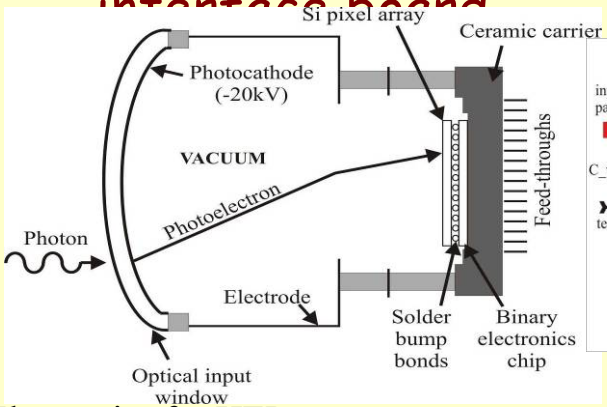

MDT Signal
Disc Threshold
1
"TOT"
output option
Leading Edge
Trailing Edge
Dead Time
2
Wilkinson ADC
output option
(time-slew correction)
Width = k*Charge
(ADC gate)

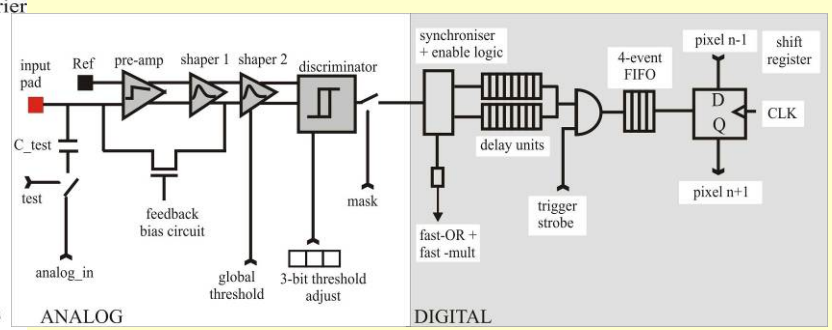
LHCb RICH

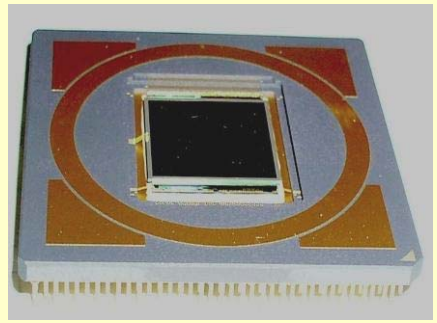
- Two RICH detectors for particle identification
- Based on 500 Hybrid Photon Detectors
- Each HPD vacuum tube contains a binary silicon pixel detector (1024 pixels)
  - Common development with ALICE
  - Does not have a L0 pipeline but a 16 hit buffer with time tags
- Local front-end card based on antifuse FPGA.
- Optical links to dedicated DAQ interface board

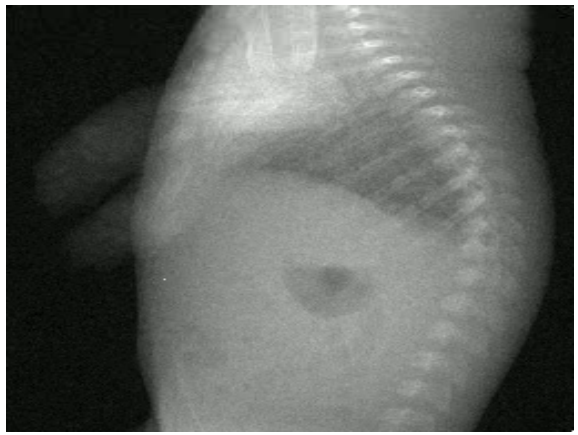


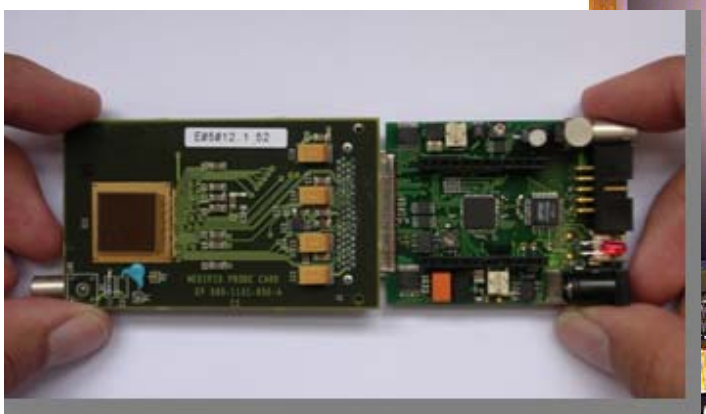


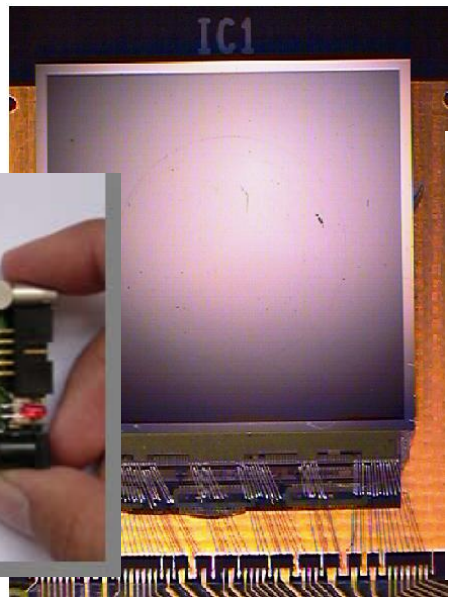


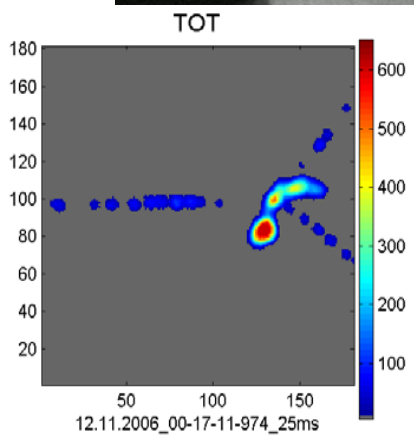


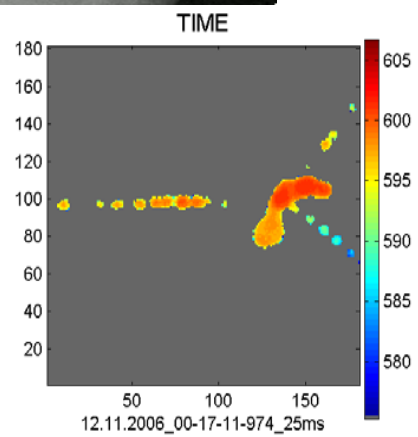


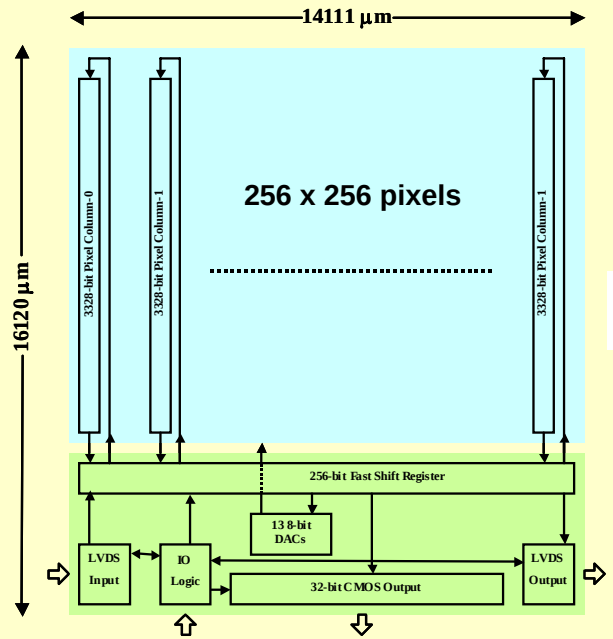


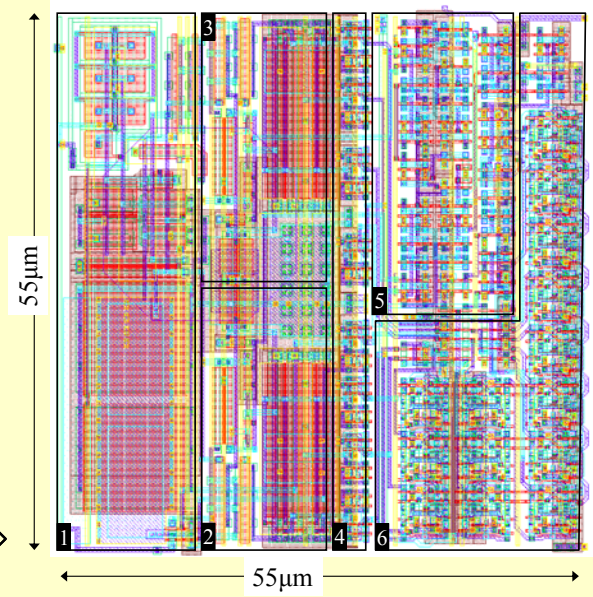


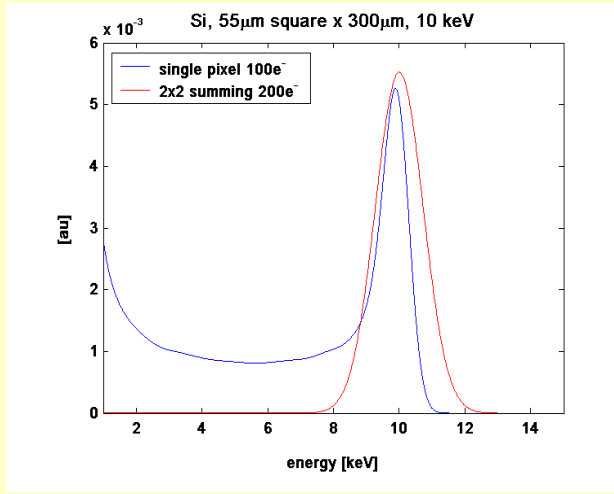

IC1


TOT
180
160
140
120
100
80
60
40
20
50
100
150
600
500
400
300
200
100
12.11.2006_00-17-11-974_25ms

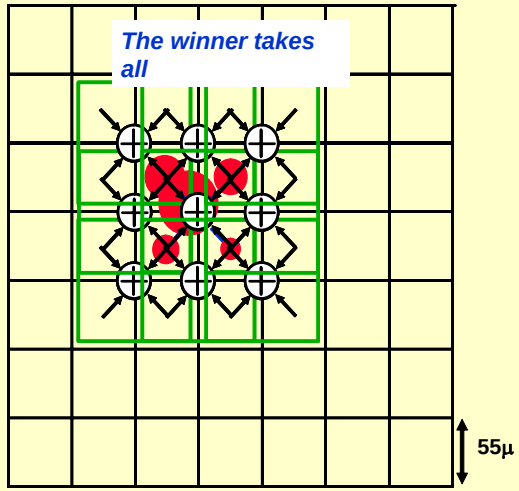

TIME
180
160
140
120
100
80
60
40
20
50
100
150
605
600
595
590
585
580
12.11.2006_00-17-11-974_25ms

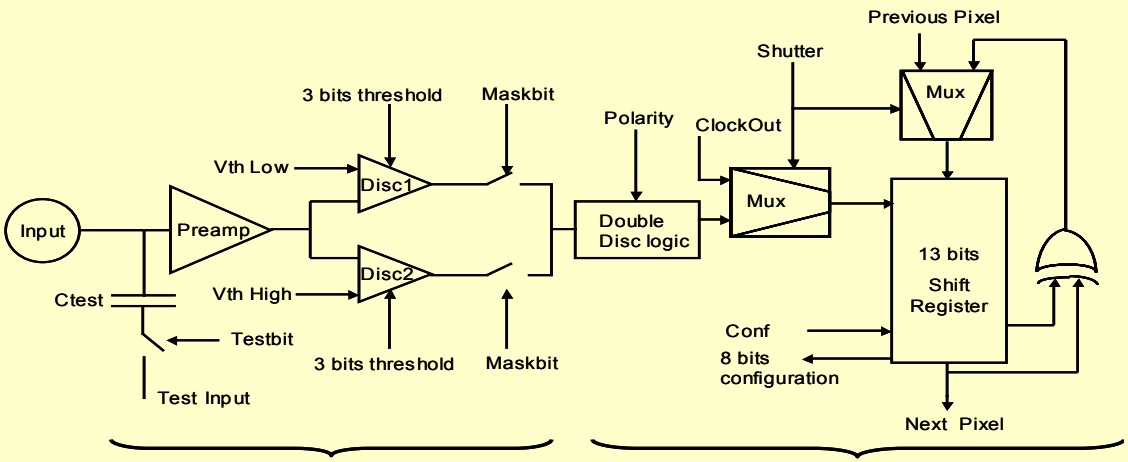






New improved version with charge summing across pixels

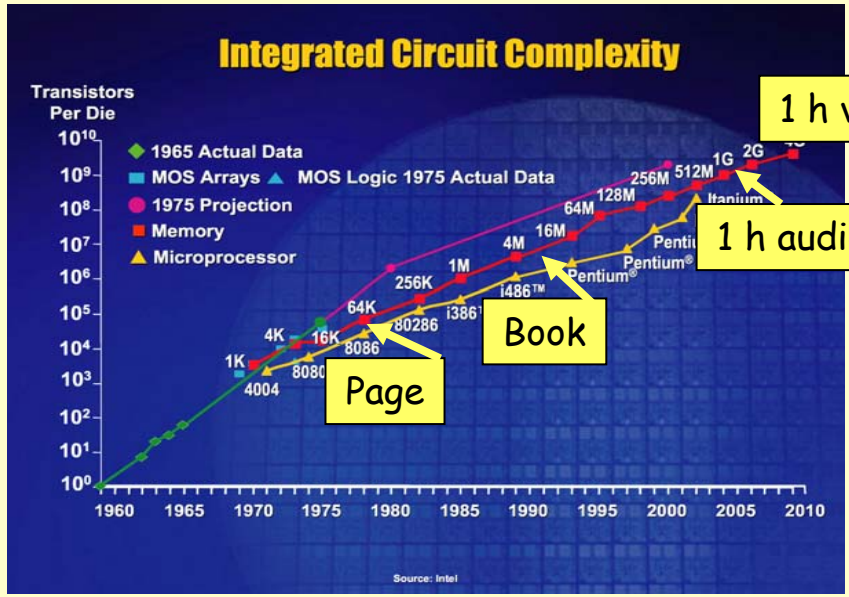


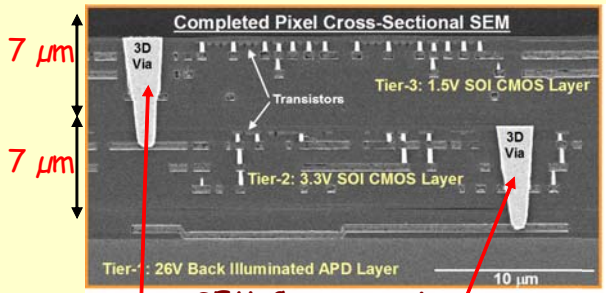


Analog *Digital*

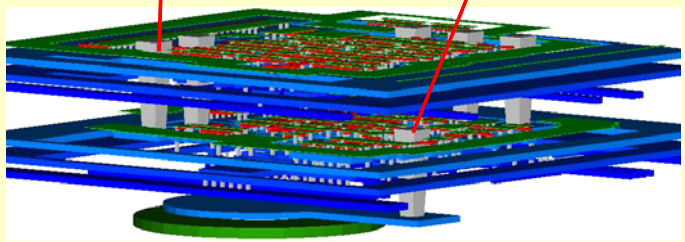
Future

- The electronics of future detectors will be tightly integrated with the detectors themselves
  - MAPS
  - 3D packaging
  - High density hybrids and bump bonding
  - New and other ideas (SiPM, , ,)
- Radiation hardness of the electronics will remain a critical issue for hadron machines (but not so much for linear colliders)
- Power is a critical issue for detectors with all this electronics
  - Can become one of the major design criteria to keep the material of trackers at an acceptable level
- Increasing use of digital processing on detector (if power allows)
- High speed optical links will be needed in large quantity to get data out of the detector
- DAQ interfaces will benefit from the fast improvements in commercial electronics (e.g. FPGA's)





SEM Cross section


CAD Drawing

That's the end