Implementation of the Timepix chip in the Scalable Readout System

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Topical Workshop on Electronics for Particle Physics

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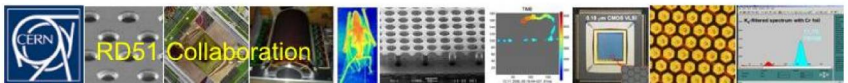
GEFÖRDERT VOM

Bundesministerium für Bildung und Forschung

AIDA



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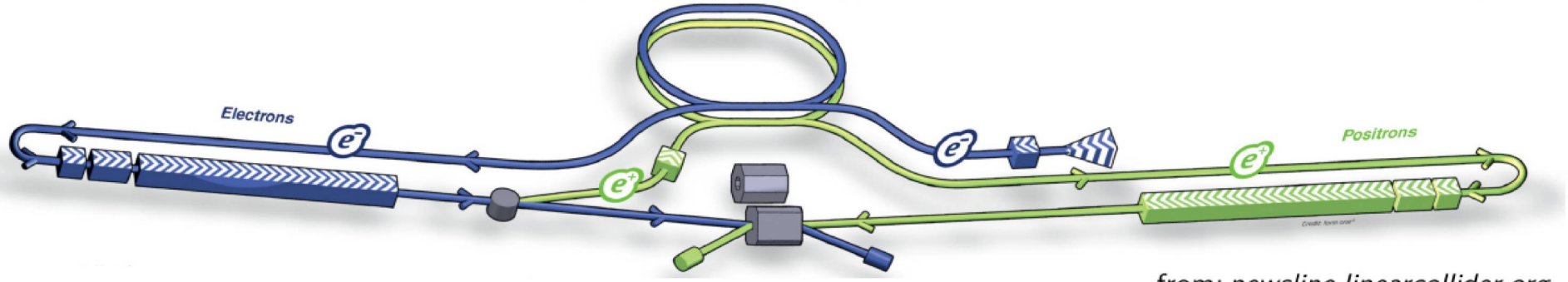
Outline

- Motivation
- The Timepix ASIC
- The Scalable Readout System
- Implementation of the ASIC
- 2015 test beam
- Conclusion and summary

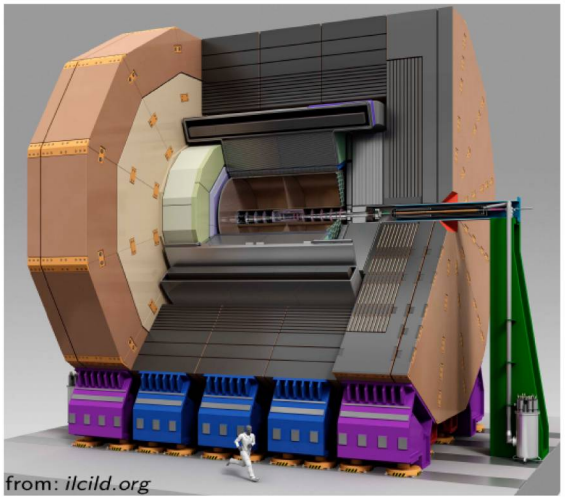
Motivation

Context: The International Linear Collider



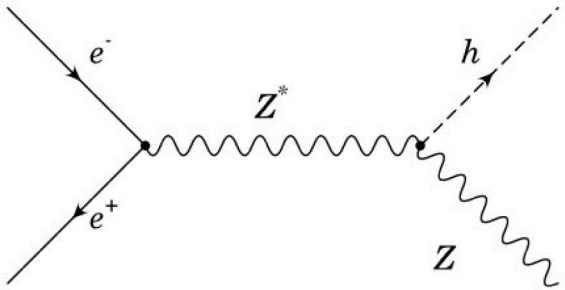
from: *newsline.linearcollider.org*

The ILD detector at ILC foresees a TPC as main tracker



High precision physics at ILC requires new detector technology.

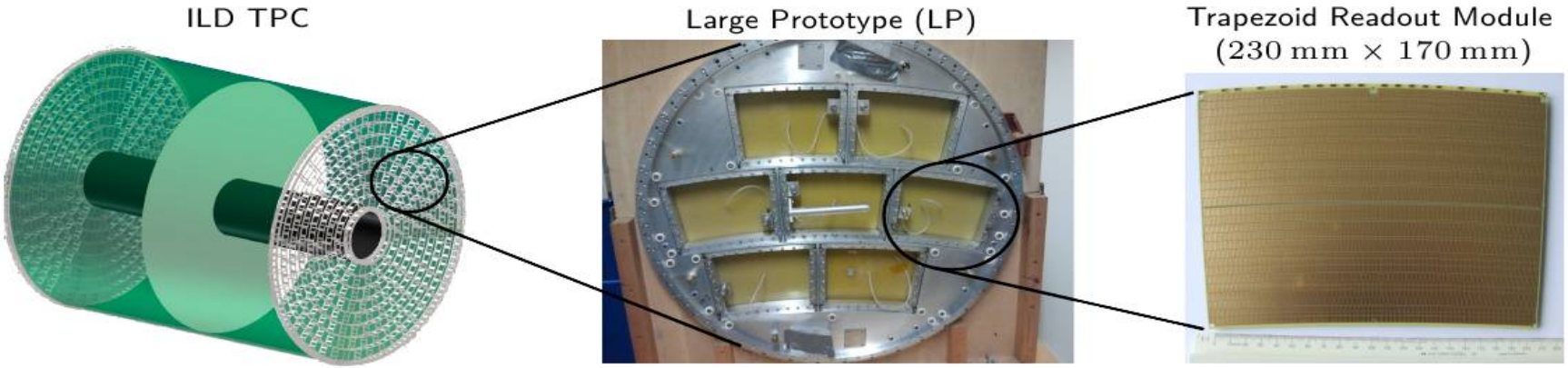
Requirement for tracker alone: $\sigma(1/P_t) < 10^{-4}$ /GeV/c

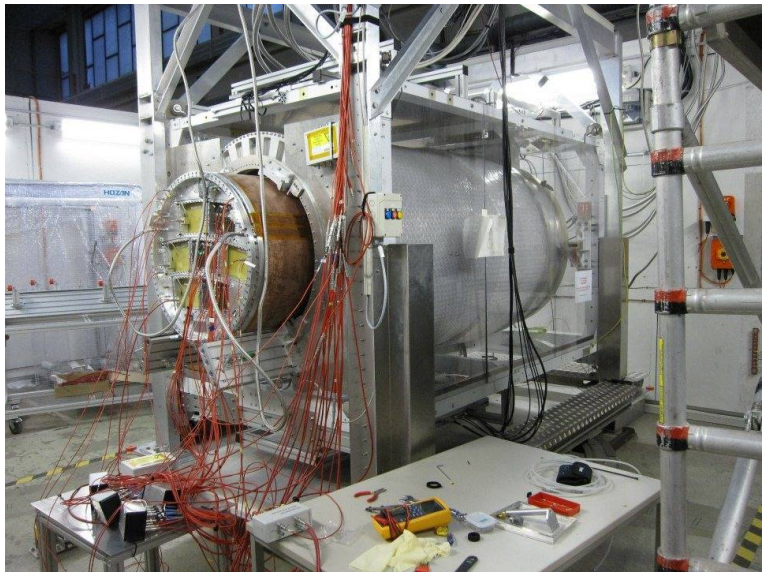


Motivation

LCTPC Collaboration: R&D for the ILD TPC

→ TPC prototype at DESY





Main field of studies:
Pad-based readout
+ MPGD (GEM, Micromegas)

MPGDs' structure size not reflected by pads
→ Spoil intrinsic resolution
→ Goal: A Pixel-TPC demonstrator

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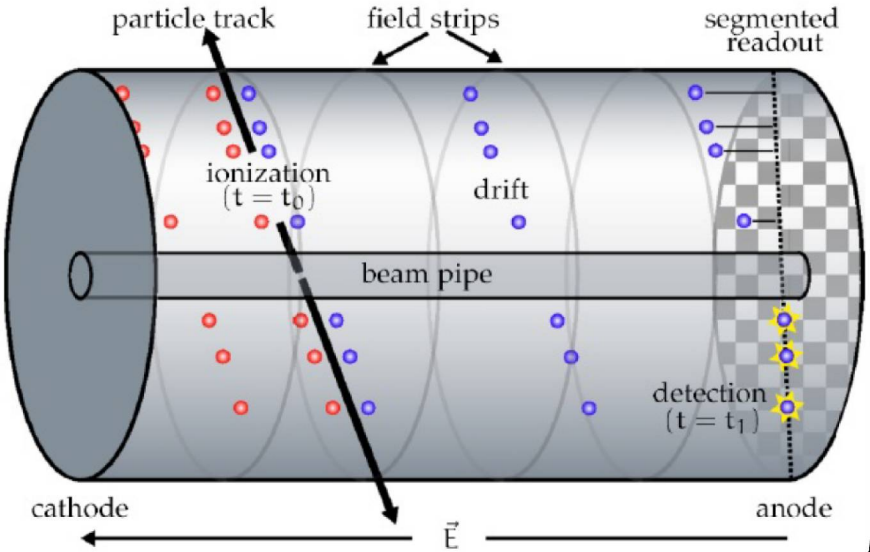
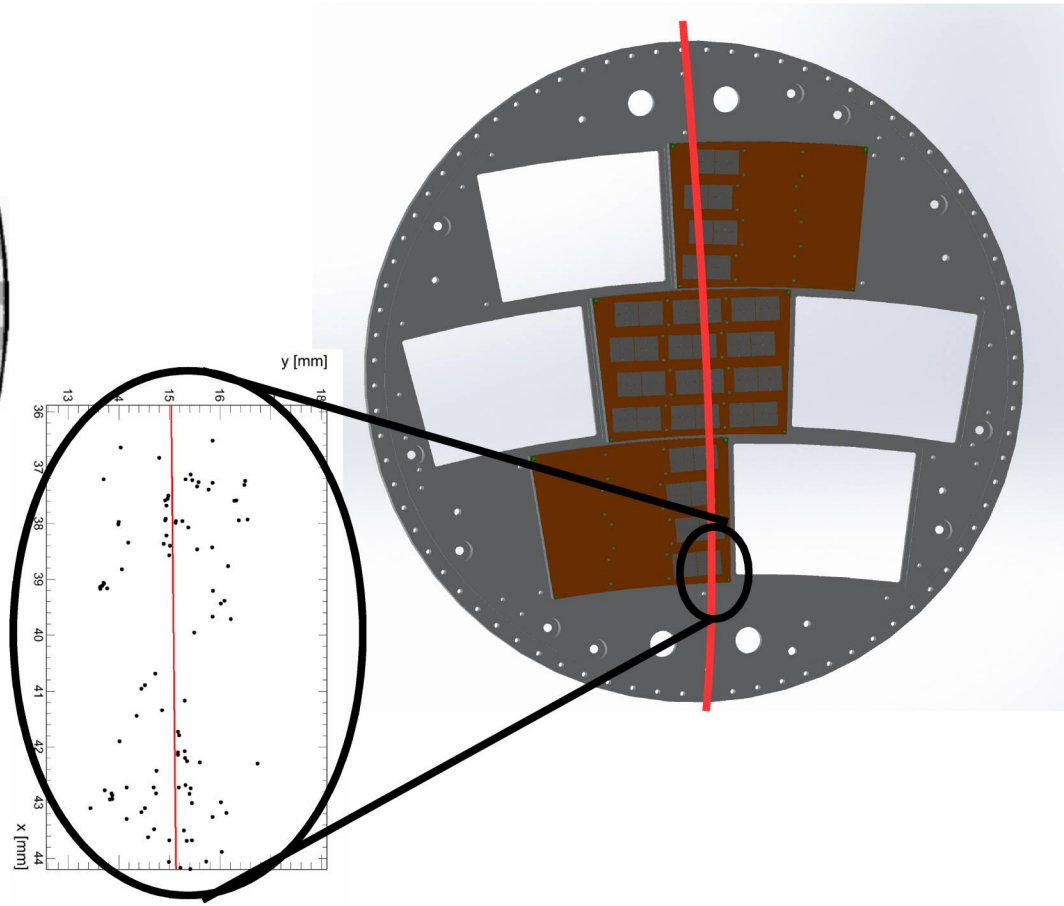
Motivation

The Pixel-TPC: a time projection chamber with pixelised readout

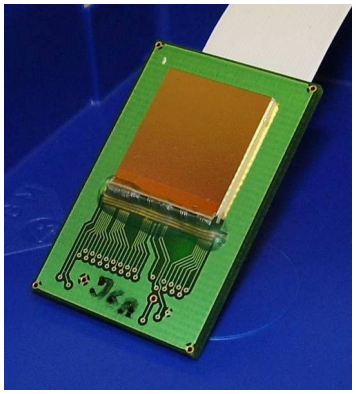


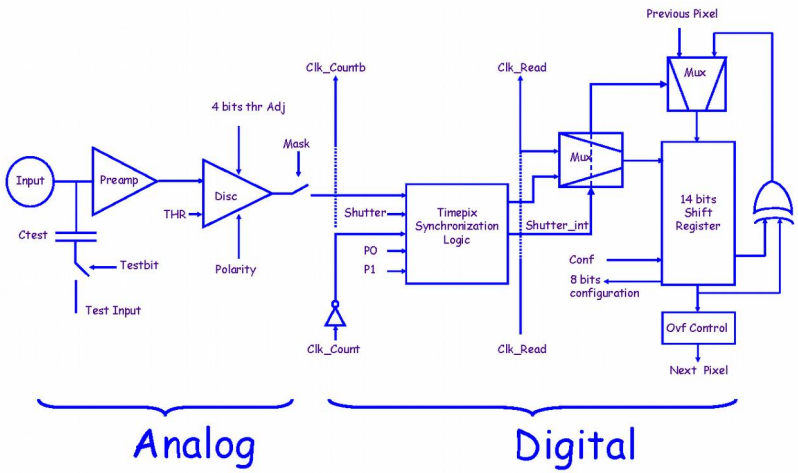


- Digital readout
- High granularity
  → pattern recognition
  → single electron detection
- Integrated gas amplification structure
- TPC endplate: large area → needs many ASICs

The Timepix ASIC

- Digital readout chip: The Timepix ASIC derived from Medipix2
- Properties
  - 1.4 x 1.4 cm² active surface
  - 256 x 256 pixel matrix
  - CMOS 250 nm technology, IBM
  - 55 x 55 µm² per pixel
  - amplifier/shaper (t_{rise} ~150 ns)
  - 14 bits count clock cycles
    → TOT or TOA mode
  - clock up to 100 MHz in every pixel
  - threshold level ~ 500 e^- (90 e^- ENC)





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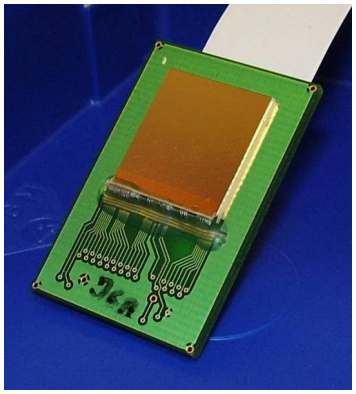
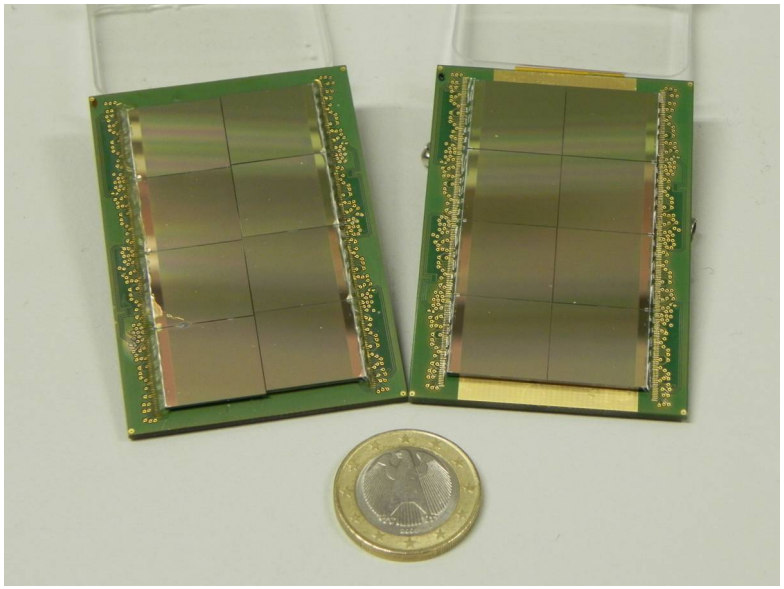
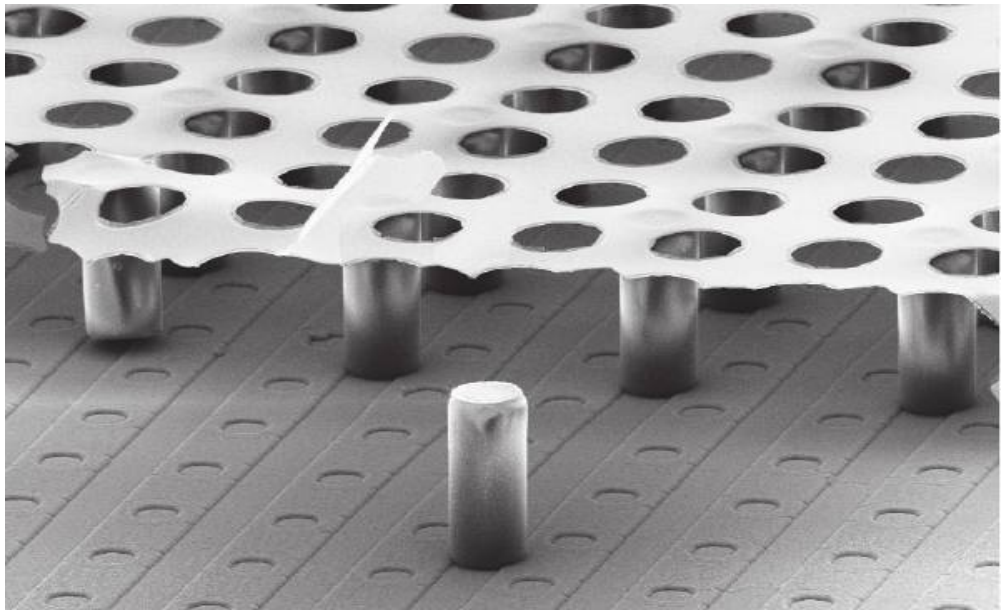


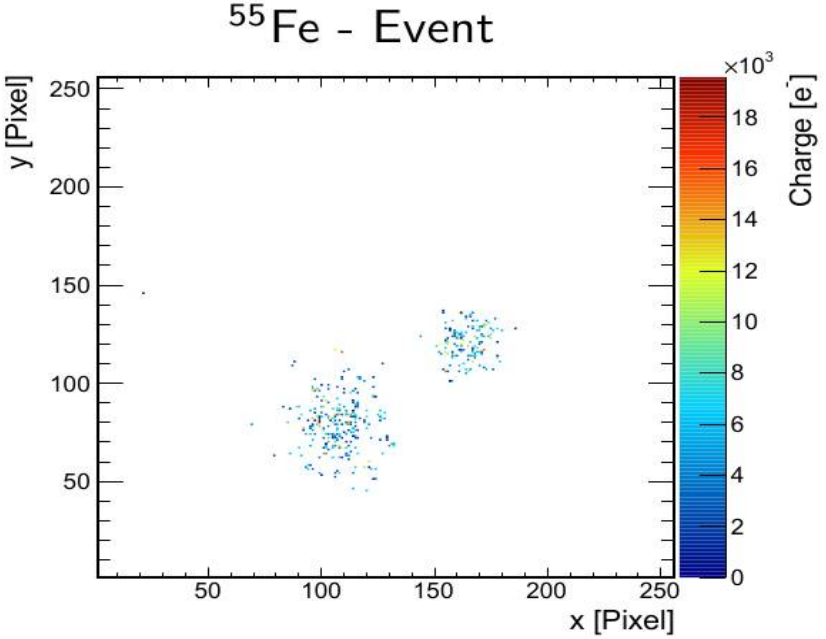


- Use bump bond pads as readout anode in gaseous detectors

Timepix+Micromegas=InGrid

- Aluminium grid on chip
- Photolithographic process
  - Align holes to pixel
  - Uniform pillar height





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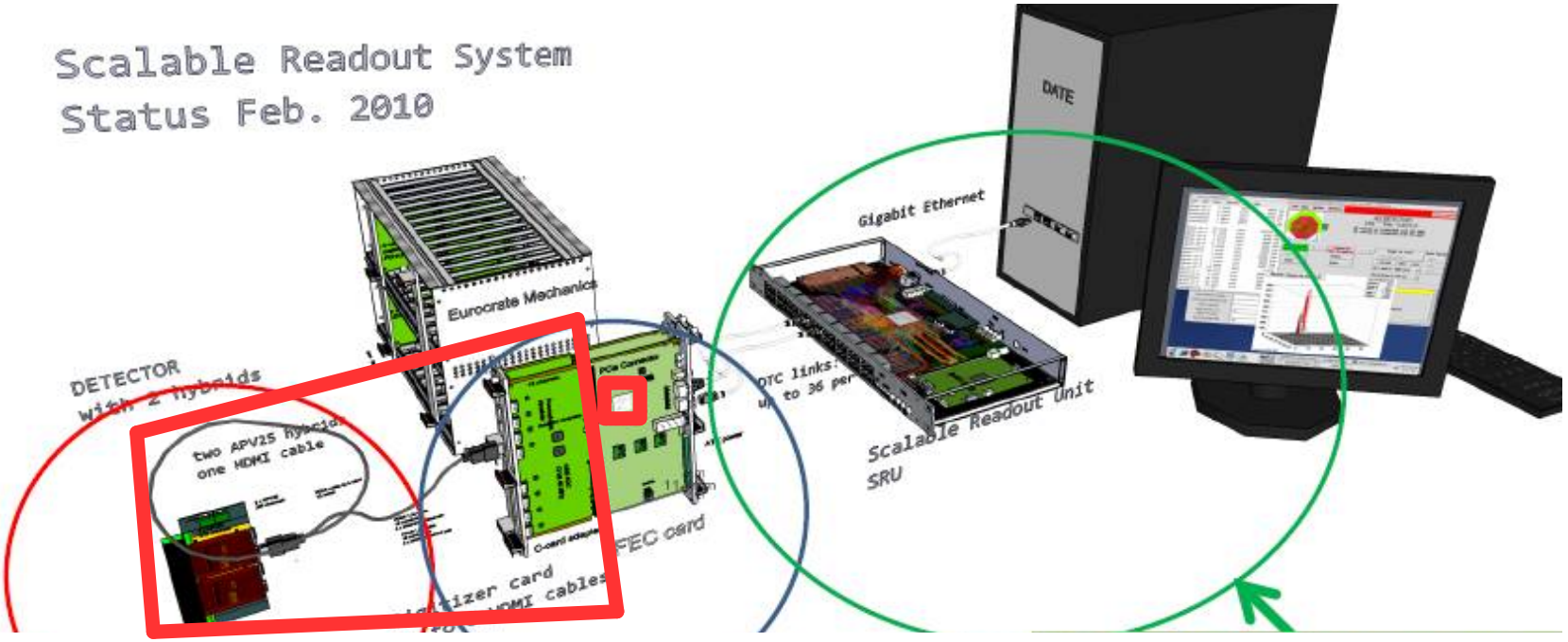
The Scalable Readout System

Developed within RD51 (open source)

- Provides common hard- and firmware
- Uses cheap standard components
- User part: chip carrier, adapter card, FPGA firmware



Used in many experiments, from single unit systems to large ones in LHC experiments.

Implementation of the ASIC

Design goals/choices:

- Readout system for more than 100 Timepix chips
- Flexible design for hardware, software and firmware

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  e.g analogue signals
  - test pulses
  - read back DAC values (DAC_out)

  → I2C network to control/read out DACs/ADCs by FPGA

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- Adapted to setup at a TPC

  e.g magnetic field of 1 T at endplate → FEC power supply far away

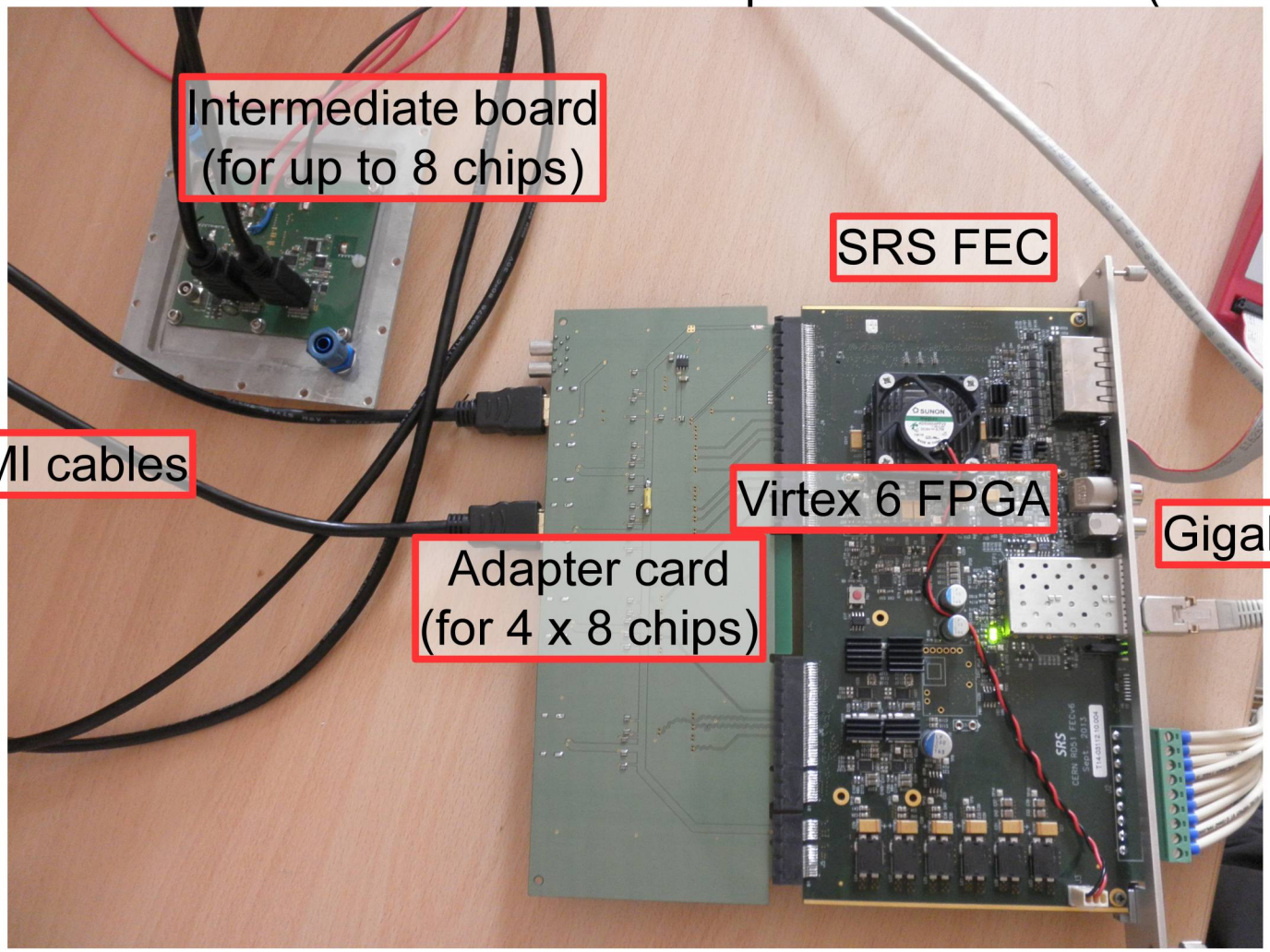
  → 15 m cables between readout system and chip

  → no transmission of analogue/CMOS signals

Implementation of the ASIC

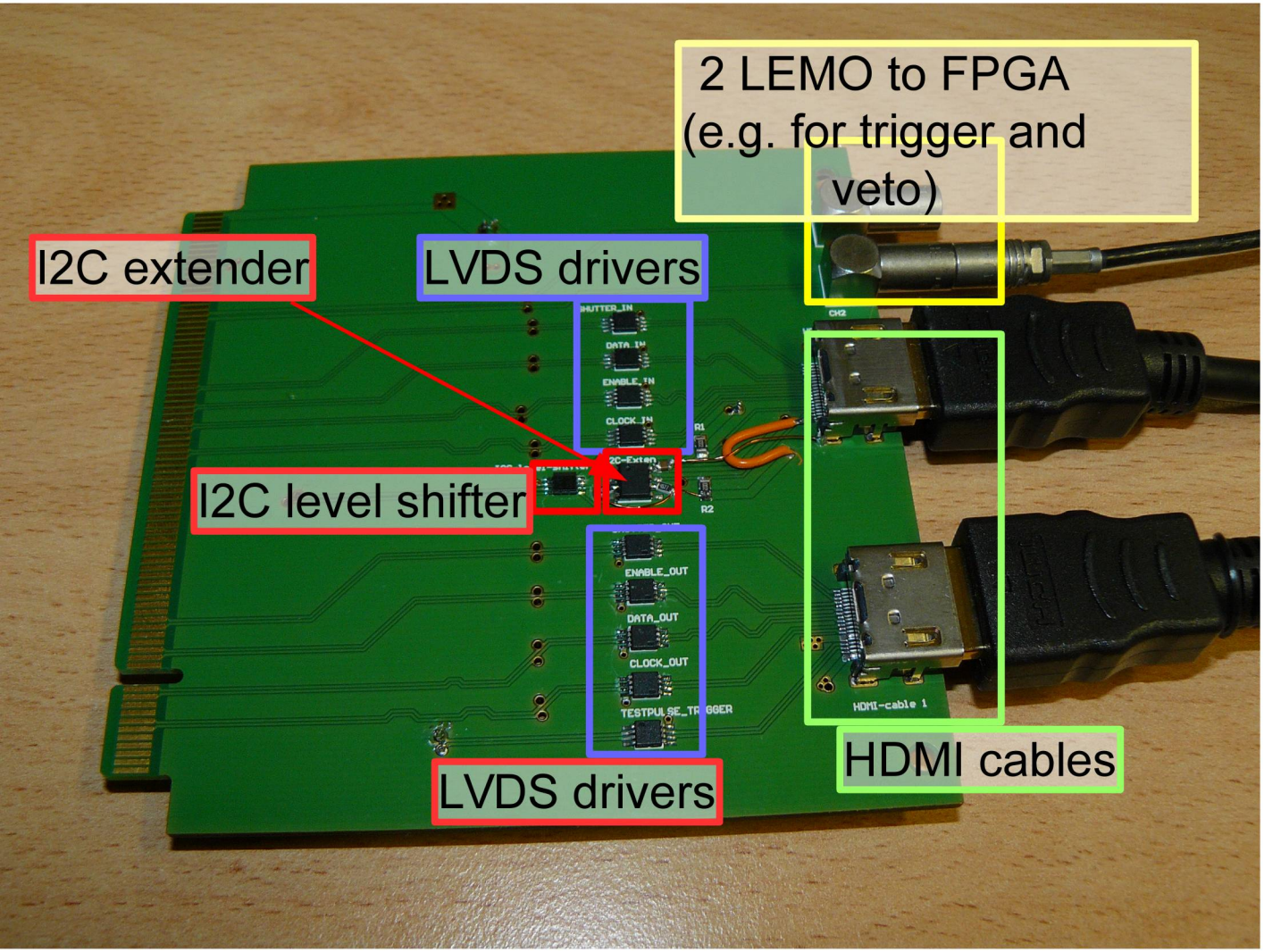
Readout chain:

Chip carrier/Intermediate board ↔ adapter board/FEC ↔(Switch) ↔ PC/DAQ



Adapter card

Smaller version shown here (for up to 1 x 8 chips)



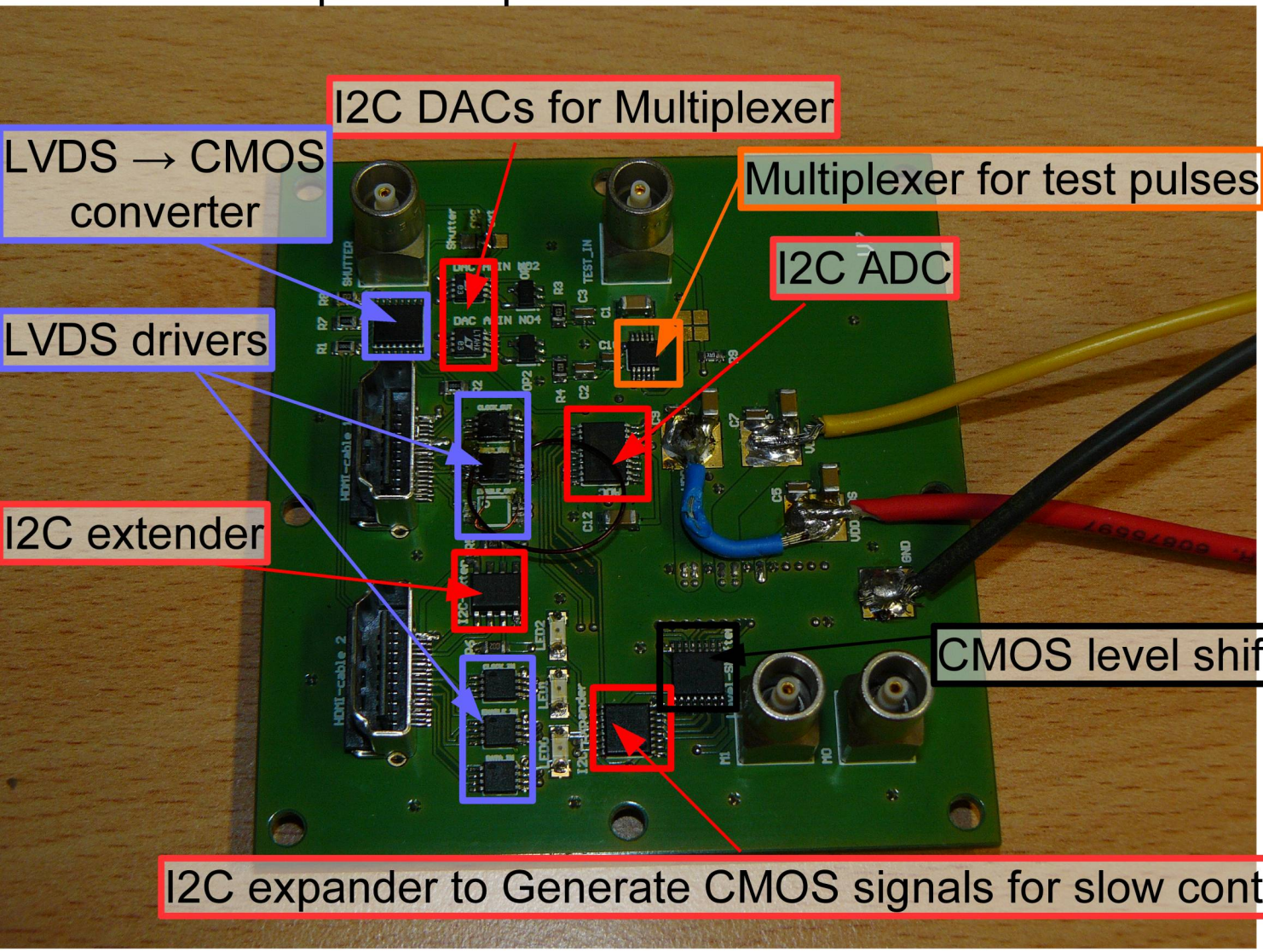
I2C signals:
- scl: clock
- sda: data

Designed for communication between PCBs next to each other.

With extenders: Several meters distance.

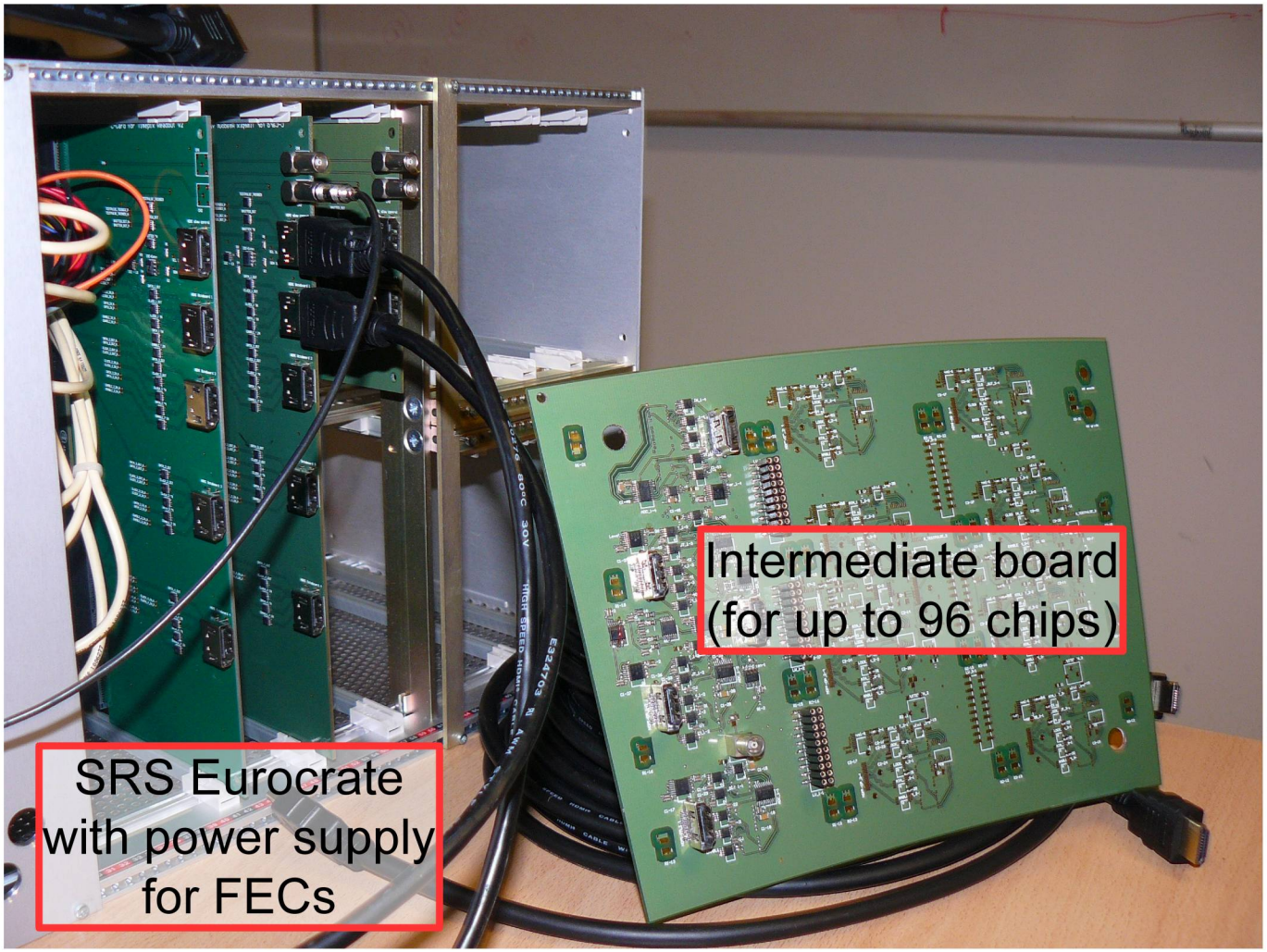
Intermediate board

Version for up to 8 chips

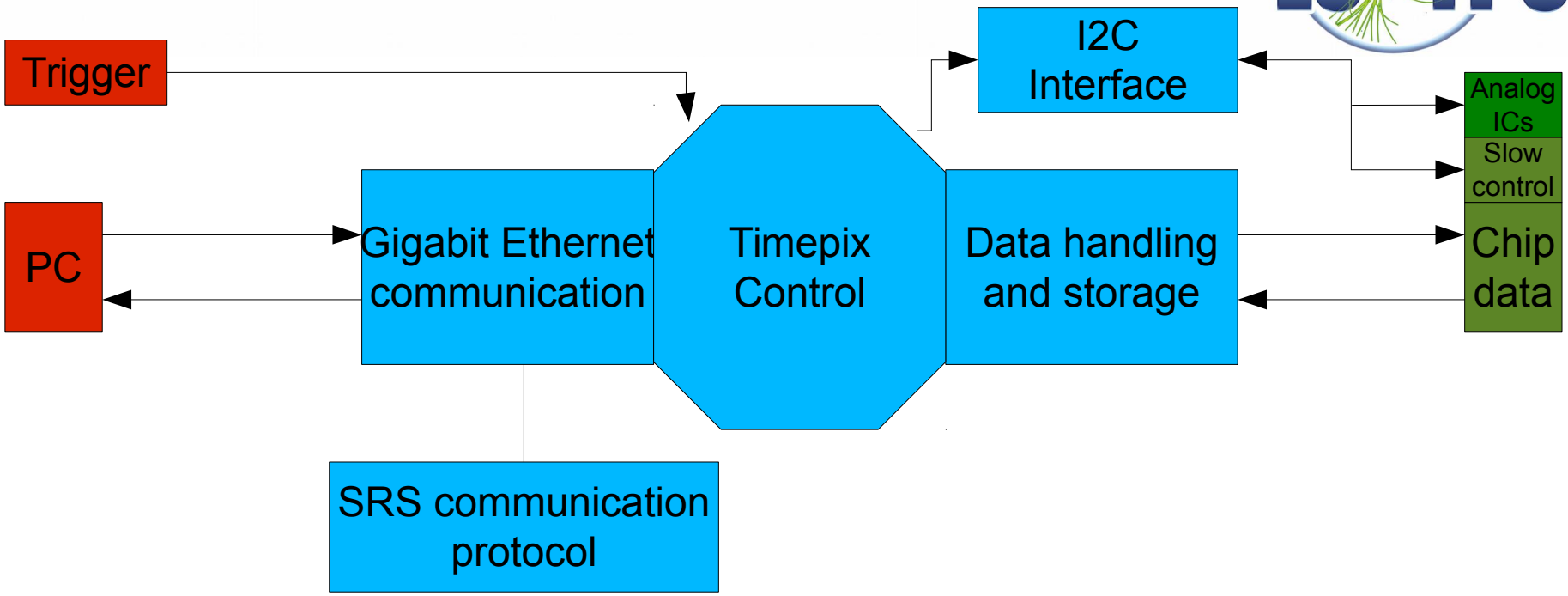


Intermediate board

Version for up to 96 chips



FPGA Firmware



Some features:

- I2C interface for chip slow control and analogue components
- Zero suppression of data from chip
- Storage of two frames in internal RAM (max. 4096 hits/chip)
- Multithreading: read out chip while sending data of last frame

Basic system tests

Operation of single chips and single octoboards in laboratory:

- Set ASIC DACs, read back chip IDs
- Set pixel matrix and read it back
- DAC scans
- Threshold equalisation with noise level
- TOT/TOA calibrations, S-Curve measurements with test pulses
- Readout speed tests

Functionality verified in comparison to a different readout system (MUROS)

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Test beam in 2013 with intermediate stage readout system and detector:

- Reliable operation of readout
- 2% of data affected by bit shifts
- SRS power supply destroyed in stray field of magnet
- Input for further developments for detector and readout

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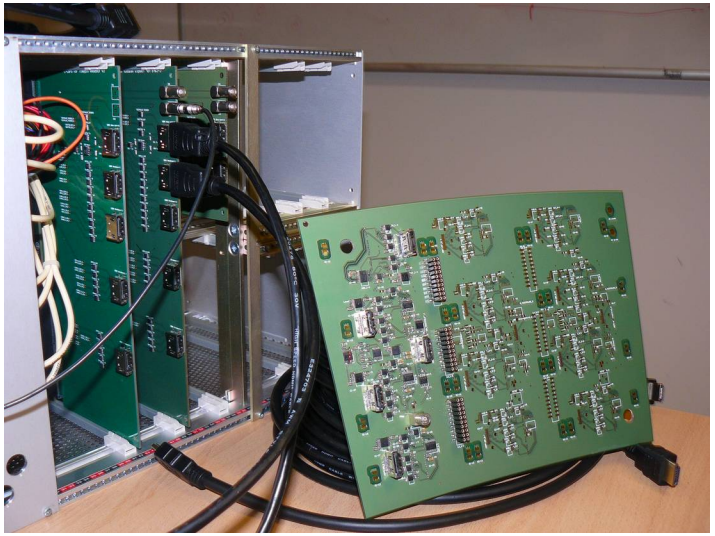
Large scale system

Use SRS scalability

Basic unit: 4 Octoboards(32 Timepix chips)/FEC with large adapter card

- 3 FECs for 96 chip Intermediate board
- Each FEC with its own IP/MAC
- Standard Gbit Ethernet switch
- Clock synchronisation between FECs



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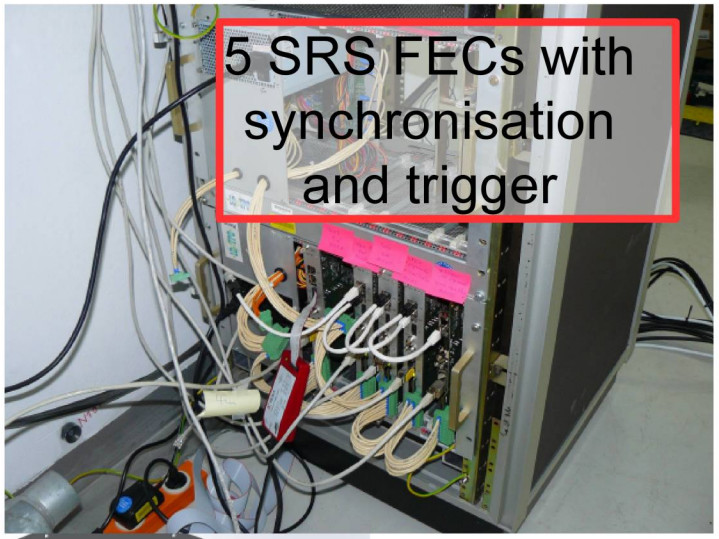
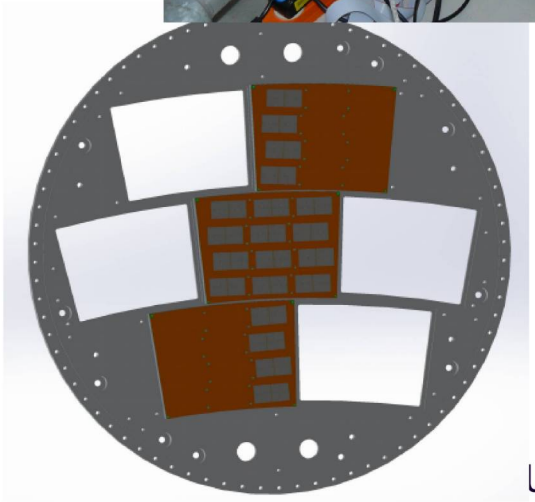


Setup for final 2015 test beam at LCTPC LP:

- 1 x 96 chip module (3 FECs)
- 2 x 32 chip module (1 FEC)

→ 160 chips ≈ 10.5 mio. channels

maximum readout speed: 5.2 frames/s



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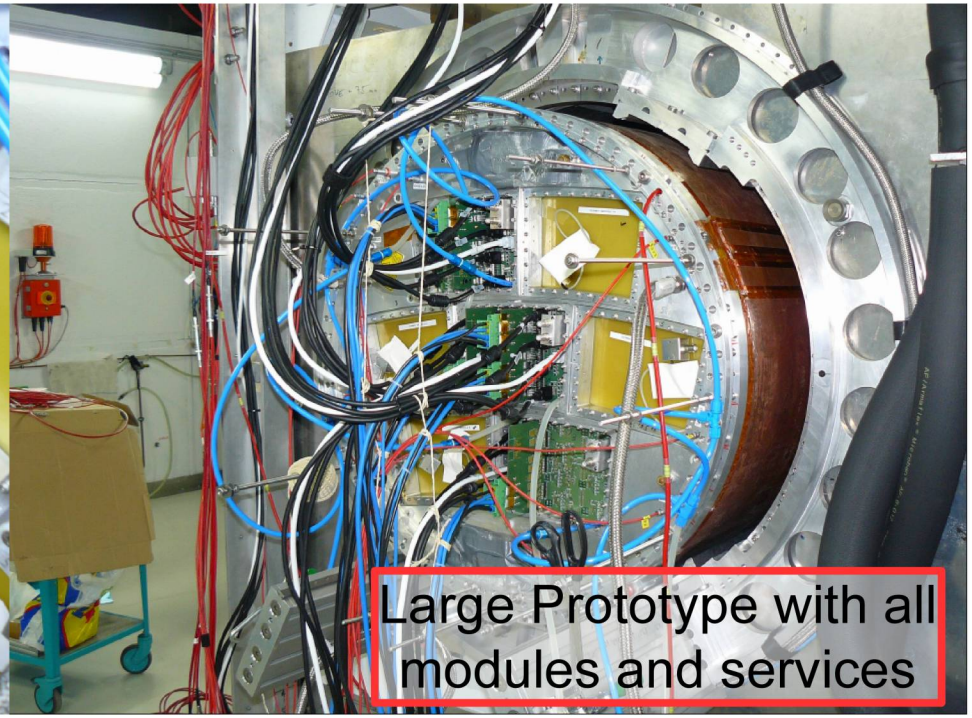
Test beam setup

Feasibility demonstration of the Pixel-TPC: March/April 2015



Services: Water cooling (blue pipes), power cables (black/blue), readout HDMI cables (black/white), temperature sensors (flex cables, not shown)

Excellent performance of readout system during entire test beam.

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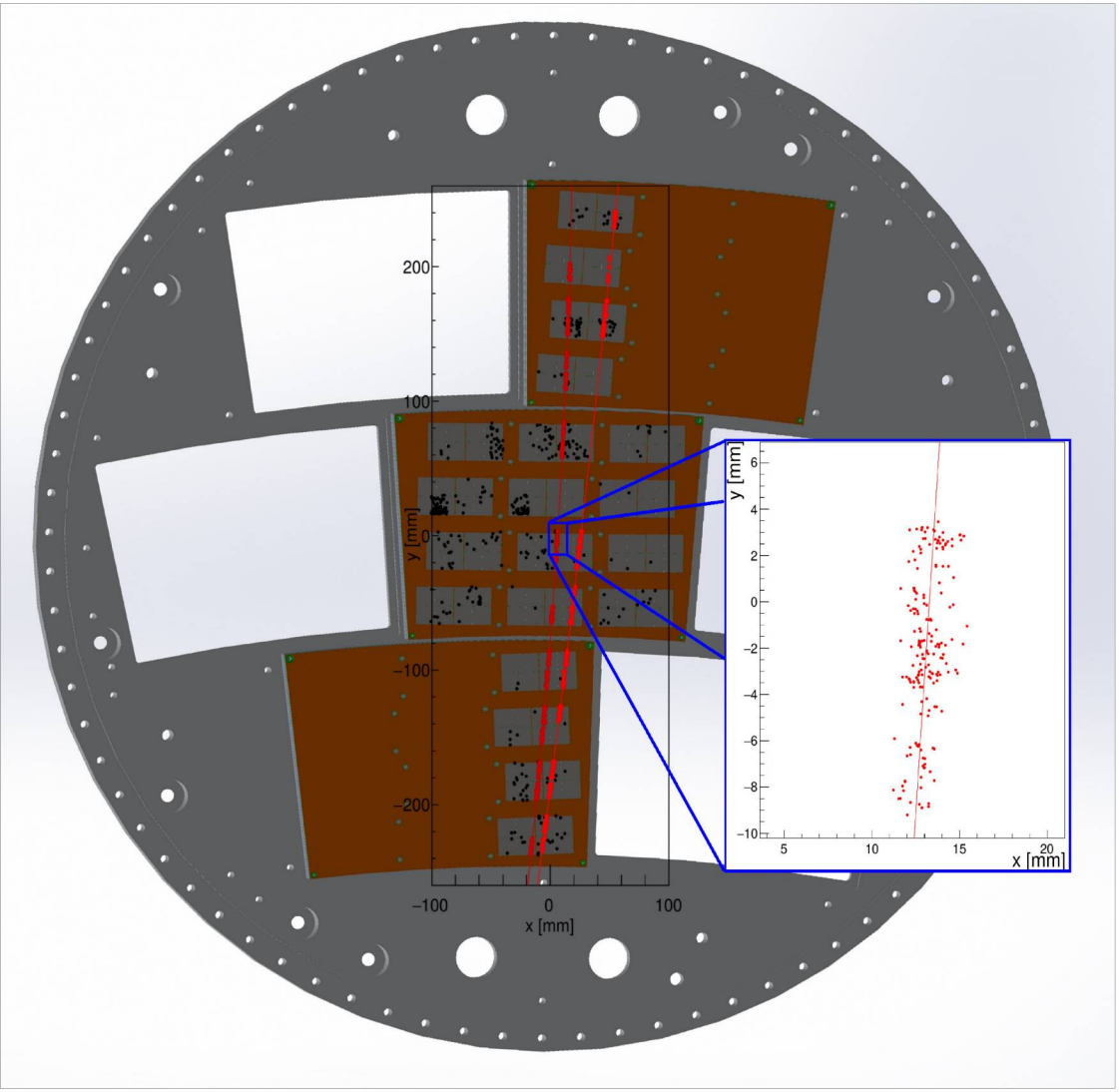
Test beam results

CAD drawing of endplate with reconstructed double track event



50 cm track length with about 3000 hits, each representing an electron from the primary ionisation.

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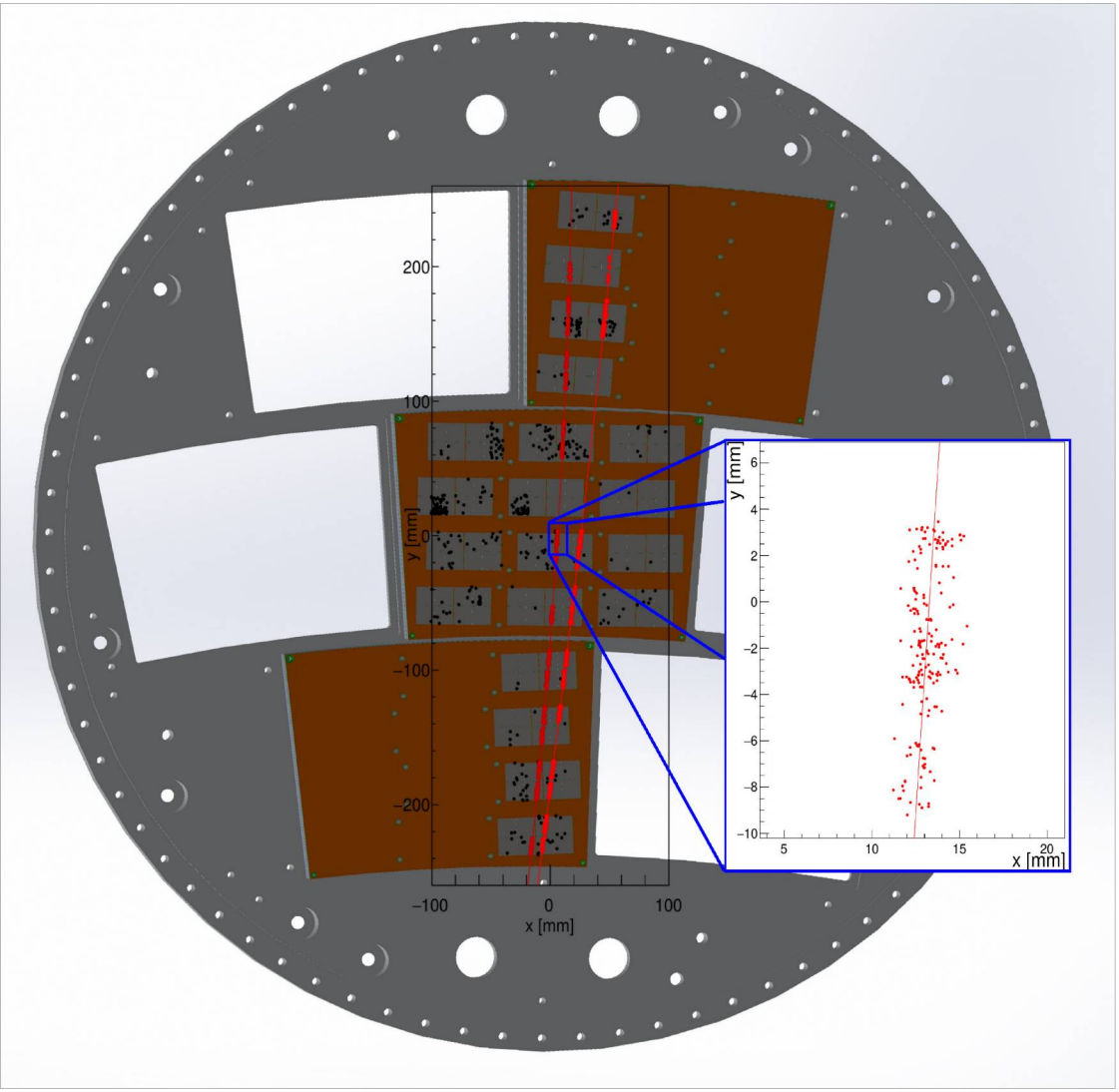

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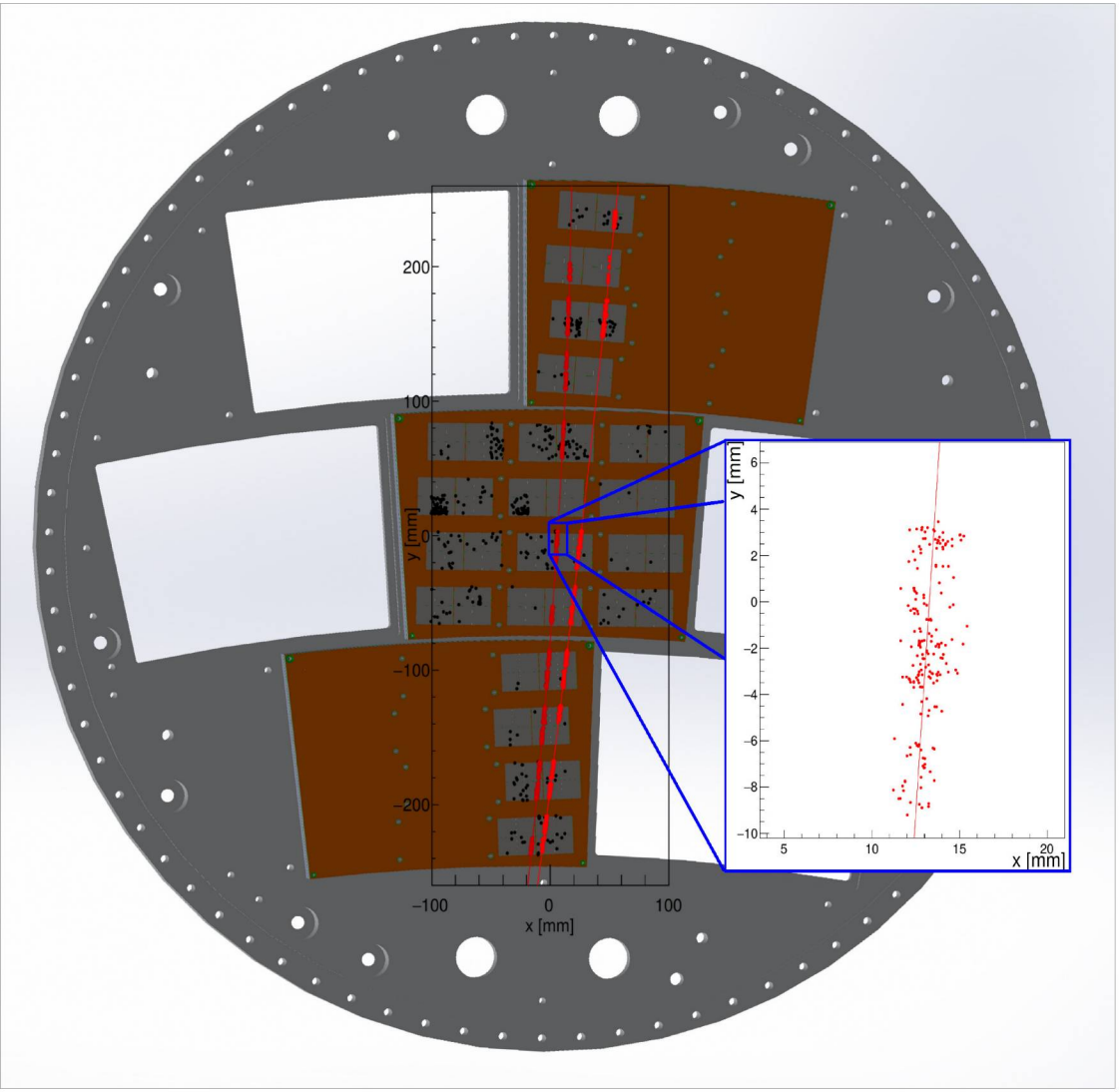

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→ preliminary analysis:

- Drift velocity
- Field distortions
- dE/dx resolution
- Single point resolution
- Track angular effect

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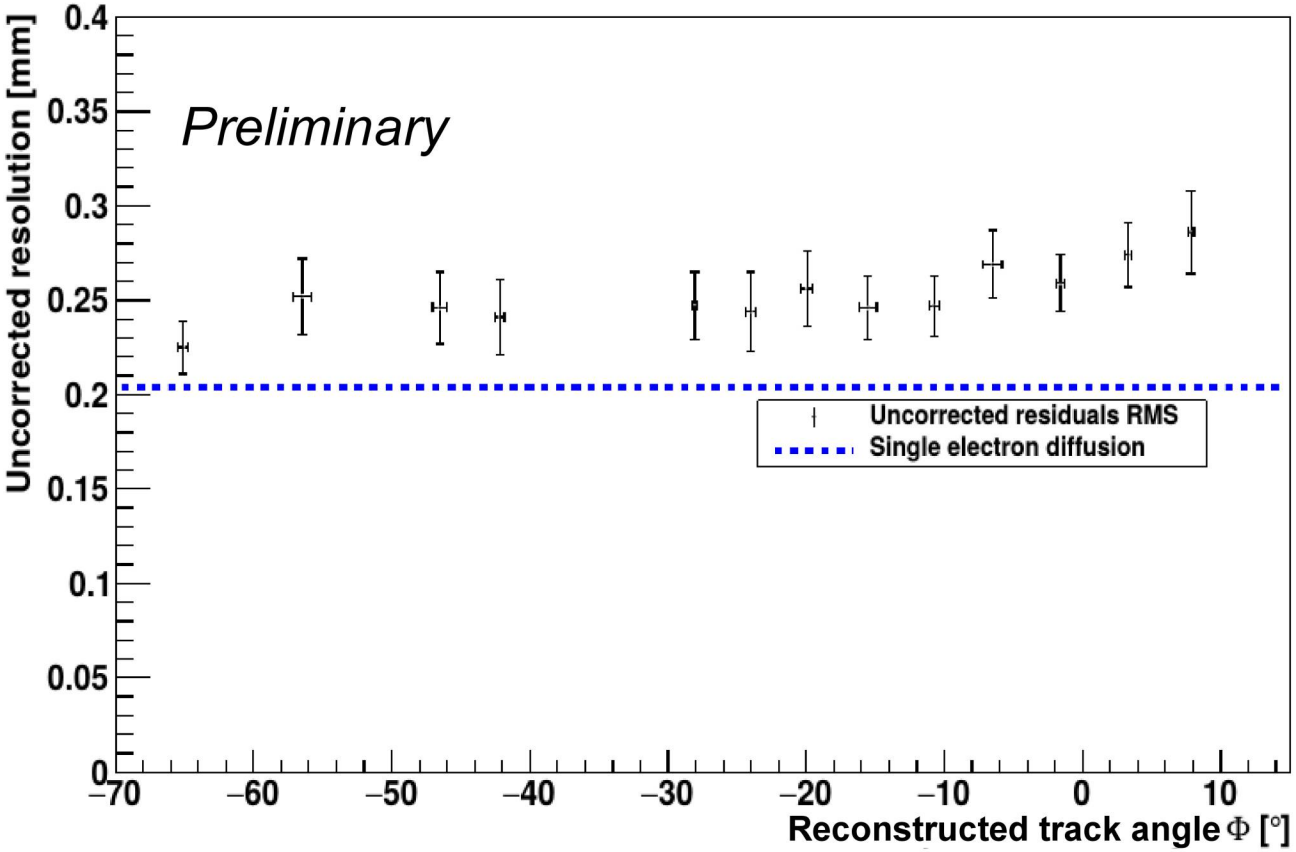
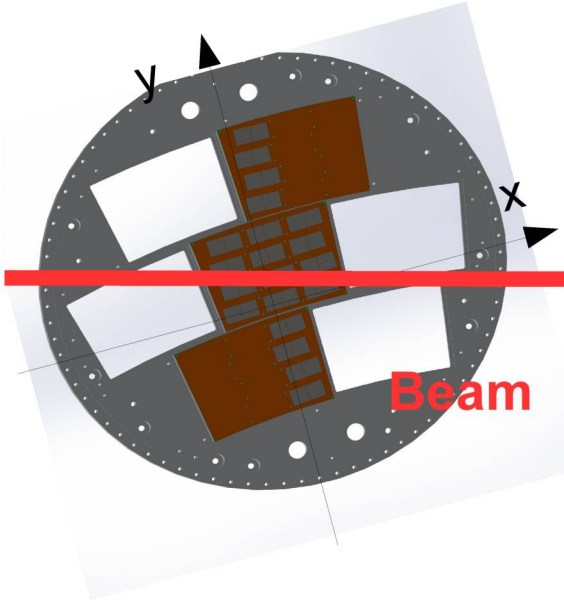
Test beam results

Exemplary result of preliminary analysis:

Single point resolution of the detector for different track angles with respect to the y-axis (= rotation of the endplate with respect to the beam-axis)





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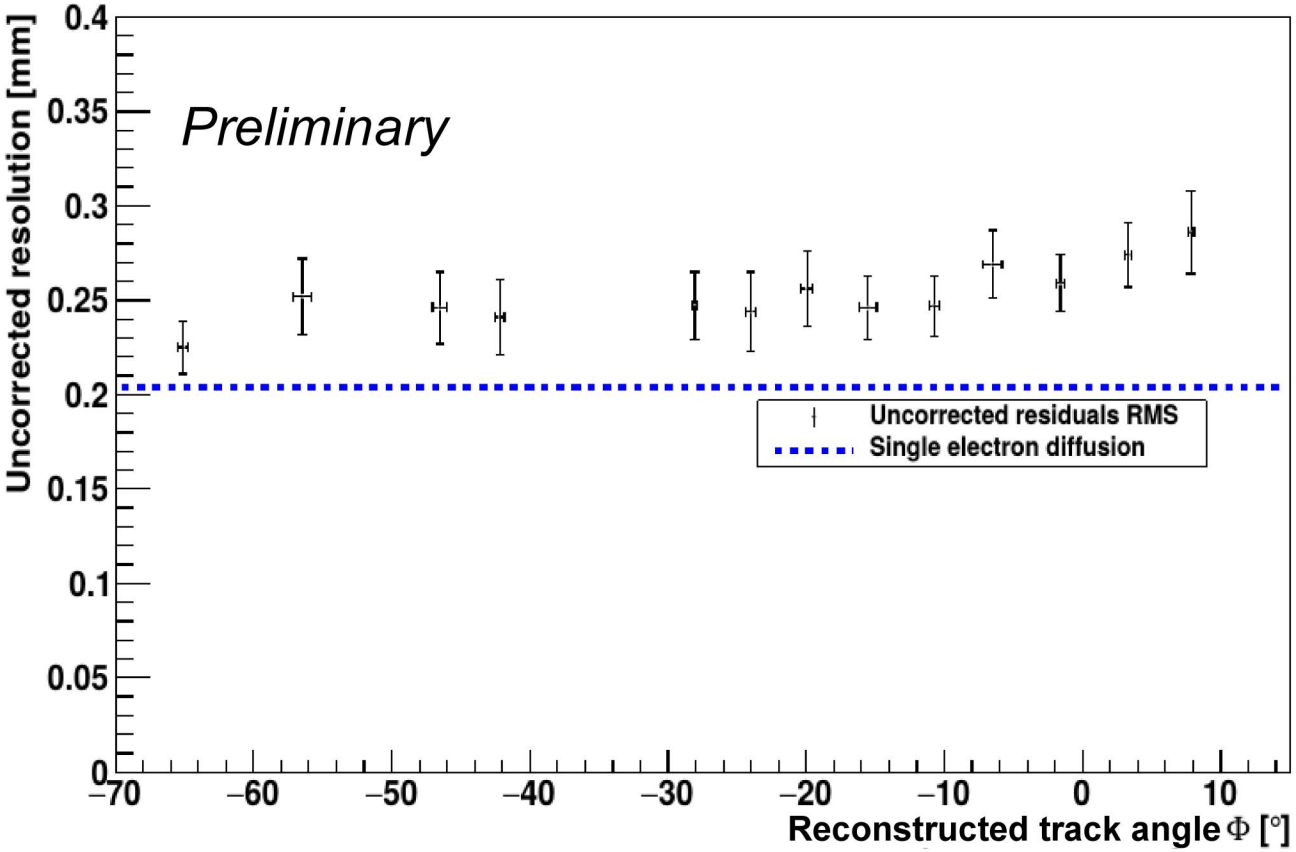

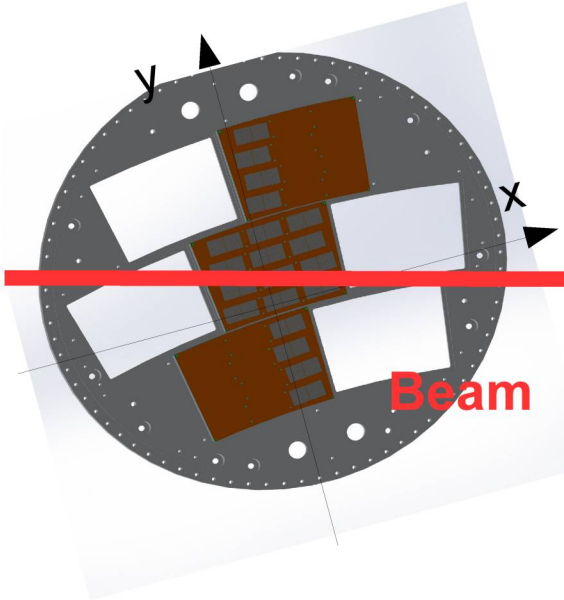

As expected for Pixel-TPC, no dependence was observed.

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Summary and Outlook

A Pixel-TPC includes many ASICs, requiring a large, scalable readout system.

- Timepix ASIC chosen for feasibility study
- Scalable Readout System (SRS) as basis for readout
  → Implementation of the Timepix chip in SRS

- Development of dedicated adapter and intermediate boards
- New FPGA firmware for the SRS FEC

- Readout system tested in laboratory and intermediate stage test beam
- Scalability of SRS used read out a large number of chips

- Final test beam in 2015: Feasibility of Pixel-TPC demonstrated

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