ALICE ITS Upgrade
Pixel Chip Status

LHCC Detector Upgrade Review

CERN, 03 March 2015

L. Musa - CERN

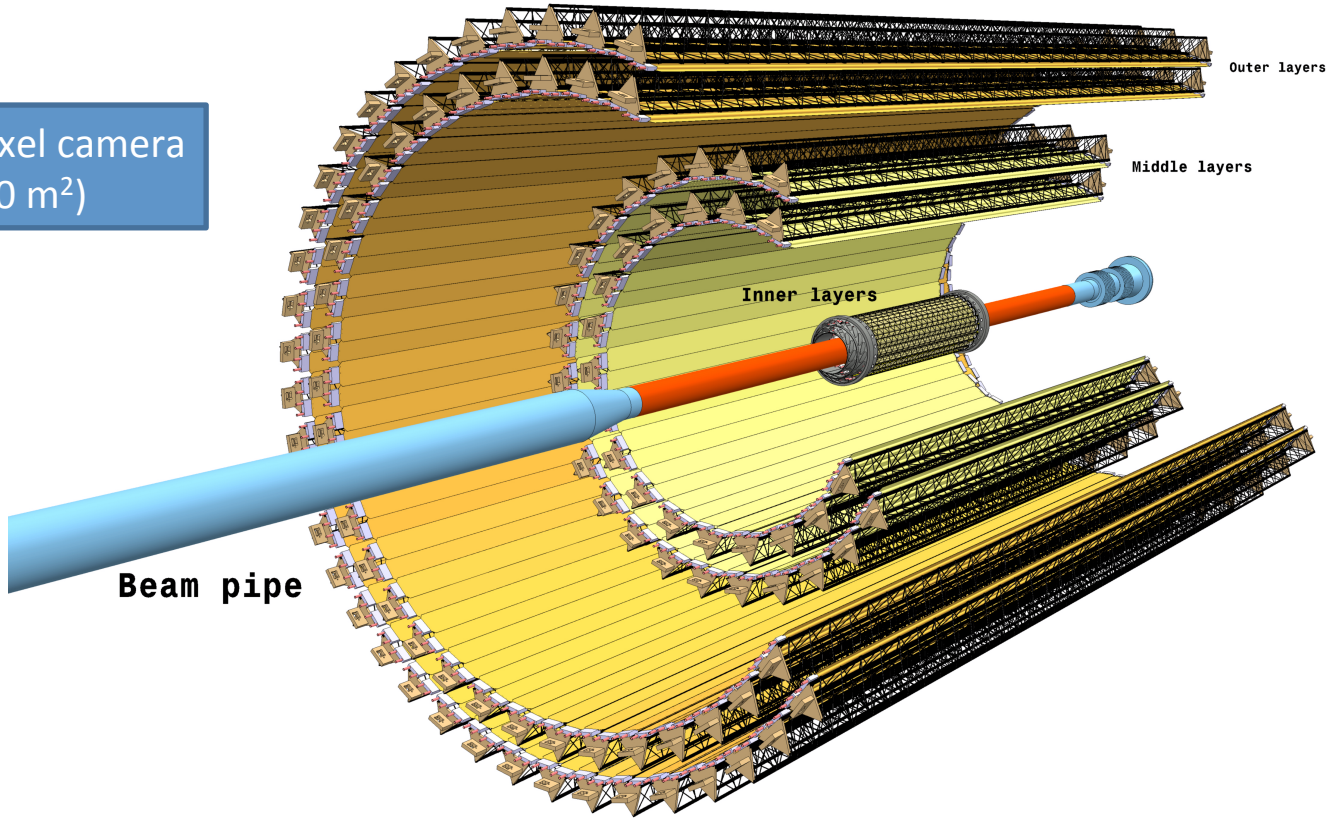
ALICE ITS Upgrade – Pixel Chip Status

OUTLINE

- Pixel Chip Requirements
- Two alternative architectures: ALPIDE and MISTRAL
- ALPIDE
  - Design roadmap
  - p-ALPIDE-1 (full-scale prototype) results
- MISTRAL-O
  - Design roadmap
  - MISTRAL FSBB (full-scale building block) results
- Conclusions

New ITS Layout

12.5 G-pixel camera
(~10 m^2)



7-layer barrel geometry based on MAPS

r coverage: 23 – 400 mm

η coverage: $|\eta| \leq 1.22$
for tracks from 90% most luminous region

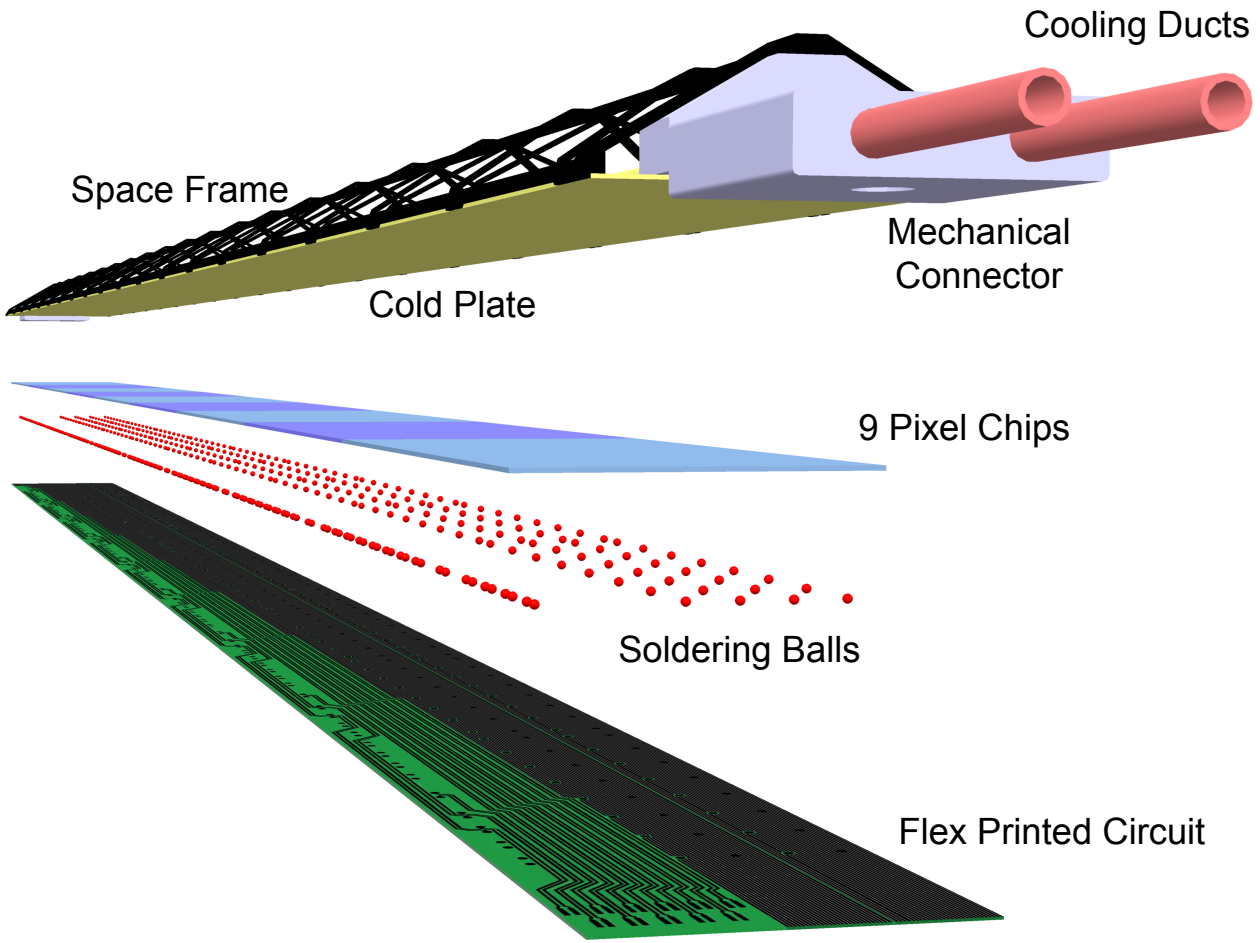
3 Inner Barrel layers (**IB**)

4 Outer Barrel layers (**OB**)

Material /layer : 0.3% X_0 (IB), 1% X_0 (OB)

Integration of chip into detector stave

Inner Barrel Stave



PIXEL Chip – General Requirements

Parameter	Inner Barrel	Outer Barrel
Max silicon thickness	50 μm	
spatial resolution	5 μm	10 μm
chip dimensions	15 mm x 30 mm	
Max power density	300 mW/cm^2	100 mW/cm^2
Max event time resolution	< 30 μs	
Min detection efficiency	> 99%	
Max fake hit rate	< 10^{-5} per readout frame	
TID radiation hardness (*)	700 krad (TDR) 2700 krad (rev Dec 14)	10 krad (TDR) 100 krad (rev Dec 14)
NIEL radiation hardness (*)	10^{13} 1MeV n_{eq}/cm^2 (TDR) 1.7x10^{13} 1MeV n_{eq}/cm^2 (rev)	3x10^{11} 1MeV n_{eq}/cm^2 (TDR) 10^{12} 1MeV n_{eq} / cm^2 (rev)

(*) 10 x radiation load integrated over approved programme (~ 6 years of operation)

ITS Pixel Chip – technology choice

Genesis

- Owing to the intensive R&D work on CMOS pixel sensors carried out by IPHC (… and the vision and support of STAR) over the last 15 years

☛ First monolithic pixel detector in a HEP experiment (STAR HFT detector)

- Based on AMS 0.35μm twin-well CMOS process
- Readout speed and radiation hardness not adequate for ALICE ITS upgrade

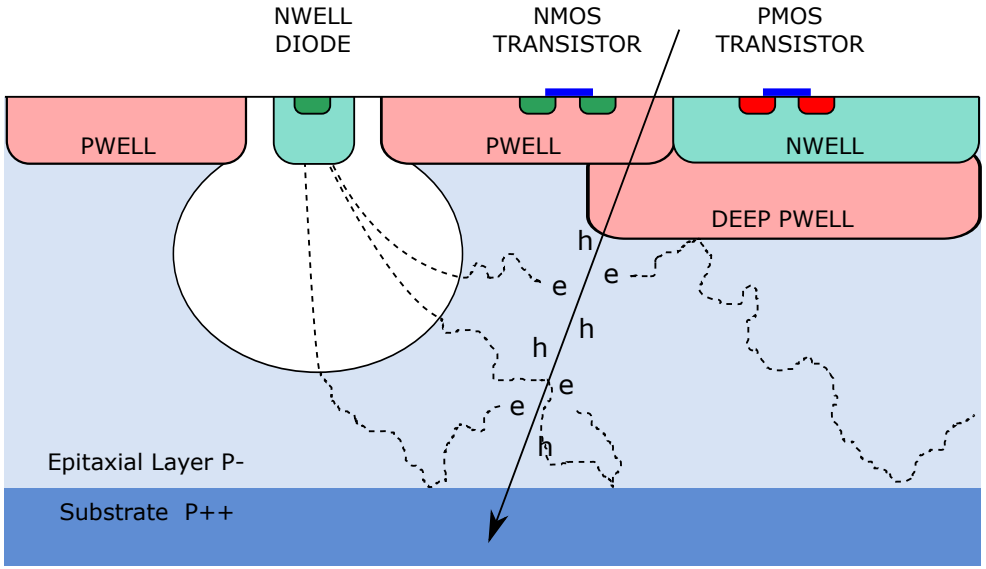
The industrial development of CMOS imaging sensors (e.g. TowerJazz CIS) + R&D work from RAL and IPHC

☛ development of first exploratory pixel chips based on a quadruple-well 0.18mm CMOS Imaging Sensor (CIS) process

☛ based on the R&D work of IPHC in 2011 and 2012, ALICE decided to adopt MAPS as baseline technology for the ITS upgrade (LoI)

ITS Pixel Chip – technology choice

CMOS Pixel Sensor using TowerJazz 0.18μm CMOS Imaging Process



Tower Jazz 0.18 μm CMOS

- feature size 180 nm
- metal layers 6

➔ Suited for high-density, low-power

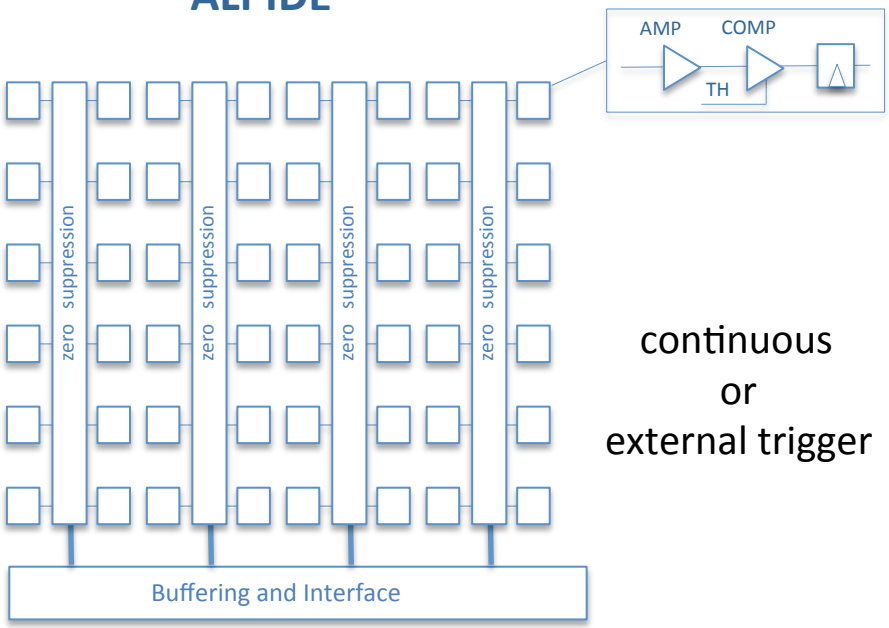
- Gate oxide 3nm

➔ Circuit rad-tolerant

- High-resistivity (> 1kΩ cm) p-type epitaxial layer (20μm - 40μm thick) on p-type substrate
- Small n-well diode (2-3 μm diameter), ~100 times smaller than pixel => low capacitance
- Application of (moderate) reverse bias voltage to substrate can be used to increase depletion zone around NWELL collection diode
- Quadruple well process: deep PWELL shields NWELL of PMOS transistors, allowing for full CMOS circuitry within active area

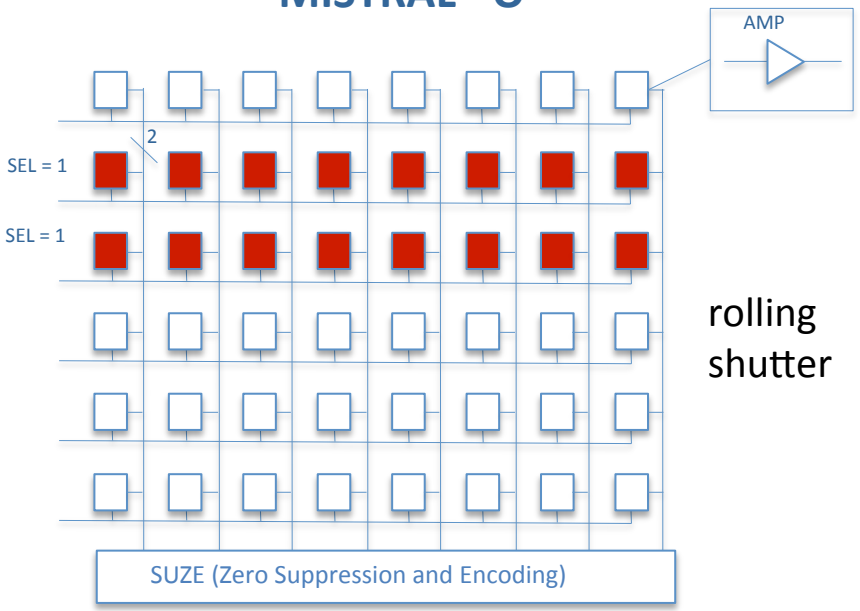
ITS Pixel Chip – two architectures

ALPIDE



continuous
or
external trigger

MISTRAL - O



rolling
shutter

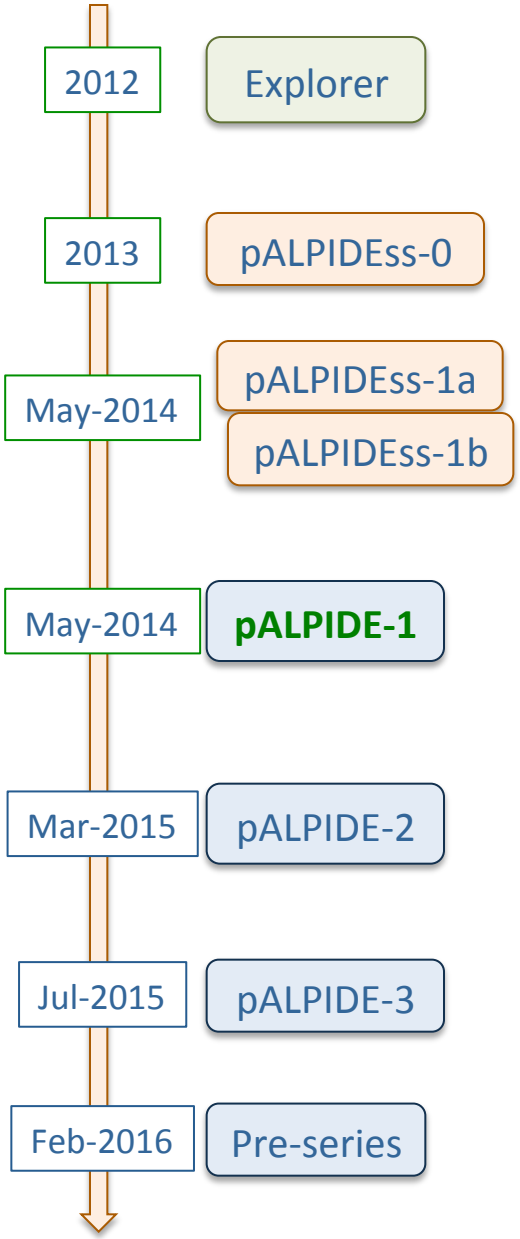
Pixel pitch	28μm x 28μm
Event time resolution	~2μs
Power consumption	39mW/cm^2
Dead area	1.1 mm x 30mm

Pixel pitch	36μm x 64μm
Event time resolution	~20μs
Power consumption$^{(*)}$	97mW/cm^2
Dead area	1.7 mm x 30mm

ALPIDE and MISTRAL-O have same dimensions (15mm x 30mm), identical physical and electrical interfaces: position of interface pads, electrical signaling, protocol

$^{(*)}$ might further reduce to 73mW/cm^2

ALPIDE Development



- 20μm x 20μm and 30μm x 30μm pixels with analogue readout
- pixel geometry, starting material, sensitivity to radiation

- Matrix with 64 columns x 512 rows
- 22μm x 22μm pixels with in-pixel discrimination and buffering
- zero suppression within pixel matrix (standard cells)
- Different flavours of front-end circuit

- **Full-scale prototype:** 1024 x 512, 4 sectors with different pixels
- Final pixel pitch: 28μm x 28μm
- Interface pads over matrix
- 1 register/pixel, zero-suppression (full-custom), no final interface

- Optimization of some circuit blocks
- Final interface: allows integration into ITS and MFT modules
- NO high-speed output link (1.2 Gbit/sec replaced by a 40Mb/s)

- All final features
- 3 registers/pixel, standard-cell based priority encoder
- Final interface, including high-speed output link

pALPIDE-1 – Main Design Features

ALICE

ALPIDE Full Scale prototype

- Dimensions: 30mm x 15 mm
- Pixel Matrix: 1024 cols x 512 rows
- Pixel pitch: 28μm x 28μm
- Peaking time: 2μs
- Pulse length: 10-20μs
- In-pixel discriminator + 1 register
- Power consumption: < 40mW/cm^2
- 4 sectors with different pixels

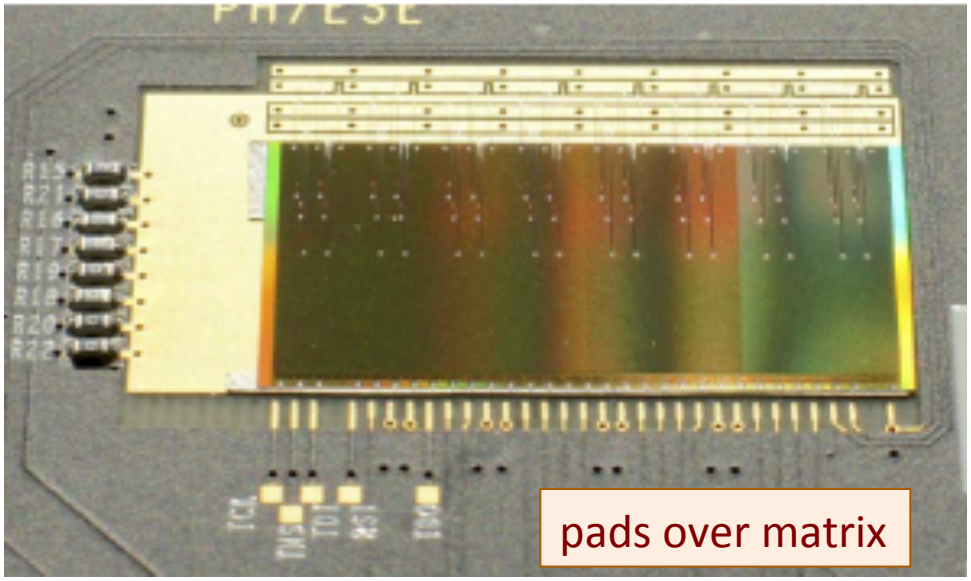
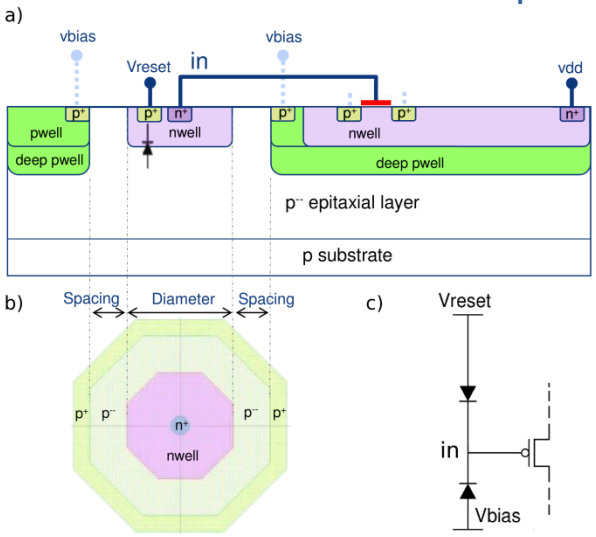


Figure: picture of pALPIDE-1



Sector	nwell diameter	spacing	pwell opening	reset
0	2μm	1μm	4μm	PMOS
1	2μm	2μm	6μm	PMOS
2	2μm	2μm	6μm	Diode
3	2μm	4μm	10μm	PMOS

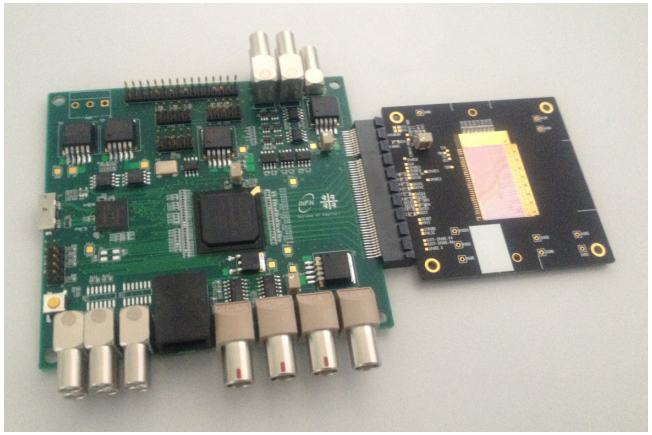
pALPIDE-1 Characterization

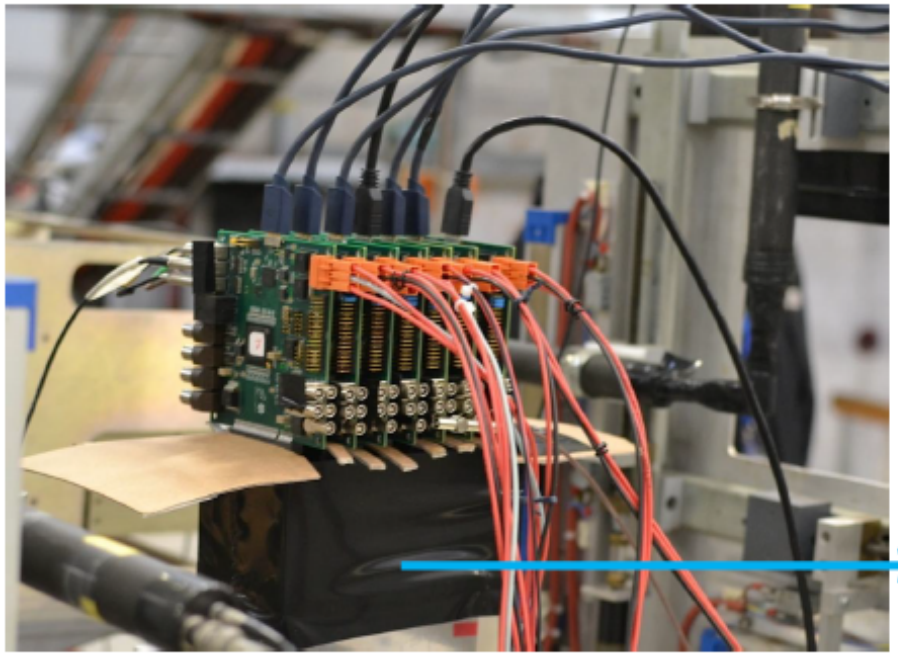
Intensive test beam campaign

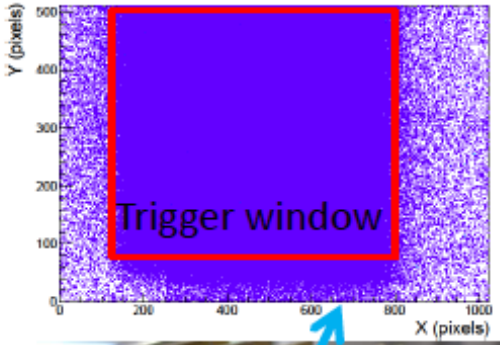
- PS: 5-7 Gev π^-
- SPS: 120 Gev π^-
- PAL (Korea): 60 MeV e^-
- BTF (Frascati): 450 MeV e^-
- DESY: 5.8 Gev e^+

Scan of main parameters ➔ ~ 200 settings

7-plane telescope based on pALPIDE-1 chip



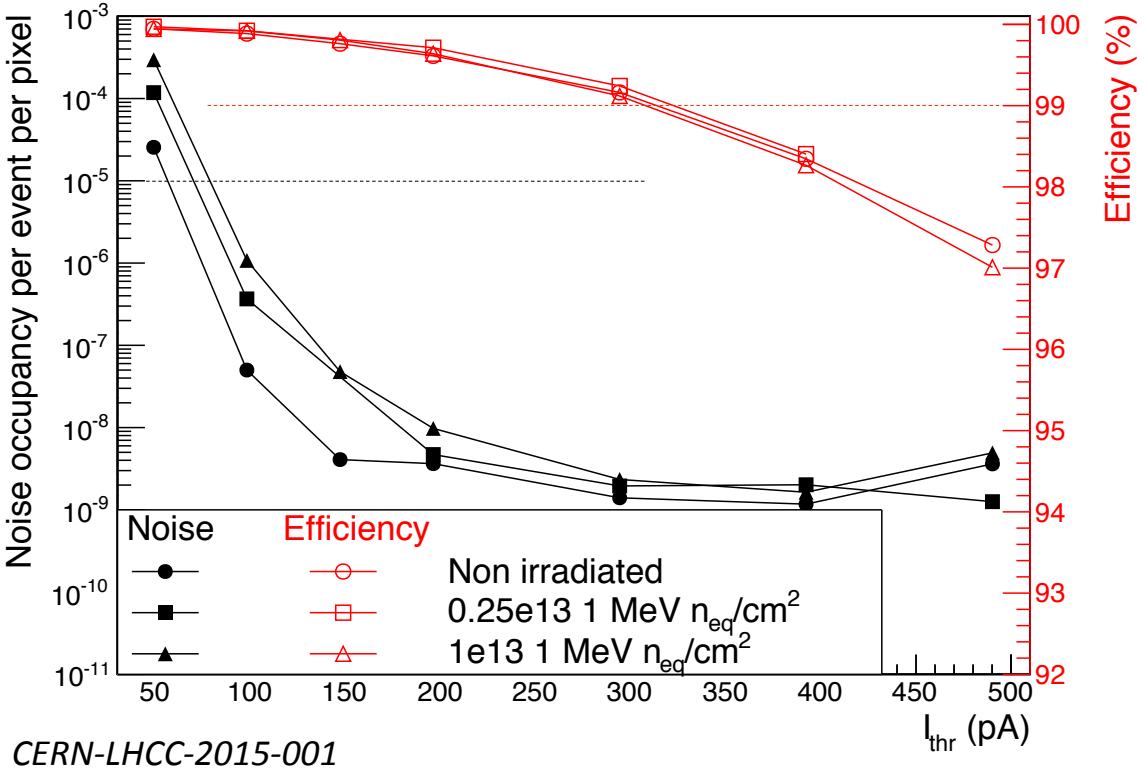




hit map

pALPIDE-1 – PS test beam (Sep 2014)

Efficiency and fake hit rate



MFT TDR, CERN-LHCC-2015-001

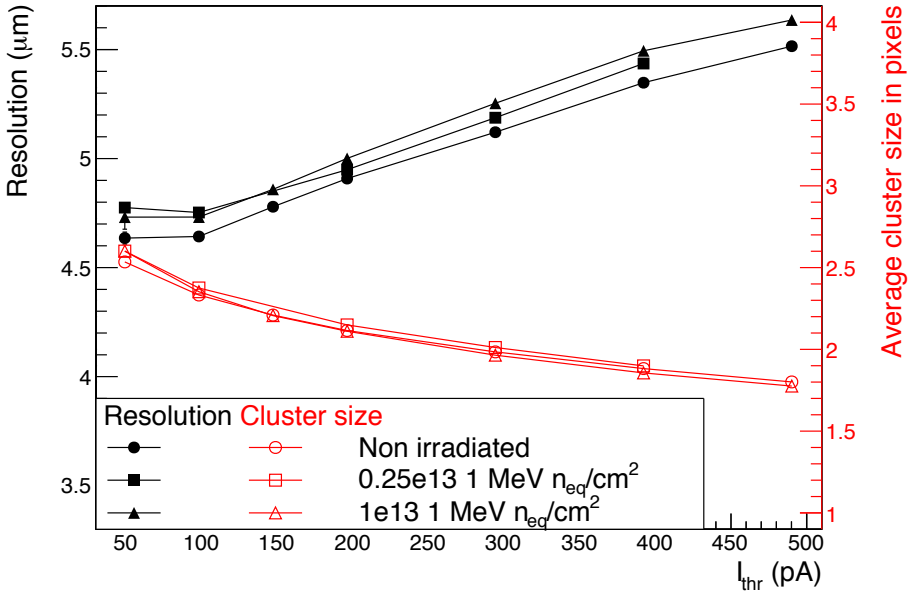
50 pA ➔ ~80 e
500 pA ➔ ~180 e

$\lambda_{fake} << 10^{-5}$ / event/pixel @ $\varepsilon_{det} > 99\%$ ➡ very large margin over design requirements

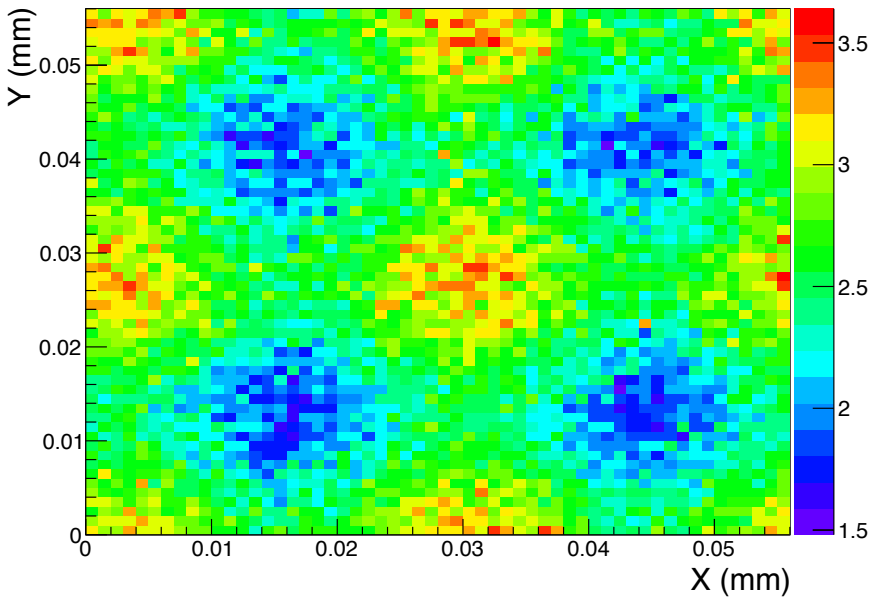
- Measurements at PS: 5 – 7 GeV π^- September 2014
- Results refer to 50 μm thick chips: non irradiated and irradiated with neutrons 0.25×10^{13} and 10^{13} 1MeV n_{eq} / cm^2

pALPIDE-1 – PS test beam (Sep 2014)

Spatial resolution



Cluster size vs. position within pixel



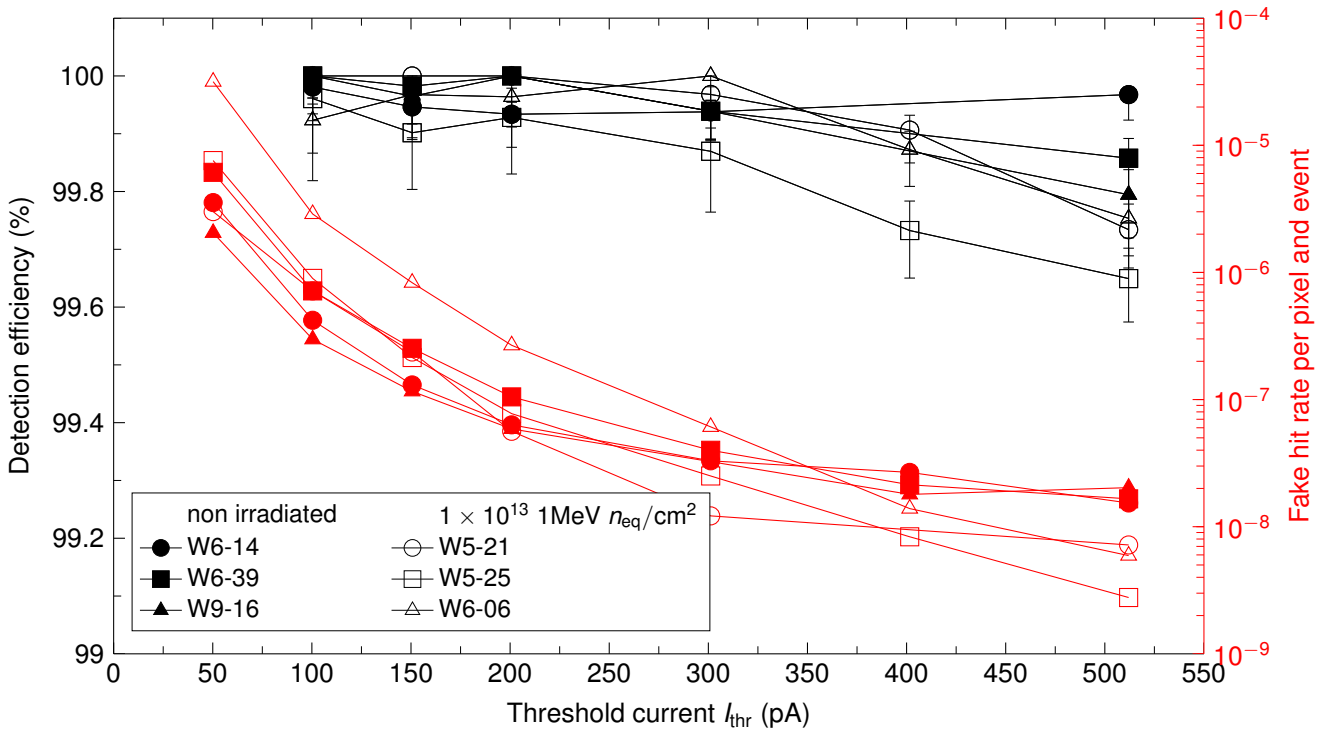
MFT TDR, CERN-LHCC-2015-001

$\sigma_{det} < 5\ \mu m$ is achieved with sufficient margin of operation

- Measurements at PS: 5 – 7 GeV π^- September 2014
- Results refer to 50 μm thick chips: non irradiated and irradiated with neutrons 0.25 x 10^{13} and 10^{13} 1MeV n_{eq} / cm^2

pALPIDE-1 – PS test beam (Dec 2014)

Efficiency and fake hit rate



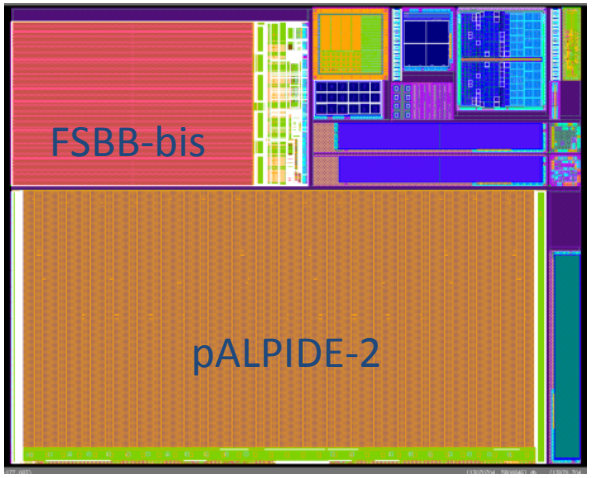
Improved test-beam data analysis

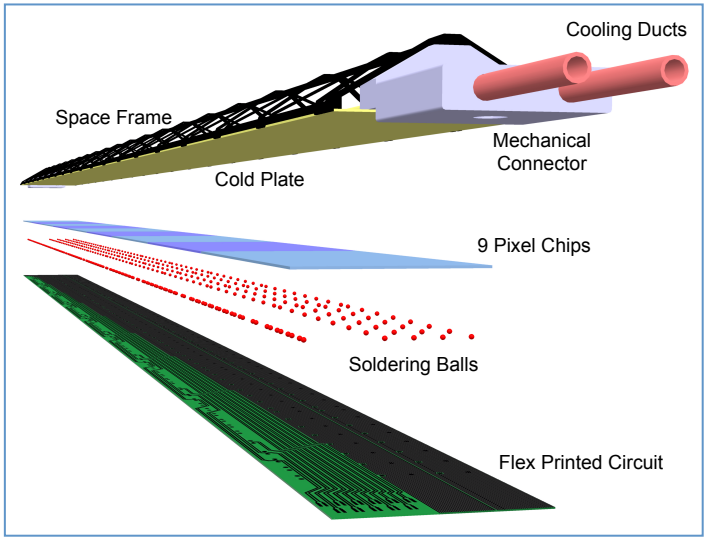
- Measurements at PS: 5 – 7 GeV π^- December 2014
- Results refer to 50 μm thick chips: 3 non irradiated and 3 irradiated with neutrons

ALPIDE finalization

p-ALPIDE-2: 2nd full-scale prototype

- Optimization of some circuit blocks
- NO high-speed output link (1.2 Gbit/sec replaced by a 40Mb/s)
- Full Integration in IB and OB Module: main focus in 2015
- Delivery: mid March





p-ALPIDE-3: 3rd full-scale prototype

- Contains all final elements
- Submission: April '15 Delivery: July '15

p-ALPIDE-4: pre-series production

- Submission Dec '15

MISTRAL Development

2011

Study of diode and in-pixel amplification

- MIMOSA-32, MIMOSA-32ter
- MIMOSA-32FEE, MIMOSA-32N
- MIMOSA-34 (study of large pixels, up to 22 x 66 μm^2)

2013

MISTRAL Readout Architecture

- MIMOSA-22THRa, MIMOSA-22THRb

May-2014

MISTRAL FSBB-M0

- About 1/3 of final sensor based on small pixels (22x33μm^2)
- No pads over matrix
- Power consumption too high for Outer Barrel

Sep-2014

MISTRAL Readout Architecture + large pixels (small matrix)

- MIMOSA-22THR(5-9)

Sep-2015

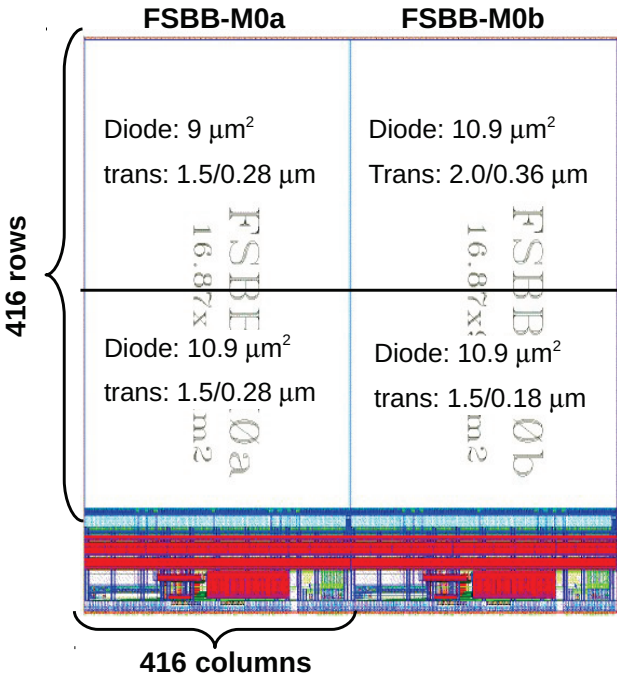
MISTRAL-O

- 4 FSBB units with 208 x 208 large pixels of 36 x 64μm^2
- Power consumption ~ 100mW/cm2
- Event time resolution (integration time) 20μs
- Pin-to-pin compatible with ALPIDE + common interface

MISTRAL FSBB-M0

FSBB Main Features

- About 1/3 of complete sensor (approx. 9mm x 17mm)
- Pixel Matrix: 416 Columns x 416 Rows
- Staggered Pixel: 22μm x 33μm (final chip 36μm x 64μm)
- In-pixel pre-amplification and clamping (6 metals)
- Double row-readout at 160MHz
- Integration time: 40μs (final chip 20μs)
- 2 versions (FSBB-M0 a & b): only results for M0-a will be shown



NB: the FSBB is not opimized in some respects (pixel dimensions, speed, power consumption, pads over matrix, ...)

Currently MISTRAL-O is being optimized for use in the outer layers:

- less need for spatial resolution: ~10μm
- more stringent power consumption limit: < 100mW/cm²

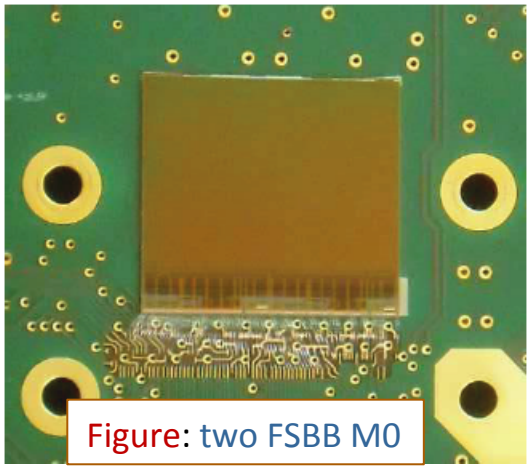
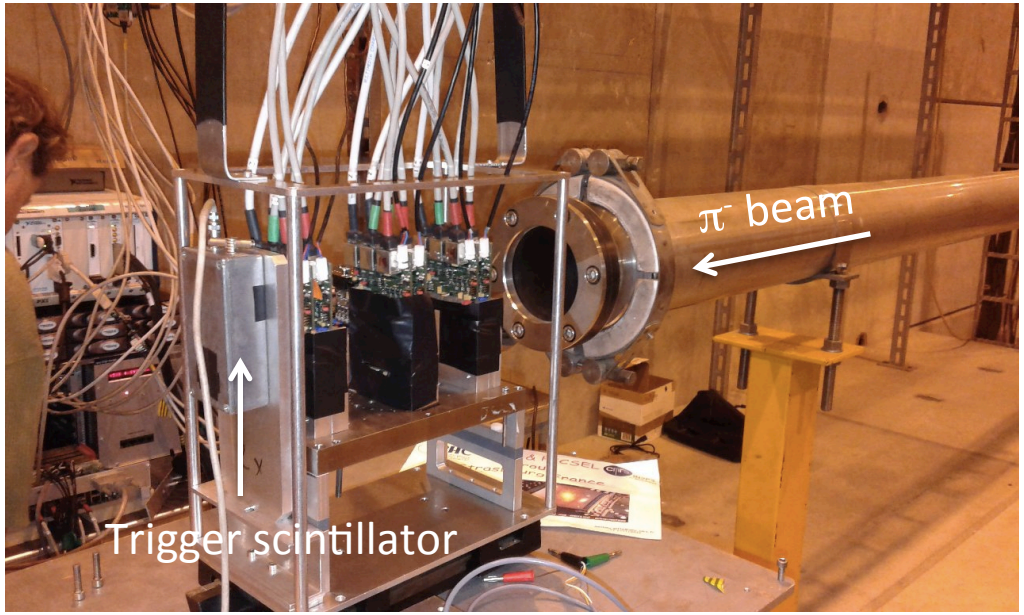
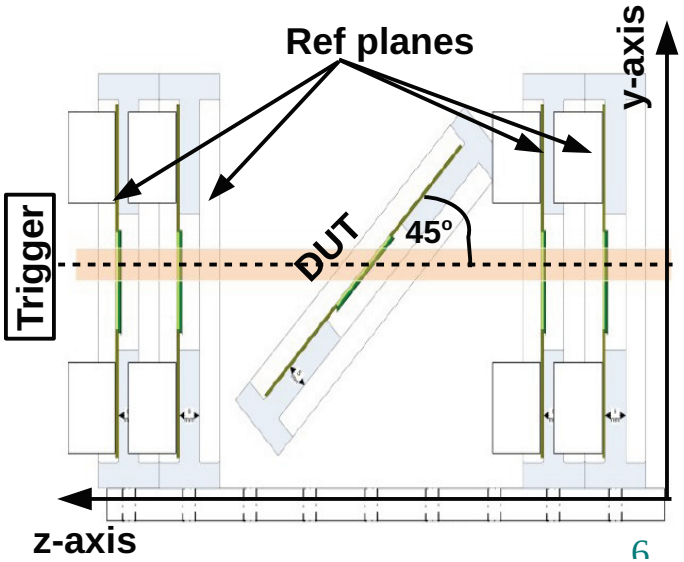


Figure: two FSBB M0

MISTRAL FSBB-M0 – SPS test beam (Oct 2014)





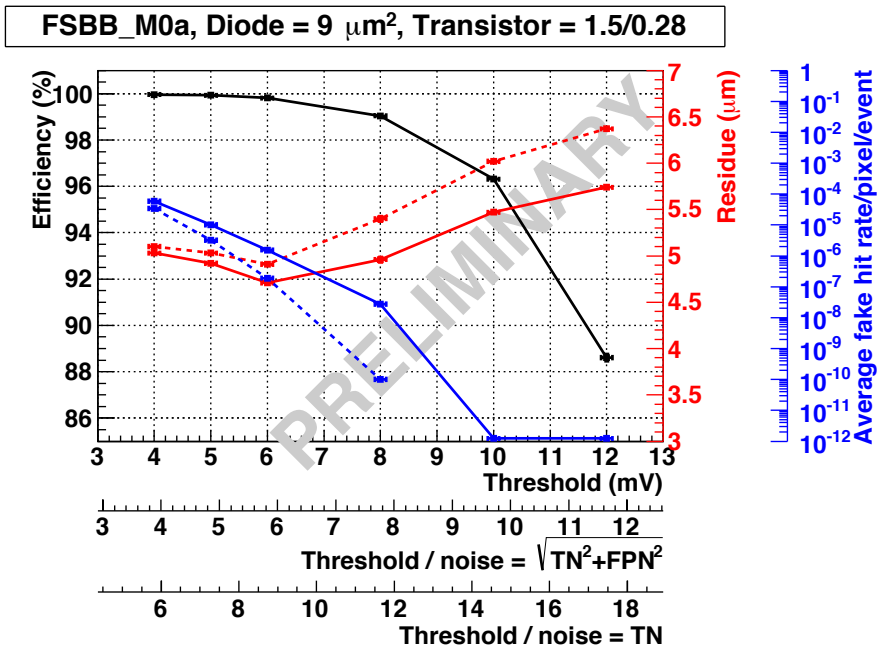
Beam conditions

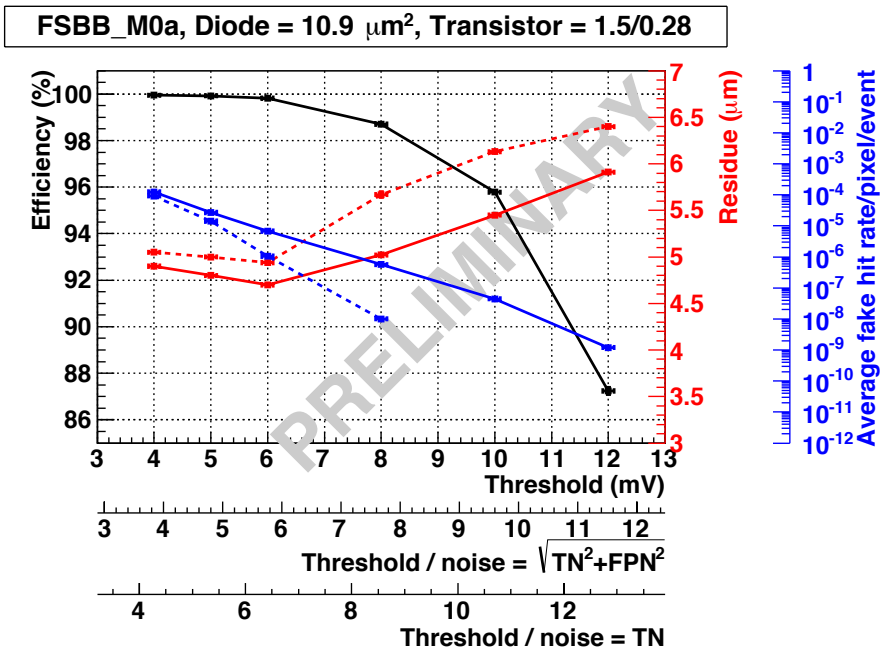
- SPS H6A area, 120 Gev π^-
- Particle flux: trigger rate in the range 2.5 to 100 kHz / 5x10 mm^2

Device and operational conditions

- 6 FSBB-M0a thinned to 50μm
- All measurements performed at T_{op} = 30 °C

MISTRAL FSBB-M0 – detection performance





Diode size (μm²)	$\varepsilon_{det} \geq 99.8\%$	$\varepsilon_{det} \geq 99.5\%$	$\varepsilon_{det} \geq 99.0\%$	$\lambda_{fake}^{(*)} \leq 10^{-5}$
11	Thr ≤ 6.0 mV	Thr ≤ 6.5 mV	Thr ≤ 8.0 mV	Thr ≥ 6.0 mV
9	Thr ≤ 6.0 mV	Thr ≤ 7.0 mV	Thr ≤ 8.0 mV	Thr ≥ 5.0 mV

(*)
- Fake rate drops by O(10) masking 20 noisiest pixels.
- Final chip includes masking feature

Conclusions

ALPIDE

- Full-scale prototype (p-ALPIDE-1) includes most of final features
- Extensive characterization shows large margin over design requirements
- Integration of chip into detector modules starts in Apr ’15 till Dec ‘15
- Pre-series production starts Dec ’15
- ☛ Project baseline … however full validation will take till end of 2015

MISTRAL-O

- Opimized for Outer Barrel layers
- MISTRAL FSBB-M0 (small pixel pitch) shows also very good performance
- Submission of full-scale prototype with all final features: July ’15
- Integration into detector modules starts Oct ’15

The full pin-to-pin compatibility allows switching from ALPIDE to MISTRAL-O with minimum overhead on production and test plans …

… implication of reduced spatial resolution for the IB need to be studied but expected to be small

SPARES

MISTRAL FSBB-M0 – other measurements

Spatial resolution

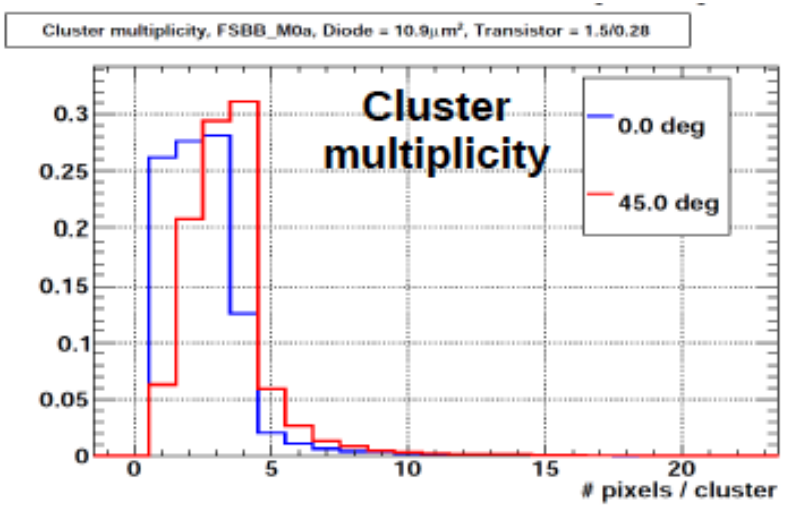
- Track reconstruction using all telescope planes but the device under test (DUT)
- Residual (DUT): $\sigma_{res} \approx (4.7 \pm 0.1)$ μm (U) & (4.9 ± 0.1) μm (V) at 6mV for both diodes
- Expected Resolution (removing telescope tracking error): $\sigma_{sp} \approx 4.5$ μm

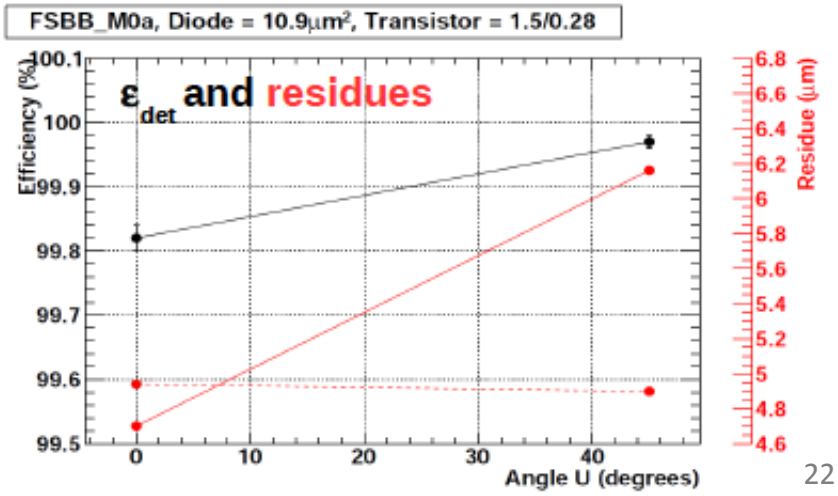
NOTE: FSBB pitch 22μm x 33μm MISTRAL-O pitch 36μm x 64μm

Sensitivity to trigger rate

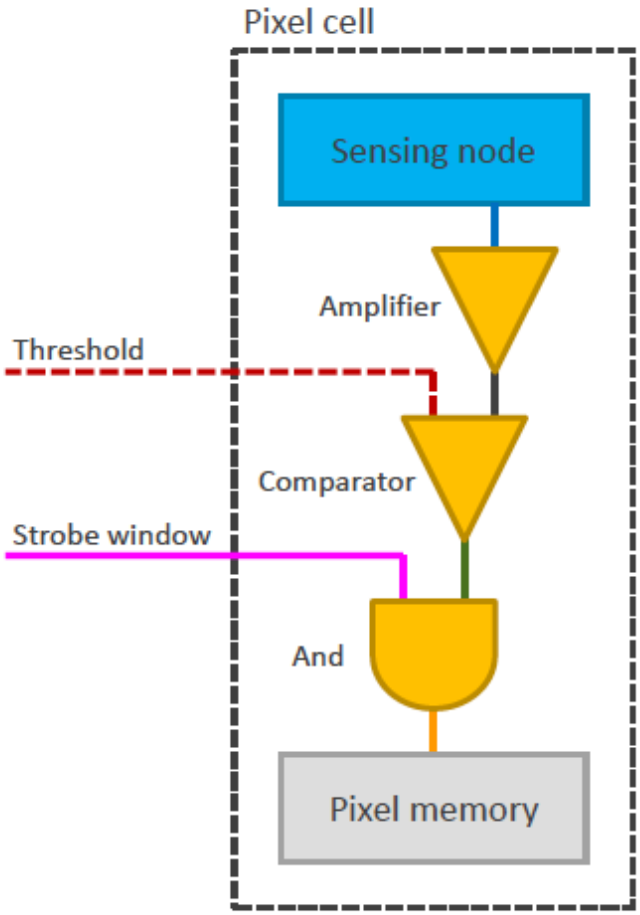
- ε_{det}, λ_{fake}, σ_{sp} are not sensitive to trigger rate (measured in the range 25-100 kHz)

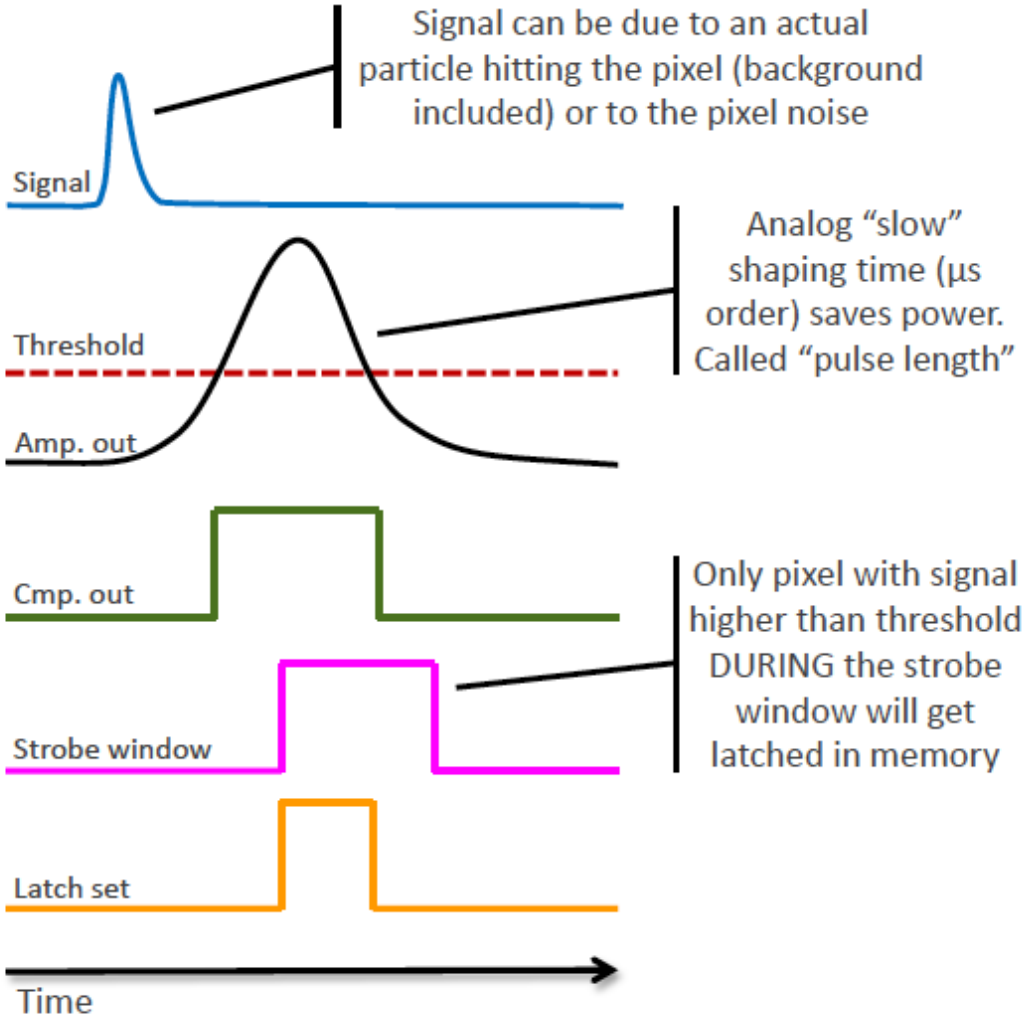
Detection performance at high incidence angles





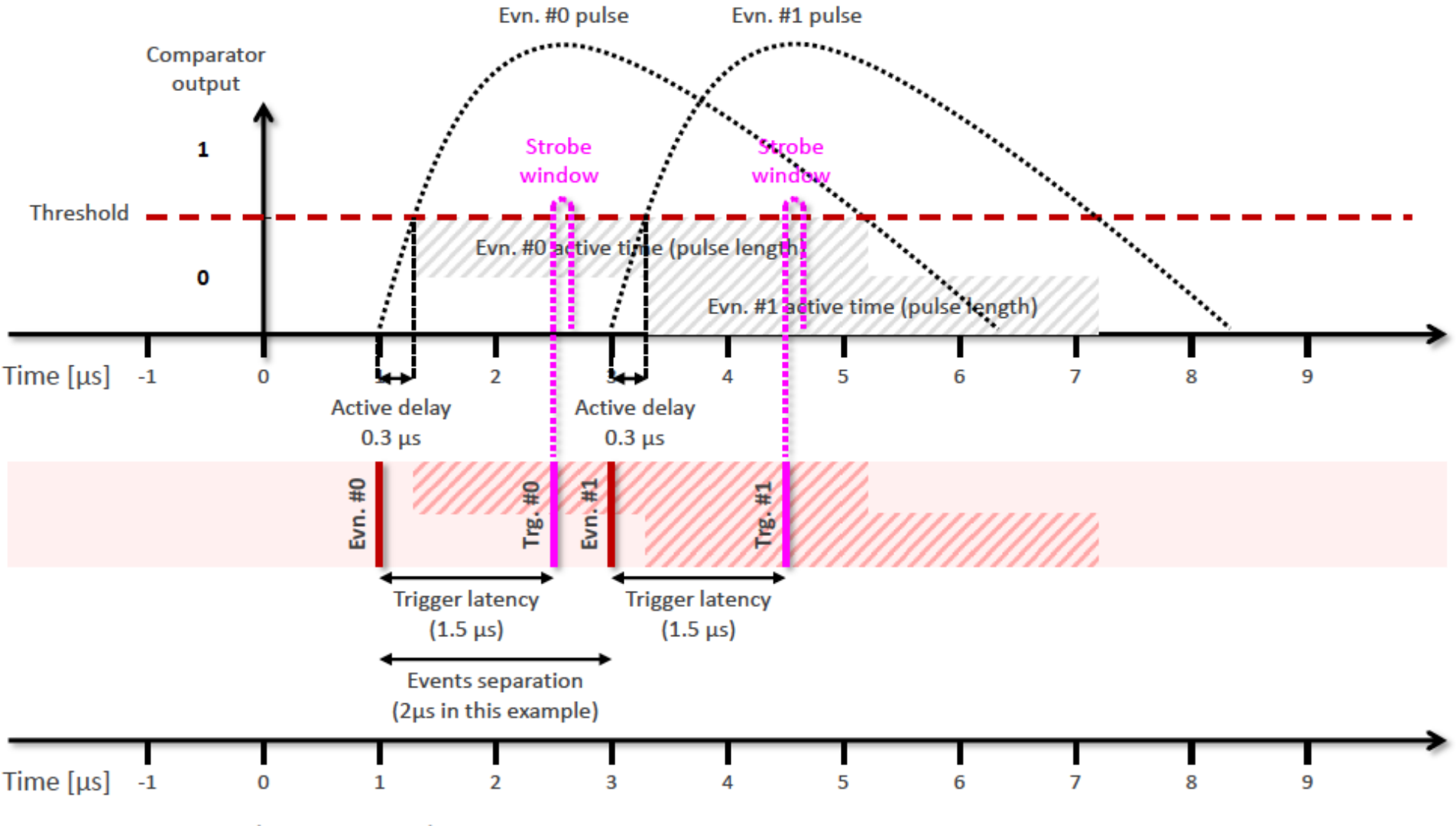
ALPIDE – Timing (1/3)



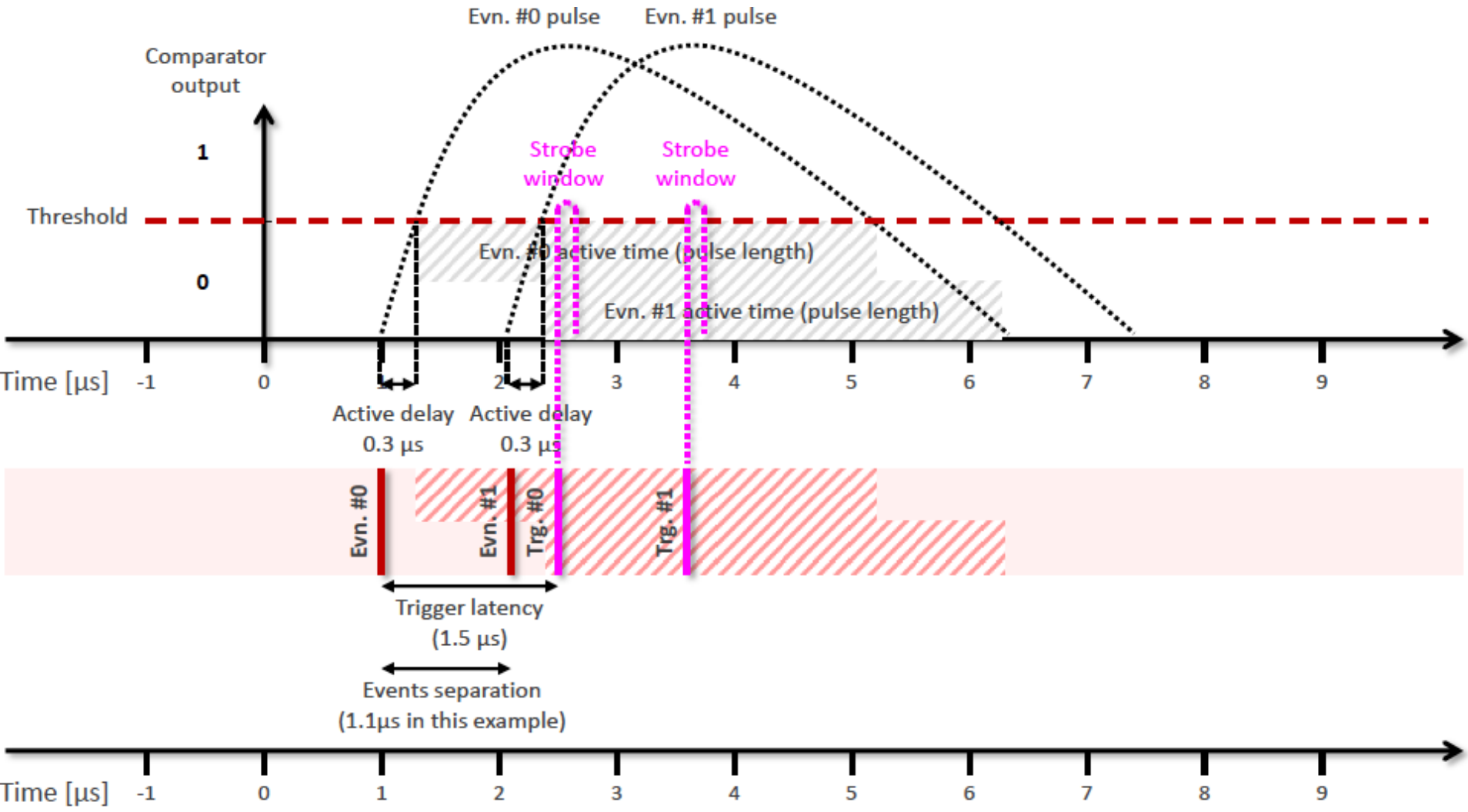


Bottom line: whichever signal high enough to trigger the comparator during the strobe windows is saved. Due to the analog shaping time, this means signals generated up to a certain time before the strobe window will be saved as well.

ALPIDE – Timing (2/3)

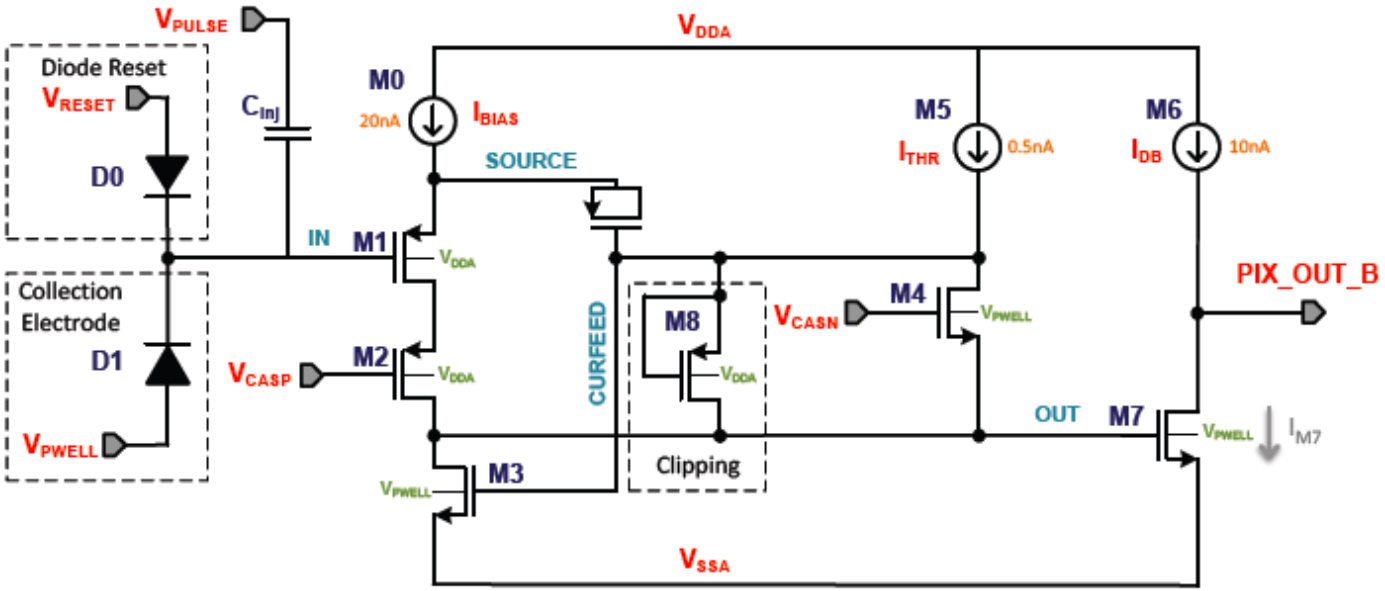


ALPIDE – Timing (3/3)

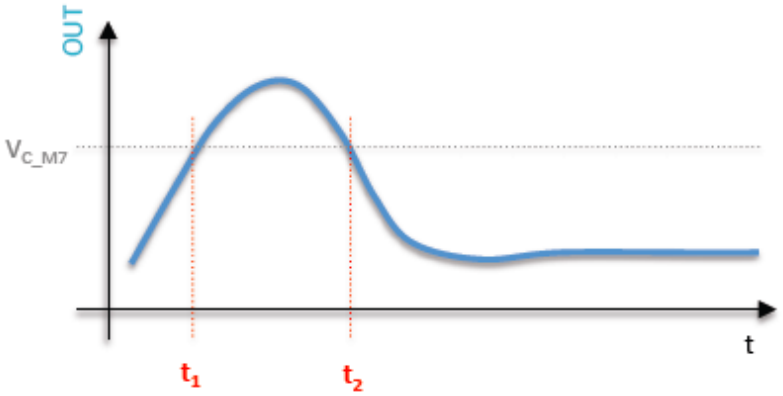


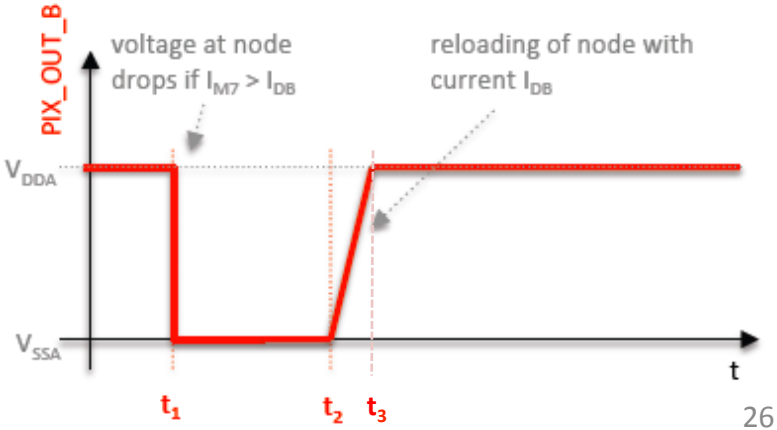
pALPIDE-1 – transient response

- Schematic:

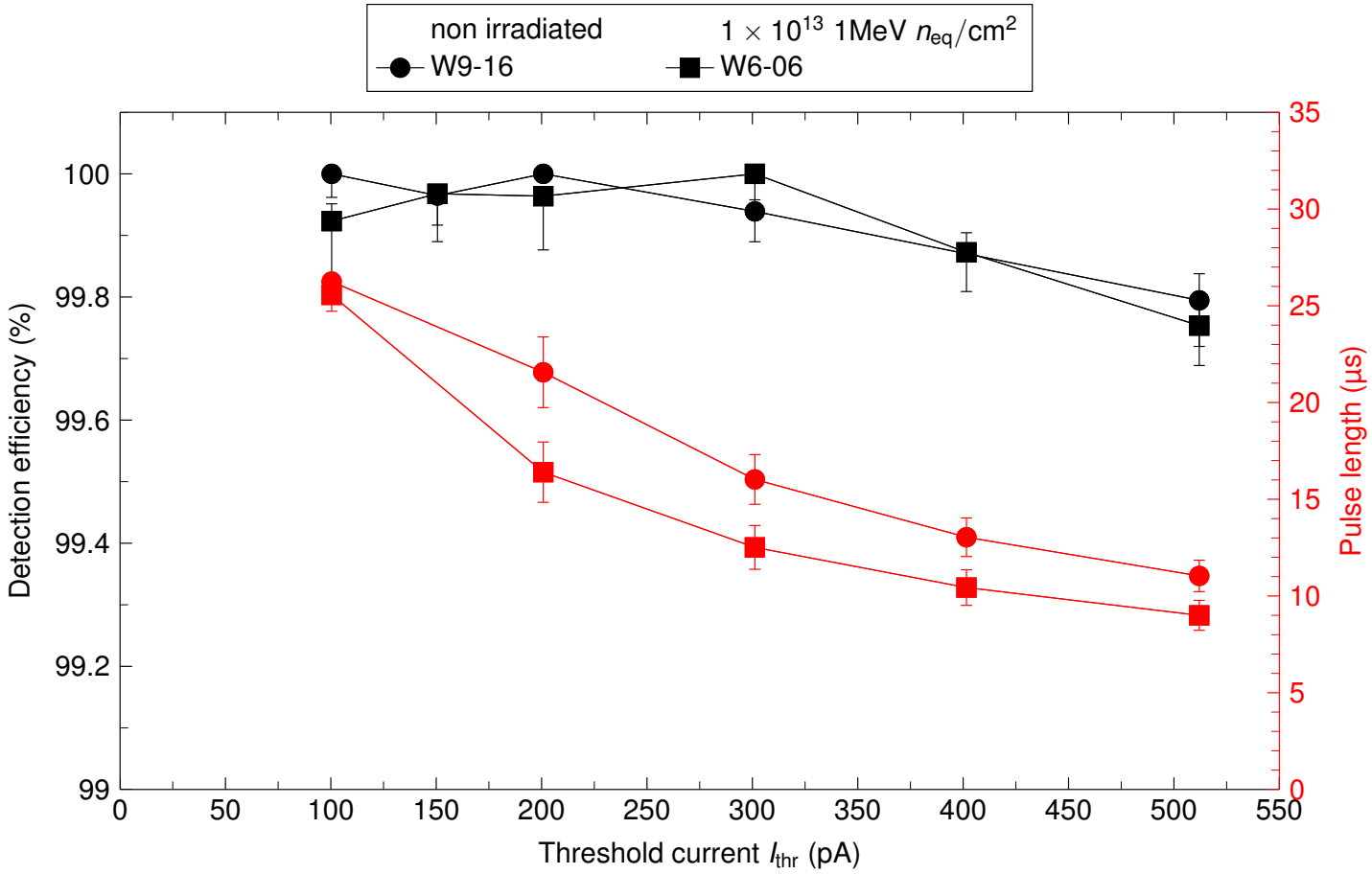


- Principle:





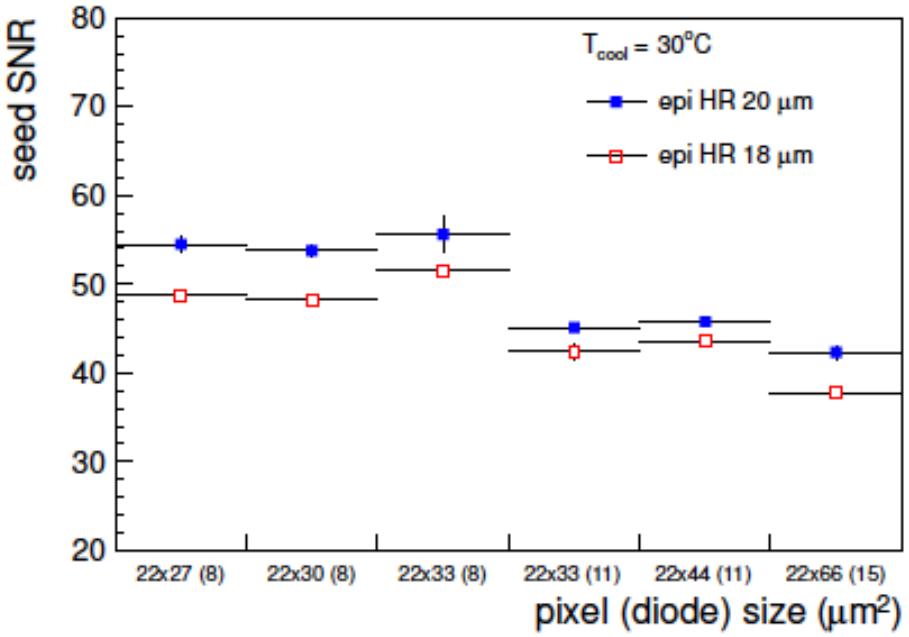
pALPIDE-1 – PS test beam (Dec 2014)



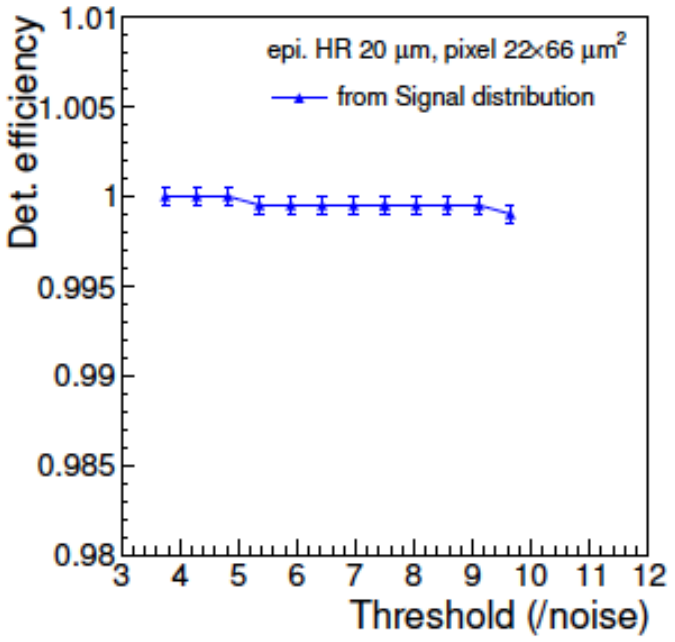
Measurement of threshold current versus pulse length and detection efficiency

MIMOSA 34 – study of pixel size

ITS Upgrade TDR, CERN-LHCC-2013-24



(a) Seed SNR (MPV) for various pixel geometries, for the HR-18 and HR-20 epitaxial layers



(b) Detection efficiency for the 22 µm × 66 µm pixel

Figure 2.12: MIMOSA-34 results.

Single Event Latch-up (SEL)

- SEL refers to a short of the supply planes induce by ionizing particles
  - Sensor needs to be protected (switched off quickly) to avoid damage
  - Power cycle needed to recover (impact on operation)
- SEL is a threshold effect depending on the linear energy transfer (LET)
  - Only recoils from nuclear reactions of primary particles with silicon have LETs that can cause SELs
  - So far, the effect is studied in the lab with heavy ions from a cyclotron to obtain the LET threshold and to identify weak parts of the circuits
  - Tests with high flux protons are foreseen
- Two structures were characterized for SEL
  - Memory chip: dense structures like memories are typically most susceptible to SEL
  - pALPIDE-1
- Collimators were used to identify weak spots:
  - Single-port memories will not be used
  - The analogue biasing of pALPIDE-2 will be improved wrt pALPIDE-1

Single Event Latch-up (SEL)

Measurements done at Louvain-la-Neuve