

ATLAS/CMS/LCD
RD53 collaboration:

**Pixel readout integrated
circuits for extreme rate
and radiation**

2nd LHCC status report

June 3 2015

Jorgen Christiansen on behalf of RD53

Reminder RD53

- Focussed R&D program to develop pixel chips for ATLAS/CMS phase 2 upgrades and LCD vertex
- Extremely challenging requirements for ATLAS/CMS:
 - Small pixels: $50 \times 50 \mu\text{m}^2$ ($25 \times 100 \mu\text{m}^2$) and larger pixels
 - Large chips: $\sim 2 \text{cm} \times 2 \text{cm}$ (~ 1 billion transistors)
 - Hit rates: **$2(3) \text{ GHz/cm}^2$**
 - 50% increase to support pile-up of 200 instead of 140
 - Radiation: 1 Grad , $2 \times 10^{16} \text{ neu/cm}^2$ (unprecedented)
 - Trigger: 1 MHz , $10 \mu\text{s}$ ($\sim 100 \times$ buffering and readout)
 - Low power - Low mass systems
- Baseline technology: 65nm CMOS
- Full scale demonstrator pixel chip in 2016.
 - To be determined if a common pixel chip will be used in the phase 2 upgrades
 - Trigger rates and trigger architecture, Pixel chip size for appropriate pixel modules, Pixel sensor, Powering, Readout, etc.

RD53 collaboration

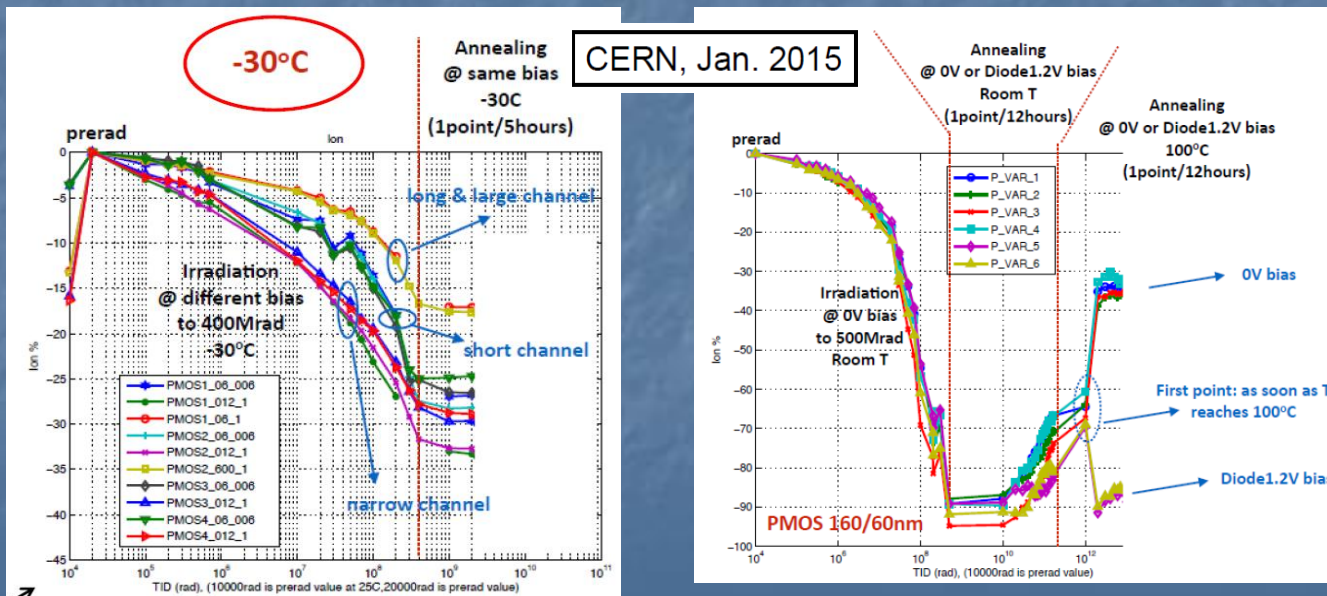
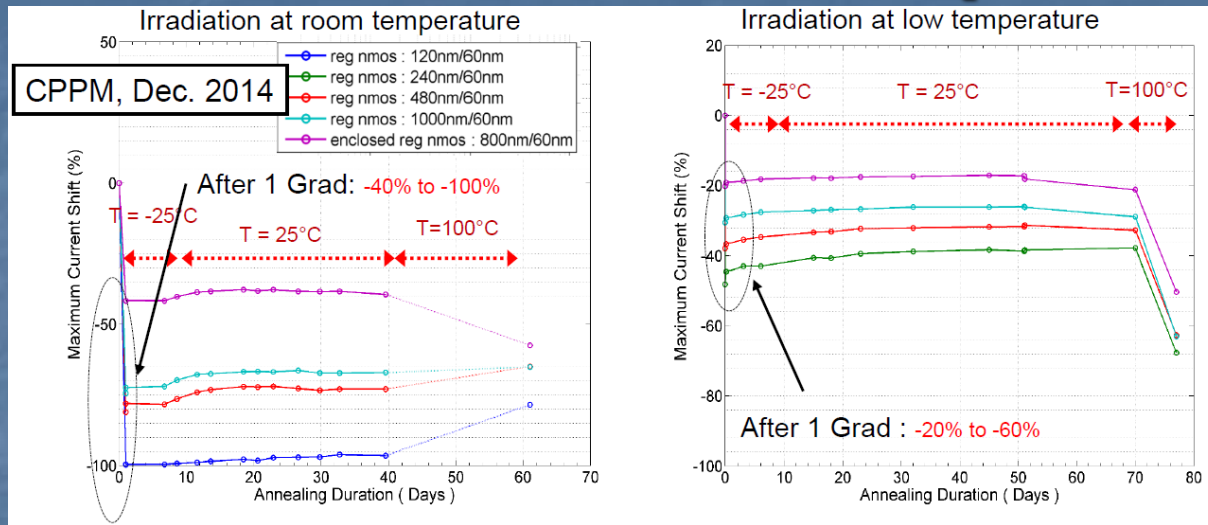
- 20 Institutes (Seville has joined)
 - Bari, Bergamo-Pavia, Bonn, CERN, CPPM, Fermilab, LBNL, LPNHE Paris, Milano, NIKHEF, New Mexico, Padova, Perugia, Pisa, Prague IP/FNSPE-CTU, PSI, RAL, Seville, Torino, UC Santa Cruz.
 - 140 on collaboration Email list
 - ~70 actively contributing
 - 2015 FTE: ~23
 - 50 on RD53 guests email list
 - Spokes persons: Maurice Garcia-Sciveres, LBNL (ATLAS), Jorgen Christiansen, CERN (CMS)
 - IB chair: Lino Demaria, Torino
 - WG conveners: Marlon Barbero, Roberto Beccherle, Jorgen Christiansen, Maurice Garcia-Sciveres, Tomasz Hemperek, Valerio Re
 - 2 year terms coming up to renewal within 3 months
- MOU defined and signed (few exceptions)
- RD53 collaboration meetings: 2 times per year
- RD53 management meetings: Monthly
- WG meetings: Monthly – bi-monthly

Activity	FTE 2015
Radiation	4
Analog	3
IP	7
Simulation	3
Top	3
IO	1
Organization	2
Total	~23

Radiation WG

- Radiation test and qualification of 65nm technology: 1Grad and 2×10^{16} neu/cm²
 - Radiation tests with X-rays, Cobalt source and 3Mev protons
 - Significant radiation damage above ~100Mrad
 - New radiation effects has made it difficult/slow to reach final conclusions
 - Strong dependence on temperature during radiation: Cold is better
 - Strong dependence on both length and width of transistors: Large is better
 - Strong dependence on biasing during high temperature (100°C) annealing: High temperature anneal bad
 - **Realistic to reach 1/2 Grad with conservative design approach**
 - **Radiation cold: -20°C**
 - **No high temperature (100°C) annealing**
(needs careful verification as this limits our ability to do accelerated aging test)
 - NMOS: Small degradation: 10% – 20%
 - PMOS: Significant degradation: 25% (Large transistors) – 50% (very small transistors)
 - Analog: Design recommendations (“large” transistors normally used in analog)
 - Digital: PMOS might need to be larger than minimum size (e.g. $W > 300\text{nm}$, possibly too conservative) and digital cells to be characterized for speed degradation.
 - **Inner barrel layer to be replaced after 5 years**
 - Further tests of devices, circuits and full chips will determine if 1Grad can be accomplished

Radiation effects (PMOS)



Requires an extended seminar to explain all this

Radiation WG

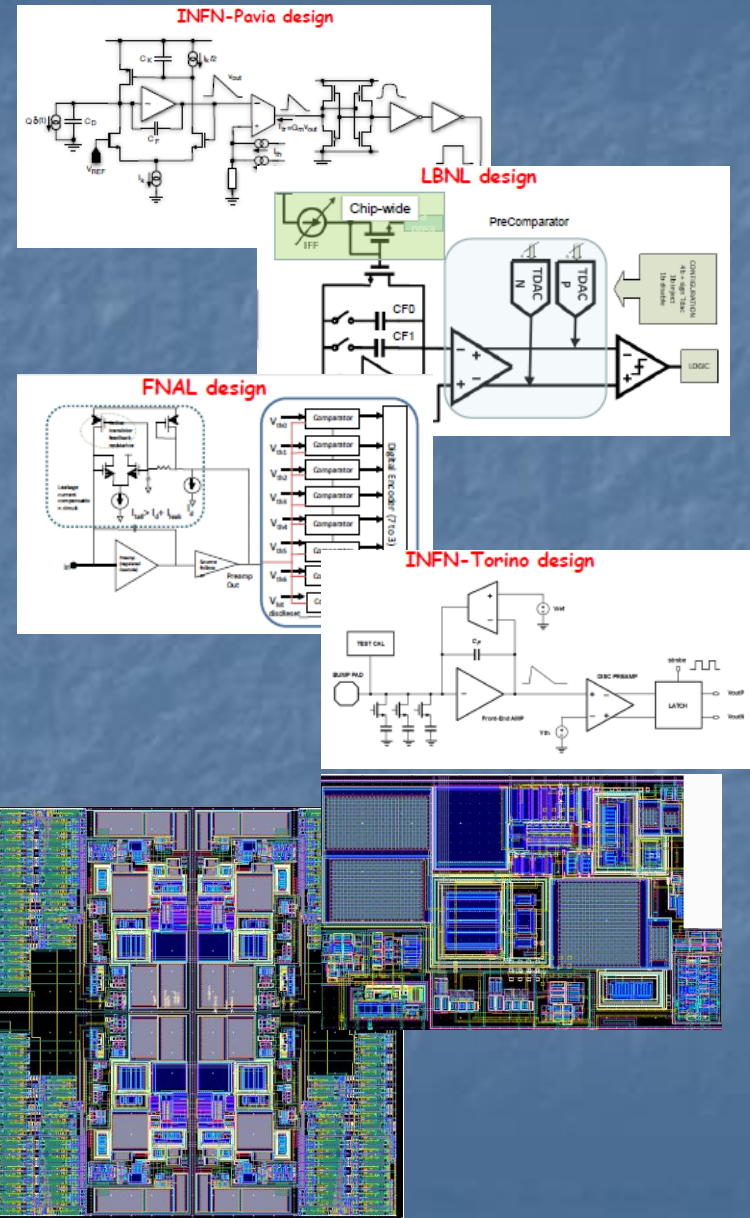
■ Plans

- Systematic radiation and annealing tests at appropriate biasing conditions
- Improve understanding of biasing during high temperature annealing
- NIEL radiation tests
- Radiation test and characterization of digital test structures (speed degradation)
- Include coming radiation test results of IPs and analog FEs
- Finalize radiation simulation corner
- Collect all results and conclusions in radiation test report

Analog WG

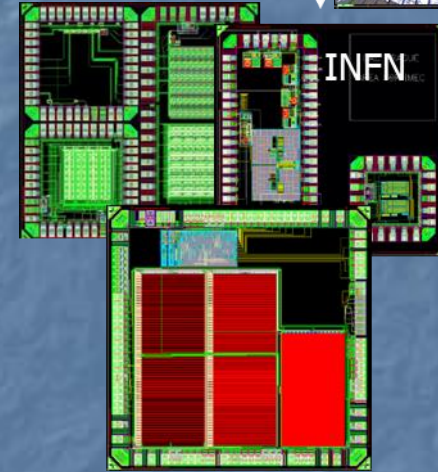
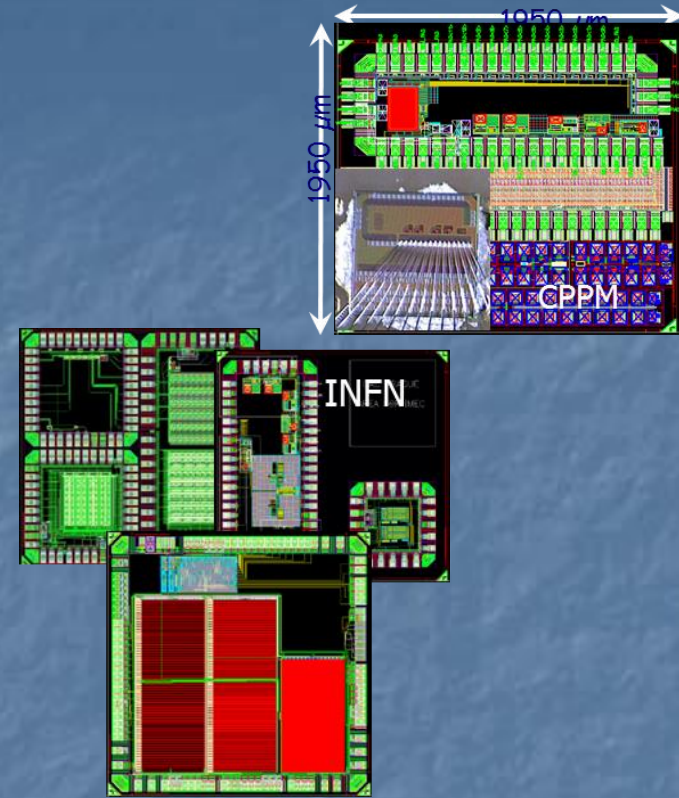
- Low power analog pixel Front-Ends
 - ~50% pixel area for analog
 - Analog front-end specifications defined
 - Capacitance, threshold, noise, power, dispersion, etc.
 - Design and evaluation of alternative FE architectures
 - Different (3) implementations of TOT FEs
 - Non linear digitizing FE
 - 1st version prototypes
 - Electrical characterization done/on-going
 - Radiation tests on-going

- Plans
 - 2nd iteration FE prototypes with improvements
 - Electrical and radiation tests
 - Define interface between analog FE and digital
 - Determine FEs appropriate for integration in full demonstrator
 - Analog performance, radiation tolerance, power consumption
 - Models of FEs for their integration into global digital design flow



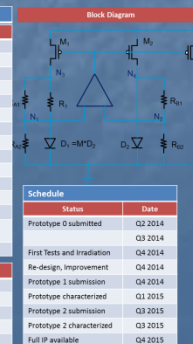
IP WG

- Building blocks required build full pixel chip
 - Large diversity of different IP blocks (30)
 - ADCs, DACs, sensors (temp, current, radiation), Bandgap references, analog buffers, specialized storage cells, PLL, programmable delay, serializer, differential inputs/outputs, shunt-LDO, etc.
 - Specs and data sheets defined
 - Will evolve together global pixel chip architecture
 - First iterations of IPs prototyped.
 - Electrical characterization done/on-going
 - Radiation tests on-going
- Plans
 - 2nd iteration of IPs (some IPs already at this stage)
 - Integration in global pixel chip design
 - Integration and simulation models
 - IP repository
 - Determine if dedicated digital library required or if current/modified digital library must be characterized for radiation conditions



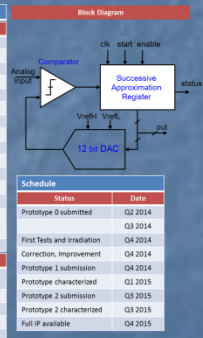
■ Significant design efforts

IP Block: Bandgap V1 Bipolar device	
Parameter	Value
Supply voltage	Typ 1.2 V (±10%)
Temperature range	-40 °C to +60 °C
Active element	BPT_1NPJ3D
Bandgap voltage output	400 mV – 600 mV – 800 mV
Temperature coefficient	400 ppm/°C max
Noise	20 μV RMS max
Max variation (PVT_mismatch)	< 4 mV
Power supply rejection	TBD
Consumption	500 μW (main stage)
Startup circuit	Yes
Trimming	Yes
Max variation (1Grad, 10 ¹⁸ n/cm ²)	1
Status(end of June)	First prototype submitted
Designer (Email)	meosun@soem.in2p3.fr axara@soem.in2p3.fr



Schedule	
Status	Date
Prototype 0 submitted	Q2 2014
Prototype 1 submitted	Q3 2014
First Tests and Irradiation	Q4 2014
Re-design, improvement	Q4 2014
Prototype 1 submission	Q4 2014
Prototype 2 submitted	Q1 2015
Prototype 2 submission	Q3 2015
Prototype 2 characterized	Q3 2015
Full IP available	Q4 2015

12 bit Monitoring ADC	
Parameter	Value
Supply voltage	1.2 V (±10%)
Temperature range	-40 °C to +60 °C
Architecture	SAR
Conversion clock CLK	312 kHz (40 MHz CLK/128) or lower ?
Resolution	12 bit
Input range	0 to 1 V (LSB = 244 μV)
Integral Non Linearity (INL)	±1 LSB
Differential Non Linearity (DNL)	±0.5 LSB
Conversion time	1/4 clock cycle
Capacitor	MINICAP
Power	< 1mW (depends on frequency)
Trimming	Yes
Status(end of June)	First prototype submitted
Designer (Email)	meosun@soem.in2p3.fr axara@soem.in2p3.fr renard.gallone@soem.in2p3.fr



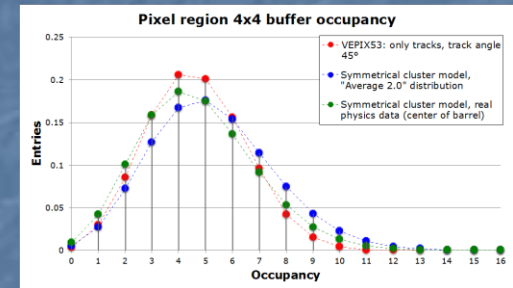
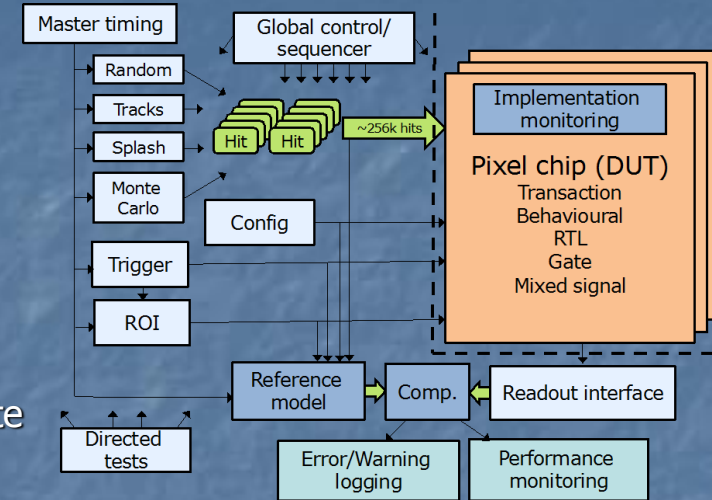
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Simulation/verification WG

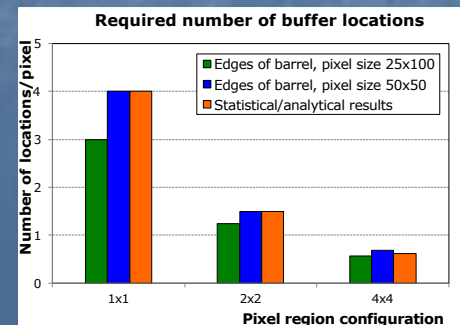
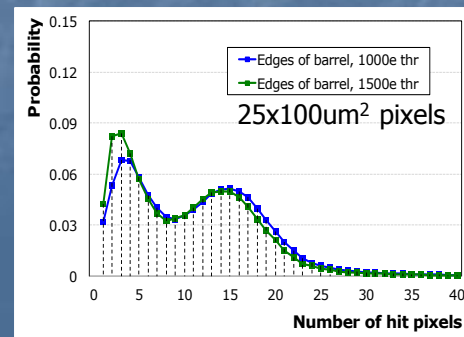
- Simulation and verification framework for pixel chip
 - Simulation framework based on system Verilog and UVM (industry standard for ASIC design and verification)
 - Available on repository and being used by several groups
 - Reference model
 - Basic/generic pixel chip
 - Integration with ROOT to import hits from detector simulations and for monitoring and analysing results.
 - Simulation of alternative architectures with imported Monte Carlo data and/or internally generated hits

■ Plans

- Refine/finalize framework with more detailed behavioural model of pixel chip
 - Gradually become RTL to be synthesized into chip
- Detailed modelling of different pixel chip architectures and optimization
- Inclusion of SEU simulation/verification
- Detailed verification pixel chip



Buffer occupancy comparison between simulation and analytical statistical model



IO WG

■ Readout and control interfaces

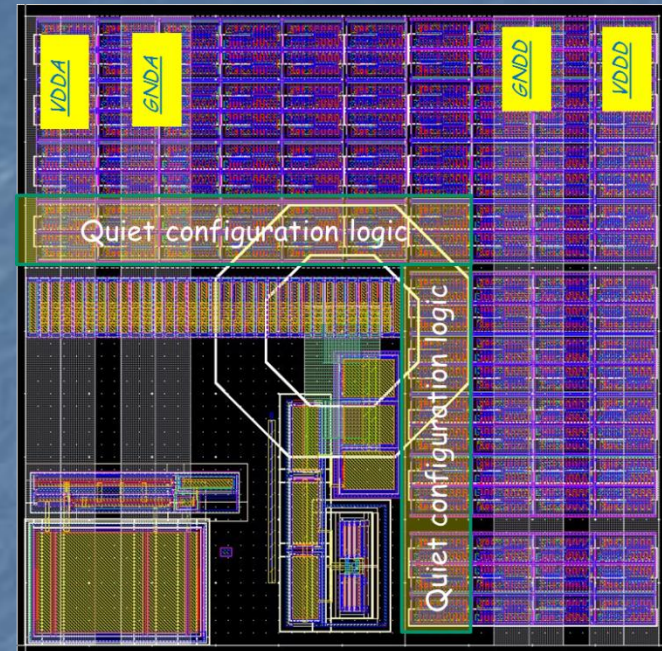
- Proposed control protocol @160Mbits/s
 - Clock, trigger, resets, commands, configuration
 - Single line (differential)
 - DC balanced
 - Appropriate for system synchronization
 - Error correction
 - Compatible with LPGBT optical link chip
 - Simulated and verified

■ Plans

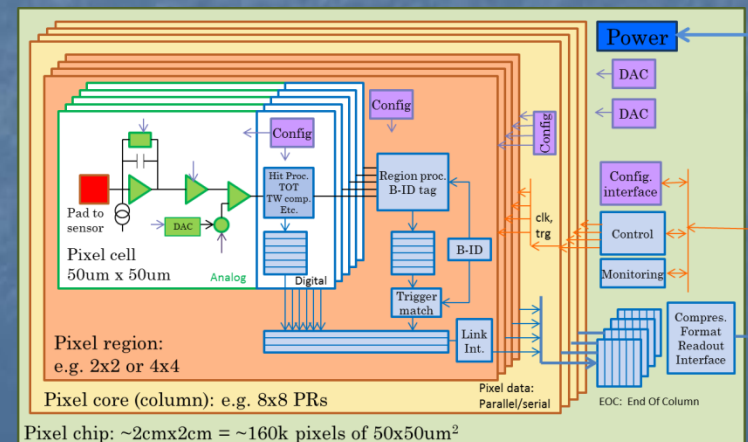
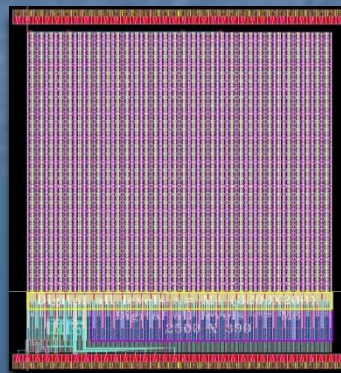
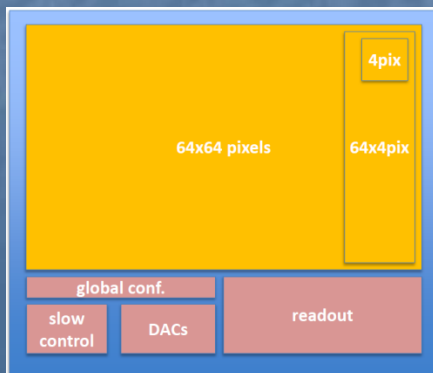
- Define readout protocol
 - Rate: 1.28 – 2.56 – (5.12) Gbits/s
Inner layer pixel chip: ~4Gbits/s raw data (can be reduced with intelligent formatting/compression)
 - Data merging across chips
Outer layer pixel chip: ~400Mbits/s
 - Appropriate for electrical links: 2 – 5m (cable driver)
 - Formatting, Encoding
 - Compatible with LPGBT or direct optical modulation
- Implement/verify IO blocks for pixel chip
- Standardize and implement pixel test systems

Top level WG

- Architecture and floor-plan for large pixel chip
 - Digital sea with analog islands floorplan
 - Distribution of power and global signals
 - Analog – Digital isolation
 - Digital “on-top” design flow
 - Pixels – Pixel regions – Pixel cores – End of column
 - Implementation of small 64x64 pixel demonstrator in 65nm (submission end of this month)
 - Re-optimized “FEI4” for small pixels, higher hit and trigger rates.
- Plans
 - Refinement of pixel chip (digital) architecture
 - Using simulation framework
 - Integration of full pixel chip demonstrator



RD53A



Full scale Demo chip

- Full scale Demo chip
 - When: Mid – end 2016
 - Cost: ~1M\$ (we better get this right !)
 - MLM: 700 k\$ but not full size chip
 - Share cost with other 65nm projects (e.g. CMS MPA)

In the process of defining detailed funding scheme
- What to demonstrate
 - Full size chip (~2cm x 2cm), small pixels (50x50um²), Large pixels (50x200um²), Very high hit and trigger rates, Radiation and SEU tolerance, Effective in-time threshold: 1000e, Low power, Appropriate powering scheme, Functional in test beams, etc.
 - To be used for pixel sensor R&D and qualification
- How to get there
 - Converge all activity in RD53 and WGs on this vital goal/milestone
 - Define project team for implementation and verification

Summary

- Many groups and people working on a focussed R&D effort to implement very high rate pixel chip for extreme radiation
- Large number of circuits, building blocks and small array pixel prototypes have been prototyped and tested in 65nm technology.
- Improved understanding of the initially “mysterious” radiation effects seen at extreme radiation levels above 100Mrad
 - 1/2 Grad appears as realistic goal
 - Test of full pixel chip will determine if 1Grad is feasible
- RD53 focussed on submitting full scale demonstrator chip in 2016

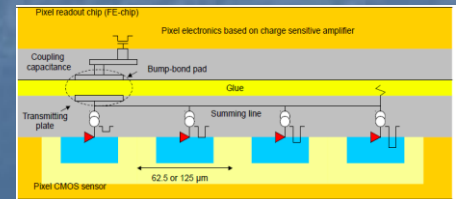
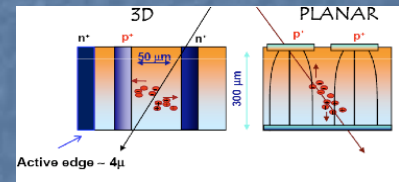
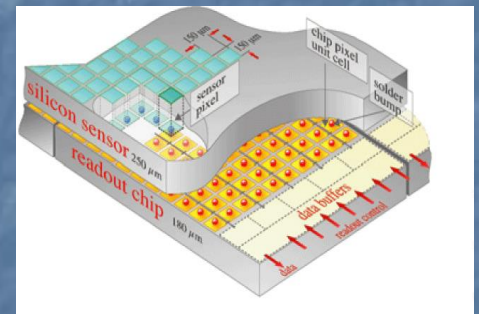
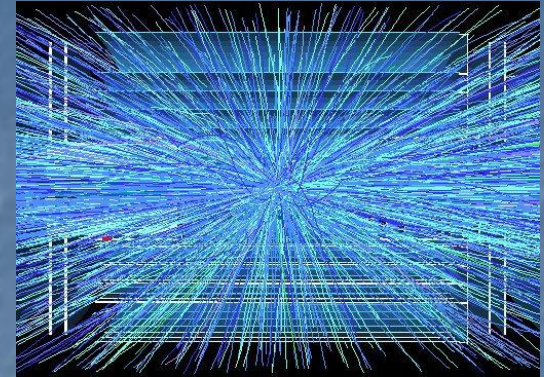
Backup slides

Phase 2 pixel challenges

- ATLAS and CMS phase 2 pixel upgrades very challenging
 - Very high particle rates: 500MHz/cm²
 - Hit rates: 2-3 GHz/cm² (factor 16 higher than current pixel detectors)
 - Smaller pixels: 1/4 - 1/2 (25 – 50 μ m x 100 μ m)
 - Increased resolution
 - Improved two track separation (jets)
 - Participation in first/second level trigger ?
 - A. 40MHz extracted clusters (outer layers) ?
 - B. Region of interest readout for second level trigger ?
 - Increased readout rates: 100kHz -> 1MHz
 - Low mass -> Low power

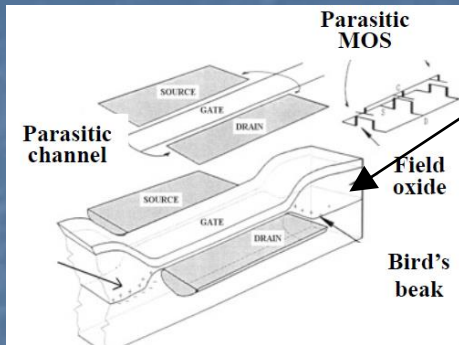
Very similar requirements (and uncertainties) for ATLAS & CMS

- Unprecedented hostile radiation: 1Grad, 2 10¹⁶ Neu/cm²
 - Hybrid pixel detector with separate readout chip and sensor.
 - Phase2 pixel will get in 1 year what we now get in 10 years
- Pixel sensor(s) not yet determined
 - Planar, 3D, Diamond, HV CMOS, , ,
 - Possibility of using different sensors in different layers
 - Final sensor decision may come relatively late.
- Very complex, high rate and radiation hard pixel readout chips required



ATLAS HVCMOS program

Radiation effects

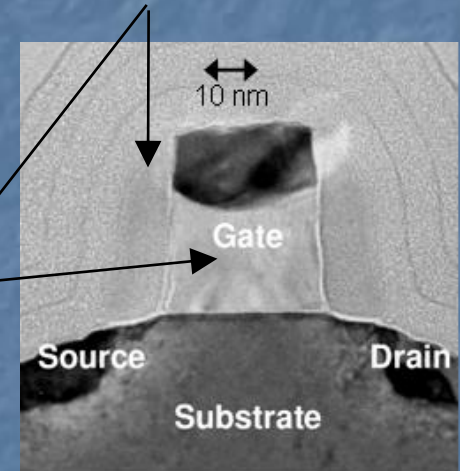


Birds beak parasitic device

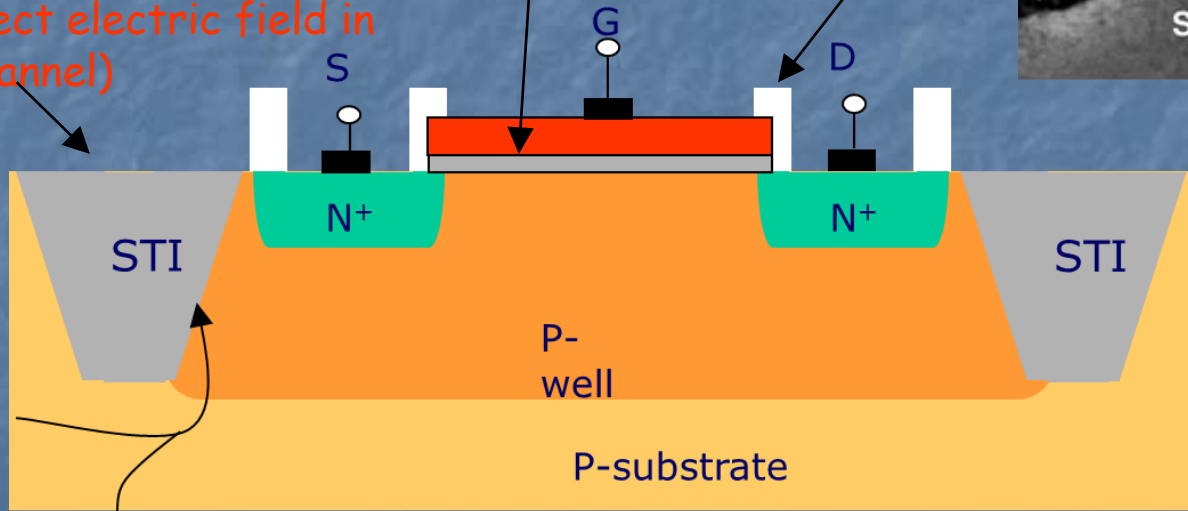
Spacer dielectrics may be radiation-sensitive

Thick Shallow Trench Isolation Oxide (~ 300 nm); radiation-induced charge-buildup may turn on lateral parasitic transistors and affect electric field in the channel)

Charge buildup in gate oxide and interface states affects V_t



Doping profile along STI sidewall is critical; doping increases with CMOS scaling, decreases in I/O devices



Increasing sidewall doping makes a device less sensitive to radiation (more difficult to form parasitic leakage paths)

Pixel chip generations

Generation	Current FEI3, PSI46	Phase 1 FEI4, PSI46DIG	Phase 2
Pixel size	100x150 μm^2 (CMS) 50x400 μm^2 (ATLAS)	100x150 μm^2 (CMS) 50x250 μm^2 (ATLAS)	25x100 μm^2 ?
Sensor	2D, ~300 μm	2D+3D (ATLAS) 2D (CMS)	2D, 3D, Diamond, MAPS ?
Chip size	7.5x10.5 mm^2 (ATLAS) 8x10 mm^2 (CMS)	20x20 mm^2 (ATLAS) 8x10 mm^2 (CMS)	> 20 x 20mm^2
Transistors	1.3M (CMS) 3.5M (ATLAS)	87M (ATLAS)	~1G
Hit rate	100MHz/cm²	400MHz/cm²	2(3) GHz/cm²
Hit memory per chip	0.1Mb	1Mb	~16Mb
Trigger rate	100kHz	100KHz	200kHz - 1MHz
Trigger latency	2.5 μs (ATLAS) 3.2 μs (CMS)	2.5 μs (ATLAS) 3.2 μs (CMS)	6 - 20 μs
Readout rate	40Mb/s	320Mb/s	1-4Gb/s
Radiation	100Mrad	200Mrad	1Grad
Technology	250nm	130nm (ATLAS) 250 nm (CMS)	65nm
Architecture	Digital (ATLAS) Analog (CMS)	Digital (ATLAS) Analog (CMS)	Digital
Buffer location	EOC	Pixel (ATLAS) EOC (CMS)	Pixel
Power	~1/4 W/cm ²	~1/4 W/cm ²	1/2 - 1 W/cm²

Working groups

WG	Domain
WG1	Radiation test/qualification
	<p>Coordinate test and qualification of 65nm for 1Grad TID and 10^{16} neu/cm²</p> <p>Radiation tests and reports.</p> <p>Transistor simulation models after radiation degradation</p> <p>Expertise on radiation effects in 65nm</p>
WG2	Top level
	<p>Design Methodology/tools for large complex pixel chip</p> <p>Integration of analog in large digital design</p> <p>Design and verification methodology for very large chips.</p> <p>Design methodology for low power design/synthesis.</p> <p>Clock distribution and optimization.</p>
WG3	Simulation/verification framework
	<p>System Verilog simulation and Verification framework</p> <p>Optimization of global architecture/pixel regions/pixel cells</p>
WG4	I/O + (Standard cell)
	<p>Development of rad hard IO cells (and standard cells if required)</p> <p>Standardized interfaces: Control, Readout, etc.</p>
WG5	Analog design / analog front-end
	<p>Define detailed requirements to analog front-end and digitization</p> <p>Evaluate different analog design approaches for very high radiation environment.</p> <p>Develop analog front-ends</p>
WG6	IP blocks
	<p>Definition of required building blocks: RAM, PLL, references , ADC, DAC, power conversion, LDO, ,</p> <p>Distribute design work among institutes</p> <p>Implementation, test, verification, documentation</p>