The ultralight DEPFET Pixel Detector of the Belle II Experiment

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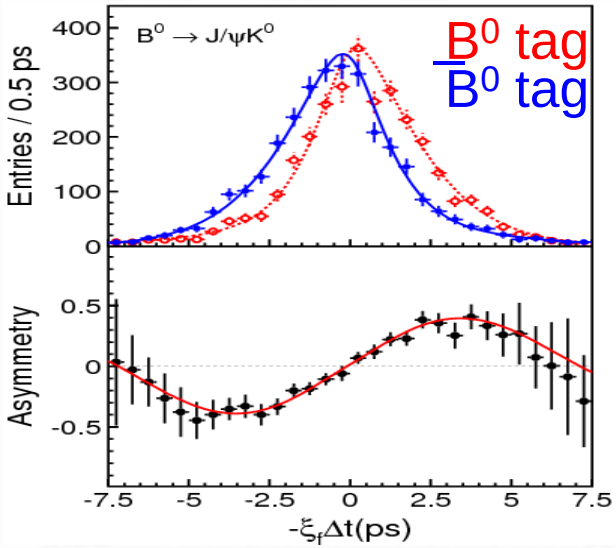
On behalf of the DEPFET Collaboration

Overview

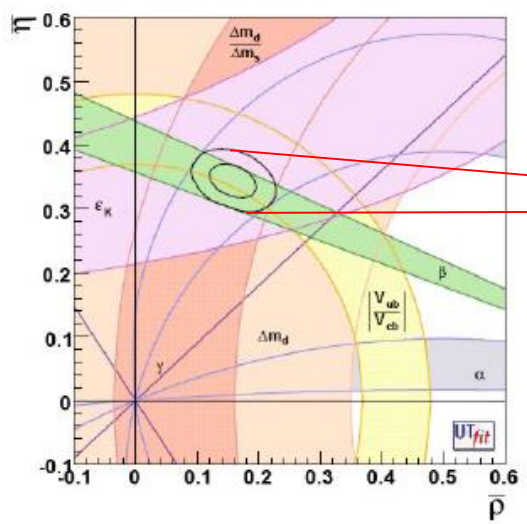
- Super flavor factory: Physics Motivation
- SuperKEKB and Belle II
- DEPFET pixel detector system
  - Module design
  - Latest results

B-Factory detectors – a huge success

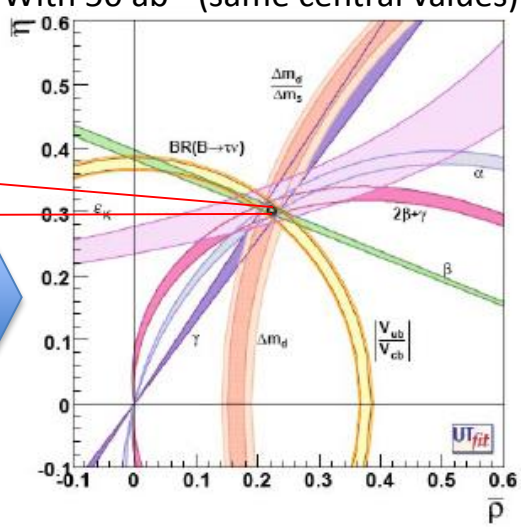
- Measurement of CKM matrix elements and angles of unitary triangle
- Observation of direct CP Violation in B decays
- Measurement of rare decays
- b->s transitions: probe for new sources of CPV and constraints from the b->sγ branching fraction
- Forward-backward asymmetry (A_{fb}) in b->sll as tool for search for physics beyond SM
- Observation of D mixing
- Searches for rare τ decays
- Observation of new hadrons



Current constraints



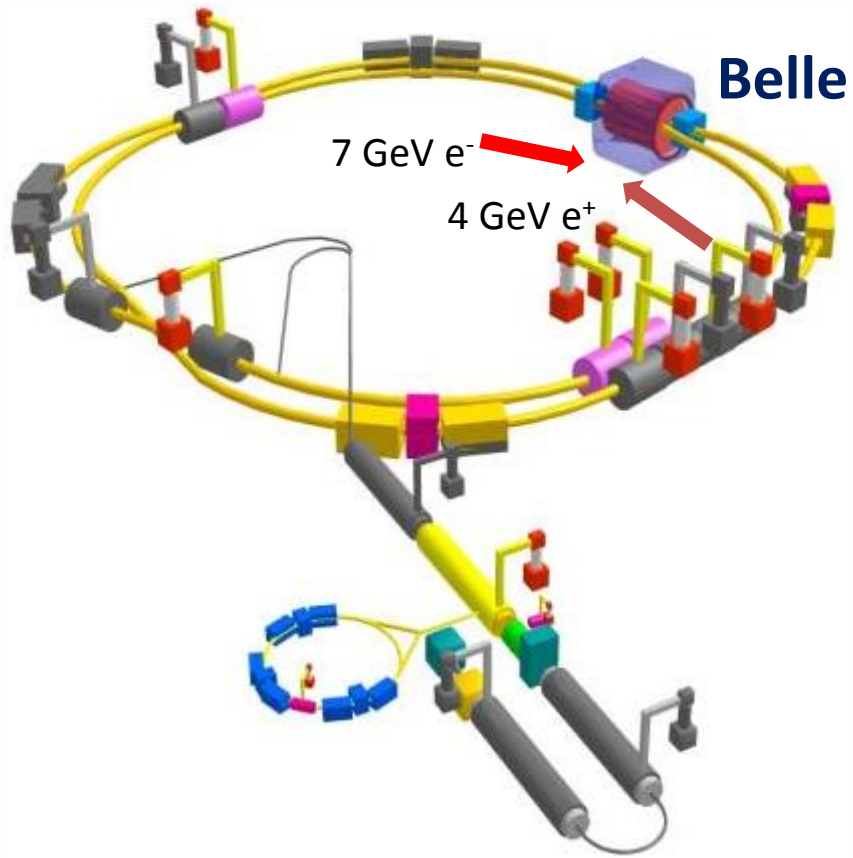
With 50 ab^{-1} (same central values)

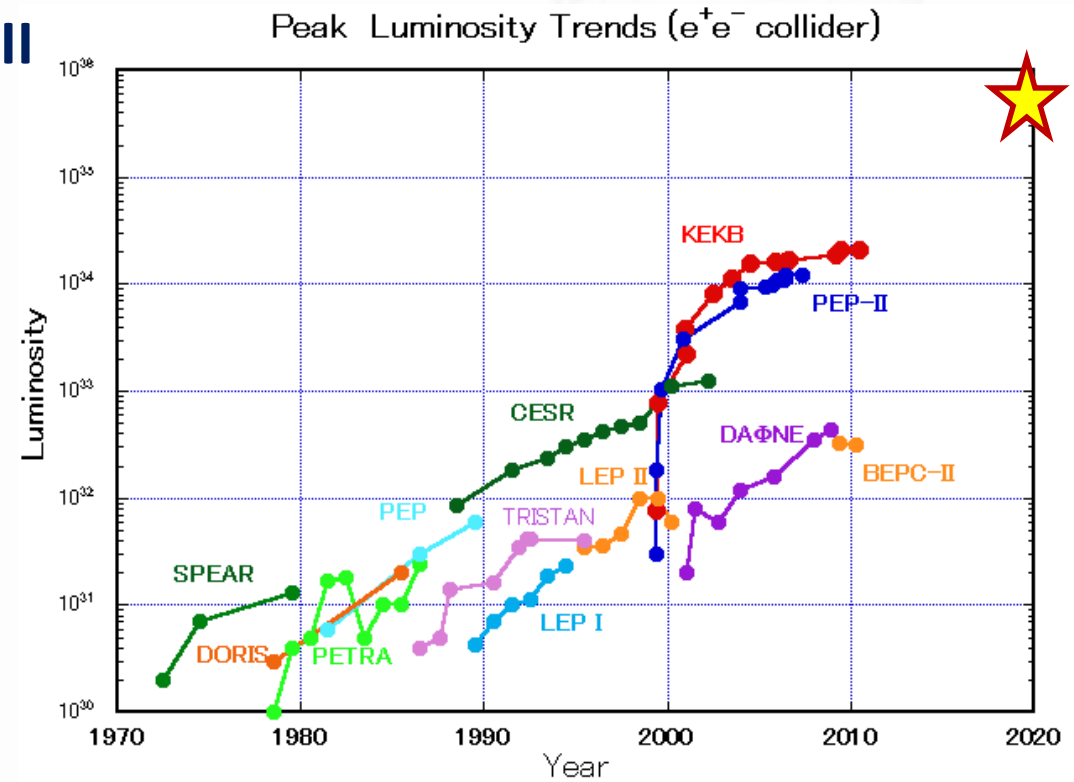


Measure CKM elements as precisely as possible
Over constrain unitarity triangle
Look for deviations from SM

→ **Need 50 ab^{-1}**

KEKB upgrade - SuperKEKB





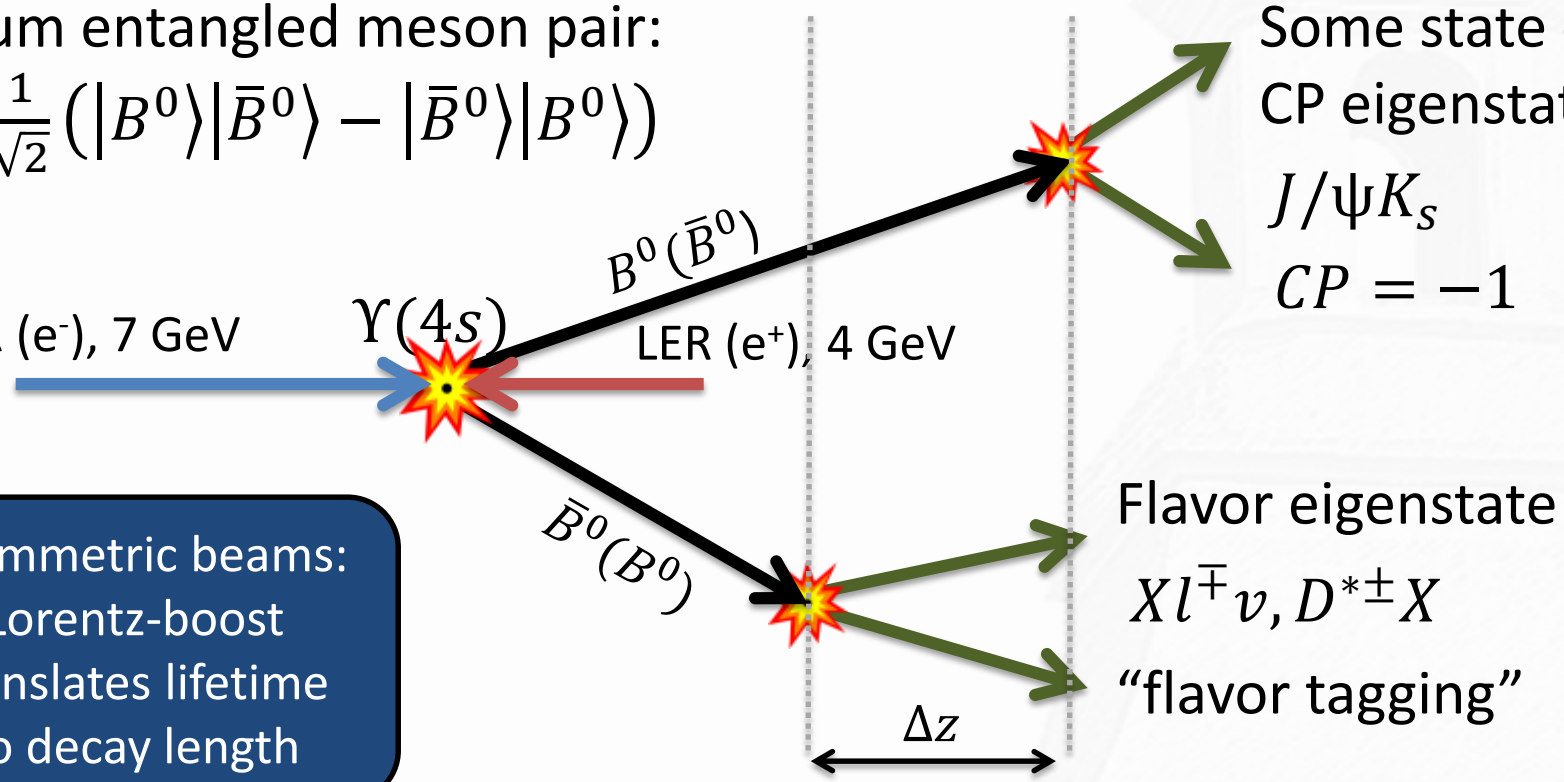
- Asymmetric energy (4 GeV, 7 GeV) e^+e^- collider at the E_{cm}=m(Y(4S)) to be realized by upgrading the existing KEKB machine
- Final luminosity $8 \cdot 10^{35}$ cm^{-2} s^{-1}, 40 times higher than the existing KEKB Factory
- Luminosity: Beam size reduction (nano beam) and higher current

What do we measure? – $\not{C}\not{P}$ observables

$e^+e^- \to \Upsilon(4s) \to B^0\bar{B}^0$ E_{cm} = 10.58 GeV

Quantum entangled meson pair:

$$|\psi\rangle = \frac{1}{\sqrt{2}}\left(|B^0\rangle|\bar{B}^0\rangle - |\bar{B}^0\rangle|B^0\rangle\right)$$



Asymmetric beams: Lorentz-boost translates lifetime to decay length

$$\Delta z = \beta\gamma c\Delta t \sim 150\ \mu m$$

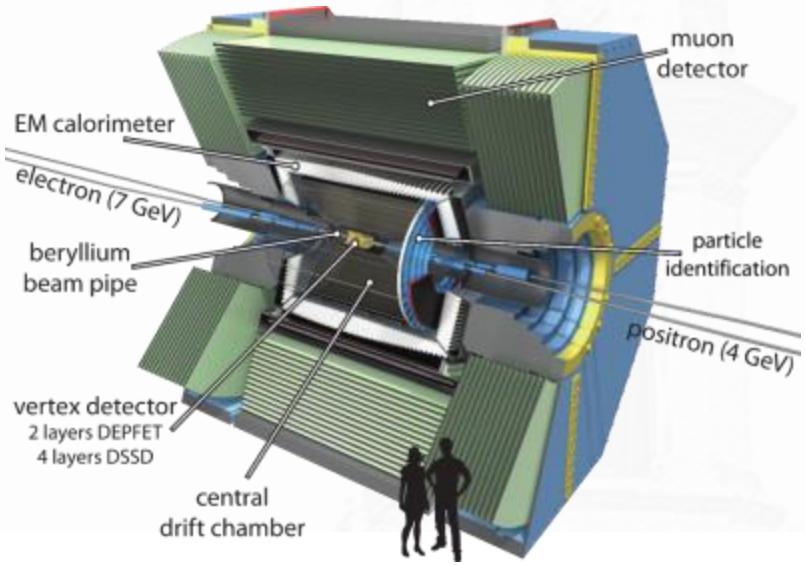
Precise vertexing essential to measure CP violation

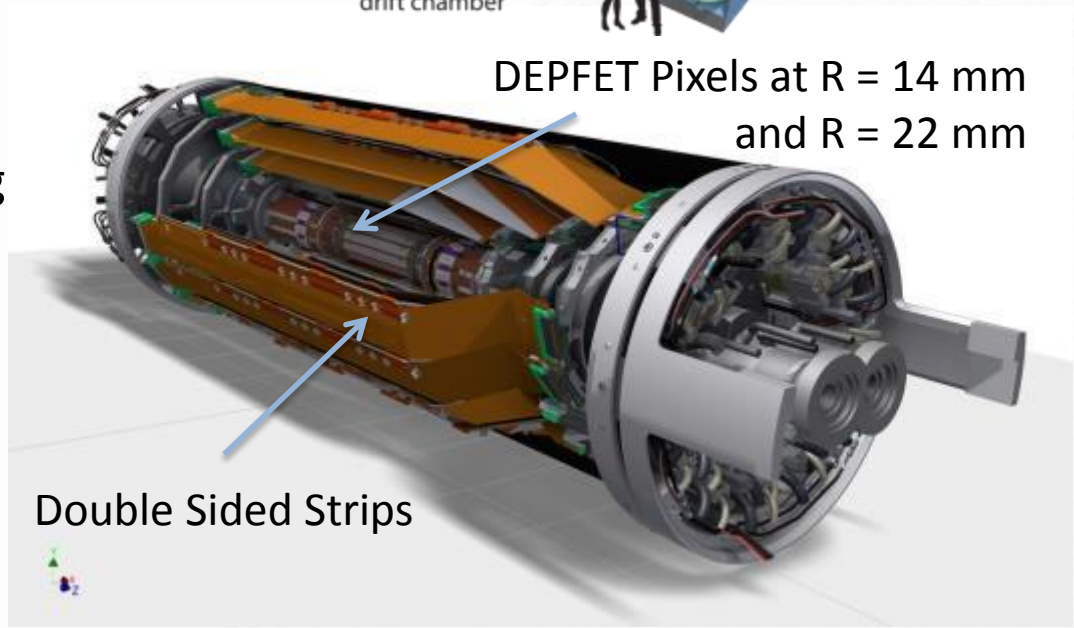
Belle upgrade – Belle II

Higher luminosity implies

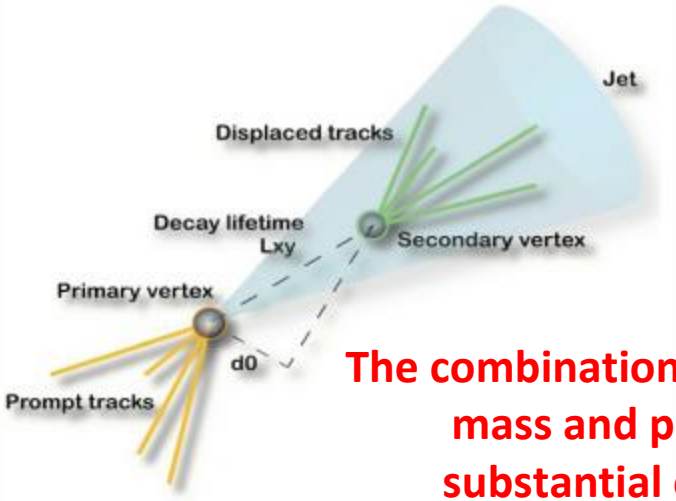
- Higher background
  - **Radiation damage**
  - **Occupancy**
  - Fake hits and pile-up noise in EM Calorimeter
- Higher event rate
  - Higher trigger rate
  - Increased DAQ and computing requirements
- Changes in detector
  - $\beta\gamma$ reduced by factor of 2

  → **Improved vertexing needed**





Vertexing Requirements



$$\sigma_{d0} \approx \sqrt{\frac{r_2^2\sigma_1^2 + r_1^2\sigma_2^2}{(r_2 - r_1)^2}} \oplus \frac{r}{p\sin^{\frac{3}{2}}\theta} 13.6MeV\sqrt{\frac{x}{X_0}}$$

The combination of resolution, mass and power is a substantial challenge

$$\sigma_{d0} \approx a \oplus \frac{b}{p\sin^{\frac{3}{2}}\theta}$$

	a (µm)	b (µm GeV)
LHC	12	70
STAR	12	19
Belle II	8.5	10
ILC	5	10

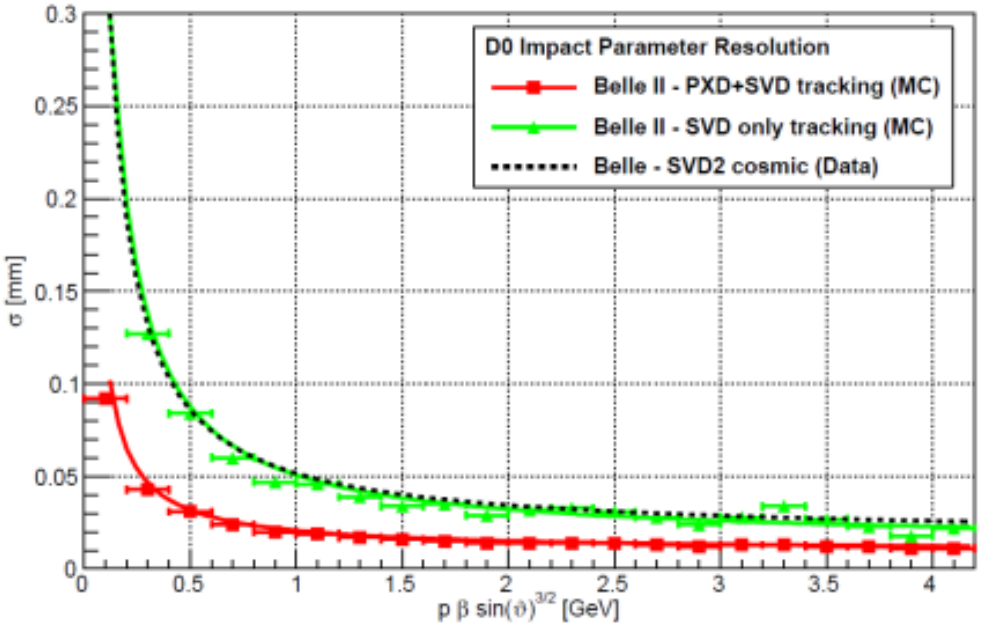
a: Governs high momentum
b: Dominates at low momentum

Common vertex detector requirements

- **First layer close to the IP**
- **Low material budget**
- Reduced services
- **Low power dissipation**
- High granularity
- Good spatial resolution
- Fast readout
- Radiation hardness

Belle II Vertex Detector Requirements

Occupancy	0.4 hits/µm²/s
Radiation	2 Mrad/year
	$2 \cdot 10^{12}$ 1 MeV n_{eq} per year
Frame time	20 µs
Momentum range	Low momentum (< 1 GeV)
Acceptance	17º-155º
Material budget	0.2% X_0 per layer
Resolution	15 µm (50x75 µm²)



- Modest resolution (15 µm), dominated by multiple scattering → Pixel size (50 x 75 µm²)
- Lowest possible material budget (0.2% X_0/layer)
  - Ultra-transparent detectors
  - Lightweight mechanics and minimal services

DEPFET – DEpleted P-channel Field Effect Transistor

FET in saturation: $V_{GS} > V_{th}$ and $V_{DS} \geq (V_{GS} - V_{th})$

$$I_d = \frac{W}{2L}\mu C_{ox}\left(V_{GS} - V_{th} - \frac{\alpha q_s}{C_{ox}WL}\right)^2$$

I_d: source-drain current
C_{ox}: sheet capacitance of gate oxide
W,L: Gate width and length
μ: mobility (p-channel: holes)
V_{GS}: gate voltage
V_{th}: threshold voltage

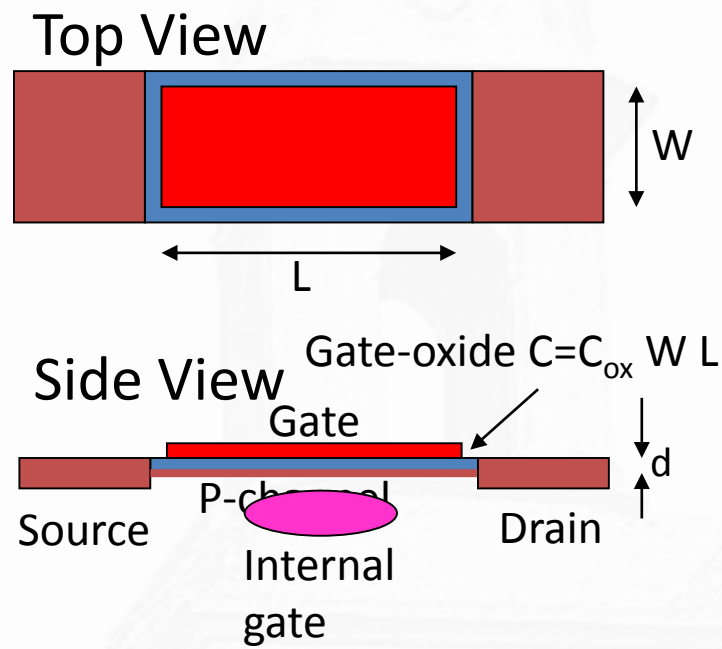
Transconductance:

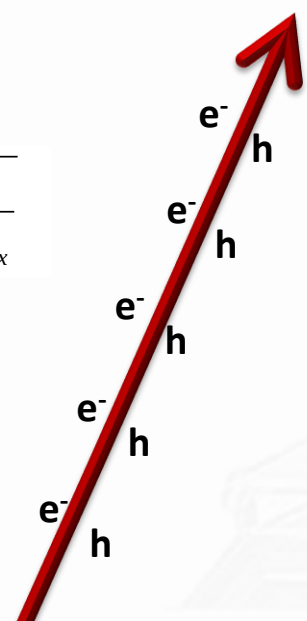
$$g_m = \frac{dI_d}{dV_{GS}} = \frac{W}{L}\mu C_{ox}(V_{GS} - V_{th}) = \sqrt{2\frac{I_d\mu}{L^3WC_{ox}}}$$

Conversion factor:

$$g_q = \frac{dI_d}{dq_s} = \frac{\alpha\mu}{L^2}\left(V_{GS} - V_{th} - \frac{\alpha q_s}{C_{ox}WL}\right) = \alpha\sqrt{2\frac{I_d\mu}{L^3WC_{ox}}}$$

$$g_q = \alpha\sqrt{2\frac{W\mu C_{ox}I_d}{LL}} = \alpha\frac{g_m}{C_{ox}}$$

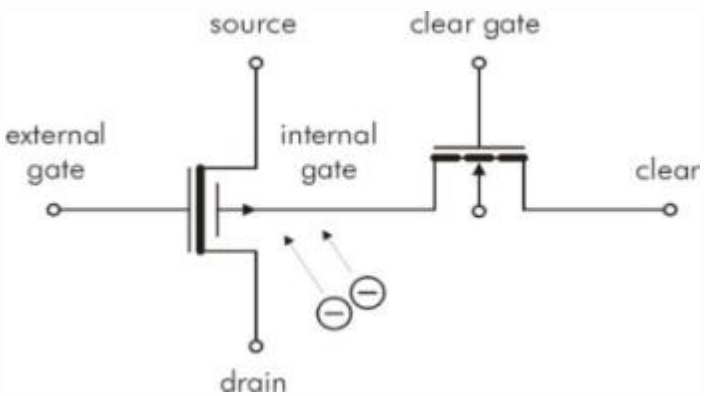




Charge q in the internal gate induces mirror charge αq in the channel (α <1 due to stray capacitance).
This mirror charge is compensated by a change of the gate voltage:
$\Delta V = \alpha\, q / C = \alpha\, q / (C_{ox}\, W\, L)$
which in turn changes the transistor current I_d .

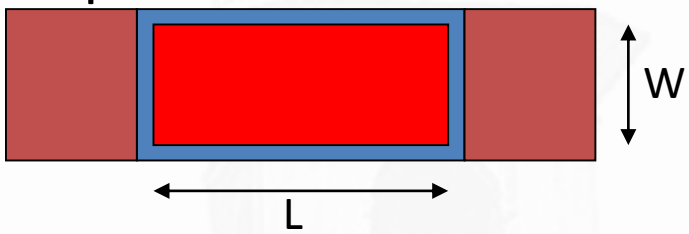
DEPFET – DEpleted P-channel Field Effect Transistor

- **Internal amplification, g_q~ 500 pA/e$^-$**
- Small intrinsic noise
- **Sensitive off state – no power consumption**

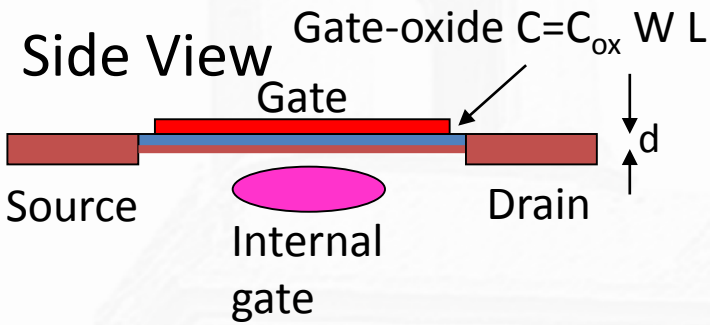


- Nondestructive readout
- **Charge needs to be cleared**
- Clear contact attractive for electrons

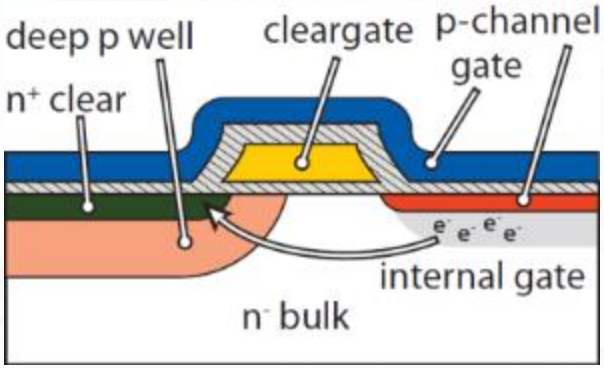
Top View



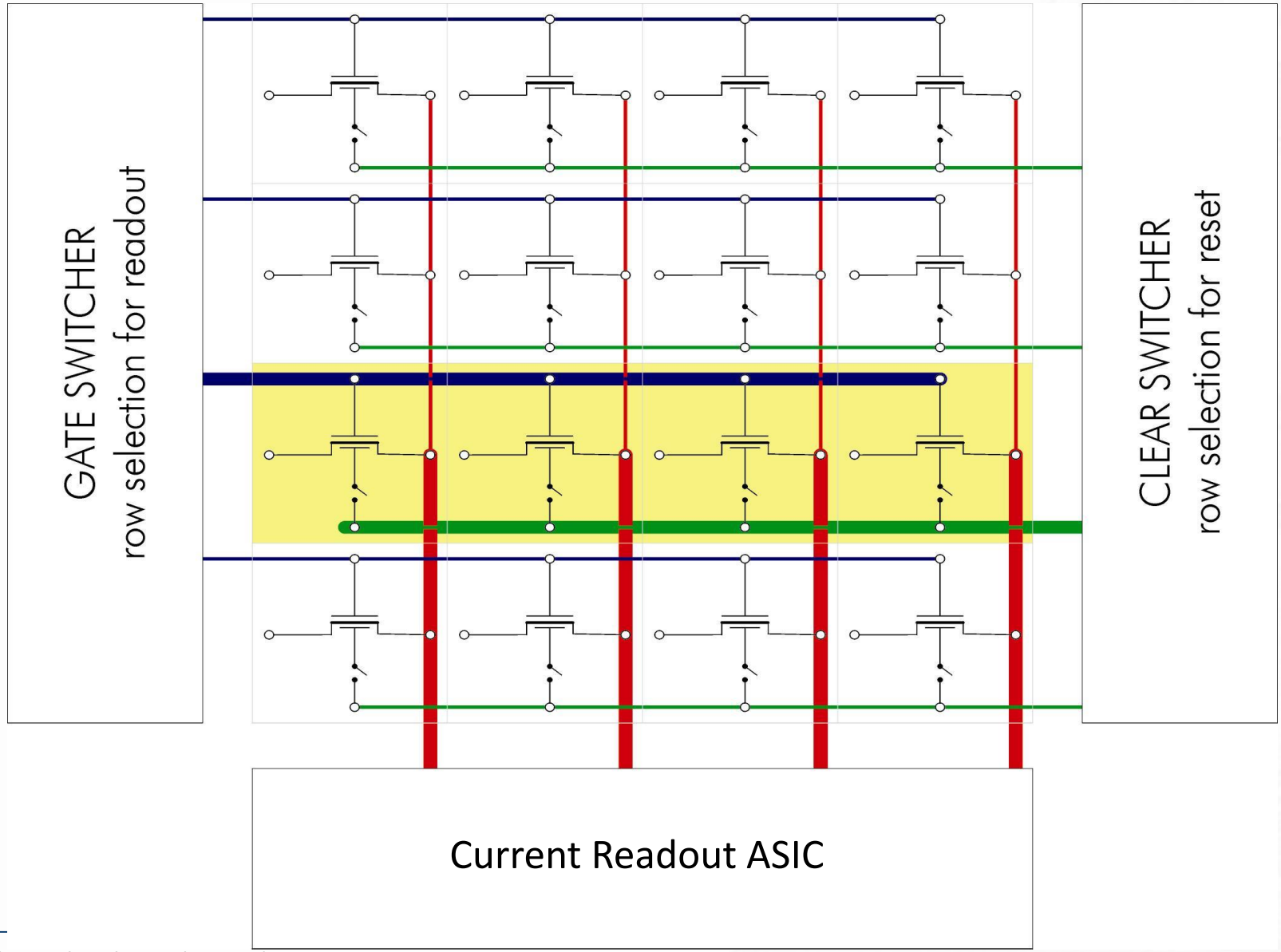
Side View



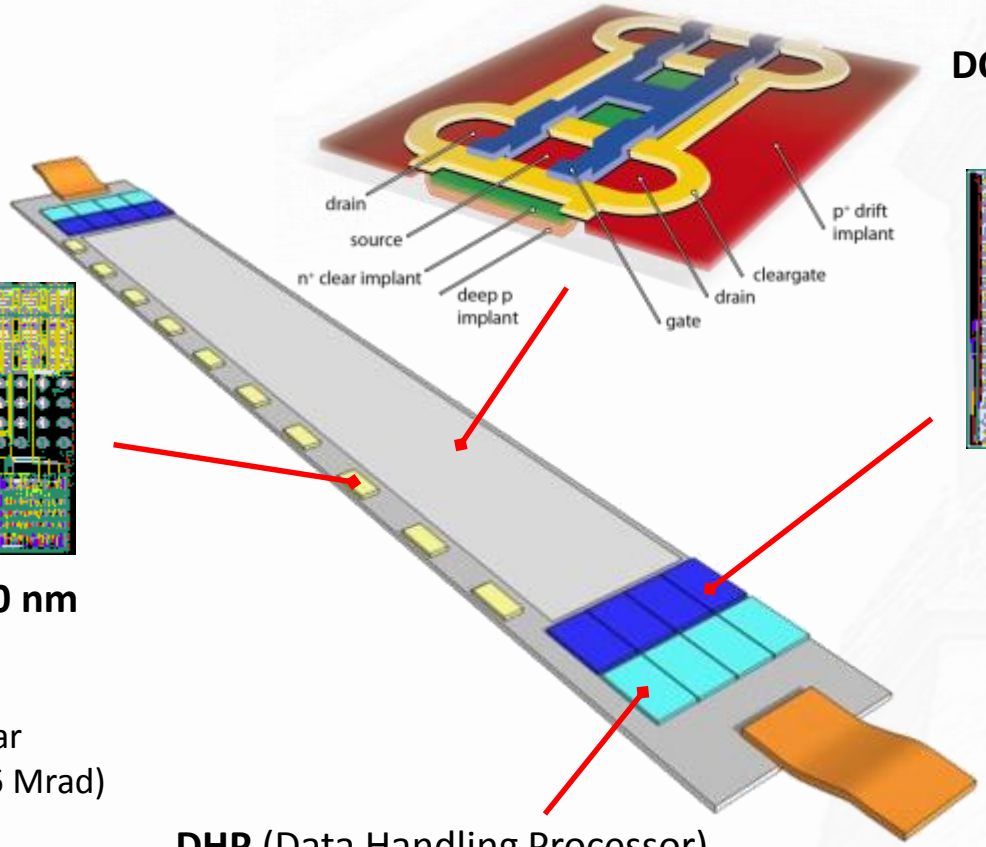
Side View – 90° rotated



DEPFET Readout and Matrix Design

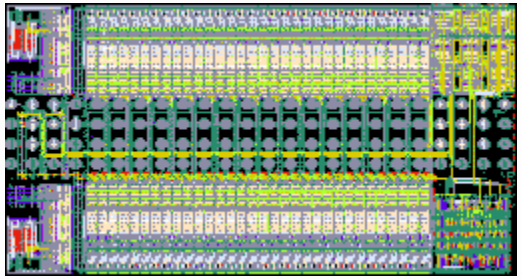


The DEPFET Ladder



SwitcherB

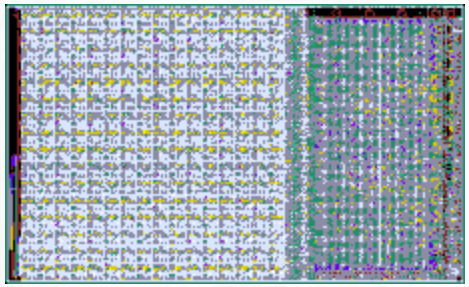
Row control



AMS HVCMOS 180 nm

Size 3.6 × 1.5 mm²
Gate and Clear signal
Fast HV ramp for Clear
Rad. Hard proved (36 Mrad)

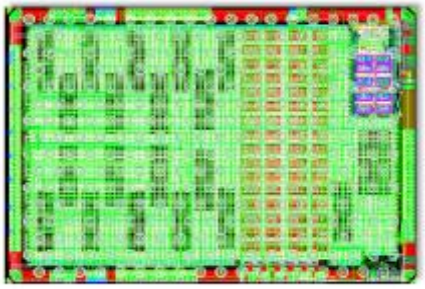
DCDB (Drain Current Digitizer)
Analog frontend



UMC 180 nm

Size 5.0 × 3.2 mm²
TIA and ADC
Pedestal compensation
20 Gbit/s output data
Rad. Hard proved (20 Mrad)

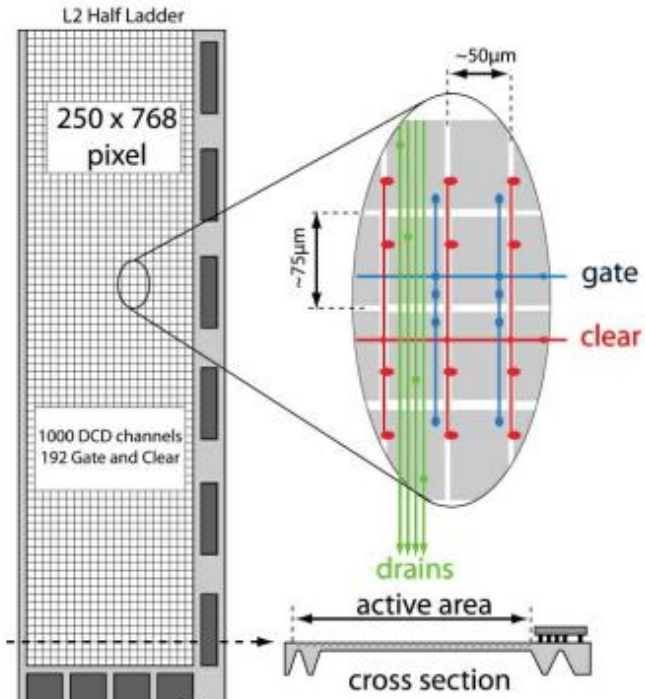
DHP (Data Handling Processor)
First data compression



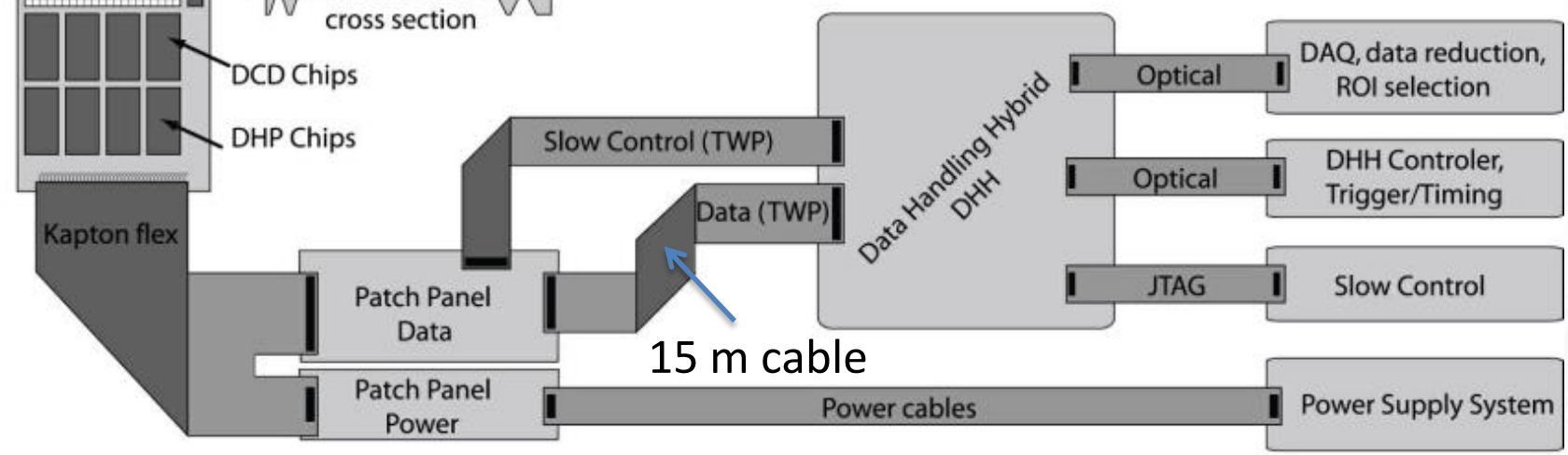
TSMC 65 nm

Size 4.0 × 3.2 mm²
Stores raw data and pedestals
Common mode and pedestal correction
Data reduction (zero suppression)
Timing signal generation
1.6 Gbit/s Highspeed link over 15 m cable
Rad. Hard proved (100 Mrad)

Back End

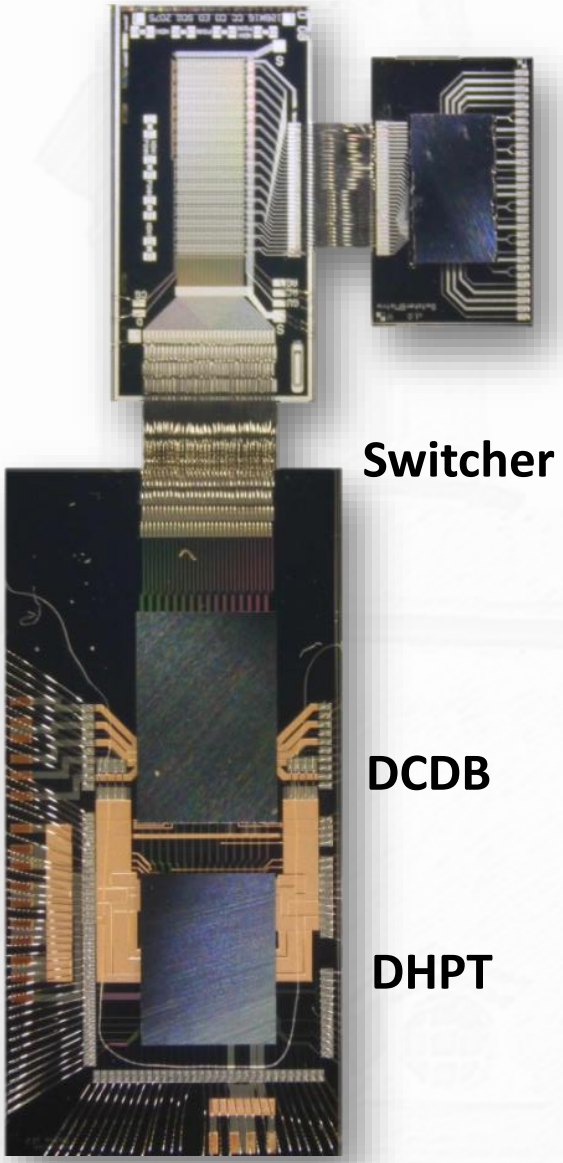


- DHH (Data Handling Hybrid)
  - Electrical - optical interface
  - Slow control master (JTAG)
  - Clustering, Slow Pion Rescue
- ONSEN
  - Data buffer
  - Reduction via ROI selection (DATCON, HLT)



Hybrid 5 – Full system demonstrator

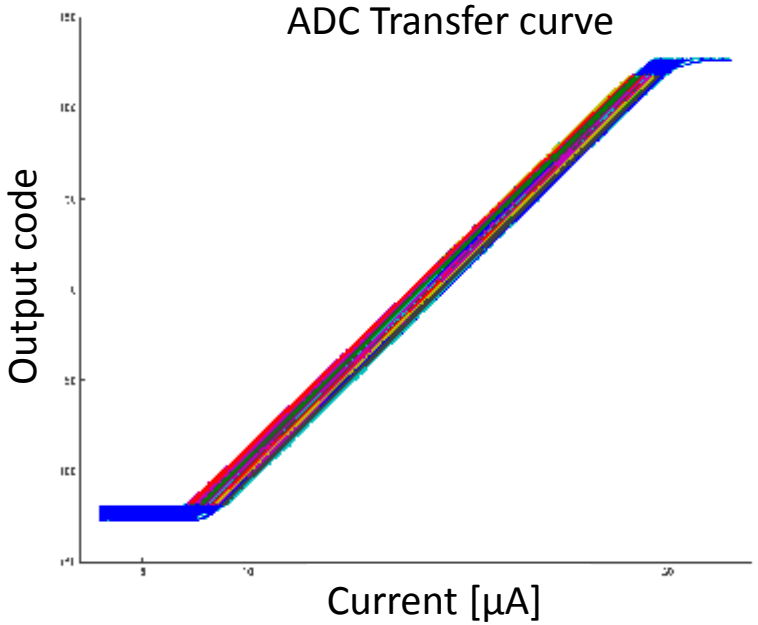
- PXD9 small Belle II type matrix
  - Pixel pitch: 50x55 μm^2
  - Thinned to 75 µm
  - Gate length: 5 µm
  - Thin gate oxide
  - 32x64 pixels readout
  - Sampling time 128 ns (80% targeted)
- Final readout chain
  - SwitcherB
  - DCDB
  - DHPT
  - DHPT → DHH



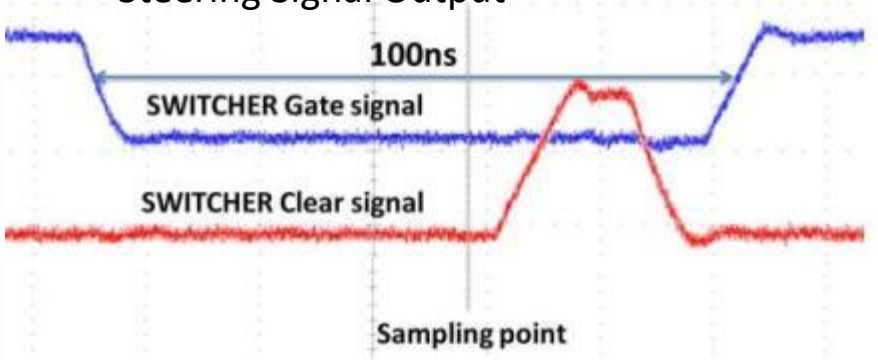
Hybrid 5 – ASIC Optimization

- Drain Current Digitizer (DCD):
  - Uniformity and linearity of ADCs
- Data Handling Processor (DHPT):
  - High speed link settings
  - Steering sequences
  - Signal timing

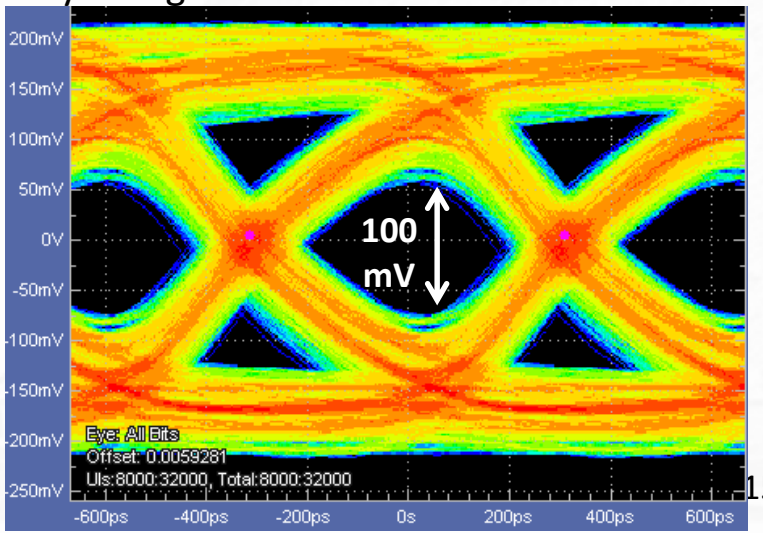
ADC Transfer curve



Steering Signal Output

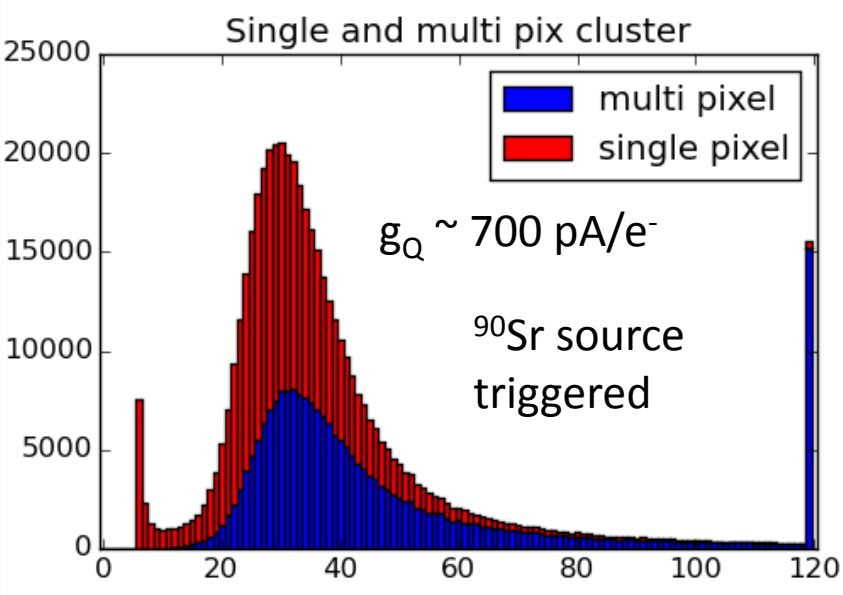


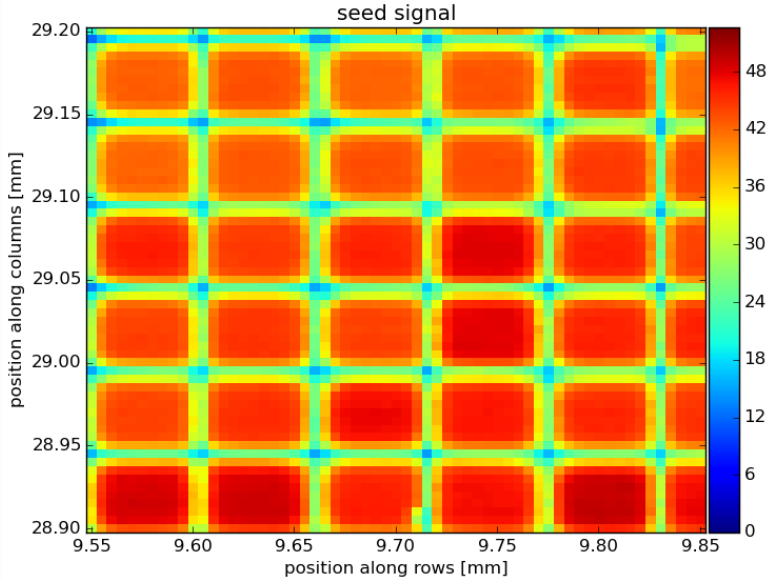
Eye Diagram after 15m cable Cable

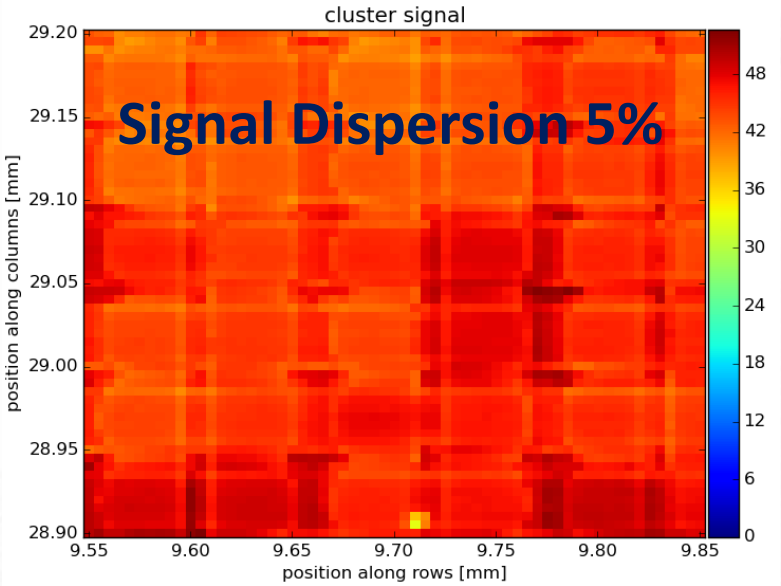


Hybrid 5 – Matrix Optimization

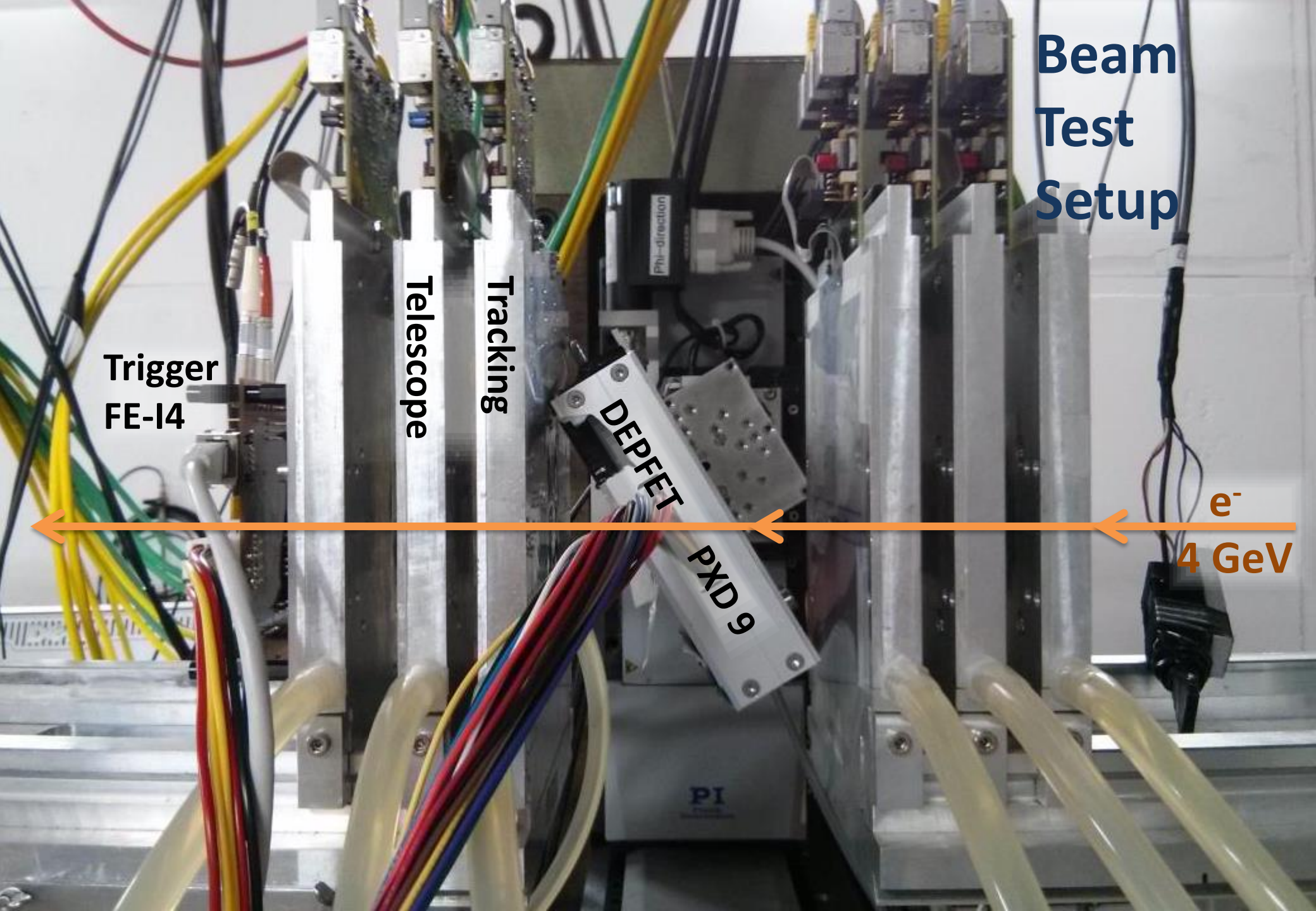
- Optimization of DEPFET voltages
  - Laser measurements
  - Source measurements





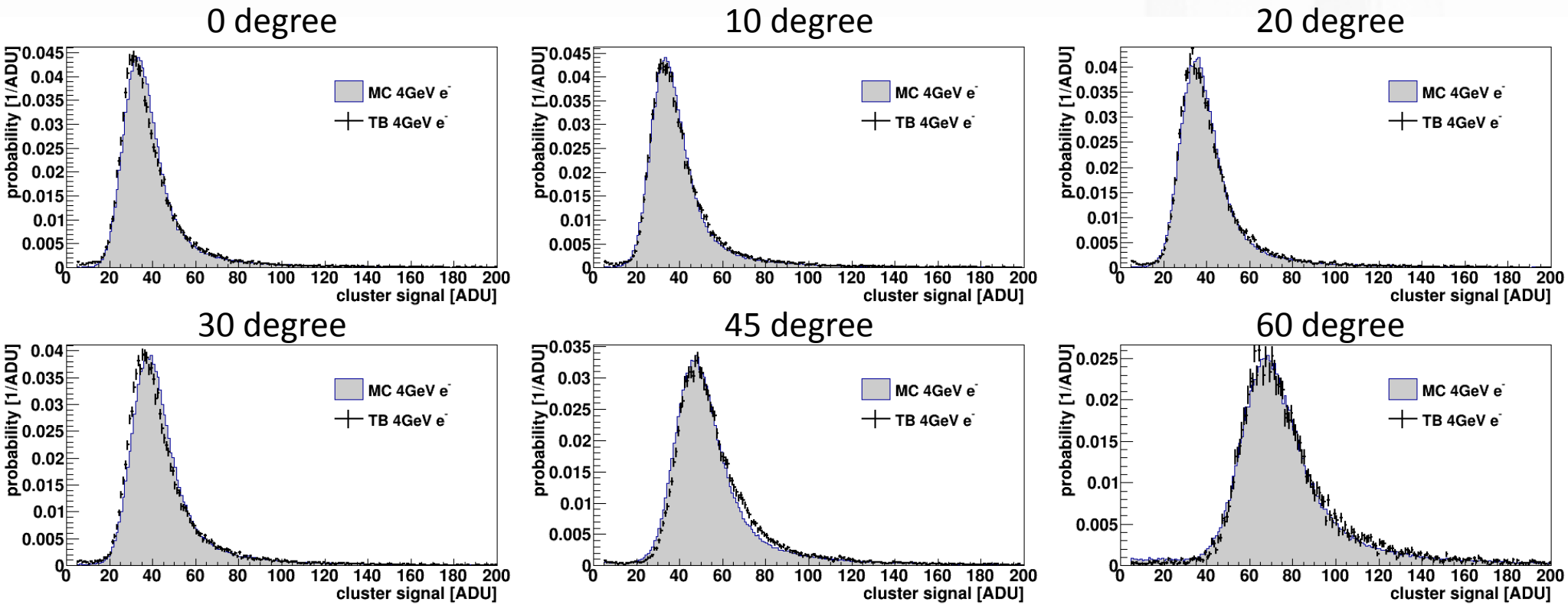


- Laser focused through microscope
- ~3 µm spot size
- Laser moves over matrix – position resolution


Beam
Test
Setup
Trigger
FE-I4
Telescope
Tracking
DEPFET
PXD 9
e-
4 GeV
Phi-direction
PI

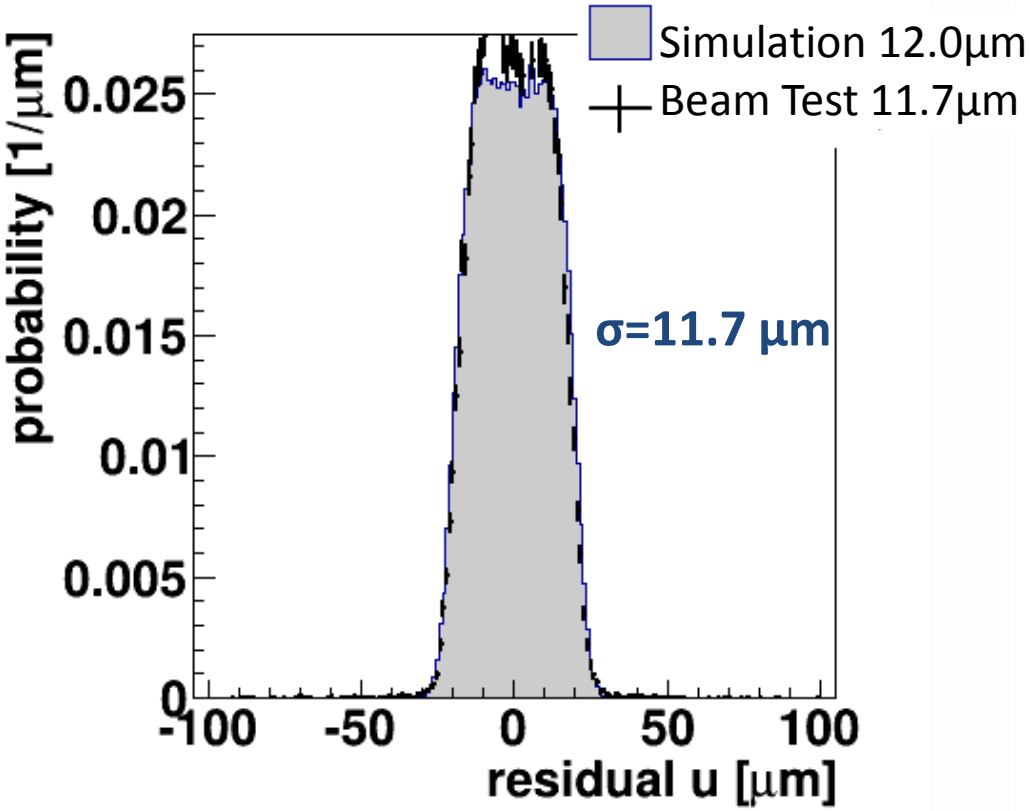
Hybrid 5 Testbeam Results

- Measured 4 GeV electrons at different incidence angles
- Checked against Geant4 simulation with DEPFET Clusterizer
- g_q = 740 ± 20 pA/e^- measured

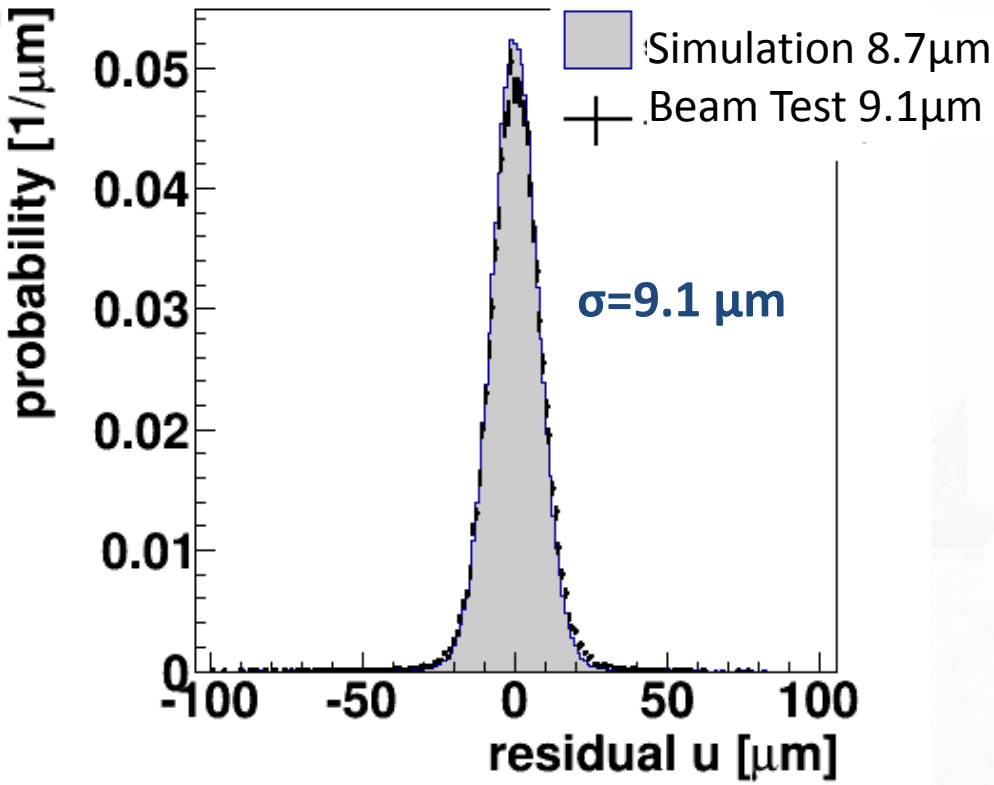


Position Resolution

0° tilt: perp. incidence

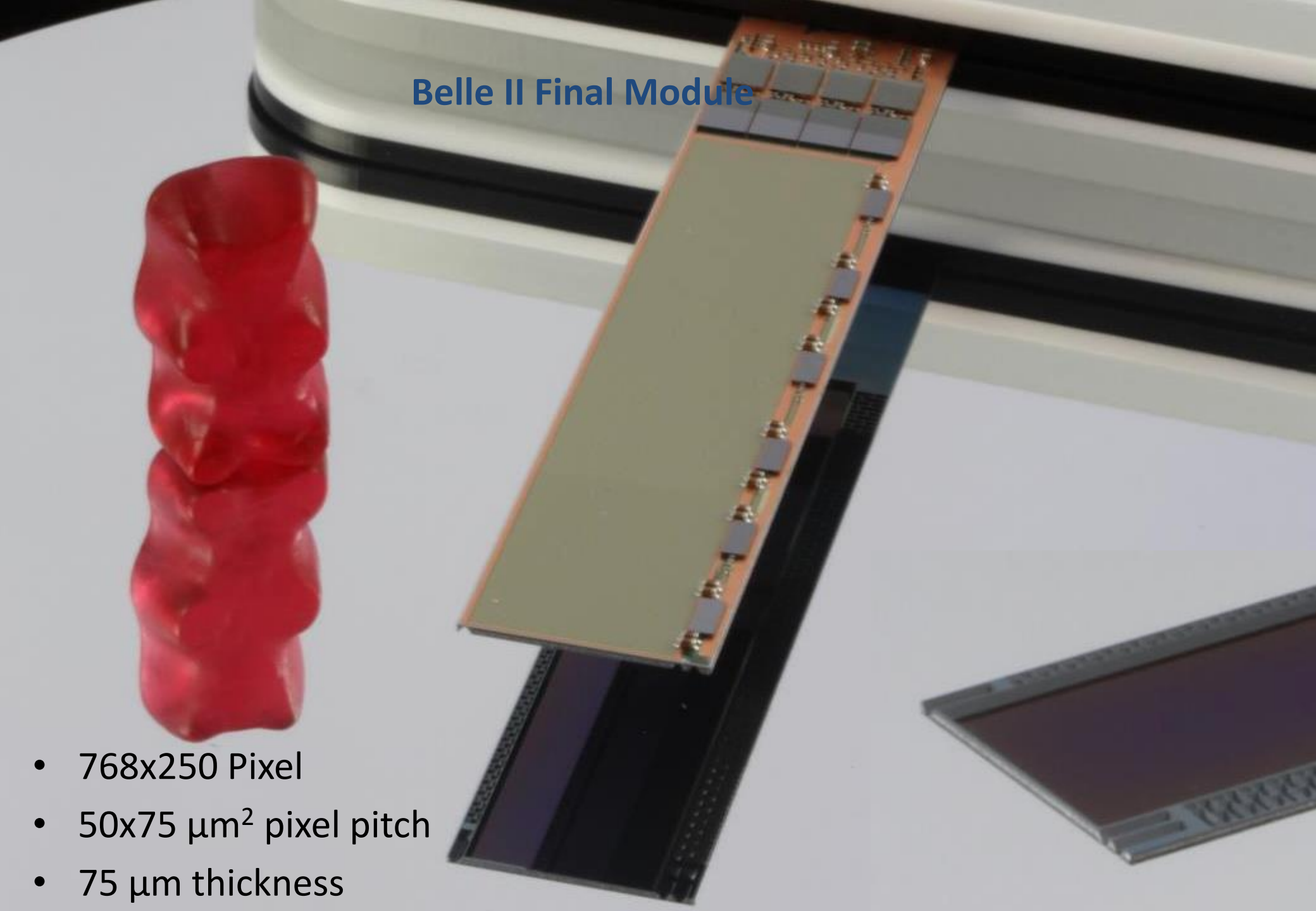


30° tilt: many 2 pixel clusters

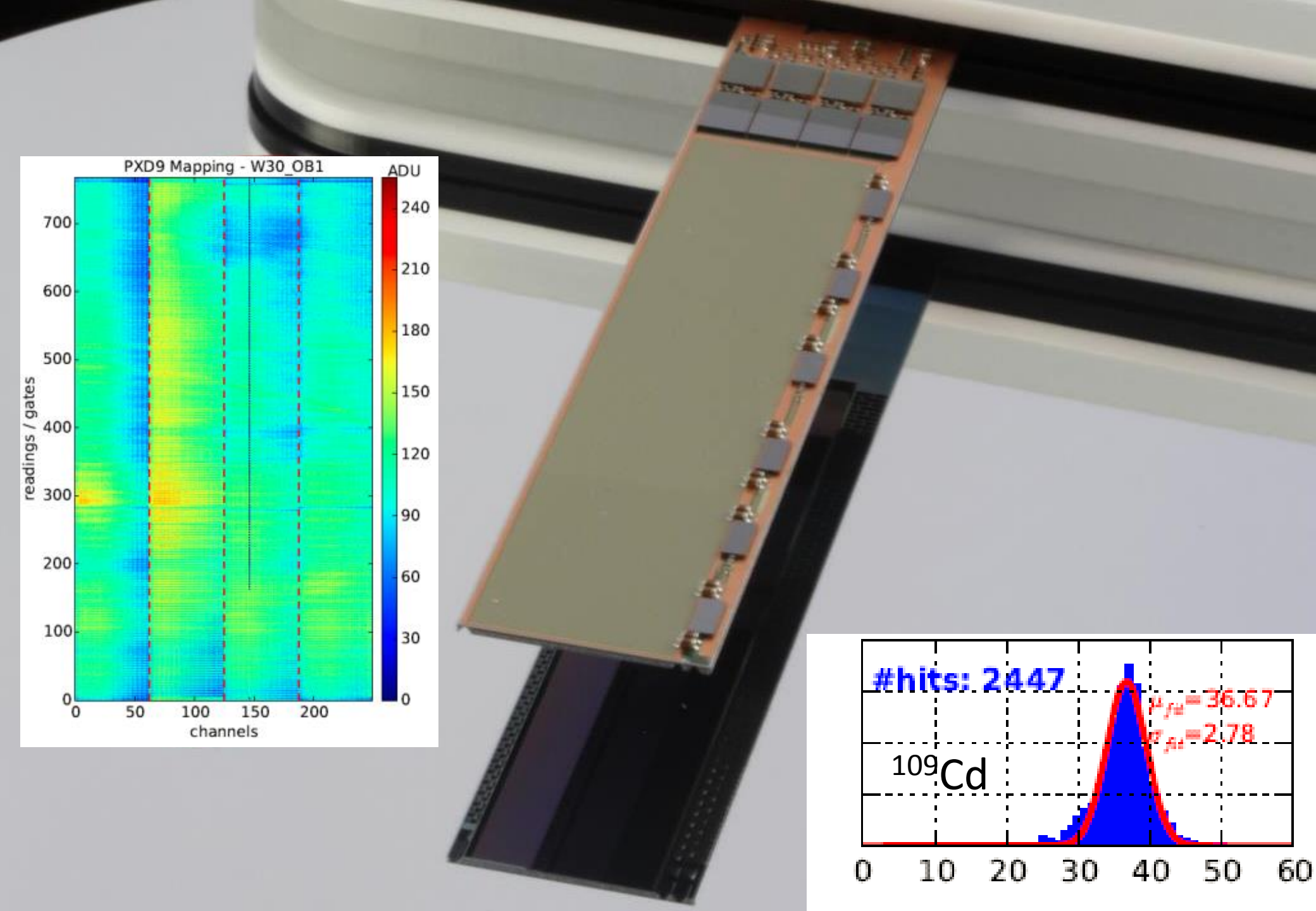


- Matrix tilted along column: multi-column clusters
- Expectation for single pixel readout: $\mathrm{RMS} = 50\,\mu\mathrm{m}/\sqrt{12} \approx 14.5\mu\mathrm{m}$

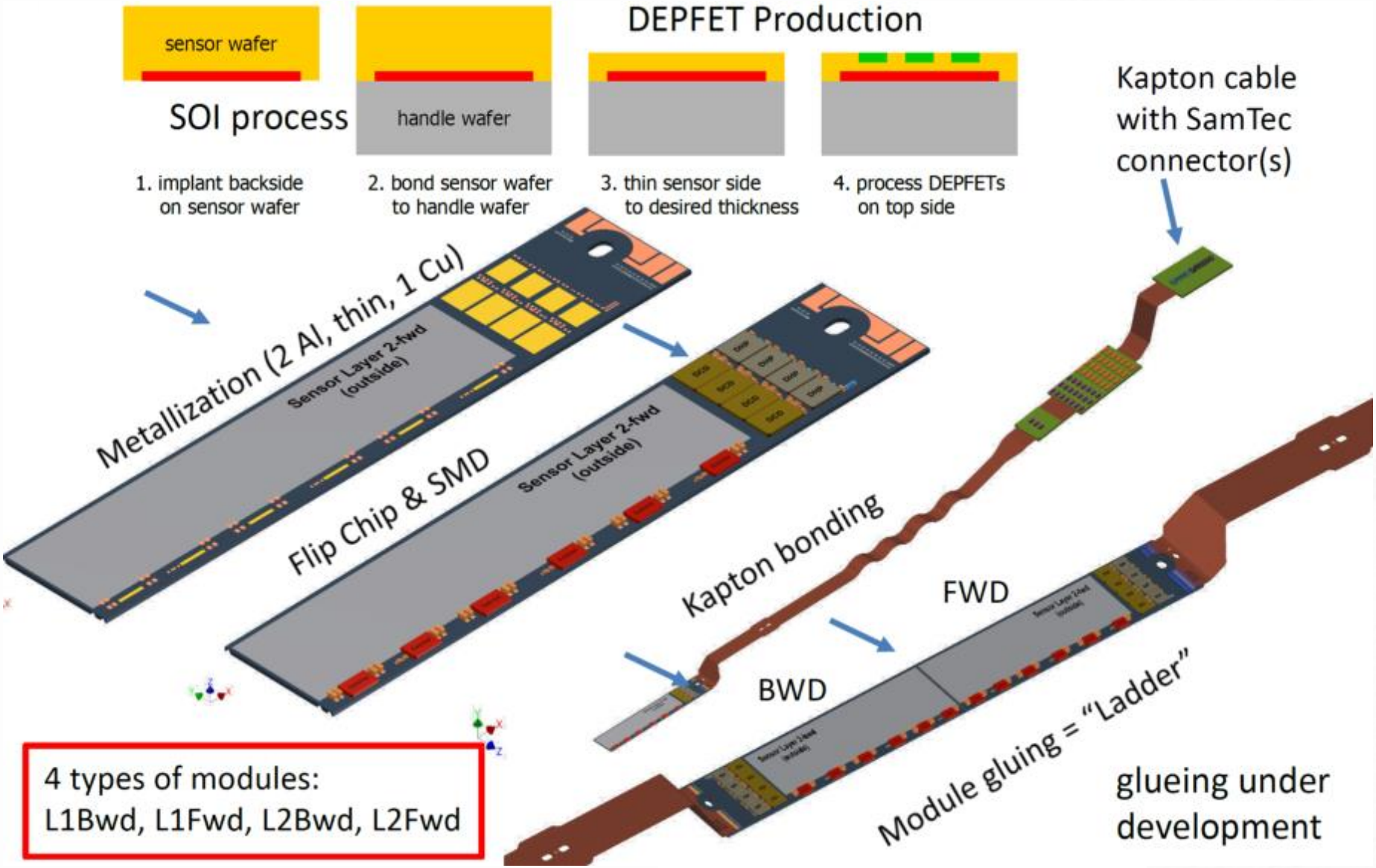
Belle II Final Module



- 768x250 Pixel
- 50x75 µm^2 pixel pitch
- 75 µm thickness

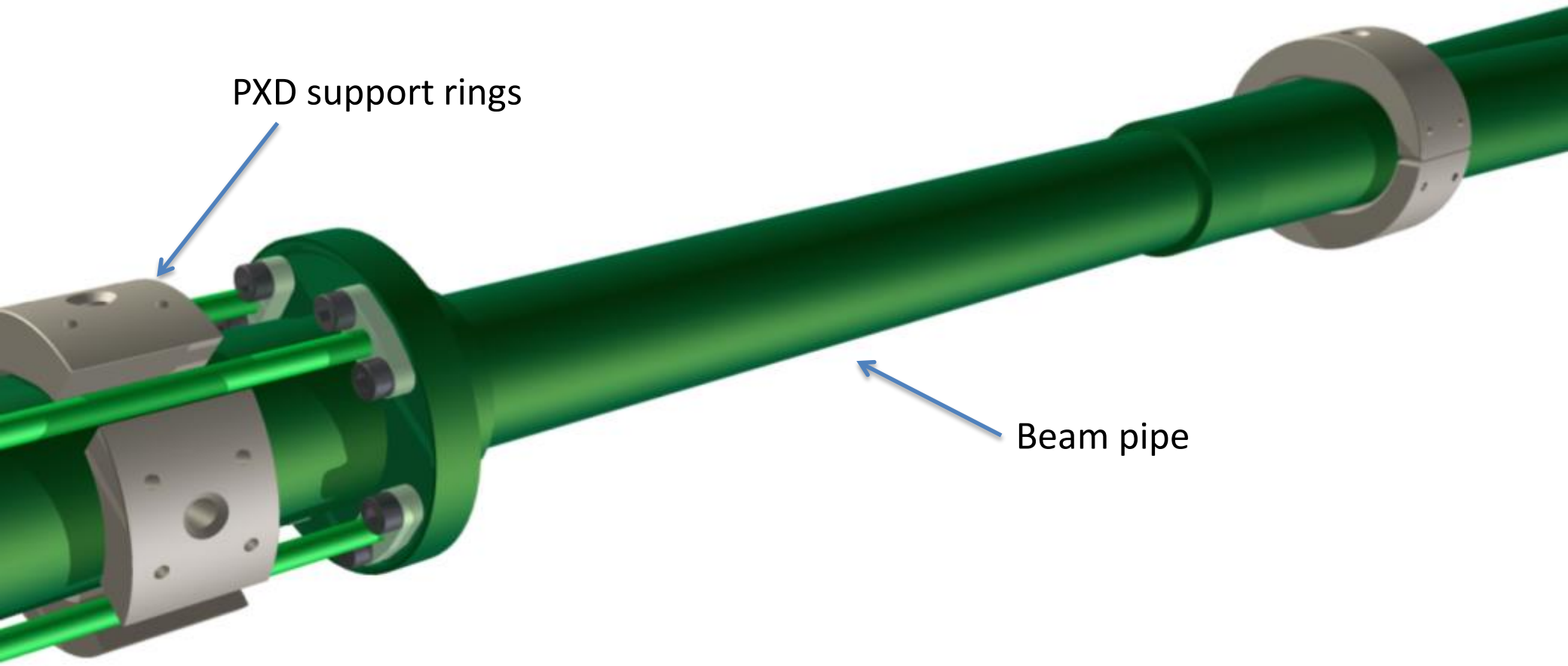

PXD9 Mapping - W30_OB1
ADU
240
210
180
150
120
90
60
30
0
readings / gates
0
100
200
300
400
500
600
700
0
50
100
150
200
channels
#hits: 2447
μ_{fit}=36.67
σ_{fit}=2.78
^{109}Cd
0
10
20
30
40
50
60

DEPFET Production

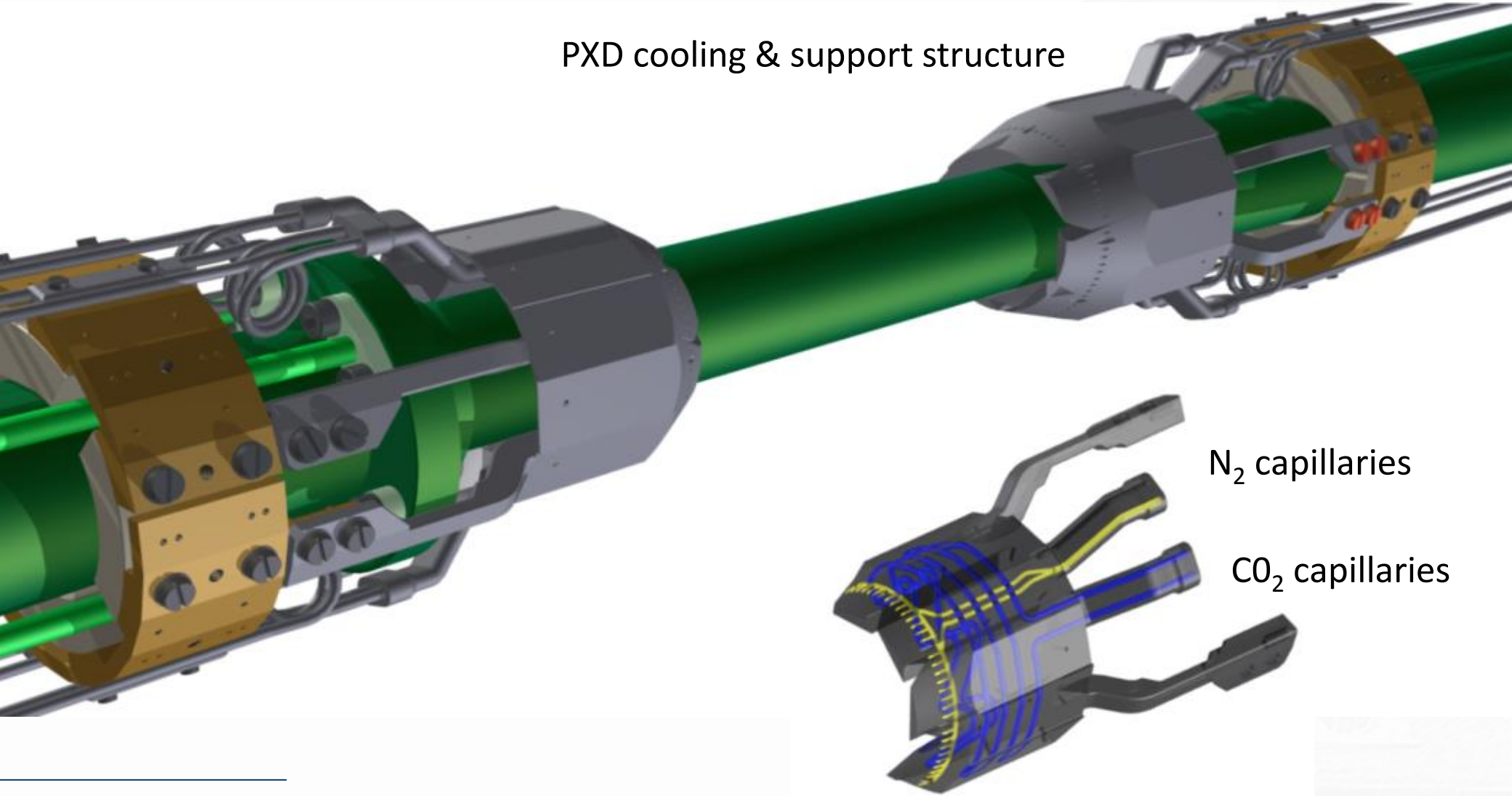


C. Kiesling, 10th BPAC, KEK, Japan, Feb. 7-9, 2016

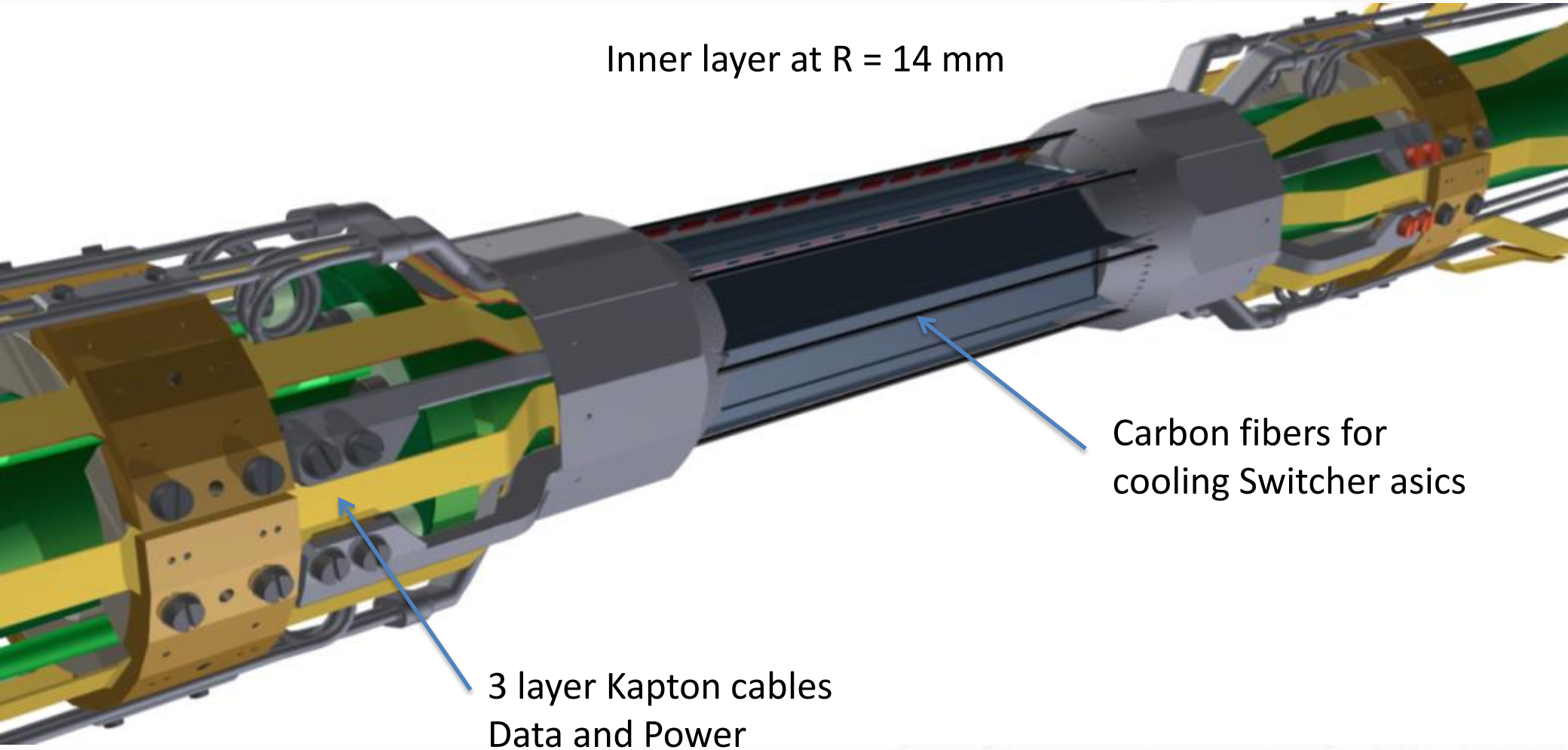
Beampipe



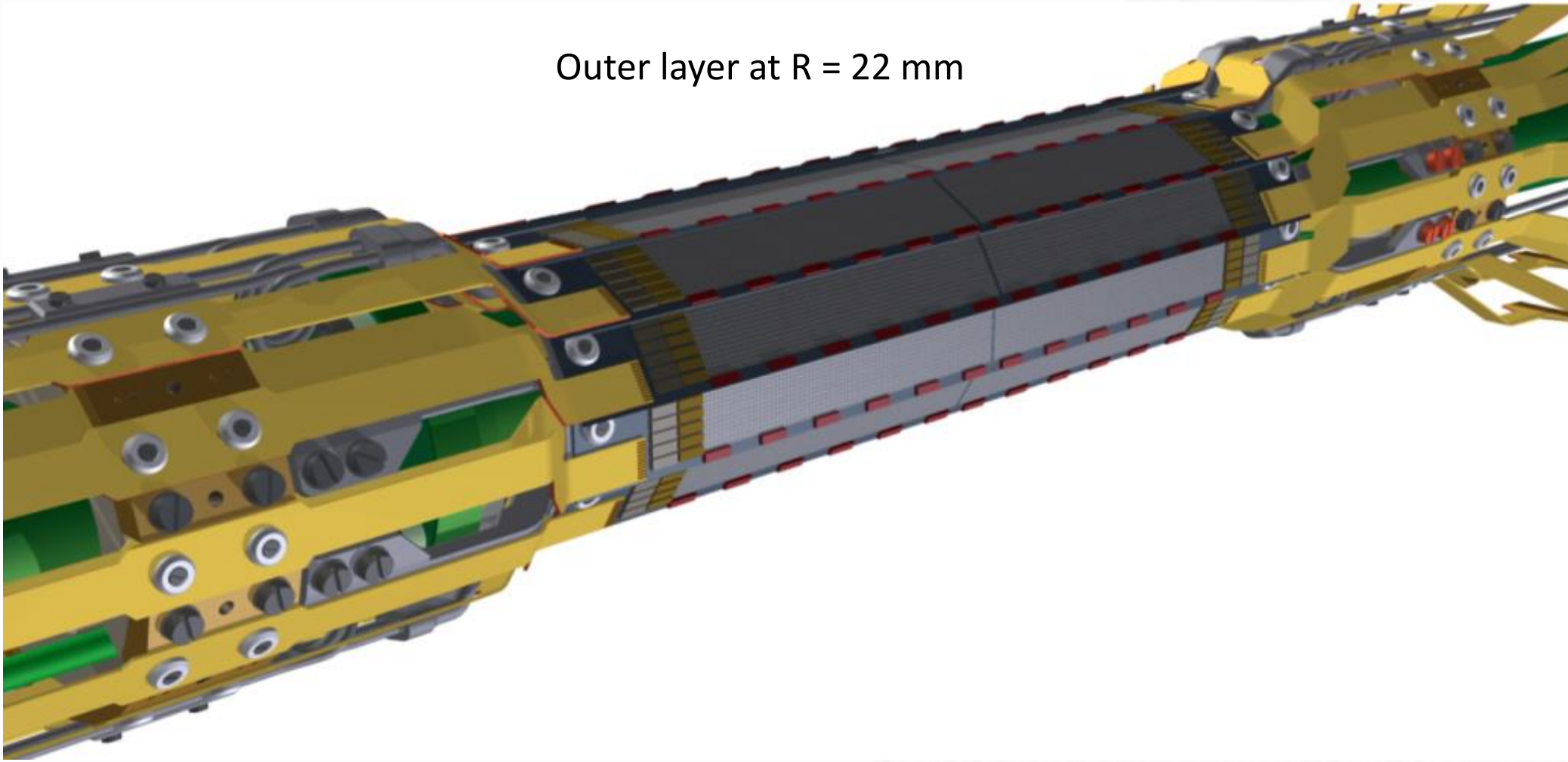
Cooling blocks



Inner Layer


Inner layer at R = 14 mm
Carbon fibers for
cooling Switcher asics
3 layer Kapton cables
Data and Power

Outer Layer



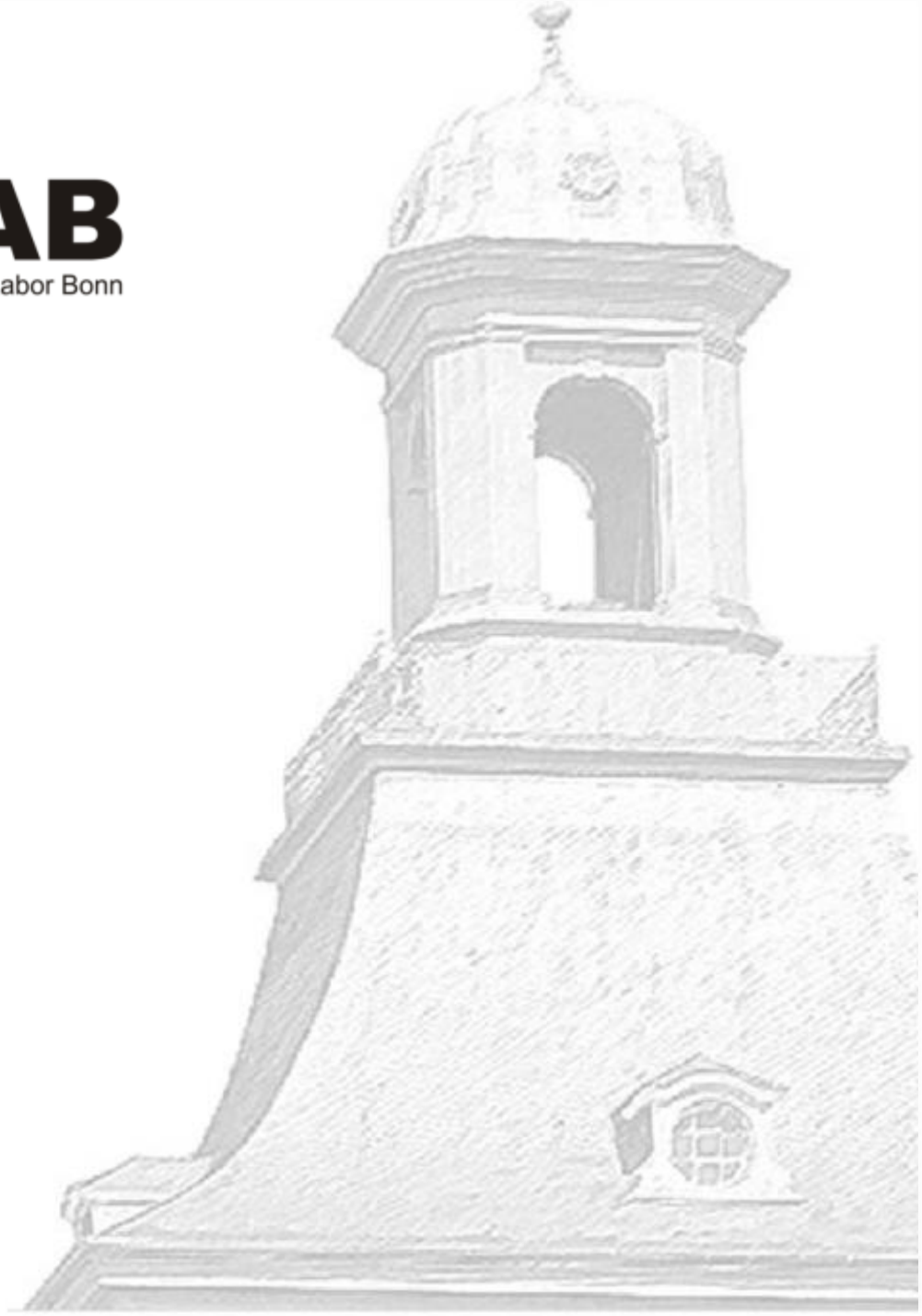
Conclusion

- Belle II will feature ultra thin DEPFET Pixel sensors
- Small sensors in latest technology characterized and tested with 4GeV electrons at DESY
- First large modules successfully produced
- Full detector to start operation in 2018

universitätbonn

SI LAB
Silizium Labor Bonn

Thank you



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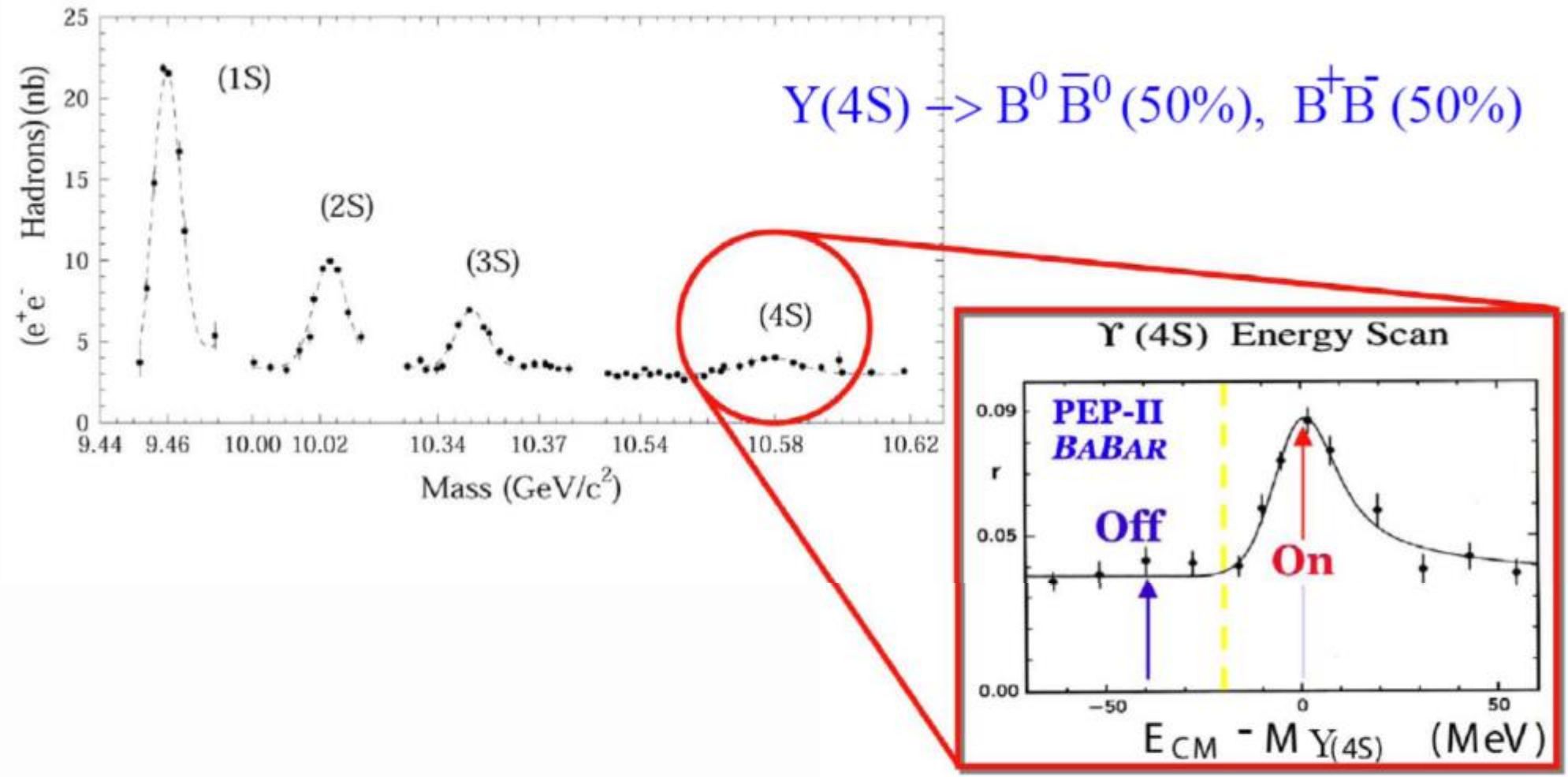
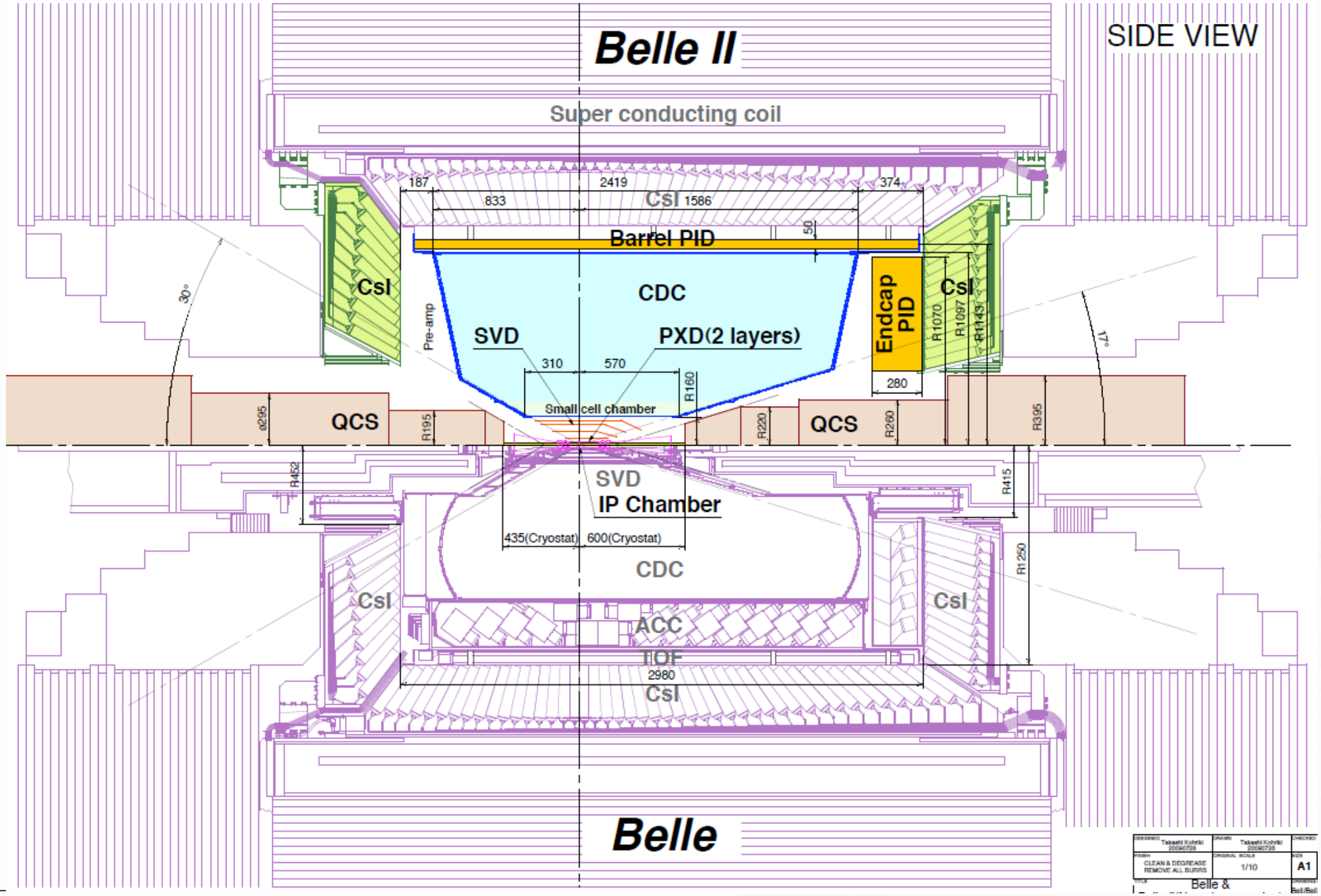
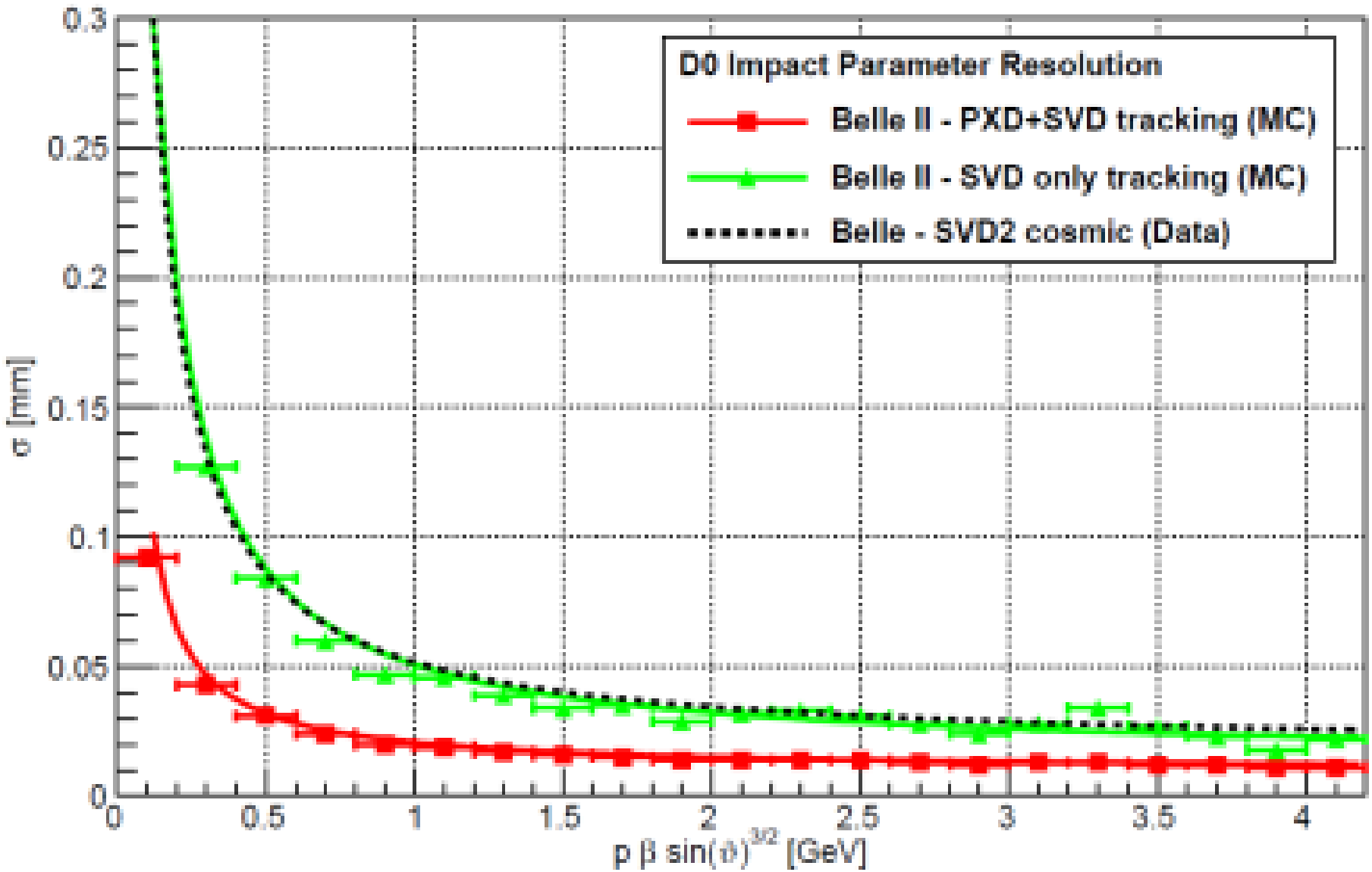
BACKUP


Υ(4S) -> B0 B̄0 (50%), B+B- (50%)
(1S)
(2S)
(3S)
(4S)
(e+e- Hadrons)(nb)
Mass (GeV/c2)
9.44 9.46 10.00 10.02 10.34 10.37 10.54 10.58 10.62
Υ (4S) Energy Scan
PEP-II
BABAR
Off
On
r
E CM - M Υ(4S) (MeV)


Belle II
SIDE VIEW
Super conducting coil
CsI
Barrel PID
CDC
SVD
PXD(2 layers)
Endcap PID
Pre-amp
Small cell chamber
QCS
SVD
IP Chamber
CDC
ACC
TOF
Belle


D0 Impact Parameter Resolution
Belle II - PXD+SVD tracking (MC)
Belle II - SVD only tracking (MC)
Belle - SVD2 cosmic (Data)
σ [mm]
p β sin(ϑ)^3/2 [GeV]
0
0.05
0.1
0.15
0.2
0.25
0.3
0.5
1
1.5
2
2.5
3
3.5
4

MOSFET

- Each DEPFET pixel is a **p-channel FET** on a completely depleted bulk.

- Recap on MOSFETs (here: n-channel FET):
  - Voltage on gate steers Source Drain Current
  - Gate voltage forms field beneath the gate and changes charge distribution beneath the gate
  - Linear: $V_{GS} > V_{th}$ and $V_{DS} < (V_{GS} - V_{th})$

$$I_D = \mu_n C_{ox} \frac{W}{L}\left((V_{GS} - V_{th})V_{DS} - \frac{{V_{DS}}^2}{2}\right)$$

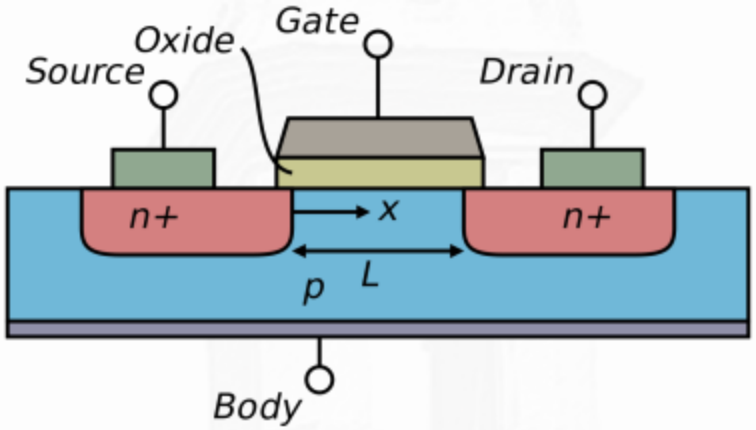
  - **Saturation:** $V_{GS} > V_{th}$ and $V_{DS} \geq (V_{GS} - V_{th})$

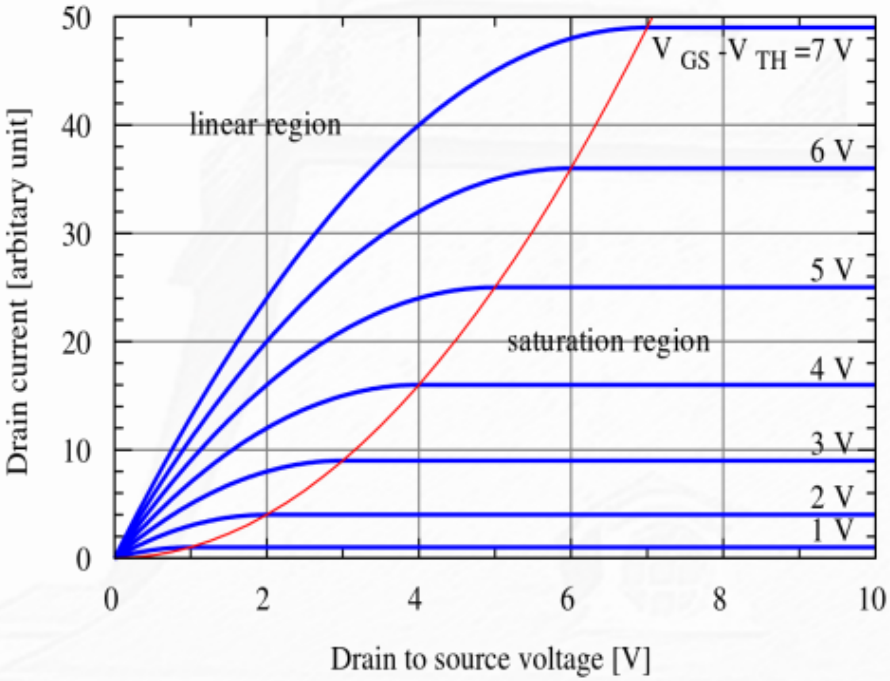
$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{th})^2(1 + \lambda(V_{DS} - V_{DSsat}))$$

  - Voltage controlled current source with gain

$$\boldsymbol{g_m = \frac{\partial I_D}{\partial V_{GS}} = \mu_p C_{ox}\frac{W}{L}(V_{GS} - V_{th})}$$

- On p-channel FETs: V_{GS} needs to be negative, $V_{GS} < V_{th}$ etc.

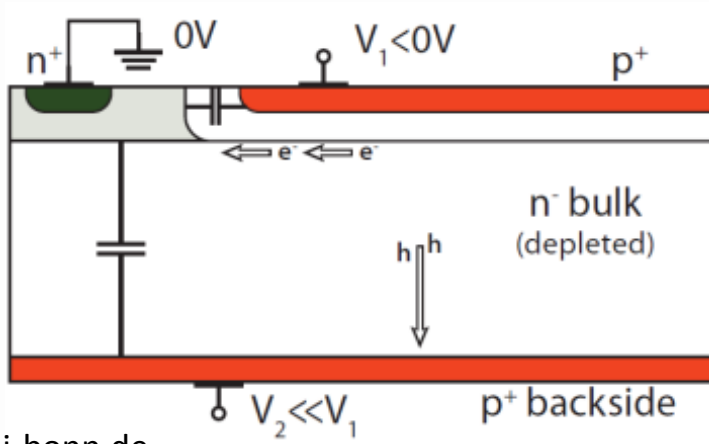


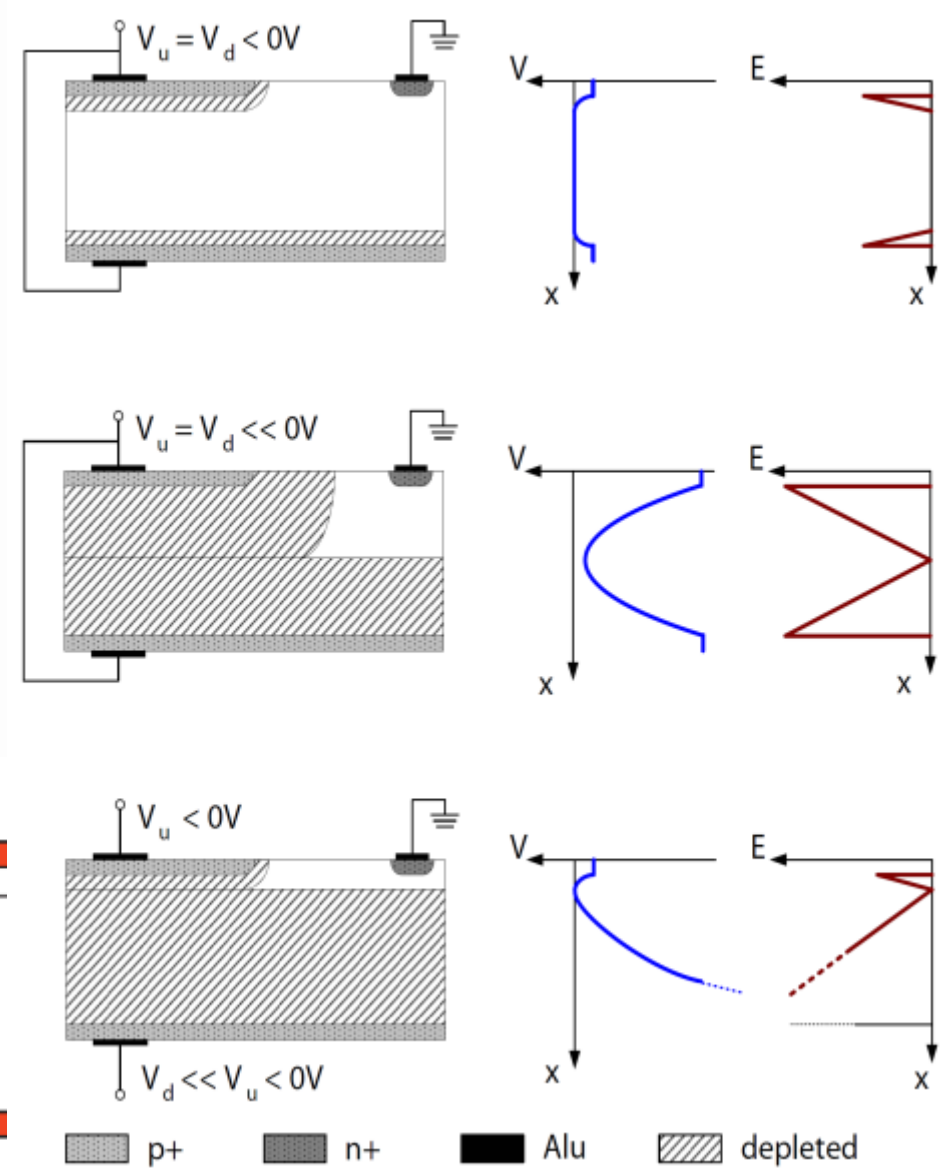


Sidewards depletion

- Each DEPFET pixel is a p-channel FET on a **completely depleted bulk**.

- Sidewards depletion
  - Depletion from front and backside simultaneous.
  - Full depletion needs lower bias voltage than pn structure depletion at same size and has lower detector capacitance.
  - Potential minimum in the sensor. Depth can be adjusted.
  - Electrons drift to potential minimum (fast) and then diffuse to n+ contact.

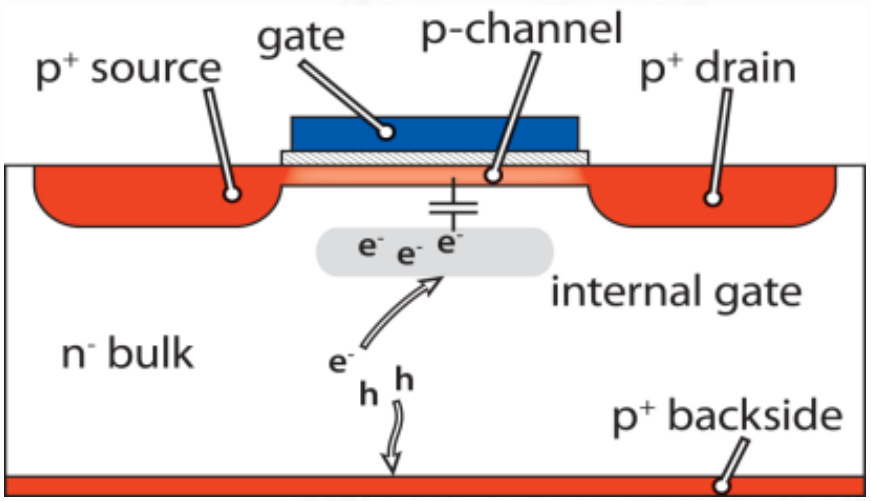


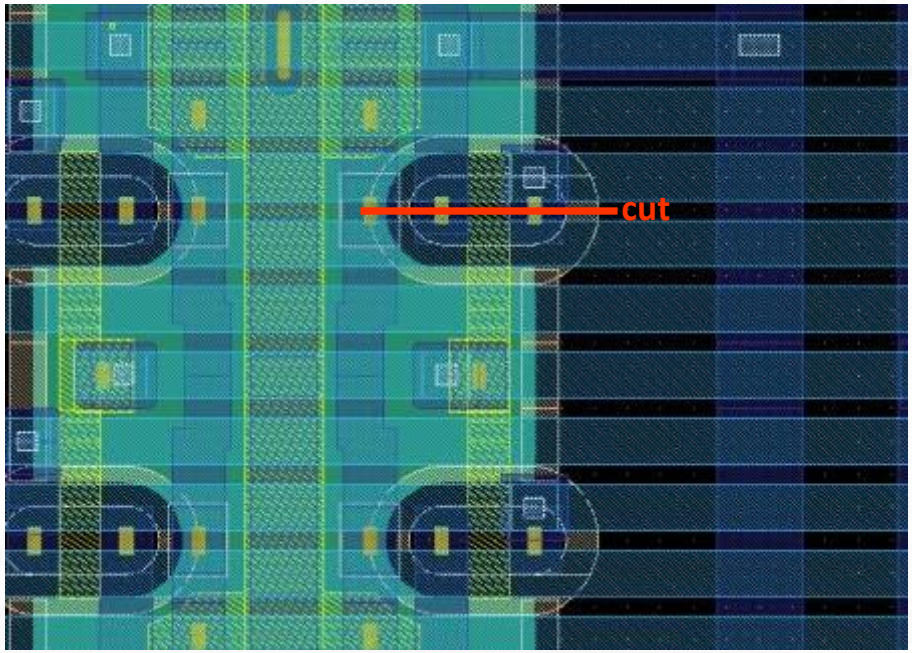


DEPFET Charge Collection

- A deep n-implant creates a potential minimum for electrons under the gate (internal gate)

- Charge created in the depleted volume drifts to potential minimum below the DEPFET surface
- Outer Pixel regions: Drift potential pushes electrons to the pixel center
- Internal gate directly below the FET channel collects electrons.
- Readout capacity small

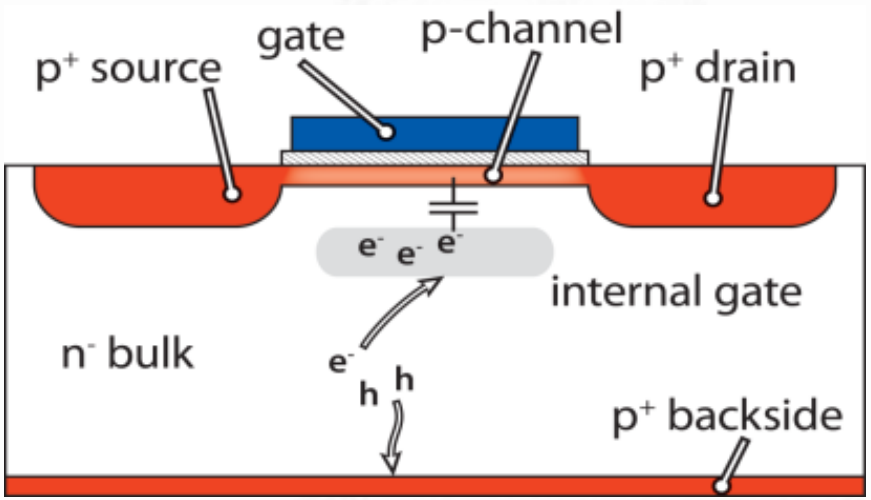




DEPFET Internal amplification

- Signal electrons in the internal gate modulate the transistor current.

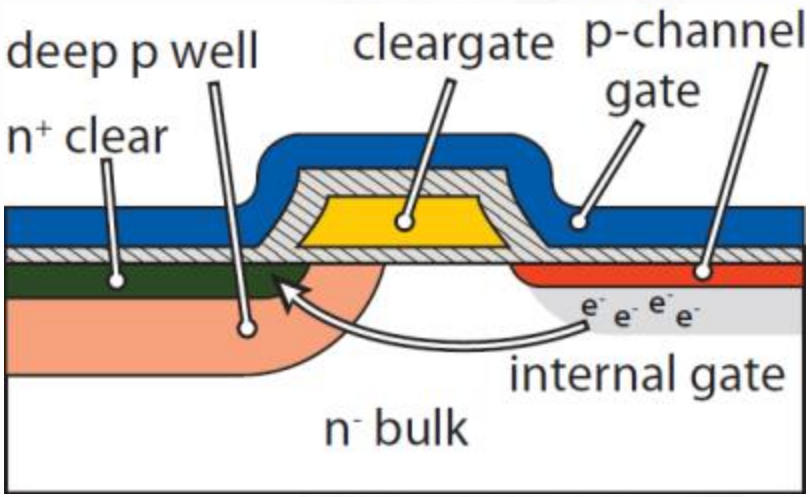
- Charge in internal gate is equivalent to gate source potential $\partial V_{GS} = f\frac{\partial q}{C_{gate}} = f\frac{\partial q}{C_{ox}WL}$
- $I_D = \frac{\mu_p C_{ox}}{2}\frac{W}{L}\left(f\frac{\partial q}{C_{gate}} + V_{GS} - V_{th}\right)^2$
- **Internal amplification:** $g_q = \frac{\partial I_D}{\partial q} = \frac{g_m}{C_{gate}} \propto \sqrt{\frac{I_d}{L^3\ WC_{gate}}} \approx 500\frac{pA}{e^-}$
- **Current based readout system**
- Source connected to constant potential
- Drain current read
- Baseline current (pedestal) needs to be substracted.
- Threshold voltage variations change pedestal current

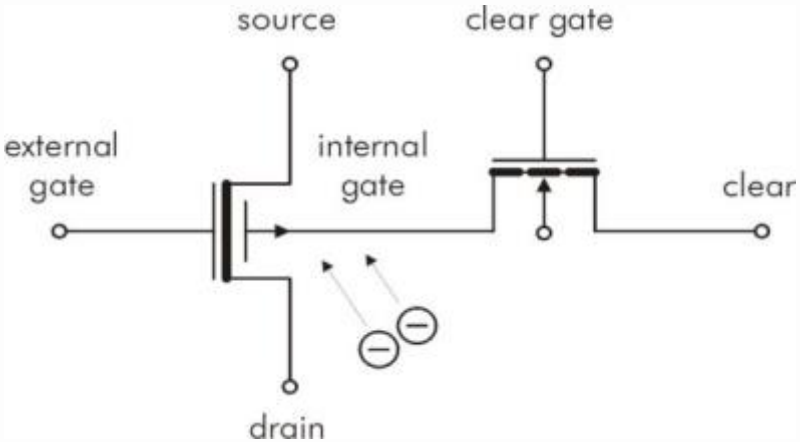


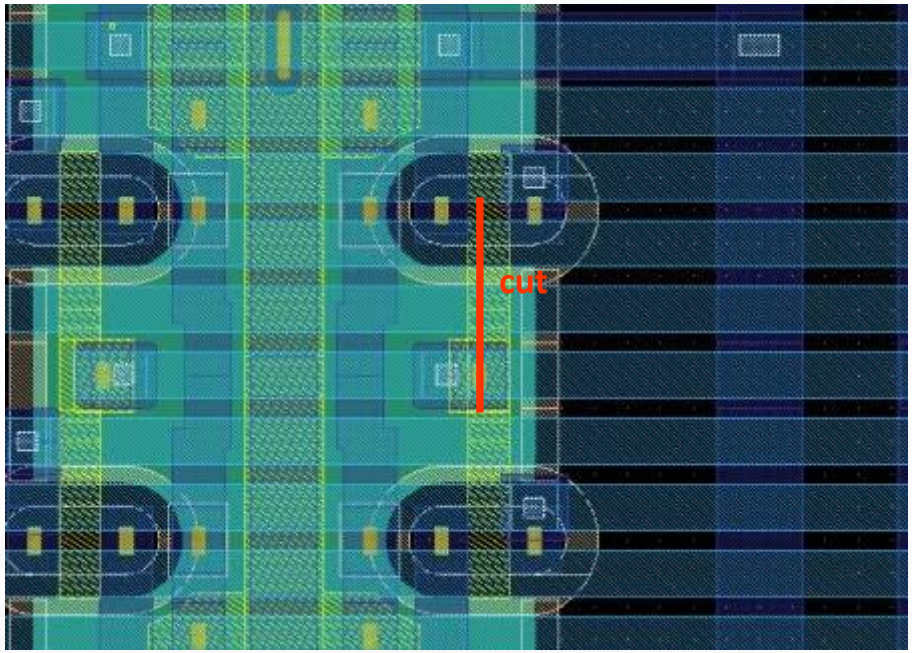
- Voltage based readout possible
- Source follower configuration
- Less sensitive to threshold variations
- µs readout time due to line capacitance

DEPFET charge clear

- Nondestructive readout
- Charge needs to be cleared
- Clear contact attractive for electrons
  - Deep p shields clear contact
  - High voltage needed for clear to punch trough p well
  - Clear gate helps form a channel between internal gate and clear







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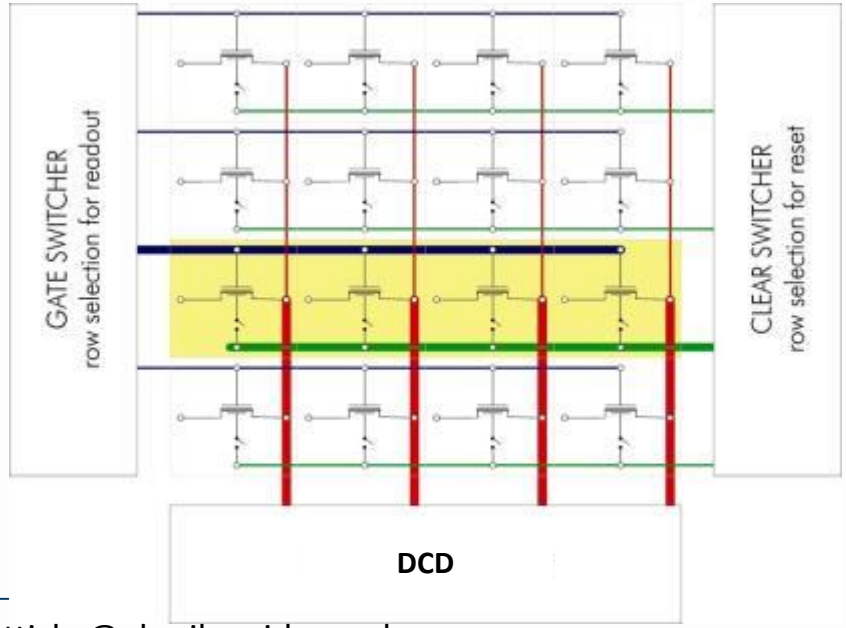
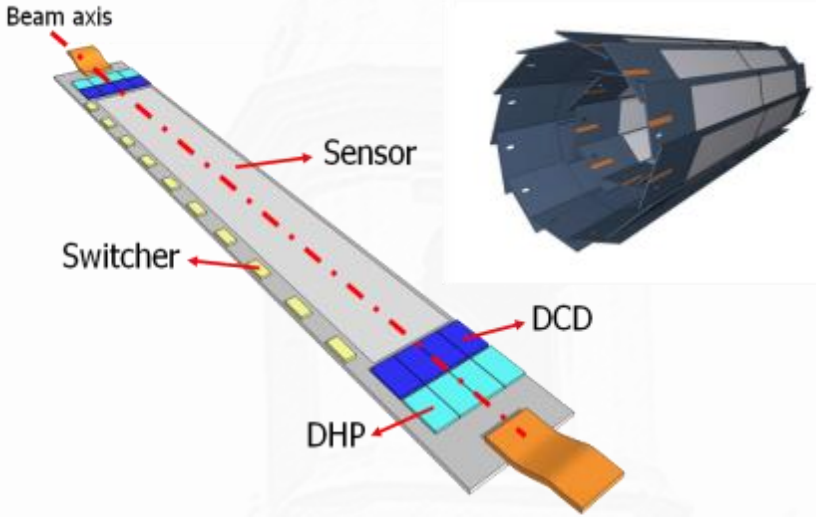
DEPFET Readout and Module design

- „Rolling-Shutter" readout
  1. Activate Gate
  2. Read out Drain current
  3. Activate Clear: remove charge from int. Gate
  4. Gate and Clear inactive: next row
- Final system: 4 rows read out in parallel
- **Row only active when read out – still sensitive all the time.**

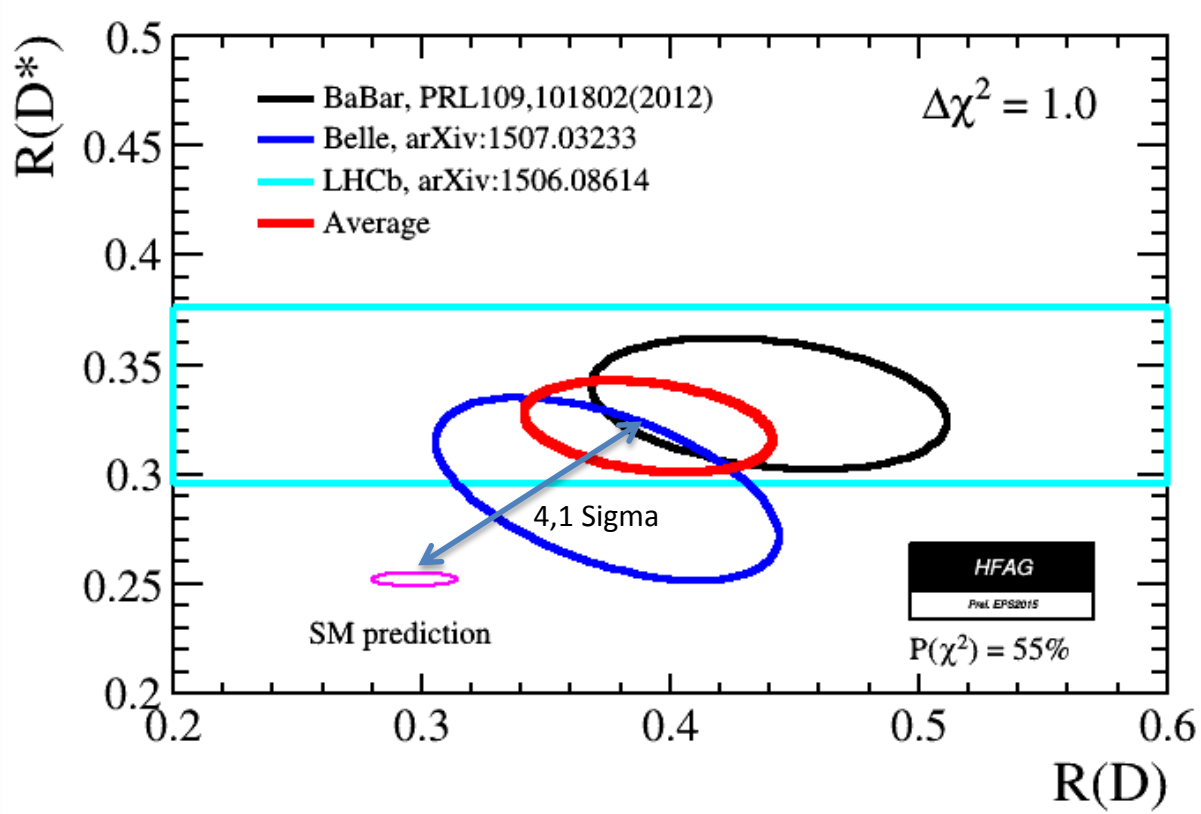




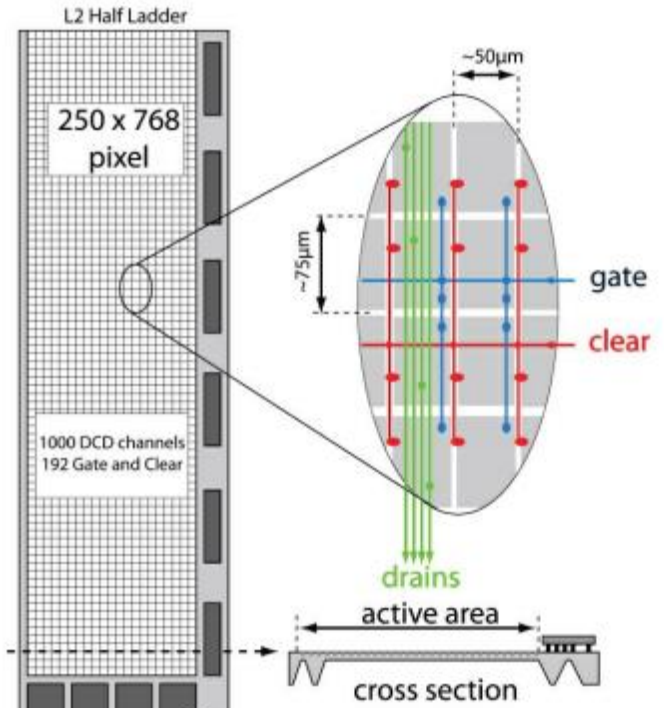
- Detection and internal amplification
- Small intrinsic noise
- Low power consumption
- Readout electronic out of acceptance region

The R(D*) Problem

- Influenced by V_{cb}
- Can be repeated with more rare decays to check V_{ub}

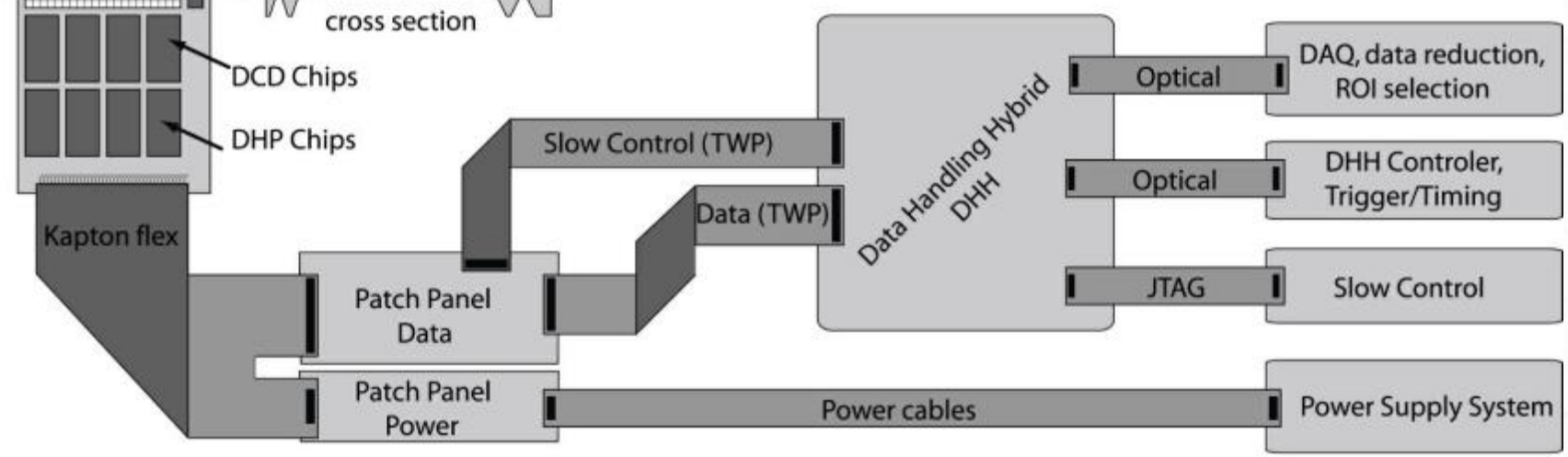


Off-module Data Flow



- **DHH** (Data Handling Hybrid)
  Electrical - optical interface
  Slow control master (JTAG)
  Clustering

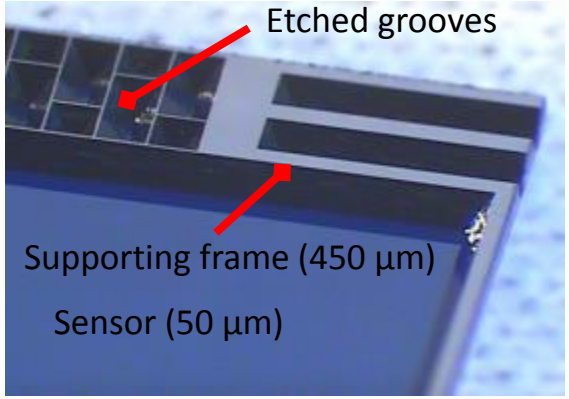
- **ONSEN**
  Data buffer
  Reduction via ROI selection (DATCON, HLT)

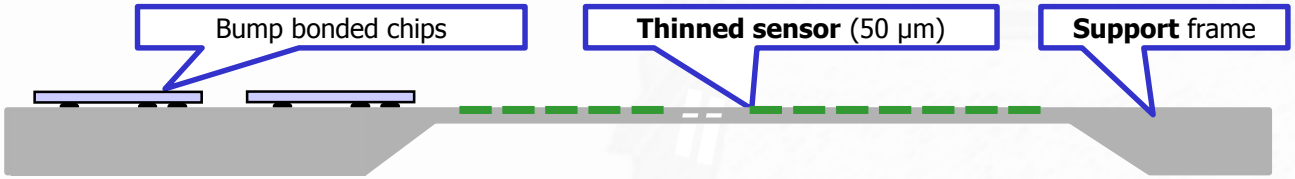


Thin DEPFET Sensors

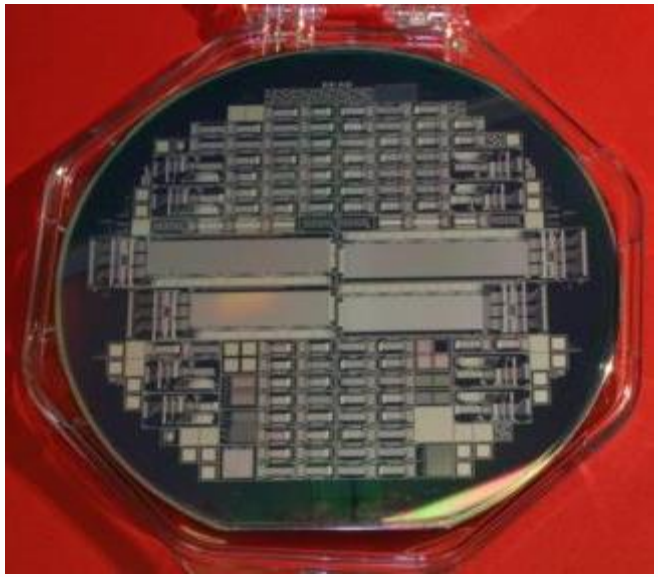
Use anisotropic etching on bonded wafers to create a thin, self-supporting sensor

- One material: uniform and small thermal expansion
- The DEPFET thickness is a free adjustable parameter



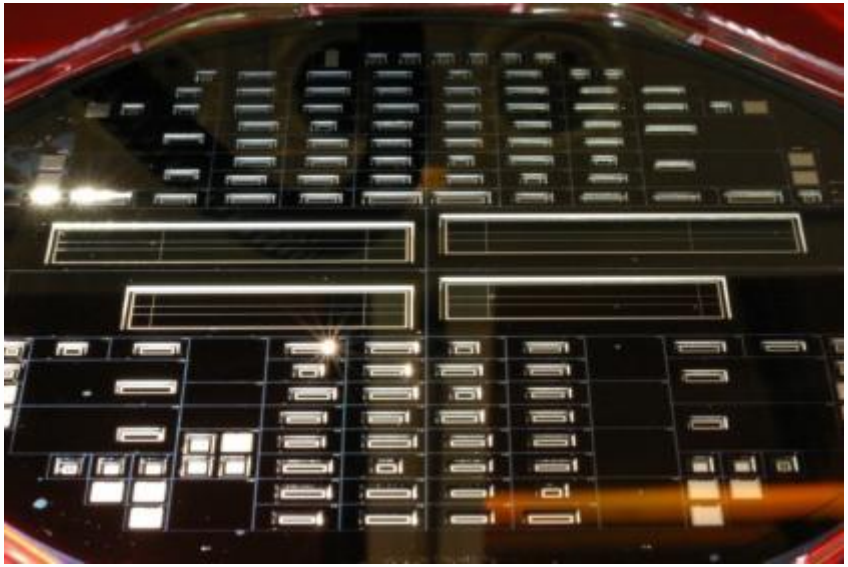


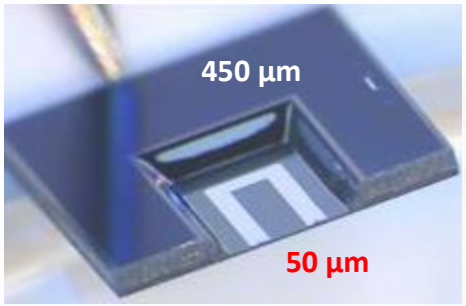
PXD6 Prototype Production



8 SOI wafers with 50 µm thin sensors (450 µm handle)

- Small test matrices with design variations
- Full size sensors for prototyping

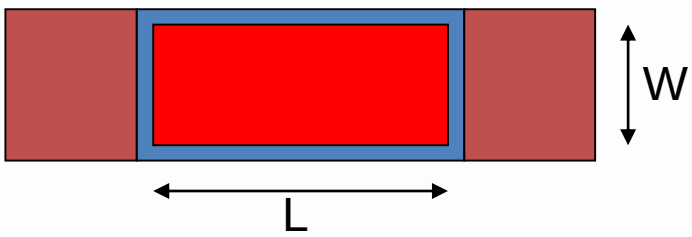


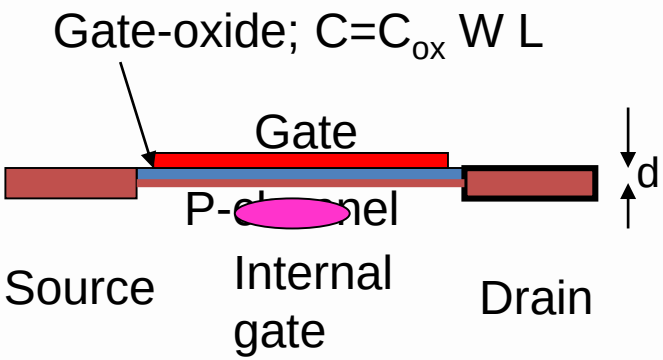


90 steps fabrication process:

- 9 Implantations
- 19 Lithographies
- 2 Poly-layers
- 2 Alu-layers
- 1 Copper layer
- Back side processing

How does a DEPFET work?





A charge q in the internal gate induces a mirror charge αq in the channel (α <1 due to stray capacitance). This mirror charge is compensated by a change of the gate voltage: $\Delta V = \alpha\, q / C = \alpha\, q / (C_{ox}\, W\, L)$ which in turn changes the transistor current I_d .

q

FET in saturation:

$$I_d = \frac{W}{2L}\mu C_{ox}\left(V_G + \frac{\alpha q_s}{C_{ox}WL} - V_{th}\right)^2$$

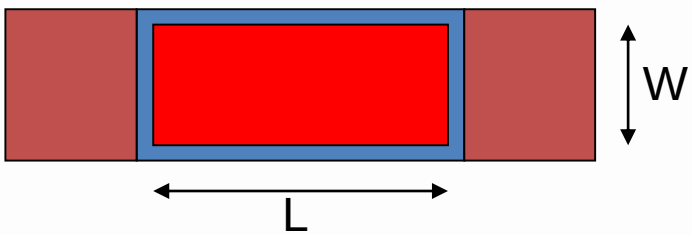
I_d: source-drain current
C_{ox}: sheet capacitance of gate oxide
W,L: Gate width and length
μ: mobility (p-channel: holes)
V_g: gate voltage
V_{th}: threshold voltage

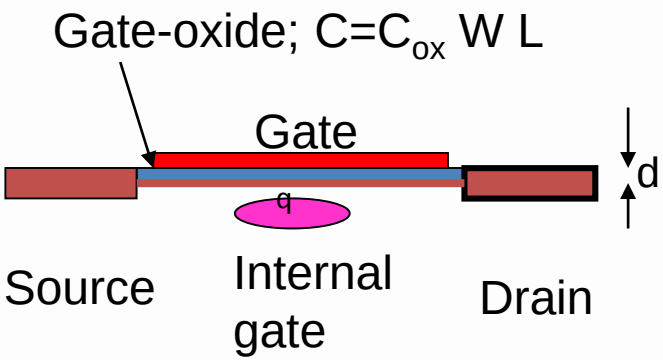
Conversion factor:

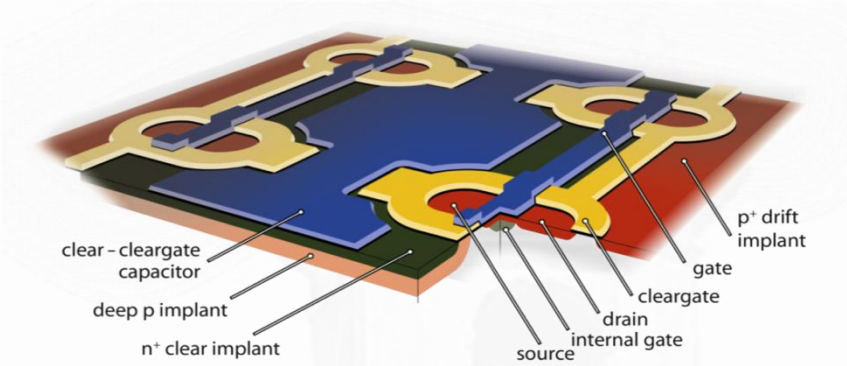
$$g_q = \frac{dI_d}{dq_s} = \frac{\alpha\mu}{L^2}\left(V_G + \frac{\alpha q_s}{C_{ox}WL} - V_{th}\right) = \alpha\sqrt{2\frac{I_d\mu}{L^3WC_{ox}}}$$

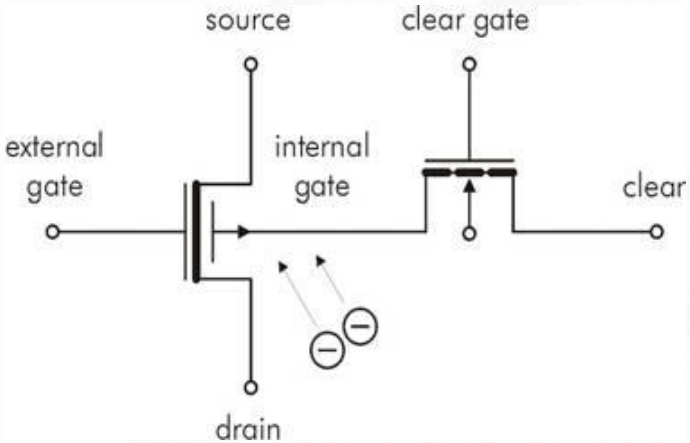
$$g_m = g_q = \alpha\frac{g_m}{WLC_{ox}} = \alpha\frac{g_m}{C}$$

How does a DEPFET work?





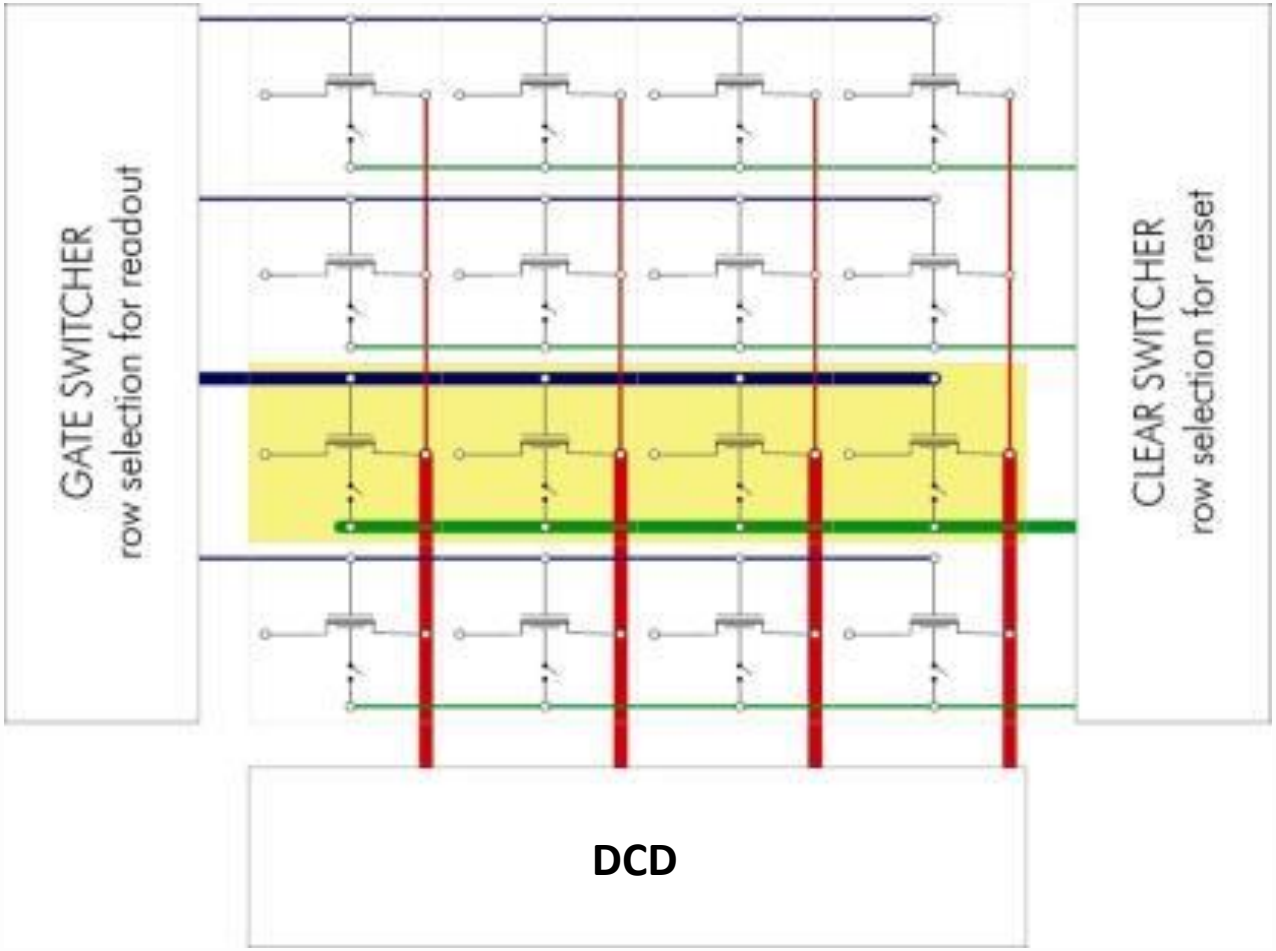




A charge q in the internal gate induces a mirror charge αq in the channel (α <1 due to stray capacitance). This mirror charge is compensated by a change of the gate voltage: $\Delta V = \alpha\ q / C = \alpha\ q / (C_{ox}\ W\ L)$ which in turn changes the transistor current I_d
.

- Internal amplification g_q~ 500 pA/e^-
- Small intrinsic noise
- Sensitive off-state, no power consumption

DEPFET Readout and Module design



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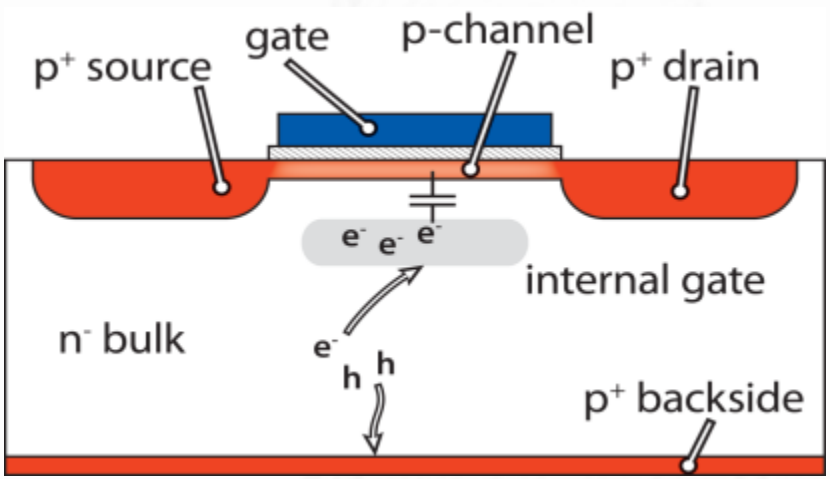
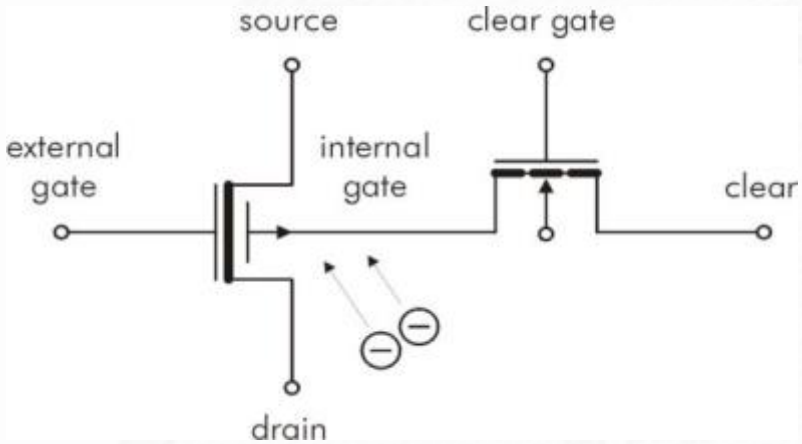
- Final system: 4 rows read out in parallel
- **Row only active when read out – still sensitive all the time.**

DEPFET – DEpleted Field Effect Transistor

- Each pixel is a p-channel FET on a completely depleted bulk.
- A deep n-implant creates a potential minimum for electrons under the gate (internal gate)
- Signal electrons in the internal gate modulate the transistor current



$$g_q = \frac{\partial I_d}{\partial q} \propto \left(\frac{I_d}{L^3 W C_{ox}}\right)^{1/2} \sim 500pA/e^-$$



- Detection and internal amplification
- Small intrinsic noise
- Low power consumption